LC5500 Series Single-Stage Power Factor Corrected Off-Line Switching Regulator ICs

Introduction

The LC5500 series is the power IC for the LED driver which has an incorporated power MOSFET, designed for input capacitorless applications, and making it possible for systems to comply with the harmonics standard (IEC61000-3-2 class C). The controller adapts the average current control method for realizing high power factors, and the quasi-resonant topology contributes to high efficiency and low EMI noise. The series is housed in either DIP8 or TO-220F-7L packages, depending on output power capability. The rich set of protection features helps to realize low component counts, and high performance-to-cost power supply.

Features and Benefits

- Non-isolated (LC551xD) and isolated (LC552xD and LC552xF) applications
- Integrated on-time control circuit (it realizes high power factor by average current control)
- Integrated startup circuit (no external startup circuit necessary)
- Integrated soft-start circuit (reduces power stress during start-up on the incorporated power MOSFET and output rectifier)
- Integrated bias assist circuit (improves startup performance, suppresses VCC voltage droop during operation, and allows use of low-rated ceramic capacitor on VCC pin)
- Integrated Leading Edge Blanking (LEB) circuit
- Integrated maximum on-time limit circuit

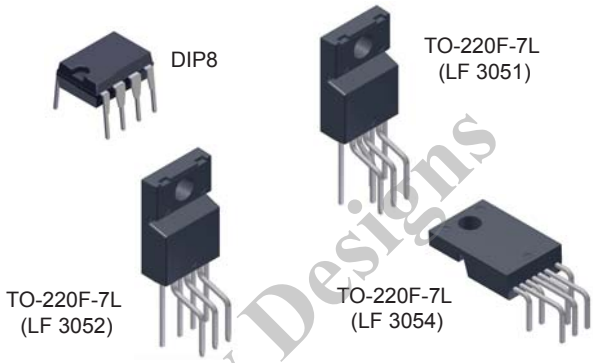

Figure 1. The LC5500 series packages for lower wattage versions are fully molded DIP8s, with pin 7 removed for greater isolation. For higher wattages, the TO-220F-7L fully molded package is provided, with three leadform options, all which provide a separation between pins 1 and 2.

- Protection features:
  - Overcurrent protection (OCP): pulse-by-pulse
  - Overvoltage protection (OVP): auto restart, OVP-activating pins vary by product series:

	OVP-Activating Pins			
Series	VCC	ISENSE	OVP	OCP
LC551xD	×	×	–	×
LC552xD	×	–	×	×
LC552xF	×	–	×	×

  - Overload protection (OLP): auto restart
  - Thermal shutdown (TSD): latched shutdown

Applications

- LED lighting fixtures
- LED light bulbs

The product lineup for the LC5500 series provides the following options:

Part Number	MOSFET V_{DSS}(min) (V)	$R_{DS(on)}$ (max) (Ω)	Isolation	Package	P_{OUT}* (W)	
					230 VAC	85 to 265 VAC
LC5511D	650	3.95	Non-isolated	DIP8	13	10
LC5513D		1.9			20	16
LC5521D		3.95	Isolated		13	10
LC5523D		1.9			20	16
LC5523F				TO-220F-7L	60	40
LC5525F		1.1			80	55

*Based on the thermal rating; the allowable maximum output power can be up to 120% to 140% of this value. However, maximum output power may be limited in an applications with low output voltage or short duty cycle.

Part Number Assignment

LC55*nna*
A BC D

A	Product series name
B	Indicates non-isolated or isolated: 1 – Non-isolated, 2 – Isolated
C	On-resistance of the incorporated MOSFET: 1 – 3.95 Ω, 3 – 1.9 Ω, 5 – 1.1 Ω
D	Indicates the package: D – DIP8, F – TO-220F-7L

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Block Diagrams and Pin Descriptions

This section provides block diagrams and pin descriptions of:

- LC551xD for non-isolated DIP8 designs
- LC552xD for isolated DIP8 designs
- LC552xF for isolated TO-220-7L designs

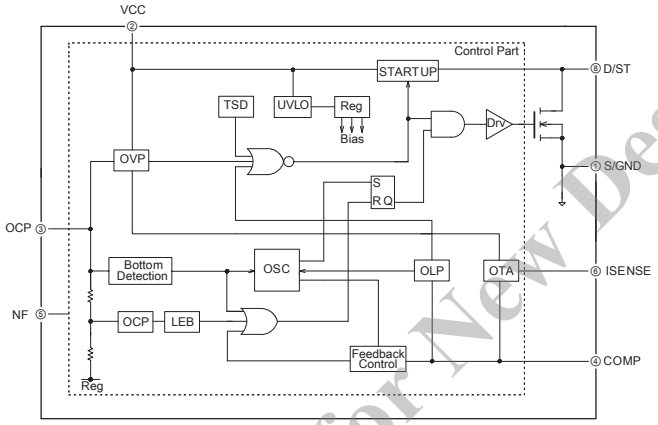
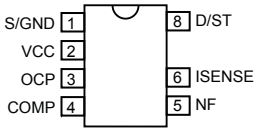


Figure 2. LC551xD series functional block diagram (for non-isolated DIP8 designs)

Pin-out Diagram (LC551xD)



LC551xD Series Pin List Table

Number	Name	Function
1	S/GND	MOSFET source and GND pin for the Control Part
2	VCC	Supply voltage input and Overvoltage protection (OVP) signal input
3	OCP	Overcurrent Protection, quasi-resonant signal input pin, and Overvoltage Protection (OVP) signal input
4	COMP	Feedback phase-compensation input
5	NF	No function; must be externally connected to S/GND pin with as short a trace as possible, for stable operation of the IC
6	ISENSE	Output current detecting voltage input and Overvoltage Protection (OVP) signal input
7	–	Pin removed
8	D/ST	MOSFET drain pin and input of the startup current

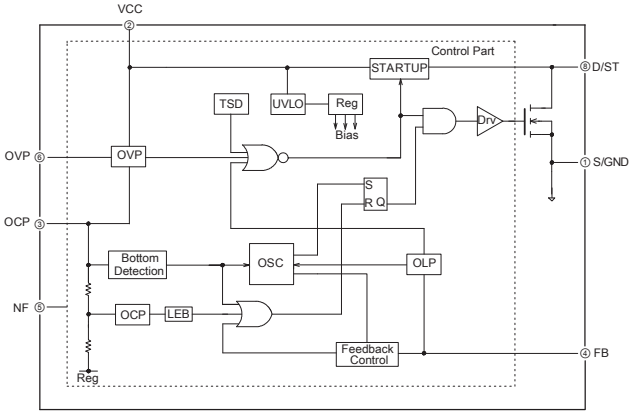
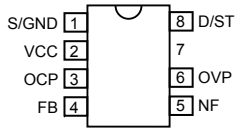


Figure 3. LC552xD series functional block diagram (for isolated DIP8 designs)

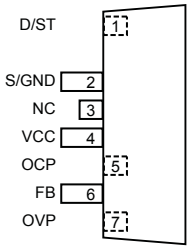
Pin-out Diagram (LC552xD)



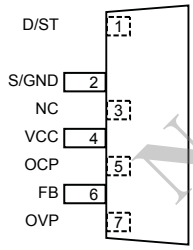
LC552xD Series Pin List Table

Number	Name	Function
1	S/GND	MOSFET source and GND pin for the Control Part
2	VCC	Supply voltage input and Overvoltage protection (OVP) signal input
3	OCP	Overcurrent Protection, quasi-resonant signal input pin, and Overvoltage Protection (OVP) signal input
4	FB	Feedback signal input and Overload Protection (OLP) signal input
5	NF	No function; must be externally connected to S/GND pin with as short a trace as possible, for stable operation of the IC
6	OVP	Overvoltage Protection (OVP) signal input
7	–	Pin removed
8	D/ST	MOSFET drain pin and input of the startup current

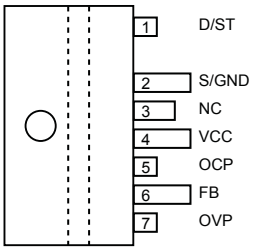
Pin-out Diagrams (LC552xF)



(LF 3051)



(LF 3052)



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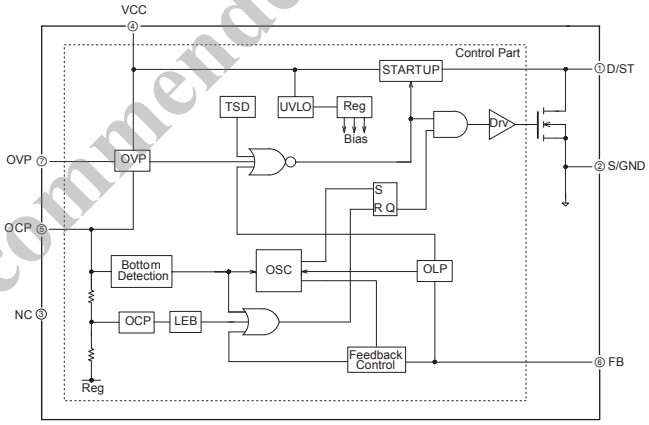


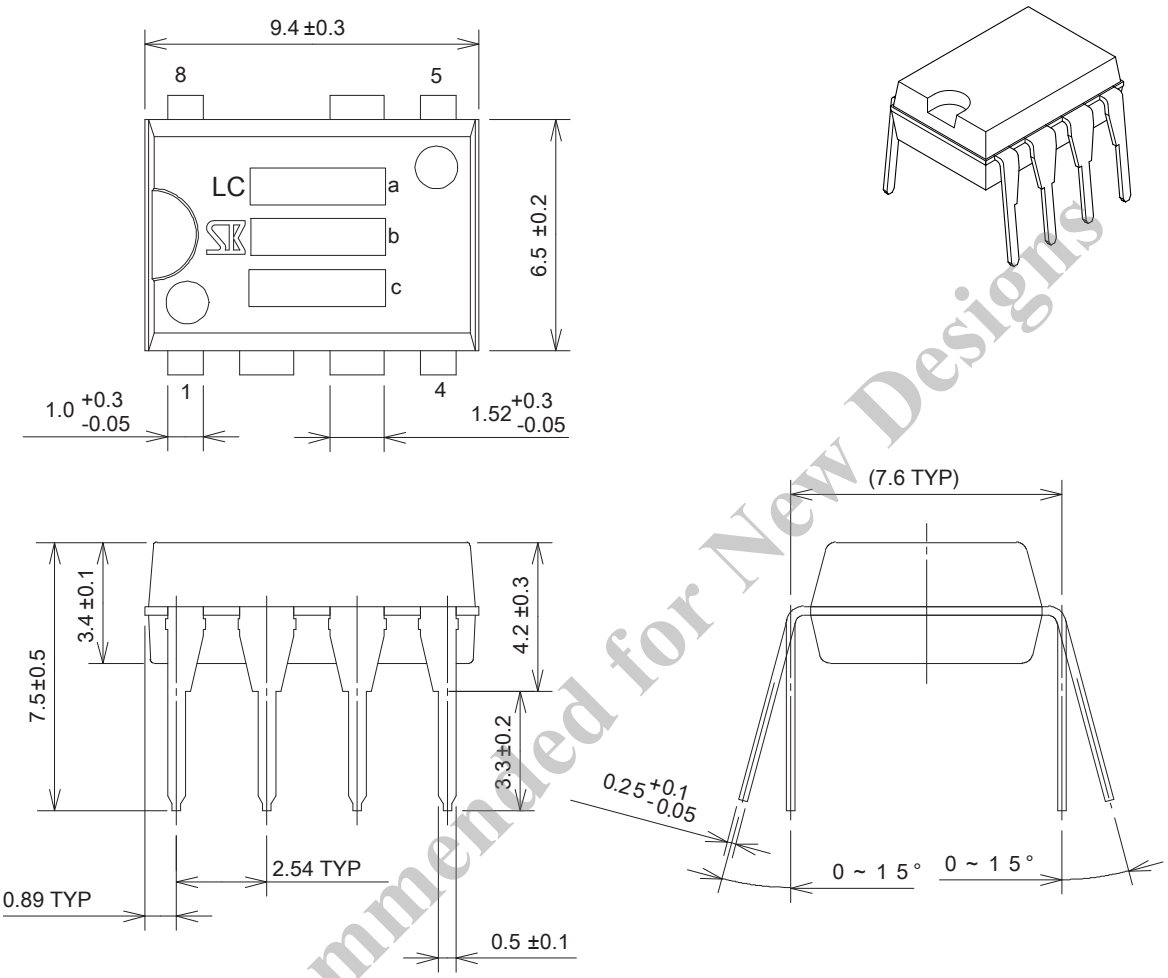
Figure 4. LC552xF series functional block diagram (for isolated TO-220F-7L designs)

LC552xF Series Pin List Table

Number	Name	Function
1	D/ST	MOSFET drain pin and input of the startup current
2	S/GND	MOSFET source and GND pin for the Control Part
3	NC	No connection
4	VCC	Supply voltage input and Overvoltage protection (OVP) signal input
5	OCP	Overcurrent Protection, quasi-resonant signal input pin, and Overvoltage Protection (OVP) signal input
6	FB	Feedback signal input and Overload Protection (OLP) signal input
7	OVP	Overvoltage Protection (OVP) signal input

Package Drawings

This section provides dimensioned drawings of the DIP8 and the TO-220-7L packages.

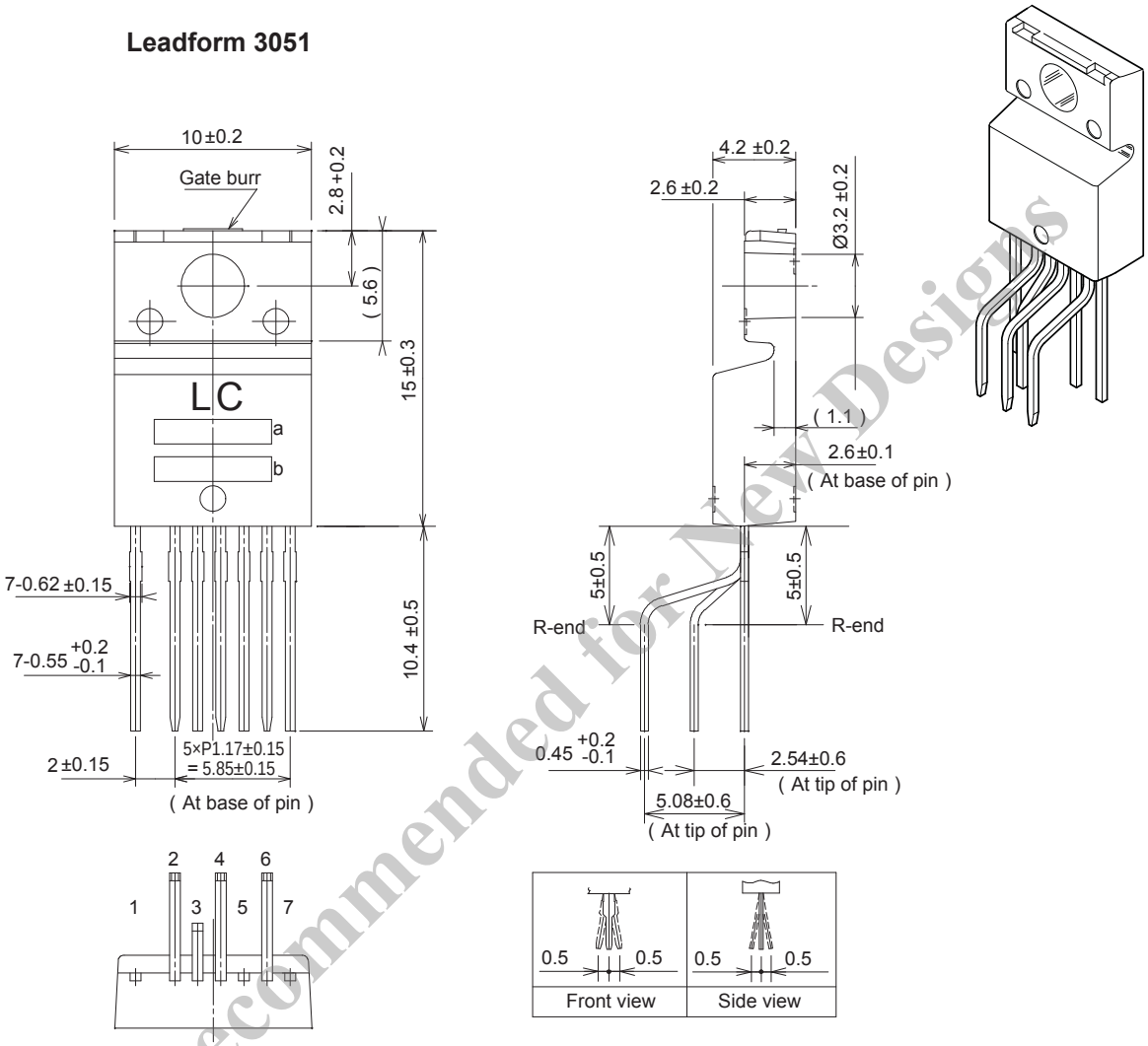


Unit: mm

a: Part #: 55xx
b: Lot number 3 digits, plus D
1st letter: Last digit of year
2nd letter: Month
Jan to September: Numeric
October: O
November: N
December: D
3rd letter: Week
Date 1 to 10: 1
Date 11 to 20: 2
Date 21 to 31: 3
c: Sanken control number

Pb-free. Device composition compliant with the RoHS directive.

Figure 5. DIP8 package drawing



Unit: mm
Package: TO-220F-7L

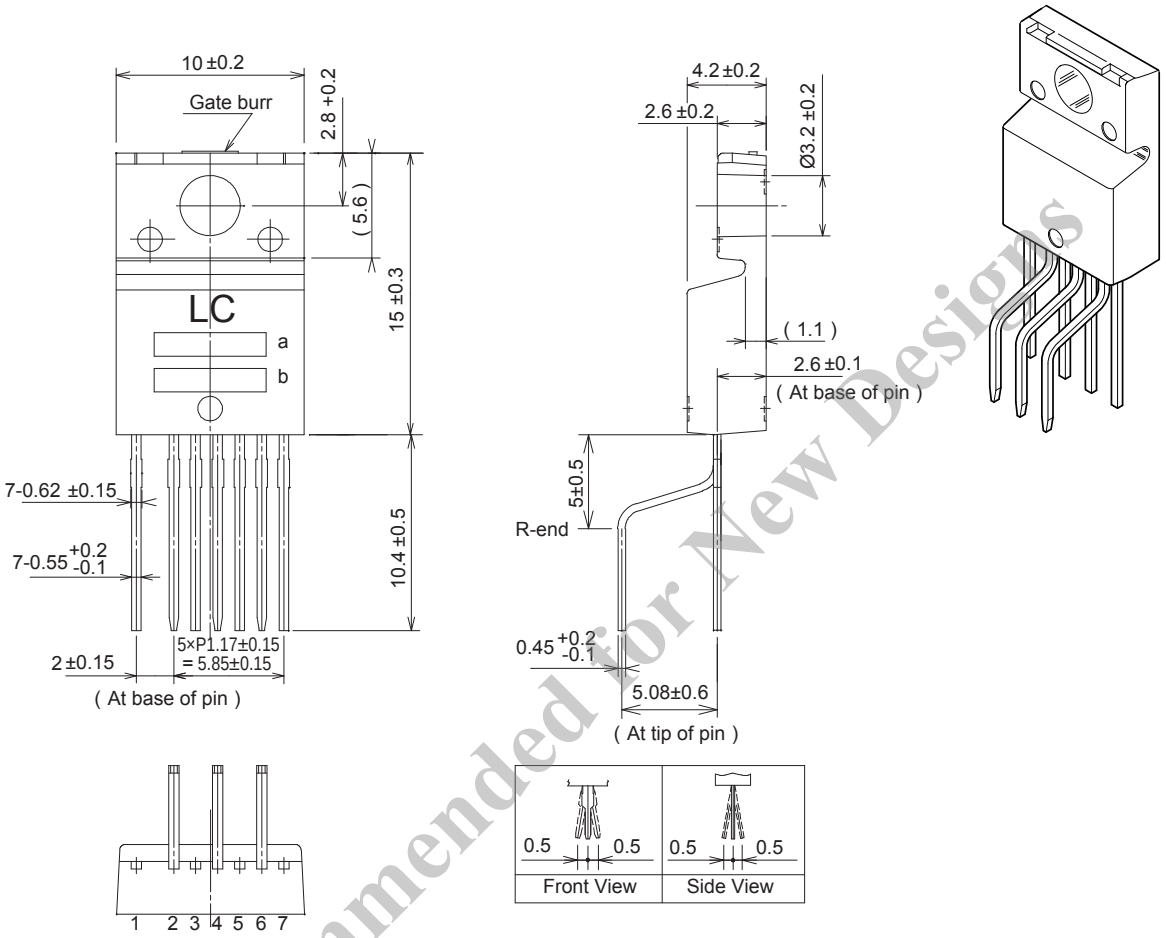
Note: "Gate Burr" shows area where 0.3 mm (max) gate burr may be present.

a: Part # 55xxF
b: Lot number
1st letter: Last digit of year
2nd letter: Month
Jan to September: Numeric
October: O
November: N
December: D
3rd and 4th letter: Date
01 to 31: Numeric
5th letter: Sanken control number

Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Figure 6. TO-220F-7L (Sanken leadform number 3051) package drawing

Leadform 3052



Unit: mm

Package: TO-220F-7L

Note: "Gate Burr" shows area where 0.3 mm (max) gate burr may be present.

a: Part # 55xxF

b: Lot number

1st letter: Last digit of year

2nd letter: Month

Jan to September: Numeric

October: O

November: N

December: D

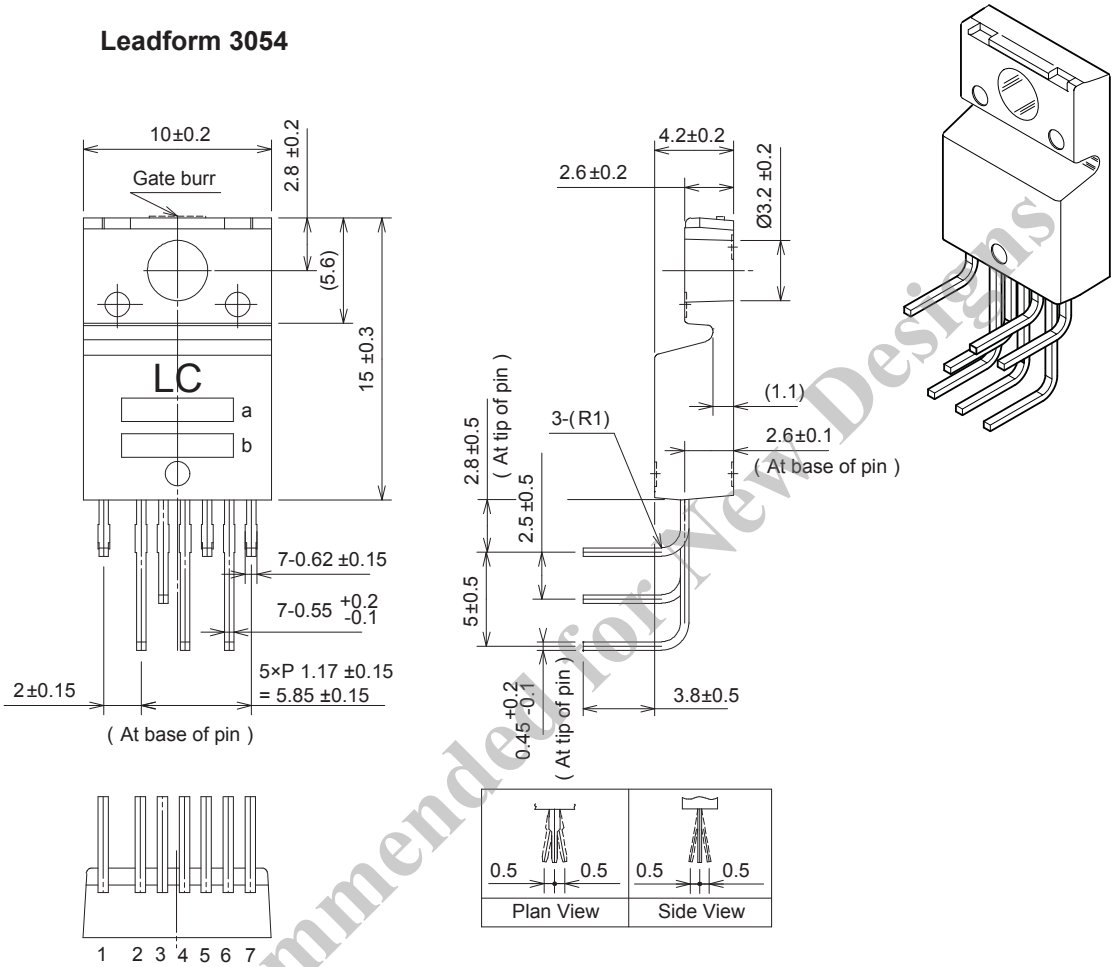
3rd and 4th letter: Date

01 to 31: Numeric

5th letter: Sanken control number

Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Figure 7. TO-220F-7L (Sanken leadform number 3052) package drawing



Unit: mm

Package: TO-220F-7L

Note: "Gate Burr" shows area where 0.3 mm (max) gate burr may be present.

a: Part # 55xxF

b: Lot number

1st letter: Last digit of year

2nd letter: Month

Jan to September: Numeric

October: O

November: N

December: D

3rd and 4th letter: Date

01 to 31: Numeric

5th letter: Sanken control number

Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Figure 8. TO-220F-7L (Sanken leadform number 3054) package drawing

Electrical Characteristics

- This section provides separate sets of electrical characteristic data for each product.
- The polarity value for current specifies a sink as "+ ," and a source as "−," referencing the IC.
- Please refer to the datasheet of each product for additional details.

LC551xD Absolute Maximum Ratings T_A = 25°C, unless otherwise specified

Characteristic	Symbol	Notes		Pins	Rating	Unit
Drain Current	I_{DPeak}	LC5511D	Single pulse	8 – 1	2.5	A
		LC5513D	Single pulse	8 – 1	4.0	A
Single Pulse Avalanche Energy	E_{AS}	LC5511D	I_{LPeak} = 2.0 A, V_{DD} = 99 V, L = 20 mH	8 – 1	47	mJ
		LC5513D	I_{LPeak} = 2.7 A, V_{DD} = 99 V, L = 20 mH	8 – 1	86	mJ
Control Part Input Voltage	V_{CC}			2 – 1	35	V
OCP Pin Voltage	V_{OCP}			3 – 1	−2.0 to 5.0	V
COMP Pin Voltage	V_{COMP}			4 – 1	−0.3 to 7.0	V
ISENSE Pin Voltage	V_{SEN}			6 – 1	−0.3 to 5.0	V
Allowable Power Dissipation of MOSFET*	P_{D1}			8 – 1	0.97	W
Operating Ambient Temperature	T_{OP}			—	−55 to 125	°C
Storage Temperature	T_{stg}			—	−55 to 125	°C
Channel Temperature	T_{ch}			—	150	°C

*Mounted on a 15 mm × 15 mm PCB.

LC551xD ELECTRICAL CHARACTERISTICS of MOSFET T_A = 25°C, unless otherwise specified

Characteristic	Symbol	Test Conditions		Pins	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V_{DSS}			8 – 1	650	—	—	V
Drain Leakage Current	I_{DSS}			8 – 1	—	—	300	μA
On Resistance	$R_{DS(on)}$	LC5511D		8 – 1	—	—	3.95	Ω
		LC5513D		8 – 1	—	—	1.9	Ω
Switching Time	t_f	LC5511D		8 – 1	—	—	250	ns
		LC5513D		8 – 1	—	—	400	ns
Thermal Resistance*	$R_{\theta ch\text{-}c}$	LC5511D		—	—	—	42	°C/W
		LC5513D		—	—	—	35.5	°C/W

*The thermal resistance between the channels of the MOSFET and the case. T_C measured at the center of the case top surface.

LC551xD ELECTRICAL CHARACTERISTICS of Control Part T_A = 25°C, V_{CC} = 20 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Unit
Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		2 – 1	13.8	15.1	17.3	V
Operation Stop Voltage*	$V_{CC(OFF)}$		2 – 1	8.4	9.4	10.7	V
Operating Current	$I_{CC(ON)}$		2 – 1	–	–	3.7	mA
Startup Circuit Operation Voltage	$V_{STARTUP}$		8 – 1	42	57	72	V
Startup Current	$I_{CC(STARTUP)}$	V_{CC} = 13 V	2 – 1	−5.5	−3.0	−1.0	mA
Startup Current Threshold Biasing Voltage-1*	$V_{CC(BIAS)1}$		2 – 1	9.5	11.0	12.5	V
Startup Current Threshold Biasing Voltage-2	$V_{CC(BIAS)2}$		2 – 1	14.4	16.6	18.8	V
Normal Operation							
PWM Operation Frequency	f_{OSC}		8 – 1	11.0	14.0	18.0	kHz
Maximum On-Time	$t_{ON(MAX)}$		8 – 1	30.0	40.0	50.0	µs
COMP Pin Control Voltage Lower Limit	$V_{COMP(MIN)}$		4 – 1	0.55	0.90	1.25	V
Error Amplifier Reference Voltage	$V_{SEN(TH)}$		6 – 1	0.27	0.30	0.33	V
Error Amplifier Source Current	$I_{SEN(SOURCE)}$		4 – 1	−11	−7	−3	µA
Error Amplifier Sink Current	$I_{SEN(SINK)}$		4 – 1	3	7	11	µA
Leading Edge Blanking Time	$t_{ON(LEB)}$		3 – 1	−	500	−	ns
Quasi-Resonant Operation Threshold Voltage-1	$V_{BD(TH1)}$		3 – 1	0.14	0.24	0.34	V
Quasi-Resonant Operation Threshold Voltage-2	$V_{BD(TH2)}$		3 – 1	0.12	0.17	0.22	V
Protection Operation							
OCP Pin Overcurrent Protection (OCP) Threshold Voltage	V_{OCP}		3 – 1	−0.66	−0.60	−0.54	V
OCP Pin Source Current	I_{OCP}		3 – 1	−120	−40	−10	µA
OCP Pin Overvoltage Protection (OVP) Threshold Voltage	$V_{BD(OVP)}$		3 – 1	2.2	2.6	3.0	V
Overload Protection (OLP) Threshold Voltage-1	$V_{COMP(OLP)1}$		4 – 1	5.0	5.5	6.0	V
Overload Protection (OLP) Threshold Voltage-2	$V_{COMP(OLP)2}$		4 – 1	4.1	4.5	4.9	V
ISENSE Pin OVP Threshold Voltage	$V_{SEN(OVP)}$		6 – 1	1.6	2.0	2.4	V
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 1	28.5	31.5	34.0	V
Thermal Shutdown Activating Temperature	$T_{J(TSD)}$		–	135	–	–	°C

*$V_{CC(BIAS)1}$ > $V_{CC(OFF)}$ always.

LC552xD Absolute Maximum Ratings T_A = 25°C, unless otherwise specified

Characteristic	Symbol	Notes		Pins	Rating	Unit
Drain Current	I_{DPeak}	LC5521D	Single pulse	8 – 1	2.5	A
		LC5523D		8 – 1	4.0	A
Single Pulse Avalanche Energy	E_{AS}	LC5521D	I_{LPeak} = 2.0 A, V_{DD} = 99 V, L = 20 mH	8 – 1	47	mJ
		LC5523D	I_{LPeak} = 2.7 A, V_{DD} = 99 V, L = 20 mH	8 – 1	86	mJ
Control Part Input Voltage	V_{CC}			2 – 1	35	V
OCP Pin Voltage	V_{OCP}			3 – 1	−2.0 to 5.0	V
FB Pin Voltage	V_{FB}			4 – 1	−0.3 to 7.0	V
OVP Pin Voltage	V_{OVP}			6 – 1	−0.3 to 5.0	V
Allowable Power Dissipation of MOSFET*	P_{D1}			8 – 1	0.97	W
Operating Ambient Temperature	T_{OP}			—	−55 to 125	°C
Storage Temperature	T_{stg}			—	−55 to 125	°C
Channel Temperature	T_{ch}			—	150	°C

*Mounted on a 15 mm × 15 mm PCB.

LC552xD ELECTRICAL CHARACTERISTICS of MOSFET T_A = 25°C, unless otherwise specified

Characteristic	Symbol	Test Conditions		Pins	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V_{DSS}			8 – 1	650	—	—	V
Drain Leakage Current	I_{DSS}			8 – 1	—	—	300	μA
On Resistance	$R_{DS(on)}$	LC5521D		8 – 1	—	—	3.95	Ω
		LC5523D		8 – 1	—	—	1.9	Ω
Switching Time	t_f	LC5521D		8 – 1	—	—	250	ns
		LC5523D		8 – 1	—	—	400	ns
Thermal Resistance*	$R_{\theta ch-c}$	LC5521D		8 – 1	—	—	42	°C/W
		LC5523D		—	—	—	35.5	°C/W

*The thermal resistance between the channels of the MOSFET and the case. T_C measured at the center of the case top surface.

LC552xD ELECTRICAL CHARACTERISTICS of Control Part T_A = 25°C, V_{CC} = 20 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Unit
Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		2 – 1	13.8	15.1	17.3	V
Operation Stop Voltage*	$V_{CC(OFF)}$		2 – 1	8.4	9.4	10.7	V
Operating Current	$I_{CC(ON)}$		2 – 1	–	–	3.7	mA
Startup Circuit Operation Voltage	$V_{STARTUP}$		8 – 1	42	57	72	V
Startup Current	$I_{CC(STARTUP)}$	V_{CC}= 13 V	2 – 1	−5.5	−3.0	−1.0	mA
Startup Current Threshold Biasing Voltage-1*	$V_{CC(BIAS)1}$		2 – 1	9.5	11.0	12.5	V
Startup Current Threshold Biasing Voltage-2	$V_{CC(BIAS)2}$		2 – 1	14.4	16.6	18.8	V
Normal Operation							
PWM Operation Frequency	f_{OSC}		8 – 1	11.0	14.0	18.0	kHz
Maximum On-Time	$t_{ON(MAX)}$		8 – 1	30.0	40.0	50.0	µs
FB Pin Voltage Minimum Limit	$V_{FB(MIN)}$		4 – 1	0.55	0.90	1.25	V
Maximum Feedback Current	$I_{FB(MAX)}$		4 – 1	−40	−25	−10	µA
Leading Edge Blanking Time	$t_{ON(LEB)}$		3 – 1	−	500	−	ns
Quasi-Resonant Operation Threshold Voltage-1	$V_{BD(TH1)}$		3 – 1	0.14	0.24	0.34	V
Quasi-Resonant Operation Threshold Voltage-2	$V_{BD(TH2)}$		3 – 1	0.12	0.17	0.22	V
Protection Operation							
OCP Pin Overcurrent Protection (OCP) Threshold Voltage	V_{OCP}		3 – 1	−0.66	−0.60	−0.54	V
OCP Pin Source Current	I_{OCP}		3 – 1	−120	−40	−10	µA
OCP Pin Overvoltage Protection (OVP) Threshold Voltage	$V_{BD(OVP)}$		3 – 1	2.2	2.6	3.0	V
Overload Protection (OLP) Threshold Voltage-1	$V_{FB(OLP)1}$		4 – 1	5.0	5.5	6.0	V
Overload Protection (OLP) Threshold Voltage-2	$V_{FB(OLP)2}$		4 – 1	4.1	4.5	4.9	V
OVP Pin OVP Threshold Voltage	$V_{OVP(OVP)}$		6 – 1	1.6	2.0	2.4	V
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 1	28.5	31.5	34.0	V
Thermal Shutdown Activating Temperature	$T_{J(TSD)}$		–	135	–	–	°C

*$V_{CC(BIAS)1}$ > $V_{CC(OFF)}$ always.

LC552xF Absolute Maximum Ratings T_A = 25°C, unless otherwise specified

Characteristic	Symbol	Notes		Pins	Rating	Unit
Drain Current	I_{DPeak}	LC5523F	Single pulse	1 – 2	9.2	A
		LC5525F		1 – 2	13.0	A
Single Pulse Avalanche Energy	E_{AS}	LC5523F	I_{LPeak} = 2.9 A, V_{DD} = 99 V, L = 20 mH	1 – 2	99	mJ
		LC5525F	I_{LPeak} = 4.4 A, V_{DD} = 99 V, L = 20 mH	1 – 2	233	mJ
Control Part Input Voltage	V_{CC}			4 – 2	35	V
OCP Pin Voltage	V_{OCP}			5 – 2	−2.0 to 5.0	V
FB Pin Voltage	V_{FB}			6 – 2	−0.3 to 7.0	V
OVP Pin Voltage	V_{OVP}			7 – 2	−0.3 to 5.0	V
Allowable Power Dissipation of MOSFET	P_{D1}	LC5523F	With infinite heatsink	1 – 2	20.2	W
		LC5525F		1 – 2	23.6	W
		Without heatsink		1 – 2	1.8	W
Internal Frame Temperature in Operation	T_F			—	−20 to 115	°C
Operating Ambient Temperature	T_{OP}			—	−55 to 115	°C
Storage Temperature	T_{stg}			—	−55 to 125	°C
Channel Temperature	T_{ch}			—	150	°C

LC552xF ELECTRICAL CHARACTERISTICS of MOSFET T_A = 25°C, unless otherwise specified

Characteristic	Symbol	Test Conditions		Pins	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V_{DSS}			1 – 2	650	—	—	V
Drain Leakage Current	I_{DSS}			1 – 2	—	—	300	μA
On Resistance	$R_{DS(on)}$	LC5523F		1 – 2	—	—	1.9	Ω
		LC5525F		1 – 2	—	—	1.1	Ω
Switching Time	t_f			1 – 2	—	—	400	ns
Thermal Resistance	$R_{\theta ch-F}$	LC5523F	Between channel and internal frame	—	—	—	3.1	°C/W
		LC5525F		—	—	—	2.2	°C/W

LC5523xF ELECTRICAL CHARACTERISTICS of Control Part T_A = 25°C, V_{CC} = 20 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Unit
Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		4 – 2	13.8	15.1	17.3	V
Operation Stop Voltage*	$V_{CC(OFF)}$		4 – 2	8.4	9.4	10.7	V
Operating Current	$I_{CC(ON)}$		4 – 2	–	–	3.7	mA
Startup Circuit Operation Voltage	$V_{STARTUP}$		1 – 2	42	57	72	V
Startup Current	$I_{CC(STARTUP)}$	V_{CC} = 13 V	4 – 2	−5.5	−3.0	−1.0	mA
Startup Current Threshold Biasing Voltage-1*	$V_{CC(BIAS)1}$		4 – 2	9.5	11.0	12.5	V
Startup Current Threshold Biasing Voltage-2	$V_{CC(BIAS)2}$		4 – 2	14.4	16.6	18.8	V
Normal Operation							
PWM Operation Frequency	f_{OSC}		1 – 2	11.0	14.0	18.0	kHz
Maximum On-Time	$t_{ON(MAX)}$		1 – 2	30.0	40.0	50.0	µs
FB Pin Voltage Minimum Limit	$V_{FB(MIN)}$		6 – 2	0.55	0.90	1.25	V
Maximum Feedback Current	$I_{FB(MAX)}$		6 – 2	−40	−25	−10	µA
Leading Edge Blanking Time	$t_{ON(LEB)}$		5 – 2	–	500	–	ns
Quasi-Resonant Operation Threshold Voltage-1	$V_{BD(TH1)}$		5 – 2	0.14	0.24	0.34	V
Quasi-Resonant Operation Threshold Voltage-2	$V_{BD(TH2)}$		5 – 2	0.12	0.17	0.22	V
Protection Operation							
OCP Pin Overcurrent Protection (OCP) Threshold Voltage	V_{OCP}		5 – 2	−0.66	−0.60	−0.54	V
OCP Pin Source Current	I_{OCP}		5 – 2	−120	−40	−10	µA
OCP Pin Overvoltage Protection (OVP) Threshold Voltage	$V_{BD(OVP)}$		5 – 2	2.2	2.6	3.0	V
Overload Protection (OLP) Threshold Voltage-1	$V_{FB(OLP)1}$		6 – 2	5.0	5.5	6.0	V
Overload Protection (OLP) Threshold Voltage-2	$V_{FB(OLP)2}$		6 – 2	4.1	4.5	4.9	V
OVP Pin OVP Threshold Voltage	$V_{OVP(OVP)}$		7 – 2	1.6	2.0	2.4	V
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		4 – 2	28.5	31.5	34.0	V
Thermal Shutdown Activating Temperature	$T_{J(TSD)}$		–	135	–	–	°C

*$V_{CC(BIAS)1}$ > $V_{CC(OFF)}$ always.

Application Circuit Examples

This section provides typical application circuits for LED lighting.

- LC551xD series (non-isolated)
- LC552xD series (isolated)
- LC552xF series (isolated)

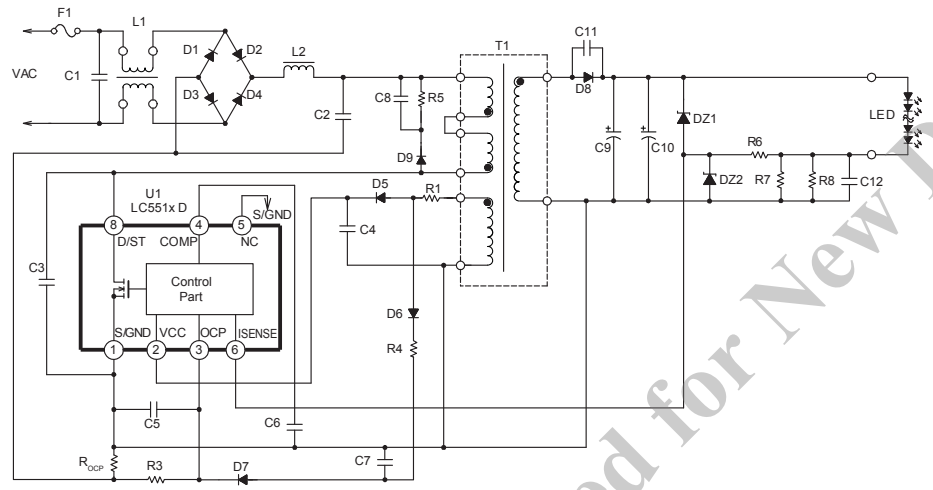


Figure 9. Non-isolated application circuit example, with LC551xD series device

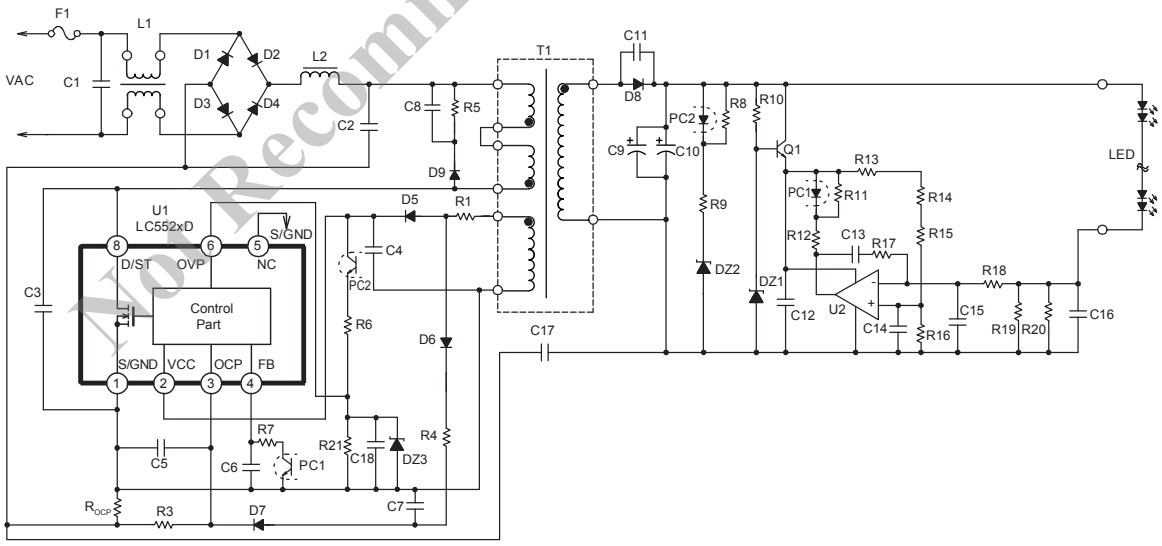


Figure 10. Isolated application circuit example, with LC552xD series device

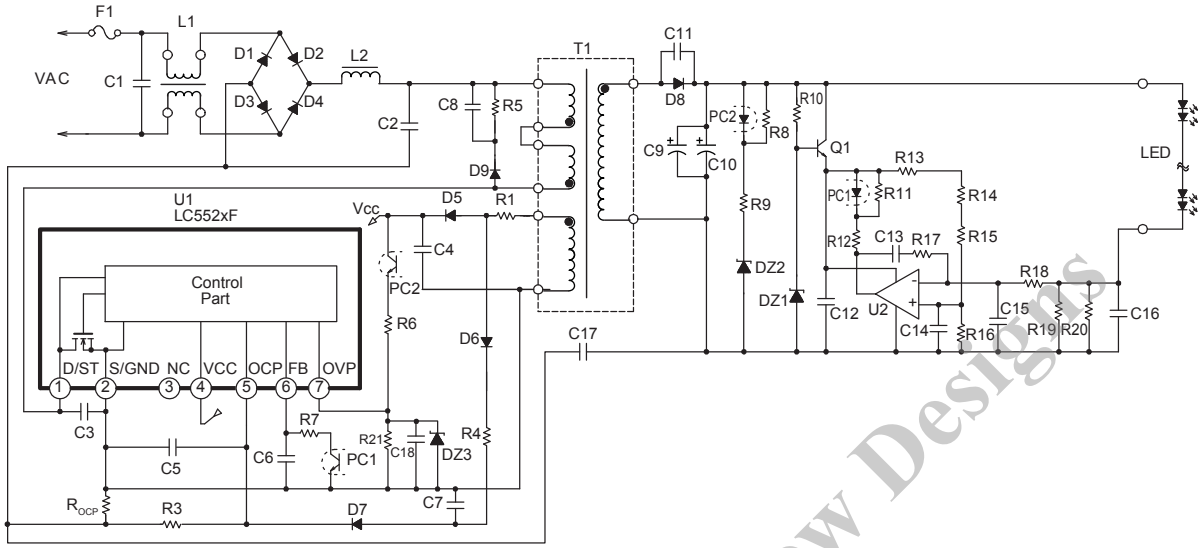


Figure 11. Isolated application circuit example, with LC552xF series device

Functional Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. This section describes IC operations as it is used for LED lighting power supply applications. About current direction, "+" indicates sink current toward the IC and "–" indicates source current from the IC. The pin numbers parenthesized represent LC552xF numbers.

On-Time Control Operation

LC551xD series (non-isolated designs) Figure 12 shows the peripheral circuit at the COMP pin of the LC551xD, and figure 13 shows the on-time control. The output control is done by voltage mode control, which controls on-time depending on output load, and average current control.

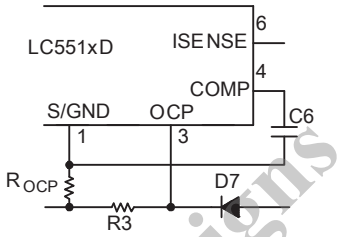


Figure 12. COMP pin peripheral circuit

As showed in figure 13, in the average current control operation, the output current detection resistor voltage is compared against the reference voltage, $V_{SEN(TH)}$ = 0.3 V, by the OTA circuit, and its output is averaged at COMP pin. This voltage is compared against the internal oscillator (OSC) by the FB comparator in order to control the on-time for the average current control operation. Here, OSC indicates the oscillator circuit, which controls the PWM operation frequency, quasi-resonant oscillation, and the maximum on-time limit.

For the LC551xD devices, the recommended value of C6, which is connected to the COMP pin, is approximately 2.2 µF.

The value of R6 is approximately 1 kΩ.

The constant output current control of the output is done as below:

- When the output load current becomes less than the target value, the ISENSE pin voltage becomes low. This causes the averaged OTA circuit output voltage at the COMP pin to become high, which increases the on-time and the output current.
- When the output current becomes greater than the target value, the circuits operate in the opposite way. The averaged voltage at the COMP pin becomes low, and reductions result in the on-time and the output current.

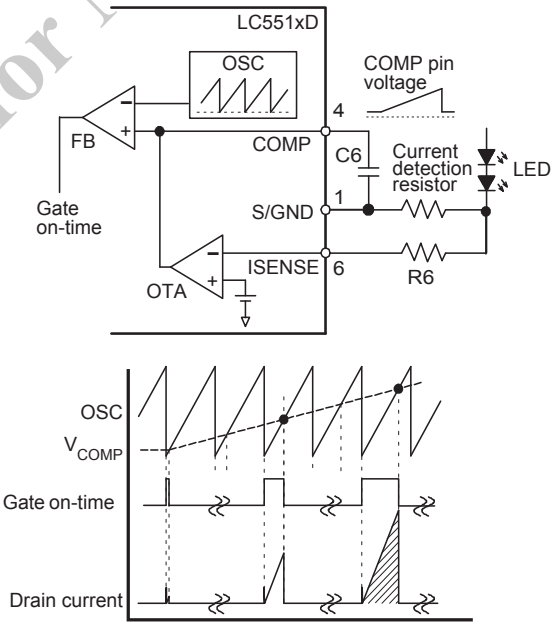


Figure 13. On-time control, LC551xD series

Figure 14 shows the average input current waveform. The averaged COMP pin voltage becomes constant, and the duty cycle is controlled according to the E_{IN} voltage (C2 voltage in figure 9). It makes an averaged input current sine waveform which realizes a high power factor.

LC552xD and LC552xF series (isolated designs) Figure 15 shows the peripheral circuit at the FB pin of the LC552xD/ LC552xF, and figure 16 shows the on-time control. The output

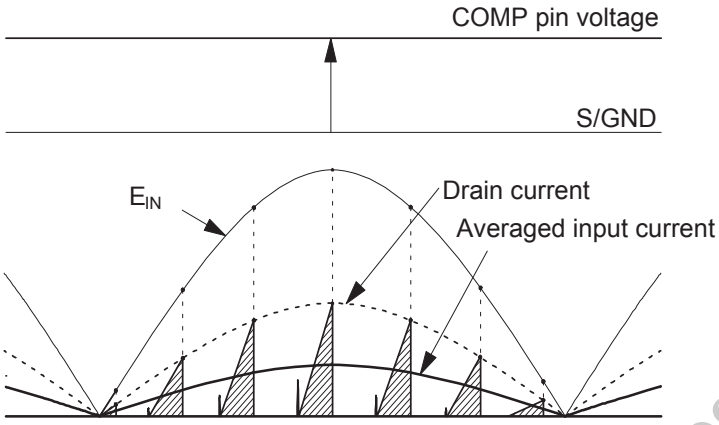


Figure 14. Averaged input current waveform, LC551xD series

control is done by voltage mode control, which controls on-time depending on output load, and average current control.

As showed in figure 16, in the average current control operation, the output current detection resistor voltage is compared by the operational amplifier, and its output is sent to the FB pin in conjunction with the opto-coupler and averaged at the FB pin. The FB pin voltage is compared against the internal oscillator (OSC) by the FB comparator in order to control the on-time for averaged current control operation. Here, OSC indicates the oscillator circuit, which controls the PWM operation frequency, quasi-resonant oscillation, and the maximum on-time limit. For the LC552xD and LC552xF series devices, the recommended value of C6, which is connected to the FB pin, is approximately 2.2 µF.

The constant output current control of the output is done as below.

- When the output load current becomes less than the target value, the secondary current detection resistor voltage becomes low and it results in low feedback current from the opto-coupler. It causes the averaged voltage at the FB pin to become high, and results in increases of the on-time and the output current.

- When the output current becomes more than the target value, the circuits operate in the opposite way The averaged voltage at the FB pin becomes low, which reduces the on-time and the output current.

Figure 17 shows the average input current waveform. The averaged FB pin voltage becomes constant, and the duty cycle is controlled according to the E_{IN} voltage (C2 voltage in figures 10 and 11). It makes an averaged input current sine waveform which realizes a high power factor.

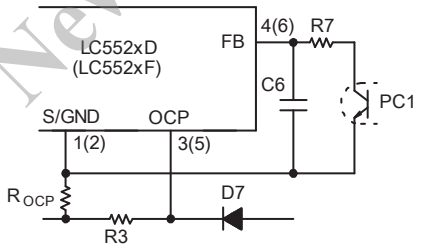


Figure 15. FB pin peripheral circuit

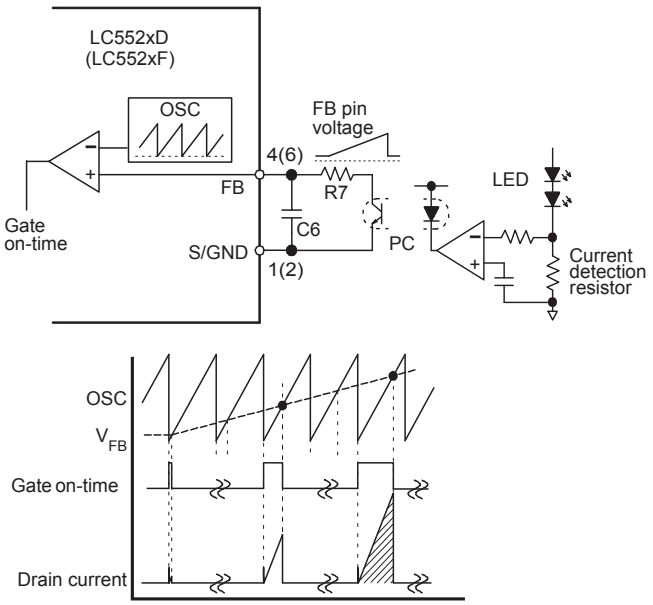


Figure 16. On-time control, LC552xD and LC552xF series

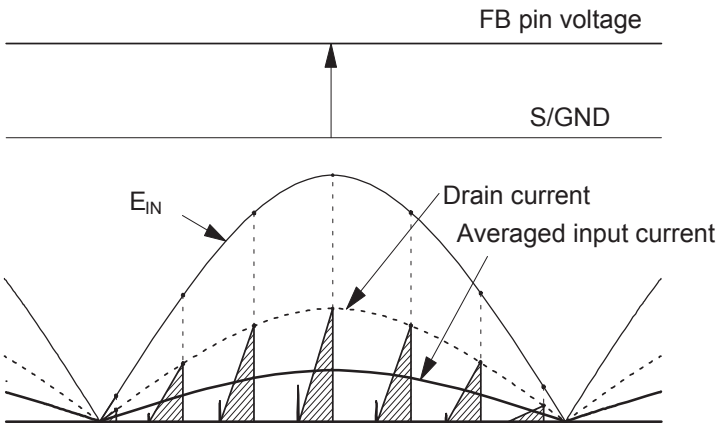


Figure 17. Averaged input current waveform, LC552xD and LC552xF series

Startup Operation

Figure 18 shows the VCC pin peripheral circuit. The integrated startup circuit is connected to the D/ST pin. When the D/ST pin voltage reaches $V_{STARTUP}$ = 57 V, the startup circuit is activated, and it generates a constant current, $I_{CC(STARTUP)}$ = –3.0 mA, to charge capacitor C4 at the VCC pin. During this process, when VCC voltage reaches $V_{CC(ON)}$ = 15.1 V, the IC starts operation, and when its voltage exceeds $V_{CC(BIAS)2}$ = 16.6 V, the startup circuit stops, in order to eliminate its own power consumption.

The startup time is determined by the C4 capacitance and is expressed by the formula below:

$$t_{START} \approx C_4 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{CC(STARTUP)}|} \quad (1)$$

where

t_{START} is the startup time (s), and

$V_{CC(INT)}$ is the VCC pin initial voltage (V).

A ceramic or film capacitor can be used for C4, and a value of 0.22 to 22 µF is generally recommended.

Figure 19 shows the relationship between VCC voltage and the operating current, I_{CC}. When VCC voltage reaches $V_{CC(ON)}$ = 15.1 V, the Control circuit operation begins and the operating current increases. After that, if VCC voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the Undervoltage Lockout (UVLO) circuit stops Control circuit operation, and the operation state returns to the startup phase.

After the IC starts operation, the rectified voltage from the auxiliary winding, D, of figure 18 becomes a power source to the IC in steady-state operation.

VCC voltage must satisfy these conditions:

$V_{CC(BIAS)1}(max) = 12.5\ V < V_{CC} < V_{CC(OVP)}(min) = 28.5\ V$

Initially, target 20 V in a transformer design, and then optimize its winding turns in a way that VCC voltage stays within the above range over the conceivable input voltage range and output load conditions.

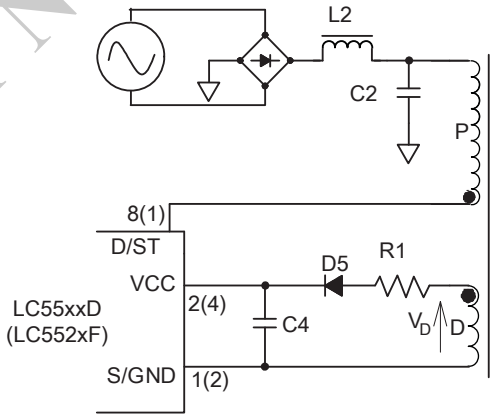


Figure 18. VCC pin peripheral circuit

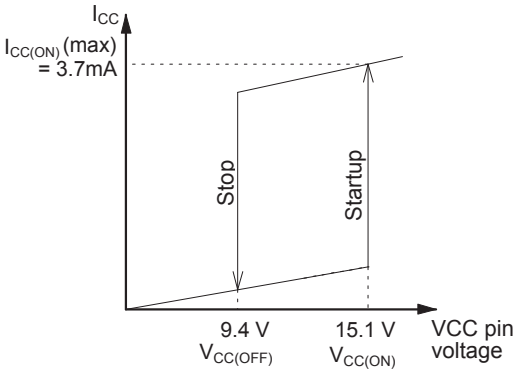


Figure 19. V_{CC} versus operation current, I_{CC}

Figure 20 shows the VCC voltage behavior at the startup phase. Immediately after the Control circuit starts operation, the auxiliary winding voltage, V_D, has not yet reached its design target value, which is determined by the transformer auxiliary winding turns. Therefore, as shown figure 20, VCC voltage starts decreasing after the startup circuit turns off at $V_{CC(BIAS)2}$ = 16.6 V. If the VCC voltage reaches $V_{CC(BIAS)1}$ = 11.0 V, the bias assisting function is activated before the voltage decreases to $V_{CC(OFF)}$ = 9.4 V. While the bias assist function is operating, any decrease of the VCC voltage is counteracted by a supplementary current from the startup circuit, and thus VCC is kept almost constant. Thanks to this function, the C4 value can be small, which results in shortening the startup period and improving the response time of the VCC pin overvoltage protection. It is necessary to check and adjust the process so that poor starting conditions may be avoided.

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output of the SMPS (see figure 21). This happens because C4 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the incorporated power MOSFET turns off.

For alleviating C4 peak charging, it is effective to add some value R1, of several tenths of ohms to several ohms, in series with D5 (see figure 22). The optimal value of R1 should be determined using a transformer matching what will be used in the actual application, because the proportion of the VCC pin voltage versus the transformer output voltage differs according to transformer structural design.

Fluctuation of V_{CC} by I_{OUT} worsens in the following cases, requiring a transformer designer to pay close attention to the placement of the auxiliary winding D:

- Poor coupling between the primary and secondary windings (this causes high surge voltage and is seen in a design with low output voltage and high output current).
- Poor coupling between the auxiliary winding D and the secondary stabilized output winding where the output line voltage is controlled constant by the output voltage feedback (this is susceptible to surge voltage).

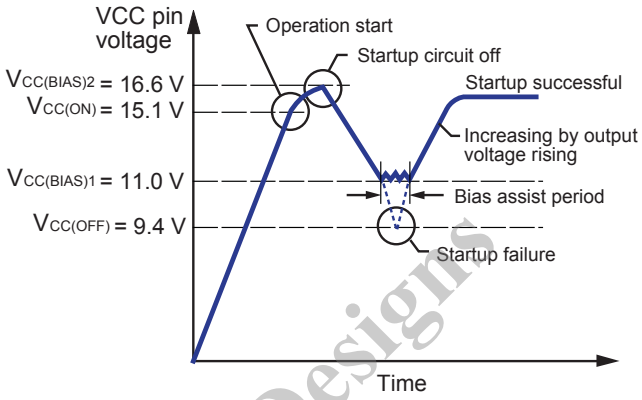


Figure 20. V_{CC} at startup period

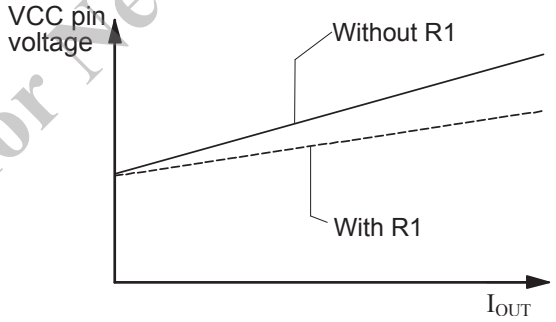


Figure 21. V_{CC} versus I_{OUT} with and without resistor R1

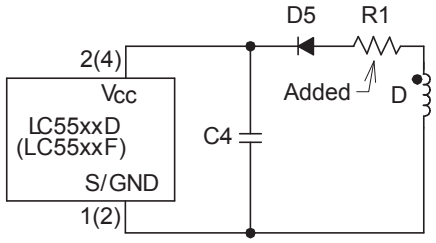


Figure 22. VCC pin peripheral circuit with R1

Figure 23 shows two transformer design examples considered the winding location of the auxiliary winding D to minimize impact of VCC surge voltage. Triple insulation wires are used for either the primary or secondary winding, and thus no margin-tape is used:

- Separate the auxiliary winding D from the primary windings P1 and P2 (figure 23 (A)); P1 and P2 are two separated primary windings.
- Place the auxiliary winding D within the secondary winding S1 in order to improve the coupling of those windings (figure 23 (B)); S1 is the secondary output winding.

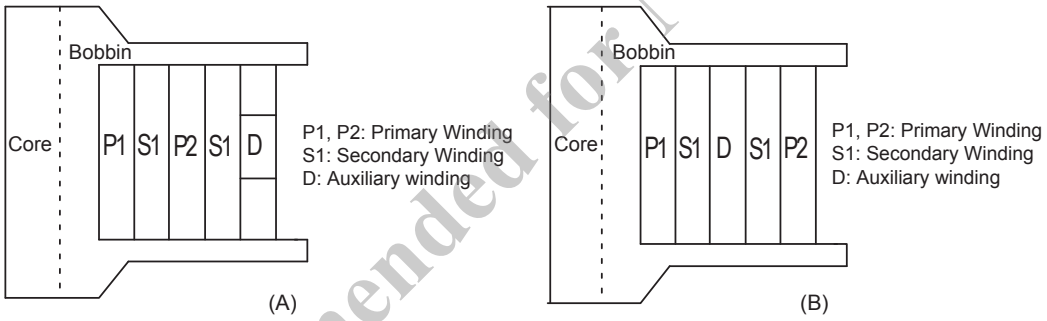


Figure 23. Transformer winding structures

Operation Modes at Startup

Figure 24 shows the operation modes during the startup phase of the LC551xD, and figure 25 shows those for the LC552xD and LC552xF. Note that OCP pin voltage, which determines the timing of quasi-resonant operation, is in positive voltage on the OCP pin, in reference to the S/GND pin.

During two periods below at startup, IC operation is set to PWM, with f_{OSC} = 14 kHz:

- While the COMP pin voltage (for LC551xD) and FB pin voltage (for LC552xD and LC552xF), in reference to S/GND, are 0 to 0.9 V (the control voltage lower limit for the COMP pin, $V_{COMP(MIN)}$, and FB pin, $V_{FB(MIN)}$): During this period, on-time is fixed at the Leading Edge Blanking Time, t_{BW} = 500 ns.
- Until the quasi-resonant signal (OCP pin voltage) reaches the Quasi-Resonant Operation Threshold Voltage-1, $V_{BD(TH1)}$= 0.24 V: During this period, the output voltage is low; therefore, the auxiliary winding voltage, V_D, is low. Thus the quasi-resonant signal is low.

After those startup operations the output voltage starts increasing, when the OCP pin voltage reaches $V_{BD(TH1)}$ = 0.24 V, the IC is switched to quasi-resonant operation (figure 26).

Soft-Start Function

The soft-start function reduces power stress on the incorporated MOSFET and secondary rectifier during the startup phase.

LC551xD series (non-isolated designs) The soft-start operation begins when the COMP pin voltage reaches $V_{COMP(MIN)}$ = 0.9 V and lasts until the output current becomes constant. During that period, the output power gradually increases.

During this period, check the items below:

- VCC pin voltage does not drop to the Operation Stop Voltage, $V_{CC(OFF)}$
- Output current reaches the target value before the overload protection (OLP) is activated by the COMP pin voltage reaching $V_{COMP(OLP)2}$ = 4.5 V

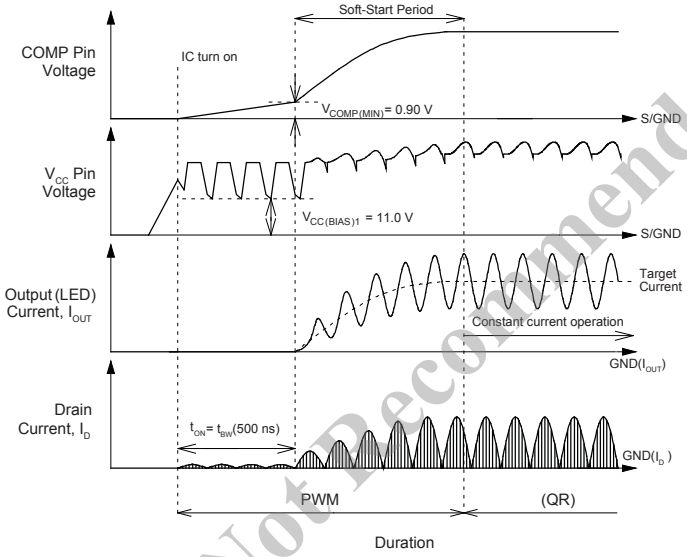


Figure 24. Soft-start operation waveforms at startup (LC551xD)

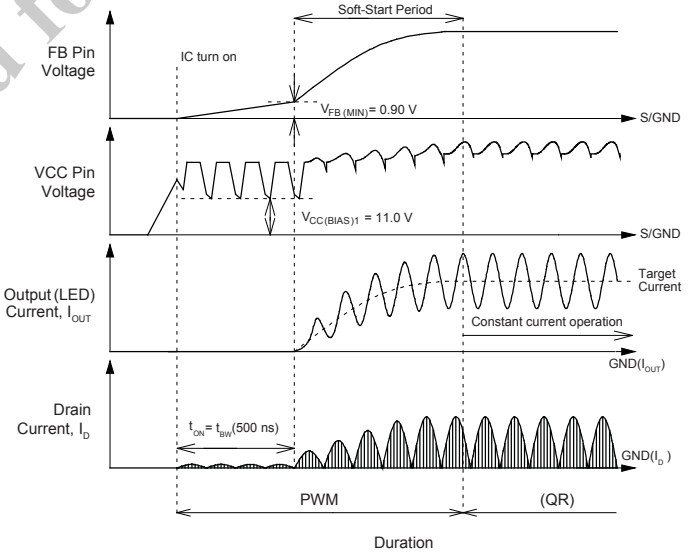


Figure 25. Soft-start operation waveforms at startup (LC552xD/ LC552xF)

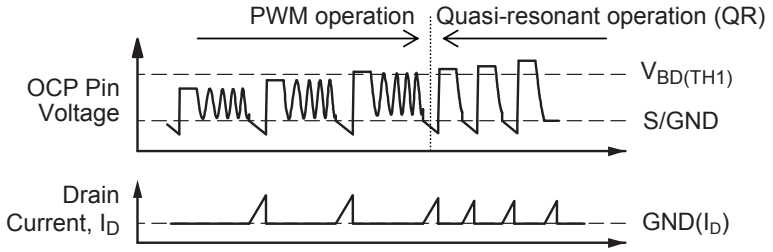


Figure 26. OCP Pin Voltage (with time scale expanded)

LC552xD/LC552xF series (isolated designs) The soft-start operation begins when the FB pin voltage reaches $V_{FB(MIN)}$ = 0.9 V and lasts until the output current becomes constant. During that period, the output power gradually increases.

During this period, check the items below:

- VCC pin voltage does not drop to the Operation Stop Voltage, $V_{CC(OFF)}$
- Output current reaches the target value before the overload protection (OLP) is activated by the FB pin voltage reaching $V_{FB(OLP)2}$ = 4.5 V

Quasi-Resonant Operation and Bottom-On Timing

Figure 27 shows a basic circuit diagram of a flyback converter, in which the energy of the transformer is transferred to the secondary side after the primary side MOSFET turns off.

When the primary side MOSFET keeps turning off after the energy is transferred to the secondary, the MOSFET drain node begins free oscillation based on the transformer L_P, and C_V across the drain and source pins, after the energy is completely transferred to the secondary. The quasi-resonant operation is the V_{DS} bottom-on operation that turns on the MOSFET at the bottom point of V_{DS} free oscillation. Because of that, switching loss and switching noise are reduced. Therefore, highly efficient and low noise converters can be realized. Figure 28 shows an ideal V_{DS} waveform of this mode. Turning on the MOSFET at the bottom of V_{DS} is done by creating certain duration, delay time t_{ONDLY}, as figure 28 shows from the start of V_{DS} free oscillation. This delay time is created by exploiting the auxiliary winding voltage, which synchronizes to the drain voltage V_{DS} waveform and it is called the quasi-resonant signal.

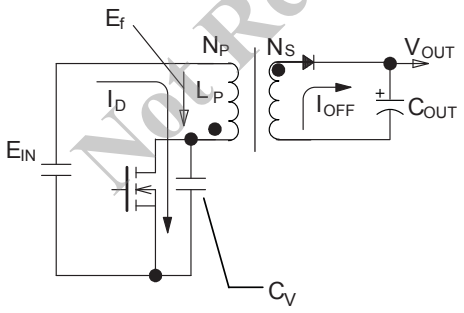


Figure 27. Basic flyback converter circuit

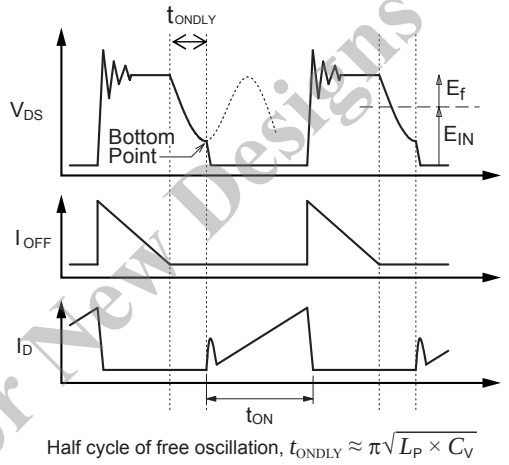


Figure 28. Ideal bottom-on operation waveform (MOSFET turn-on at a bottom point of a V_{DS} waveform)

E_{IN}: Input voltage

E_f: Flyback voltage

$$E_f = \frac{N_P}{N_S} \times (V_{OUT} + V_f) \quad (2)$$

N_P: Number of turns in the primary winding

N_S: Number of turns in the secondary winding

V_{OUT}: Output voltage

V_f: Forward voltage of the secondary rectifier

I_D: Drain current of the power MOSFET

I_{OFF}: Current running through the secondary rectifier during the power MOSFET off-period

C_V: Voltage resonant capacitor

L_P: Primary inductance

Figure 29 shows the OCP pin peripheral circuit. D6, R4, C7 and D7 form a delay circuit, and the auxiliary winding flyback voltage, E_{rev1}, is fed through the delay circuit and provides positive voltage, the quasi-resonant signal (V_{BD}), to the OCP pin. Figure 30 shows the auxiliary winding voltage and quasi-resonant signal.

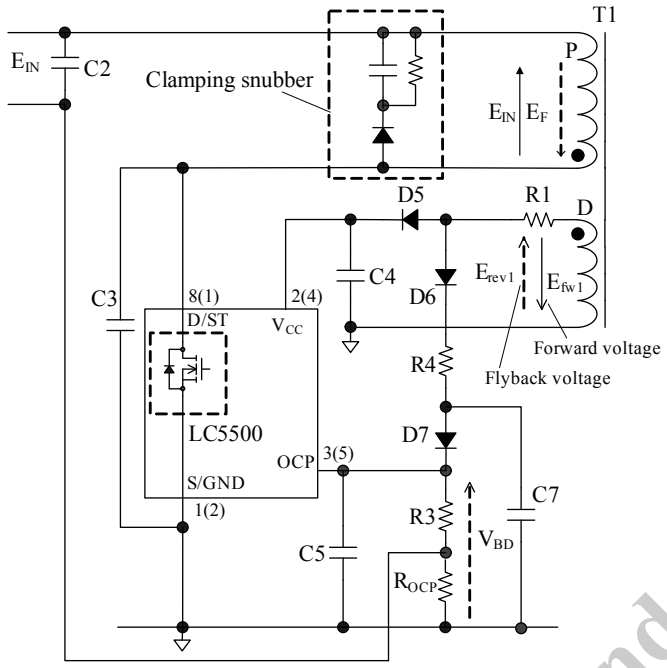


Figure 29. OCP pin peripheral circuit

After the power MOSFET turns off, the quasi-resonant signal immediately goes up and it exceeds the Quasi-Resonant Operation Threshold Voltage-1, $V_{BD(TH1)}$ = 0.24 V. After this occurs, the power MOSFET remains off until the quasi-resonant signal comes down enough to cross the Quasi-Resonant Operation Threshold Voltage-2, $V_{BD(TH2)}$ = 0.17 V. Then the power MOSFET again turns on. In addition, at the point, the threshold voltage goes up to $V_{BD(TH1)}$ automatically to prevent malfunction of the quasi-resonant operation from noise interference..

During that period, C7 must cause a delay time, t_{ONDLY}, such that the power MOSFET turns on at the bottom point of V_{DS}; so select an appropriate C7 value. R3 is recommended to be between 100 and 330 Ω, and C5 to be between 100 and 470 pF.

R4 must set the range for the quasi-resonant signal: greater than or equal to $V_{BD(TH1)}$ under input and output conditions where V_{CC} becomes lowest, but less than the OCP Pin Overvoltage Protection (OVP) Threshold Voltage, $V_{BD(OVP)}$ = 2.6 V, under conditions where V_{CC} becomes highest. Figure 31 defines the pulse width of the quasi-resonant signal. For initiating quasi-resonant operation, the quasi-resonant signal pulse width between the two points $V_{BD(TH1)}$ and $V_{BD(TH2)}$, t_{QR}, must be equal to 1.2 µs or more. This pulse width must be ensured, while at the same time the OCP pin peak voltage, $V_{BD(PK)}$, is recommended to be between 1.5 and 2.0 V. Both conditions should be satisfied throughout the power supply input and output ranges, over variations in R3 and R4 actual component values.

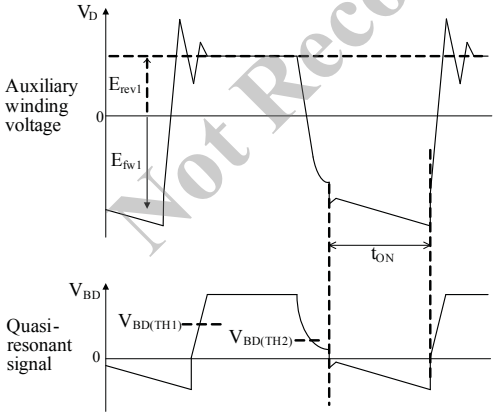


Figure 30. Auxiliary winding voltage and quasi-resonant signal

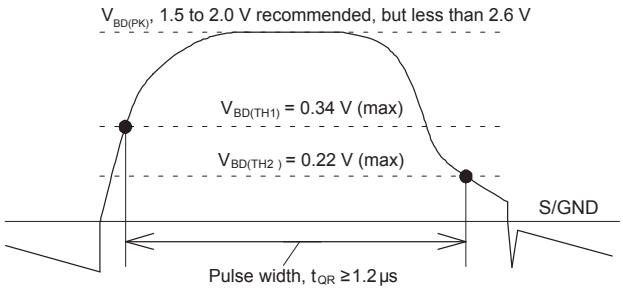


Figure 31. Definition of the pulse width of the quasi-resonant signal

Because R_{OCP} is much less than R3, the formula below is used to calculate R4:

$$R_4 = \frac{R_3 (V_{CC} - V_{BD(PK)} - 2V_f)}{V_{BD(PK)}} \quad (3)$$

given R3 = 220 Ω, $V_{BD(PK)}$ = 1.5 V, V_{CC} = 16 V, and the V_f of D6 and D7 = 0.8 V. R4 is approximately 1.89 kΩ, and it is 1.8 kΩ in the E12 series.

If the pulse width is not satisfied, increase R3 or decrease R4, in order to raise $V_{BD(PK)}$. Alternatively, increasing the capacitance of resonant capacitor C3 is also effective because it widens the free oscillation period. However, it causes an additional switching loss increase; therefore, ensure the IC temperature rise is acceptable.

Figure 32 shows two different OCP pin waveforms, comparing transformer coupling conditions between the primary and secondary winding. The poor coupling tends to happen in a low output voltage (small number of LEDs) transformer design with high N_P / N_S turns ratio (N_P and N_S indicate the number of turns of the primary winding and secondary winding, respectively), and it results in high leakage inductance. The poor coupling causes high surge voltage ringing at the power MOSFET drain pin when it turns off. That high surge voltage ringing is coupled to the auxiliary winding and then the inappropriate quasi-resonant signal, as in figure 32B, is created. The OCP pin has a blanking period of 250 ns (max) to avoid reacting to it, but if the surge voltage continues longer than that period, the IC responds to it and repeatedly turns the power MOSFET on and off at high frequency. This results in an increase of the MOSFET power dissipation and temperature, and it can be damaged.

If this phenomenon is observed, countermeasures include:

- Place C5 as close to the OCP and S/GND pins as possible
- Separate the loop trace between the OCP pin and the S/GND pin from any high current trace
- Loosen the transformer coupling between the auxiliary winding and primary winding
- Reinforce the clamping snubber circuit to reduce the surge voltage

In addition, the OCP pin waveform during operation should be measured by connecting test probes with leads to the OCP pin and the GND pin as short as possible, in order to measure any surge voltage correctly.

Timing adjustment of the bottom-on is done by selecting the value of C7 (figure 29). To do so, observe the power MOSFET drain voltage, V_{DS}, the drain current, I_D, and the quasi-resonant signal. Then optimize the C7 value to adjust the delay time of t_{ONDLY} so that the MOSFET turns on at the bottom point of V_{DS}.

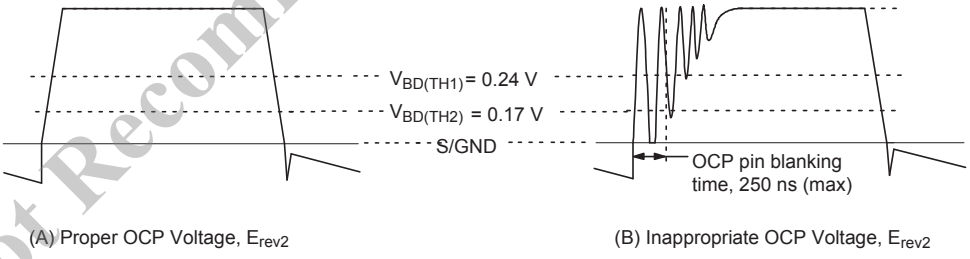


Figure 32. The difference of OCP pin voltage waveform by the coupling condition of the transformer; good coupling (left) versus inappropriate coupling (right)

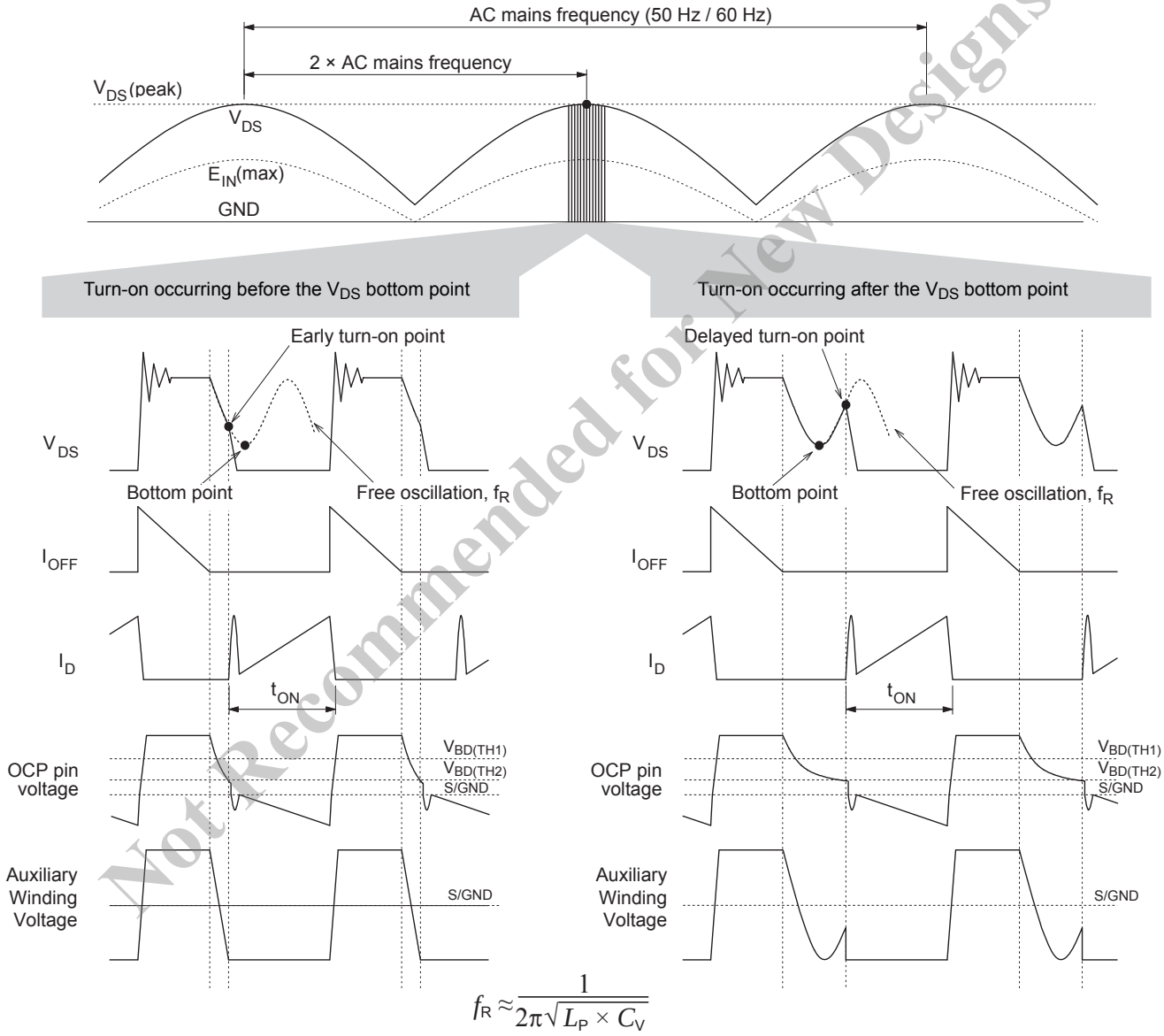
As shown in figure 33:

- If the turn-on point is earlier than the bottom of the V_{DS} signal, it causes higher switching losses. In that situation, delay the turn-on point by increasing the C7 value.
- In the converse situation, if the turn-on point is later than the V_{DS} bottom point, it also causes higher switching losses, but in that case, advance the turn-on point by decreasing the C7 value. An initial reference value for C7 is about 1000pF.

Latch Function

Thermal shutdown (TSD) protection is latched. When the latch circuit is activated, the IC stops switching operation, and therefore the VCC voltage declines.

However, the startup circuit turns on again when V_{CC} reaches $V_{CC(BIAS)1}$ = 11.0 V, in order to avoid reaching the operation stopping voltage, $V_{CC(OFF)}$ = 9.4 V. Thus IC operation in latch mode



$$f_R \approx \frac{1}{2\pi\sqrt{L_P \times C_V}}$$

Figure 33. Effects of failure to turn on precisely at the V_{DS} bottom point: (left) turn-on before a bottom point, (right) turn-on after a bottom point

is maintained. To release the IC from latch mode, cut off the AC mains and let VCC voltage drop below $V_{CC(OFF)}$.

Overvoltage Protection (OVP)

LC551xD series (non-isolated designs) The LC551xD series has three OVP activation methods link to the VCC pin, to the OCP pin, and to the ISENSE pin:

• VCC Pin Overvoltage Protection. figure 34 shows the waveforms of the OVP function on the VCC pin. When the VCC pin voltage with reference to the S/GND pin reaches and exceeds $V_{CC(OVP)}$ = 31.5 V, OVP is activated and the IC stops switching operation. During this function, the bias assist function is disabled, and the VCC voltage decreases to $V_{CC(OFF)}$ = 9.4 V. After that, the startup circuit is activated, and the operation begins intermittent operation by repeating the restart and operation process as long as the OVP condition remains.

In addition, because VCC voltage is proportional to the output voltage, it can be used to detect an output overvoltage event, such as open load condition. In this situation, the detecting voltage is expressed by the formula below:

$$V_{OUT(OVP)} = \frac{V_{OUT}(\text{normal operation})}{V_{CC}(\text{normal operation})} \times 31.5\ (\text{V}) \qquad (4)$$

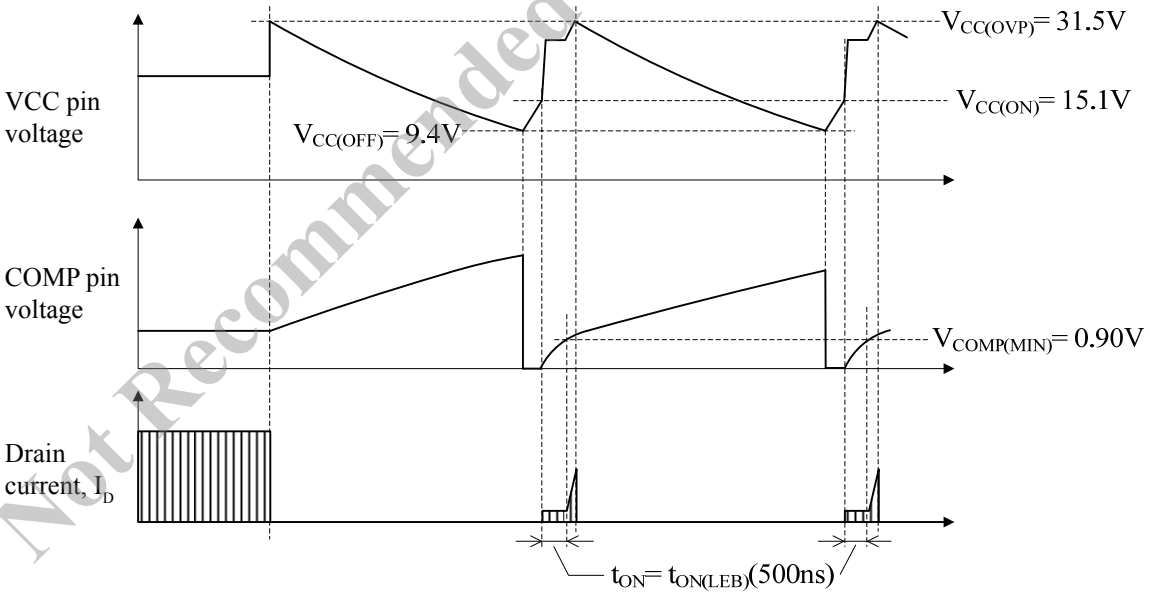


Figure 34. Waveforms when VCC pin OVP is being activated (LC551xD)

• OCP Pin Overvoltage Protection. Figure 35 shows the OCP pin OVP function. When the OCP pin voltage with reference to the S/GND pin reaches $V_{BD(OVP)}$ = 2.6 V or more, OVP is activated. This input voltage must be less than the absolute maximum rating, 5V.

During this function, the bias assist function is disabled, and thus the IC enters intermittent operation as described in the VCC pin OVP section, above. This can be used as protection in the event that the quasi-resonant signal setup is mistaken or excess load current happens in the use of a poor coupling transformer between the primary and secondary winding.

• ISENSE Pin Overvoltage Protection. Figure 36 shows the ISENSE pin OVP operation. When the ISENSE pin voltage with reference to the S/GND pin reaches and exceeds $V_{SEN(OVP)}$ = 2.0 V or more, OVP is activated. This input voltage must be less than the absolute maximum rating, 5V.

During this function, the bias assist function is disabled, and thus the IC enters intermittent operation as described in the VCC pin OVP section, above. As shown in figure 9, with Zener diode DZ1 this function can be used to detect an excess output voltage, such as caused by an open load condition, and protect the circuit.

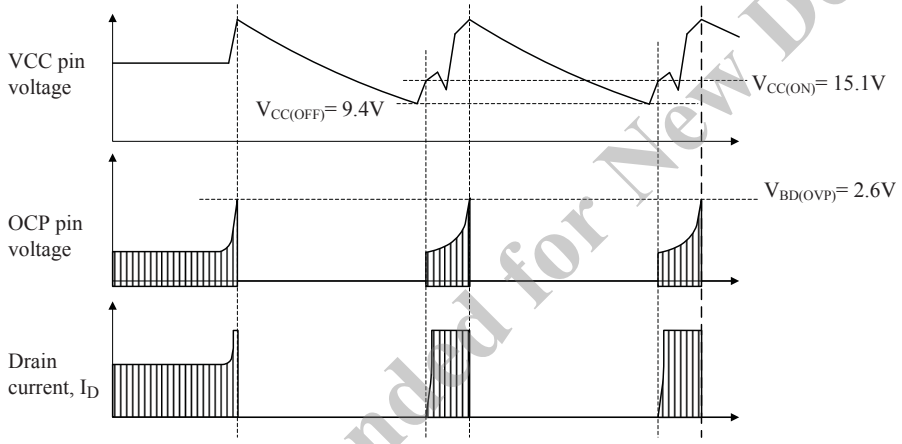


Figure 35. Waveforms when OCP pin OVP is being activated (LC551xD)

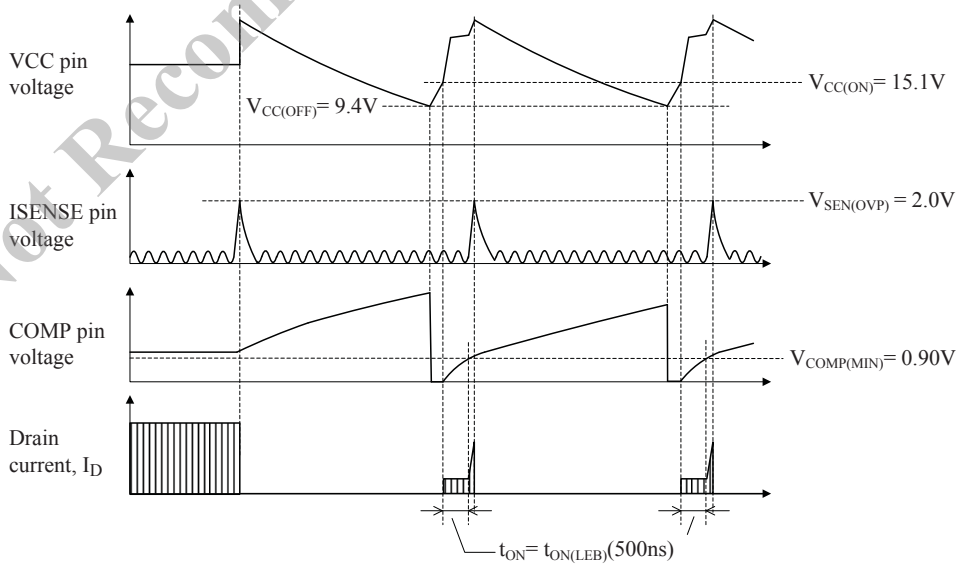


Figure 36. Waveforms when ISENSE pin OVP is being activated (LC551xD)

LC552xD/LC552xF series (isolated designs) The LC552xD and LC552xF series have three OVP activation methods link to the VCC pin, to the OCP pin, and to the OVP pin:

• VCC Pin Overvoltage Protection. figure 37 shows the waveforms of the OVP function. When the VCC pin voltage with reference to the S/GND pin reaches and exceeds $V_{CC(OVP)}$ = 31.5 V or more, OVP is activated and the IC stops switching operation. During this function, the the bias assist function is disabled, and the VCC voltage decreases to $V_{CC(OFF)}$ = 9.4 V. After that, the startup circuit is activated, and the operation begins intermittent operation by repeating the restart and operation process as long as the OVP condition remains. In addition, because VCC voltage is proportional to the output voltage, it can be used to detect output overvoltage events, such as open load condition. In this situation, the detecting voltage is expressed by equation 4.

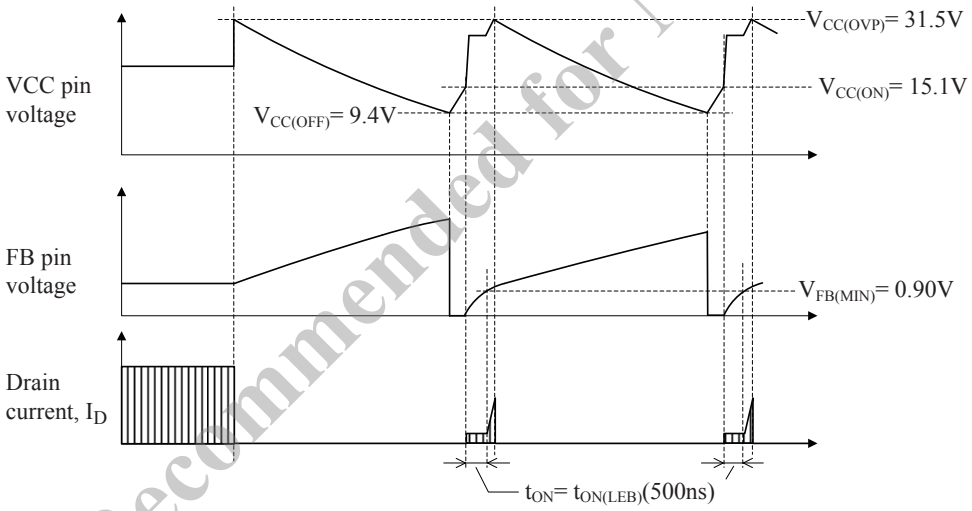


Figure 37. Waveforms when VCC pin OVP is being activated (LC552xD and LC552xF)

• OCP Pin Overvoltage Protection. Figure 38 shows the OCP pin OVP function. When the OCP pin voltage with reference to the S/GND pin reaches $V_{BD(OVP)}$ = 2.6 V, OVP is activated. This input voltage must be less than the absolute maximum rating, 5V.

During this function, the bias assist function is disabled, and thus the IC enters intermittent operation as described in the VCC pin OVP section, above. This can be used as protection in the event the quasi-resonant signal setup is mistaken or excess load current happens in the use of a poor coupling transformer between the primary and secondary winding.

• OVP pin Overvoltage Protection. Figure 39 shows the OVP pin OVP function. When the OVP pin voltage with reference to the S/GND pin reaches and exceeds $V_{OVP(OVP)}$ = 2.0 V, OVP is activated. This input voltage must be less than the absolute maximum rating, 5V.

During this function, the bias assist function is disabled, and thus the IC enters intermittent operation as described in the VCC pin OVP section, above.. As shown in figure 10 and figure 11, with PC2 this function can be used to detect high output voltage, such as an open load condition.

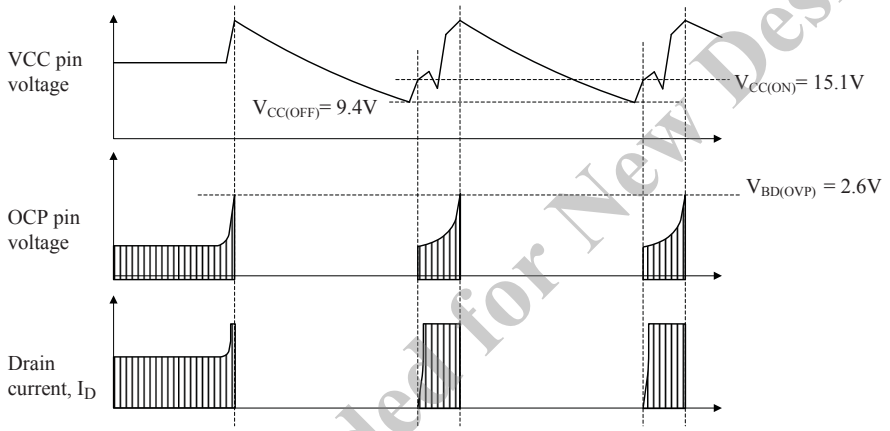


Figure 38. Waveforms when OCP pin OVP is being activated (LC552xD and LC552xF)

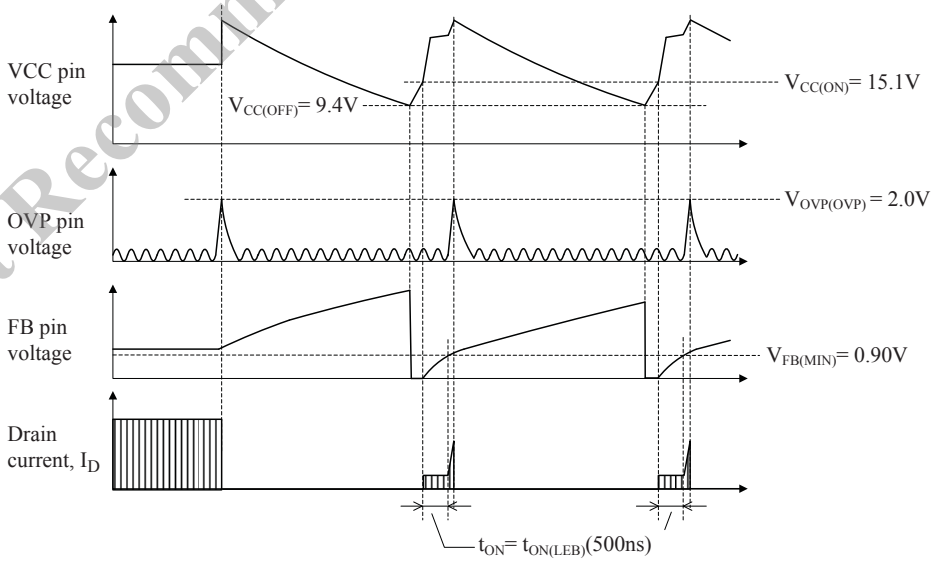


Figure 39. Waveforms when OVP pin OVP is being activated (LC552xD and LC552xF)

Overload Protection (OLP)

If the MOSFET drain current is limited by the overcurrent protection for a certain delay period, t_{DLY}, Overload Protection is activated and the IC enters intermittent oscillation mode operation. This reduces the power-up stress on the incorporated power MOSFET and secondary rectifier.

LC551xD series (non-isolated designs) Figure 40 shows the peripheral circuit at the COMP pin, and figure 41 shows operation when OLP is activated.

At an overload condition, the output voltage, the VCC pin voltage, and the ISENSE pin voltage drop. When the VCC pin voltage reaches $V_{CC(BIAS)1}$ = 11.0 V, the bias assist function is enabled in order to avoid reaching $V_{CC(OFF)}$ = 9.4 V. When the ISENSE pin voltage reaches $V_{SEN(TH)}$ = 0.30 V, the output of the OTA circuit becomes zero, and therefore the internal constant current source at the COMP pin starts charging capacitor C6.

When the COMP pin voltage reaches Overload Protection Threshold Voltage-2, $V_{COMP(OLP)2}$ = 4.5 V, the on-time is set to the Leading Edge Blanking time, $t_{ON(LEB)}$ = 500 ns. Meanwhile, the capacitor charging is ongoing and when it reaches Overload Protection Threshold Voltage-1, $V_{COMP(OLP)1}$ = 5.5 V, the switching operation stops and the VCC voltage decreases to $V_{CC(OFF)}$ = 9.4 V.

After that, the startup circuit is activated. Thus, the operation begins intermittent operation by repeating the restart and operation stop processes as long as the overload condition remains.

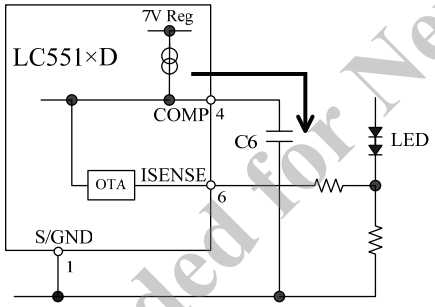


Figure 40. COMP pin peripheral circuit

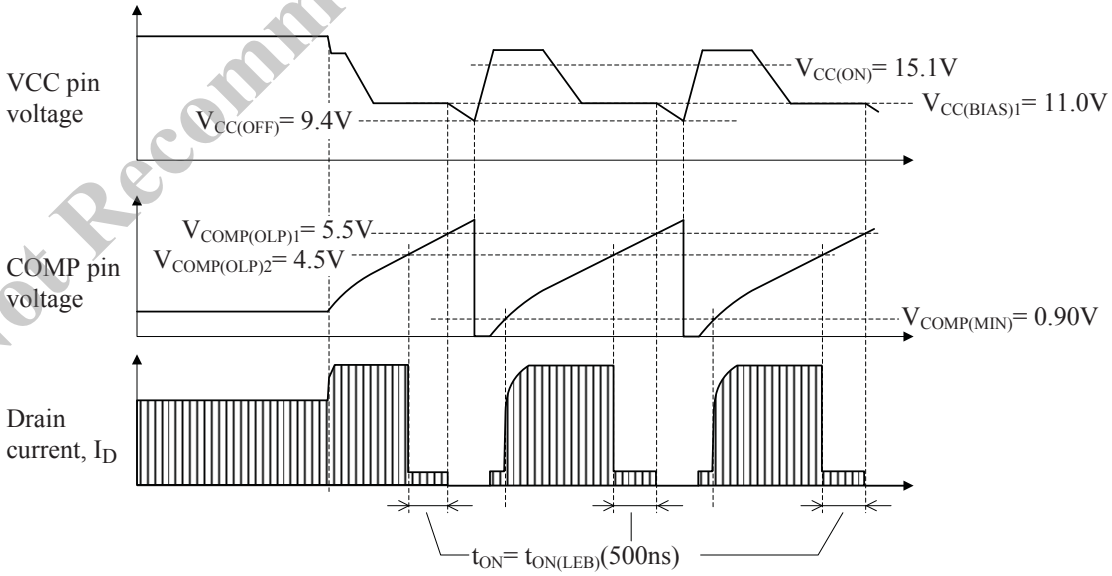


Figure 41. Waveforms when OLP is being activated (LC551xD)

LC552xD/LC552xF series (isolated designs) Figure 42 shows the peripheral circuits at the FB pin of the LC552xD/LC552xF series and figure 43 shows the waveforms when the Overload Protection (OLP) is activated. At an overload condition, the output voltage drops. When the VCC pin voltage reaches $V_{CC(BIAS)1}$ = 11.0 V, the bias assist function is enabled in order to avoid reaching $V_{CC(OFF)}$ = 9.4 V. At the time, a feedback signal from the secondary output becomes zero, and the PC1 is cut off. Thus, the feedback current from the FB pin charges the C6 capacitor, and the FB pin voltage increases.

When the FB pin voltage reaches the Overload Protection Threshold Voltage-2, $V_{FB(OLP)2}$ = 4.5 V, the on-time is set to Leading Edge Blanking time, $t_{ON(LEB)}$ = 500 ns. In the meanwhile, the capacitor charging is ongoing and when it reaches at Overload Protection Threshold Voltage-1, $V_{FB(OLP)1}$ = 5.5 V, the switching operation stops and the VCC voltage decreases to $V_{CC(OFF)}$ = 9.4 V.

After that, the startup circuit is activated. Thus, the operation begins intermittent operation by repeating the restart and operation stop processes as long as the overload condition remains.

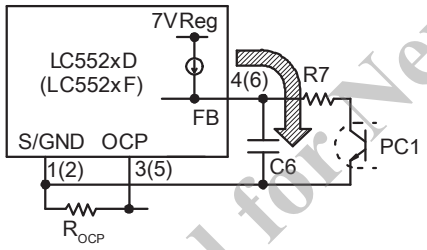


Figure 42. FB pin peripheral circuit

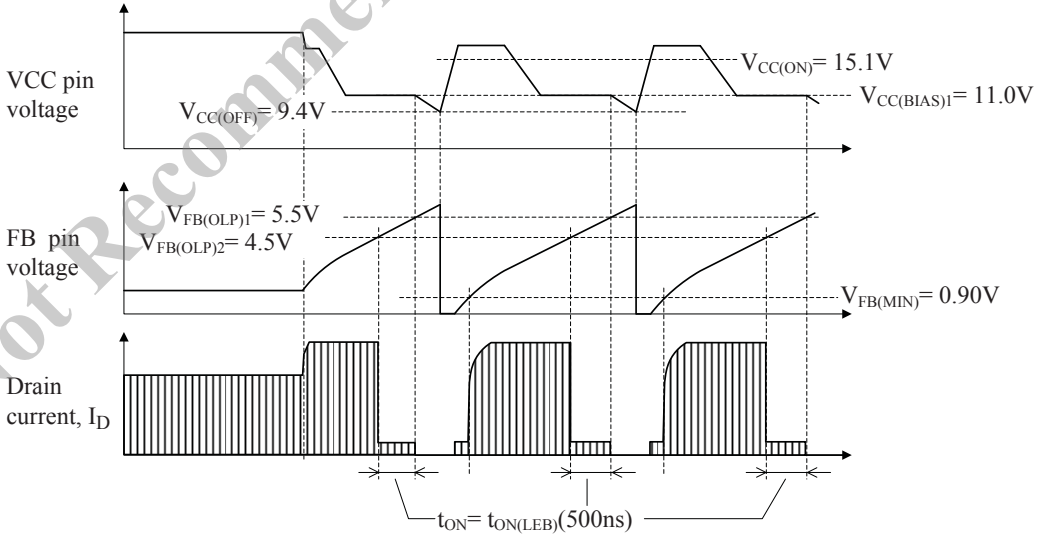


Figure 43. Waveforms when OLP is being activated (LC552xD/ LC552xF)

Overcurrent Protection (OCP)

The Overcurrent Protection (OCP) feature monitors the power MOSFET drain current on a pulse-by-pulse basis, in order to limit output power. The drain current is detected by a current detection resistor, R_{OCP}, and the voltage across it, V_{ROCP}, is fed through R3 to the OCP pin to be detected by it. When the R_{OCP} voltage, V_{ROCP}, reaches the value of the following formulas, the power MOSFET turns off.

$$V_{ROCP} = -\left(|V_{OCP}| + R_3 \times |I_{OCP}| \right) \quad (5)$$

where

V_{OCP}: Overcurrent Detection Threshold Voltage, –0.60 V,
R3: R3 Resistance, and
I_{OCP}: OCP Pin Source Current, –40 µA.

In order to minimize effects of variation in the internal resistor, R3 (figure 44) is recommended to have a value from 100 to 330 Ω. and C5 is recommended to have a value from 100 to 470 pF, with good temperature characteristics. Selecting larger capacitances slows OCP response, and results in an increase in the drain current peak at transient conditions, such as start-up.

Because the OCP function is designed for peak current detection, there is a chance that it will react to the surge current at the power MOSFET turn-on edge. In order to avoid this, the Leading Edge Blanking Time, $t_{ON(LEB)}$, = 500 ns, is set.

The surge voltage pulse width must be less than $t_{ON(LEB)}$ as shown in figure 45. In case its width is longer than that, try these measures:

- adjust the turn-on point to the V_{DS} bottom point
- reduce the voltage resonant capacitor C_V (C3 in figure 44) capacitance
- reduce the secondary rectifier snubber capacitor capacitance

With the quasi-resonant converter, the peak drain current at the same output load condition becomes different in a universal AC input voltage range (85 to 265 VAC), that is, when the AC input voltage is high, the peak drain current is low because the operation frequency becomes high.

When the OCP threshold voltage is fixed constant, the output current, I_{OUT}, in an OCP operation increases according to an increase of AC input voltage, as shown in (A) I_{OUT} without input compensation of figure 46.

In the maximum AC input voltage range, in order to control output current at OCP operation, $I_{OUT(OCP)}$, an external OCP input compensation circuit (D_{X1}, D_{ZX1}, R_{X1}) is added as shown in figure 47. For more details as to how to set it, refer to the next section, Input Compensation Function for Overcurrent Protection.

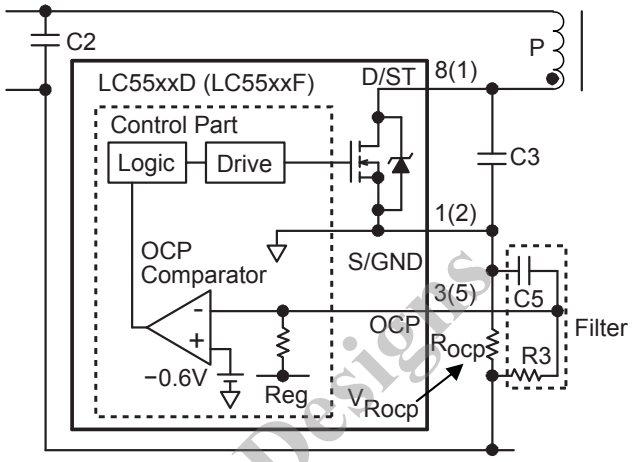


Figure 44. OCP circuit for negative side detect

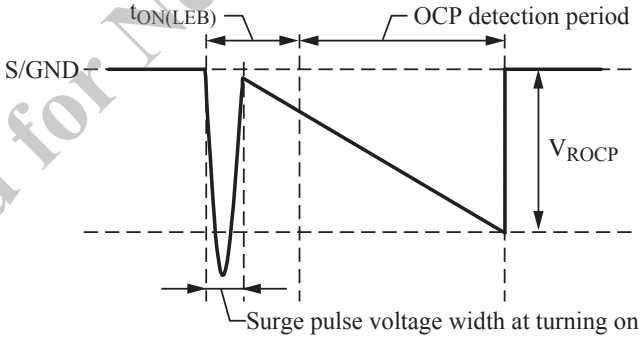


Figure 45. OCP pin voltage, converted from MOSFET drain current by R_{OCP}

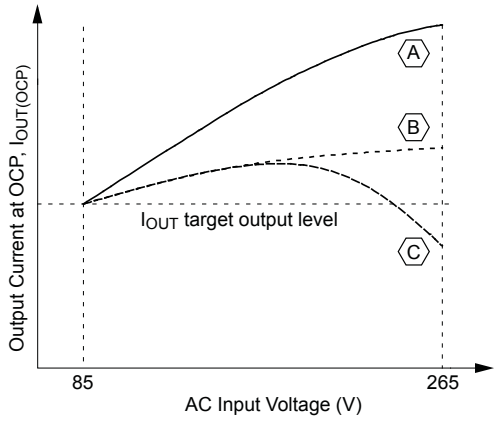


Figure 46. Input compensation OCP circuit: (A) I_{OUT} without input compensation; (B) I_{OUT} with appropriate input compensation; (C) with inappropriately set input compensation, more than enough amount of compensation, I_{OUT} cannot meet target

Input Compensation Function for Overcurrent Protection

The auxiliary winding forward voltage E_{fw1} is proportional to the input voltage, E_{IN}. E_{fw1} is applied to D_{ZX1}, and R_{X1} and R3 translate the voltage E_{fw1} – Zener voltage of D_{ZX1}, into the input Compensation Current, I.

This input Compensation Current, I, creates the voltage of $R_3 \times I$, and it lowers the absolute value of the compensated OCP threshold voltage to less than the original OCP threshold voltage, V_{OCP} = –0.6 V. This way, when E_{IN} is high, the compensation amount becomes high.

The D_{ZX1} Zener diode is used to set the voltage at which the input compensation begins, so choose the Zener voltage value that is equal to E_{fw1} at the time when input compensation begins.

Optimize the circuit in a way to minimize the difference between the overcurrent points at low and high AC input voltage. Also ensure that the output current meets its target over the entire AC input voltage range, as the normal curve shown in figure 46. The OCP pin voltage, including surge voltage, must not exceed its absolute maximum rating of –2.0 to 5.0 V at the highest AC input voltage.

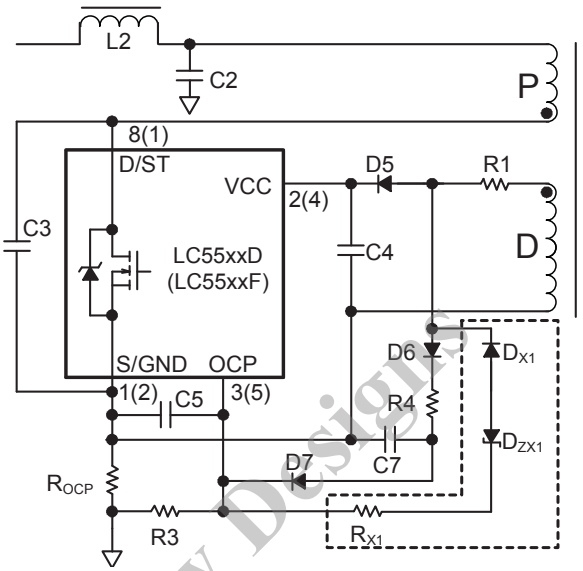


Figure 47. Input compensation OCP circuit

OCP Threshold Voltage with and without the OCP Input Compensation Circuit

Without the input compensation circuit, as shown in the figure 50 upper panel, the overcurrent detecting voltage is equal to the sum of the Overcurrent Protection Threshold Voltage, V_{OCP} = –0.60 V, and the voltage across R3 from the OCP pin source current, I_{OCP} = – 40 µA.

$$V_{ROCP} = -|R_{OCP} \times I_{DP}| = -\left(|V_{OCP}| + R_3 \times |I_{OCP}|\right) \quad (6)$$

In the converse situation, with the input compensation circuit, as shown in the figure 50 lower panel, the overcurrent detecting voltage is equal to the sum of the Overcurrent Protection Threshold Voltage, V_{OCP} = −0.60 V, the voltage across R3 from the OCP pin source current, I_{OCP}, and the voltage across R3 from the input Compensation Current, I.

$$V'_{ROCP} = -\left[\left(|V_{OCP}| + R_3 \times |I_{OCP}|\right) - R_3 \times I\right] \quad (7)$$

• Determining OCP pin input compensation circuit component values

Given:

$E_{IN(PK)}$ = C2 voltage

I_{DP} = MOSFET peak drain current

V_{FX1} = D_{X1} forward voltage

V_{ZX1} = D_{ZX1} Zener voltage

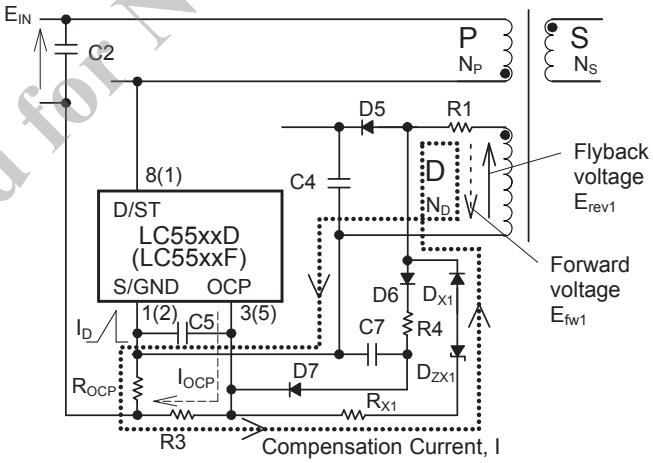


Figure 48. OCP input compensation circuit

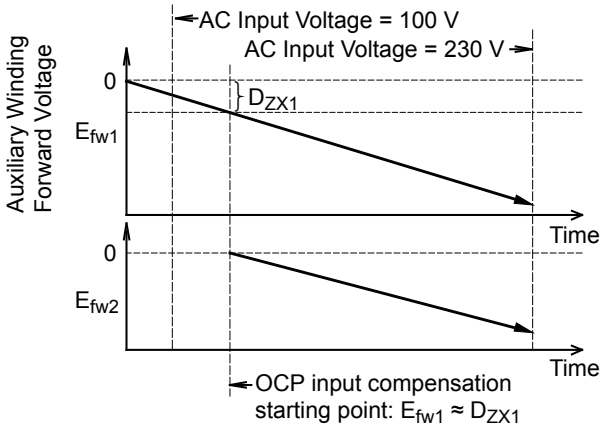


Figure 49. E_{fw1} and E_{fw2} voltage relative to AC input voltage

1. The overcurrent detecting peak drain current, $I_{DP(OCP)}$, without the input compensation circuit, is expressed by the following, based on equation 6, from figure 50, upper panel:

$$I_{DP(OCP)} = \frac{|V_{OCP}| + R_3 \times |I_{OCP}|}{R_{OCP}} \quad (8)$$

2. On the other hand, the overcurrent detecting peak drain current, $I'_{DP(OCP)}$, with the input compensation circuit, is expressed by the following, based on equation 7, from figure 50, lower panel:

$$I'_{DP(OCP)} = \frac{|V_{OCP}| + R_3 \times (|I_{OCP}| - I)}{R_{OCP}} \quad (9)$$

$I'_{DP(OCP)}$ is set to the peak drain current where the output current is equal to that at the maximum AC input voltage of the curve B in figure 46 (appropriate input compensation).

3. From equations 8 and 9, the compensation current, I, of the input compensation circuit, is expressed as follows:

$$I = (|I_{DP(OCP)}| - |I'_{DP(OCP)}|) \times \frac{R_{OCP}}{R_3} \quad (10)$$

4. The forward voltage, E_{fw1}, at C2 peak voltage $E_{IN(PK)}$(max) is expressed as follows:

$$E_{fw1} = \frac{N_D \times E_{IN(PK)}(\max)}{N_P} \quad (11)$$

5. Next, R_{X1} is expressed by the following, in order to let the compensation current, I, flow at the maximum AC input voltage, $E_{IN(PK)}$(max):

$$I = \frac{E_{fw1} - V_{ZX1} - V_{FX1}}{R_{X1} + R_3 + R_{OCP}} \quad (12)$$

assuming: R3, $R_{OCP} \ll R_{X1}$

$$R_{X1} = \frac{E_{fw1} - V_{ZX1} - V_{FX1}}{I} \quad (13)$$

from equations 11 and 13:

$$R_{X1} = \frac{\frac{N_D \times E_{IN(PK)}(\max)}{N_P} - (V_{ZX1} + V_{FX1})}{I} \quad (14)$$

• AC input compensation circuit design example with universal input

Here is an example of design specification and calculation:

Given:
AC input voltage: 85 to 265 VAC
Output power: 40 W
Transformer primary winding: 40 T
Transformer auxiliary winding: 6 T
R_{OCP} = 0.2 Ω
R_3 = 220 Ω
D_{X1} forward voltage: 0.8 V
Tentatively, OCP input compensation start voltage, $V_{IN(OCP\_ST)}$, is set to the voltage of 100 to 130 VAC.
At this time, $V_{IN(OCP\_ST)}$ is set to 120 VAC.

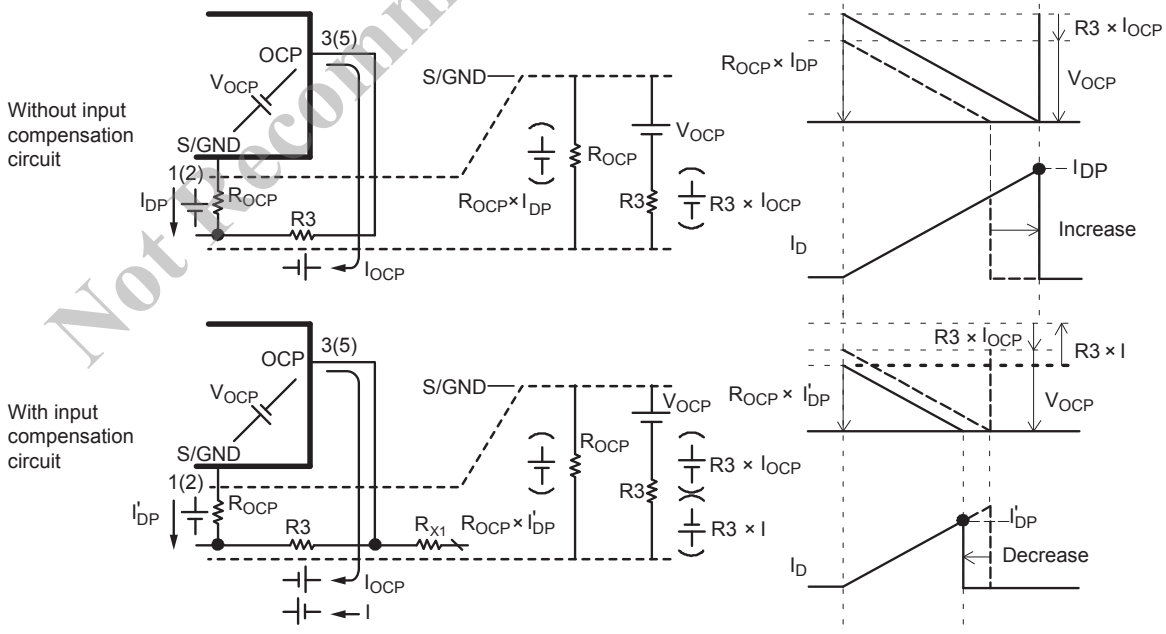


Figure 50. Compensated drain current waveforms

1. Calculate E_{fw1} at 120 VAC input:

$$E_{fw1} = \frac{N_D}{N_P} \times E_{IN(PK)}(\max) \quad (15)$$

$$= \frac{N_D}{N_P} \times V_{IN(OCP\_ST)} \times \sqrt{2}$$

$$= \frac{6}{40} \times 120\sqrt{2} = 25.5 \text{ (V)}$$

Thus, select 27 V as the Zener value for DZ_{X1}.

Assuming:

$I_{DP(OCP)}$, Drain current during OCP operation, measured at E_{IN}(min) of 85 VAC: 3.0 A

$I'_{DP(OCP)}$, Drain current when the output current is equal to that at the maximum AC input voltage of the curve B in figure 46 (appropriate input compensation): 1.9 A

2. The compensation current, I, is calculated using equation 10:

$$I = (3.0 \text{ (A)} - 1.9 \text{ (A)}) \times \frac{0.2 \text{ (}\Omega\text{)}}{220 \text{ (}\Omega\text{)}} = 1 \text{ (mA)}$$

3. R_{X1} can be calculated using equation 14:

$$R_{X1} = \frac{\frac{6 \text{ (T)} \times 265 \text{ (VAC)}\sqrt{2}}{40 \text{ (T)}} - (27 \text{ (V)} + 0.8 \text{ (V)})}{1 \text{ (mA)}}$$

$$= 28.4 \text{ (k}\Omega\text{)}$$

Thus, select R_{X1} = 27 kΩ out of the E12 series.

Finally, ensure that the output current limited by OCP operation is similar to that of the curve B in figure 46 (appropriate input compensation), in actual operation throughout AC input voltage ranges. If necessary, readjust the rating of D_{ZX1} and R_{X1} by changing the compensation startup voltage $V_{IN(OCP\_ST)}$ for OCP pin input voltage.

Thermal Shutdown Protection

Thermal Shutdown protection is activated when the temperature of the control circuit in the IC reaches $T_{j(TSD)}$ = 135°C(min), and then the IC stops switching operation in latch mode.

Maximum On-Time Limiting Function

The maximum on-time, set at $t_{ON(MAX)}$ = 40 µs (figure 51), limits lower side operation frequency, and it minimizes audible noise from the transformer, as well as power stress on the incorporated MOSFET and secondary rectifier at low AC input or during transient periods such as at switching AC mains on or off.

Ensure that the actual on-time at the minimum AC input and the maximum load condition does not reach $t_{ON(MAX)}$ = 40 µs. If that does happen, redesign the transformer, such as by reducing the primary inductance or reducing the duty cycle by lowering the turns ratio of N_P / N_S.

Design Notes

Peripheral Components

Take care to use properly rated and proper type of components.

- Output smoothing capacitor. Consider design margins for ratings of ripple current, voltage, and temperature in selecting the output capacitor. A low impedance capacitor, designed to be tolerant against high ripple current, is recommended.
- Transformer. Consider design margins for temperature rise, resulting from copper losses and core losses, in designing or selecting a transformer.

  Switching current contains a high frequency component that causes the skin effect; therefore, consider a current density of 3 to 4 A/mm² and select a wire gauge based on RMS current.

  In the event further temperature measurement is necessary, try the following measures to increase the surface area of the wire:
  - Increase the quantity of parallel wires
  - Use litz wire
  - Increase the diameter of the wires
- Current detection resistor, R_{OCP}. Choose a low equivalent series inductance and high surge tolerant type for the current detection resistor. If a high inductance type is used, it may cause malfunctioning because of the high frequency current running through it.

Transformer Design

In this section, the pin symbol *COMP/FB pin* shows instead of *COMP pin* for the LC551xD and *FB pin* for the LC552xD/ LC552xF.

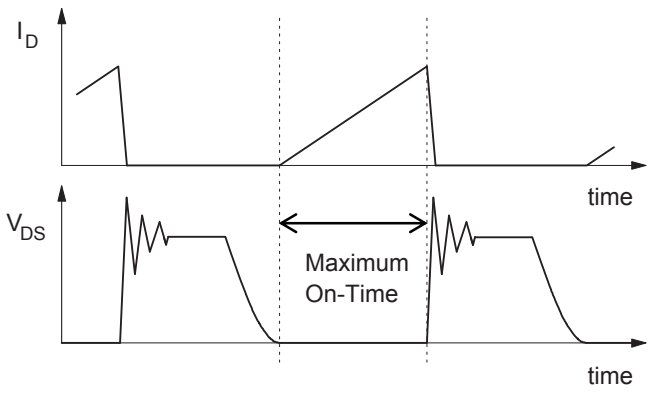


Figure 51. Confirmation of Maximum On-Time

Figure 52 shows an ideal waveform in average current control relative to a sine wave of AC input voltage. The Average Current Control function controls COMP/FB pin voltage at a fixed rate relative to the sine wave of AC input voltage, V_{IN}, at commercial frequencies. Therefore, the envelope curve of the peak drain current, I_{DP}, and the input current, I_{IN} (which is the averaged I_{DP}), shows a sine waveform which is similar to that of the AC input voltage.

To set the fixed COMP/FB pin voltage, the value of C6 and the constant current detection resistor must be be adjusted.

The transformer design is the same as for an RCC (ringing choke converter, or self-oscillation flyback converter) transformer design. However, a quasi-resonant operation includes a certain delay to turn-on, so duty cycle must be compensated. Moreover, for input capacitorless applications, the applied voltage of a transformer is the sine wave of the AC input voltage, V_{IN}, at commercial frequencies.

Therefore, the duty cycle compensation for quasi-resonant delay time is added to the basic equation of the RCC topology; moreover, the equation must be changed into the sine wave of the AC input voltage, V_{IN}.

In consideration of quasi-resonant delay time, the primary side inductance, L'_P, applied the sine wave of AC input voltage, is expressed by the following equation:

$$L'_P = \frac{(V_{INRMS(MIN)} \times D_{ON})^2}{\left(\sqrt{\frac{2 \times P_{OUT} \times f_{S(MIN)}}{\eta}} + V_{INRMS(MIN)} \times D_{ON} \times f_{S(MIN)} \times \pi \sqrt{C_V}\right)^2} \quad (16)$$

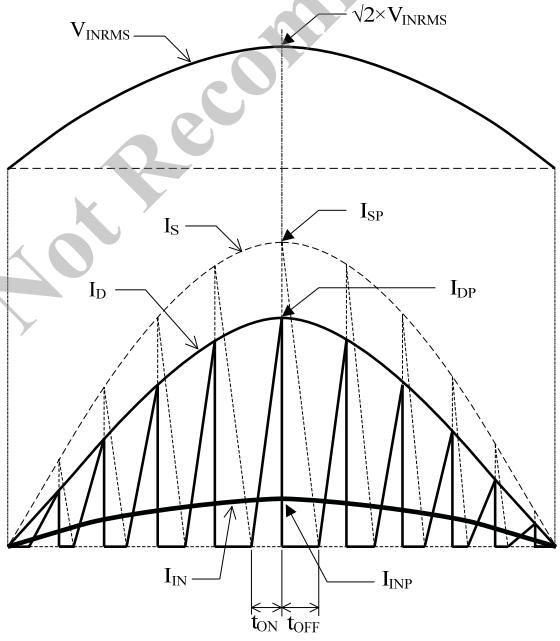


Figure 52. Ideal current waveform

where

$V_{INRMS(MIN)}$: Effective value (rms) of the sine wave of the minimum AC input voltage,

P_{OUT}: Maximum output power:

$$P_{OUT} = V_{OUT} \times I_{OUT} \quad (17)$$

where V_{OUT} is the output voltage, and I_{OUT} is the maximum output current,

$f_{S(MIN)}$: Operation frequency at the peak voltage of the sine wave of AC input voltage (the minimum operation frequency in quasi-resonant operation),

η: Efficiency rate: 80% to 90%,

C_V: Voltage resonant capacitor (C3) rating: usually 47 to 470 pF

D_{ON}: Maximum duty cycle, not compensated for the quasi-resonant delay time, at the minimum AC input voltage:

$$D_{ON} = \frac{E_f}{\sqrt{2} \times V_{INRMS(MIN)} + E_f} \quad (18)$$

E_f : Flyback voltage:

$$E_f = (N_P / N_S) \times (V_{OUT} + V_f) \quad (19)$$

where N_P is the number of turns of the primary winding, N_S is the number of turns of the secondary winding, and V_f is the forward voltage of the secondary rectifier, D8, approximately 0.7 V.

E_f is determined by the power MOSFET breakdown voltage and the surge voltage. Because the breakdown voltage of the power MOSFET of this IC is 650 V, when it is used with the specified universal input range, the target voltage of E_f is 100 to 150 V.

Quasi-resonant delay time, t_{ONDLY}:

$$t_{ONDLY} = \pi \sqrt{L'_P \times C_V} \quad (20)$$

V_{INRMS}: Effective value (RMS) of sine wave of AC input voltage
I_{IN} : Input current
I_{INP} : Peak input current
I_D : Power MOSFET drain current
I_{DP} : Power MOSFET peak drain current
I_S : Forward current of a secondary side rectifier
I_{SP} : Peak forward current of a secondary side rectifier

Maximum duty cycle, compensated for quasi-resonant delay time (t_{ONDLY}), D'_{ON}:

$$D'_{ON} = (1 - f_{S(MIN)} \times t_{ONDLY}) \times D_{ON} \quad (21)$$

Input rms current of the sine wave of the minimum AC input voltage, $I_{INRMS(MAX)}$:

$$I_{INRMS(MAX)} = \frac{P_{OUT}}{\eta \times V_{INRMS(MIN)}} \quad (22)$$

Peak drain current, compensated for quasi-resonant delay time (t_{ONDLY}), $I_{DP(DLY)}$:

$$I_{DP(DLY)} = \frac{2\sqrt{2} \times P_{OUT}}{\eta \times D'_{ON} \times V_{IN(RMS(MIN)}} \quad (23)$$

In transformer design, the AL-value of the ferrite core should be chosen so the transformer dose not saturate, in consideration of NI-Limit(AT) (= $N_P \times I_{DP(DLY)}$).

When choosing a ferrite core to match the relationship of NI-Limit (AT) versus AL-value, it is recommended to set the calculated NI-Limit value below about 30% from the NI-Limit curve of ferrite core data, as shown in the hatched area containing the design point in figure 53, to provide a design margin in consideration of temperature effects and other variations, as expressed by the formulas below:

$$\text{NI-Limit} \leq N_P \times I_{DP(DLY)} \times 130\% \quad (24)$$

$$N_P = \sqrt{\frac{L'_P}{\text{AL Value}}} \quad (25)$$

Then, the rest of the winding turns are determined by the formulas below.

$$N_S = \frac{V_{OUT} + V_f}{E_f} \times N_P \quad (26)$$

$$N_D = \frac{V_{CC}}{V_{OUT} + V_f} \times N_S \quad (27)$$

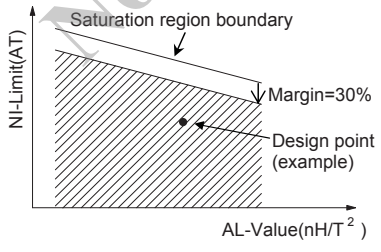


Figure 53. Example of NI-Limit versus AL-Value characteristics

Trace and Component Layout Design

PCB circuit trace design and component layout affect IC functioning during operation. Unless they are proper, malfunction, significant noise, and large power dissipation may occur.

Circuit loop traces flowing high frequency current, as shown in figure 54, should be designed as wide and short as possible to reduce trace impedance.

In addition, earth ground traces affect radiation noise, and thus should be designed as wide and short as possible.

Switching mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layout should be done in compliance with all safety guidelines.

Furthermore, because an integrated power MOSFET is being used as the switching device, take account of the positive thermal coefficient of $R_{DS(on)}$ for thermal design.

Figures 55, 56, and 57 show practical trace design examples and considerations for the LC551xD, LC552xD and LC552xF series respectively. In addition, observe the following:

• IC peripheral circuit

(1) Traces among S/GND pin, R_{OCP}, C2, T1(primary winding), and D/ST pin

- The traces carry the switching current; therefore, widen and shorten them as much as possible.
- The input capacitor C2 must be placed close to the IC or the transformer in order to reduce series inductances of the traces against high frequency current.

(2) Traces among S/GND pin, C4(–), T1(auxiliary winding D), R1, D5, C4(+), and VCC pin

- This trace is for supplying voltage to the IC. Widen and shorten the traces as much as possible. If the IC and the capacitor C4 are apart, place a film or ceramic capacitor (0.1 to 1.0 μF) as close to the VCC pin and the S/GND pin as possible.

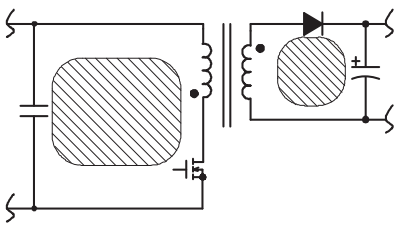


Figure 54. High frequency current loops

(3) Current Detection Resistor, R_{OCP}:

- Place R_{OCP} as close to the S/GND pin as possible. In addition, in order to avoid interference of the switching current with the control circuit, connect the trace of R3 to the base of R_{OCP} at the point A in figure 55, 56, and 57.

- Secondary side, traces among T1(secondary winding S), D8, and C9:

  The secondary-side switching current runs through this trace. Widen and shorten the traces as much as possible.

  Thin and long traces cause the series inductance to be high and it results in high surge voltage on the power MOSFET when it turns off. Therefore, proper layout pattern design helps to increase voltage margin of the power MOSFET to its break-down voltage and reduce power stress and loss of the clamping snubber circuit.

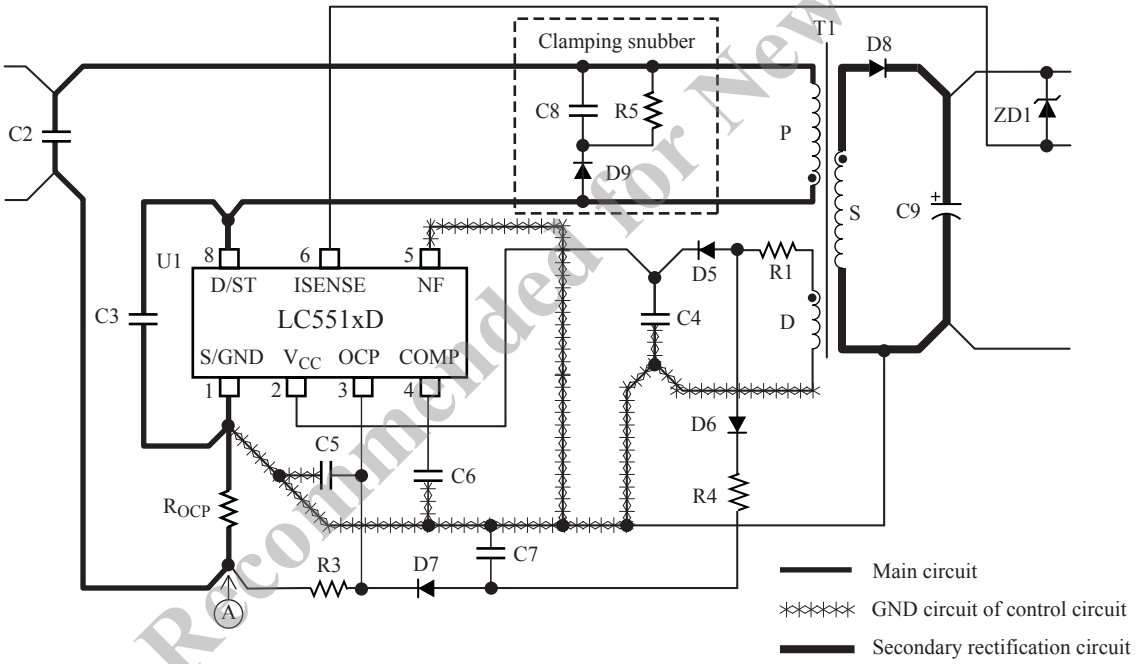


Figure 55. LC551xD (non-isolated designs) peripheral circuit connection example

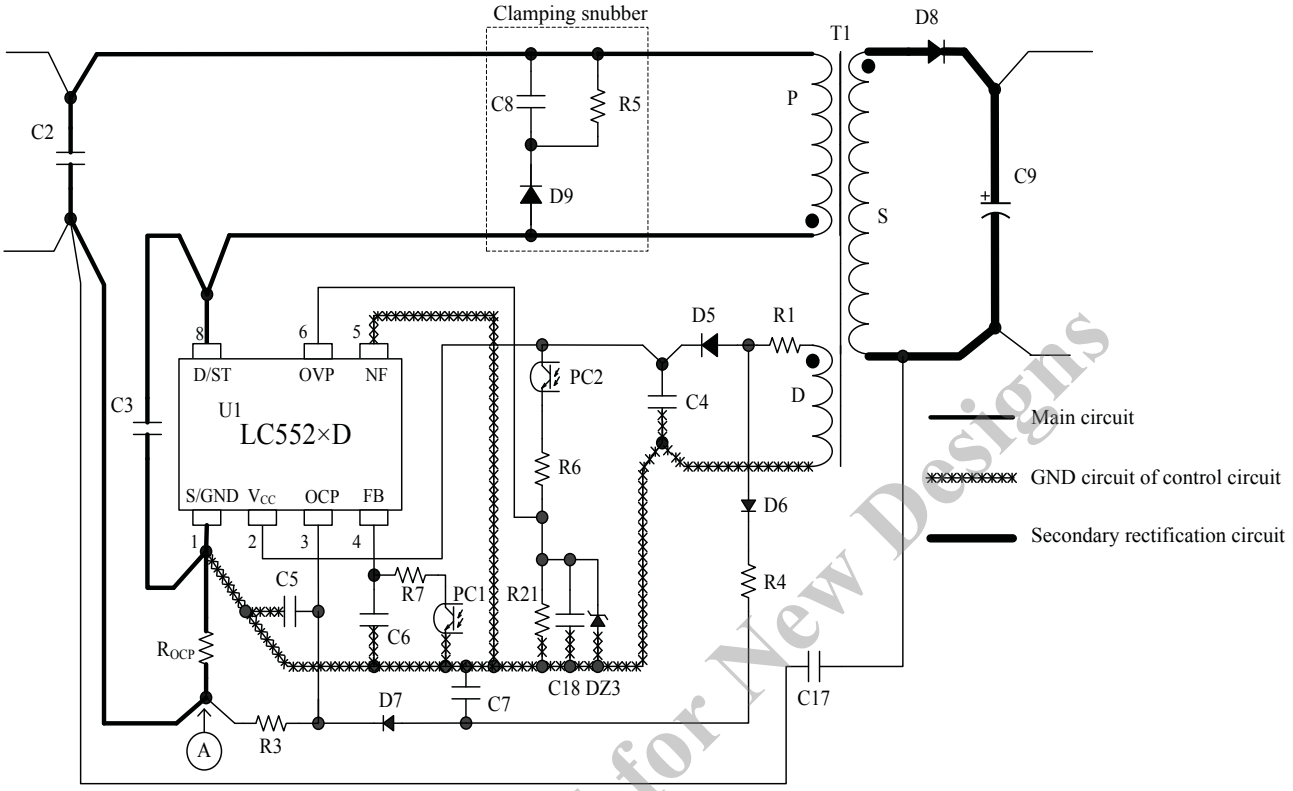


Figure 56. LC552xD (isolated designs) peripheral circuit connection example

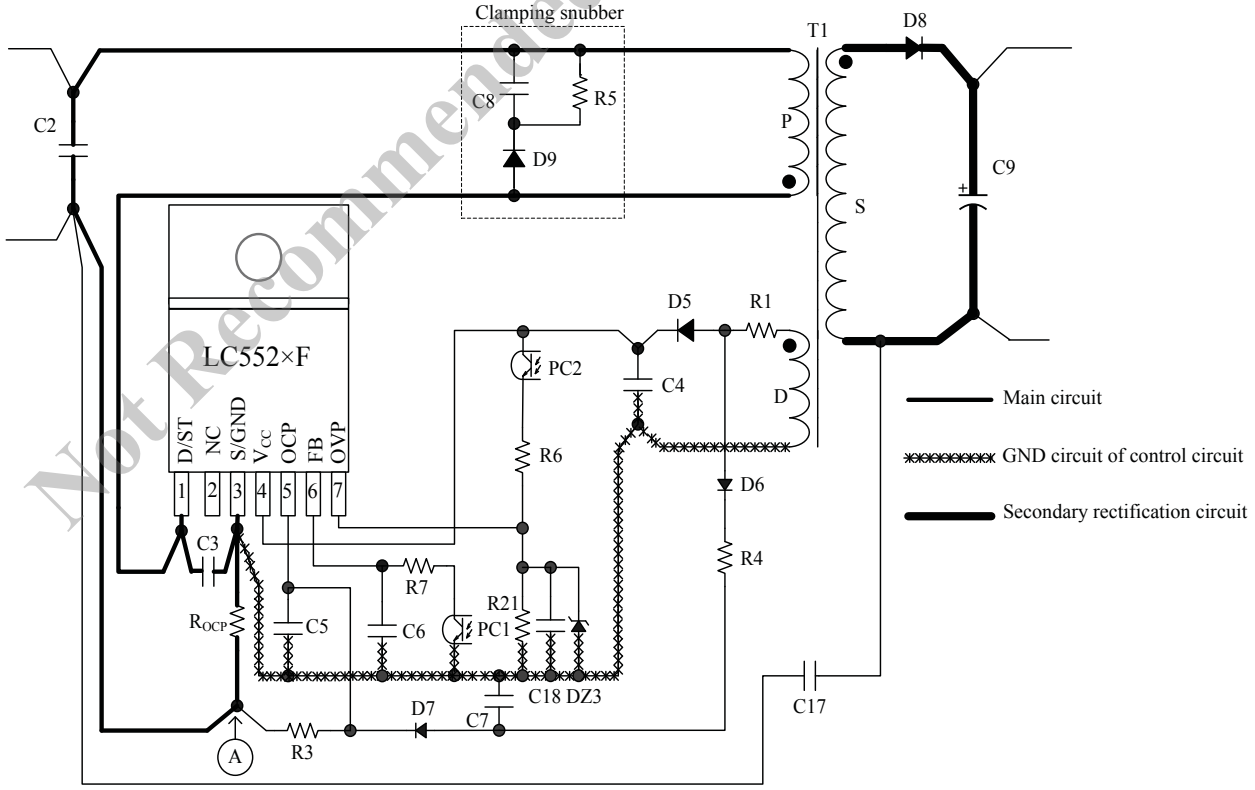


Figure 57. LC552xF (isolated designs) peripheral circuit connection example

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