LC5540LF Series Single-Stage Power Factor Corrected Off-Line Switching Regulator ICs

General Description

The LC5540LF series is the power IC for the isolated type LED driver which has an incorporated power MOSFET, designed for input capacitorless applications, and making it possible for systems to comply with the harmonics standard (IEC61000-3-2 class C), even during light load condition. The controller adapts the average current control method for realizing high power factors, and the quasi-resonant topology contributes to high efficiency and low EMI noise. The series is housed in TO-220 packages. The rich set of protection features helps to realize low component counts, and high performance-to-cost power supply.

Figure 1. The LC5540LF series package is a TO-220F-7L fully molded package, which provides a separation between pins 1 and 2.

Features and Benefits

- TO-220 package
- Integrated on-time control circuit (it realizes high power factor by average current control)
- Integrated startup circuit (no external startup circuit necessary)
- Integrated soft-start circuit (reduces power stress during start-up on the incorporated power MOSFET and output rectifier)
- Integrated bias assist circuit (improves startup performance, suppresses V_{CC} voltage droop during operation, and allows use of low-rated ceramic capacitor on VCC pin)
- Integrated Leading Edge Blanking (LEB) circuit
- Integrated maximum on-time limit circuit
- Protection features:
  - Overcurrent protection (OCP): pulse-by-pulse
  - Overvoltage protection (OVP): latched shutdown
  - Overload protection (OLP): latched shutdown
  - Thermal shutdown (TSD): latched shutdown

Applications

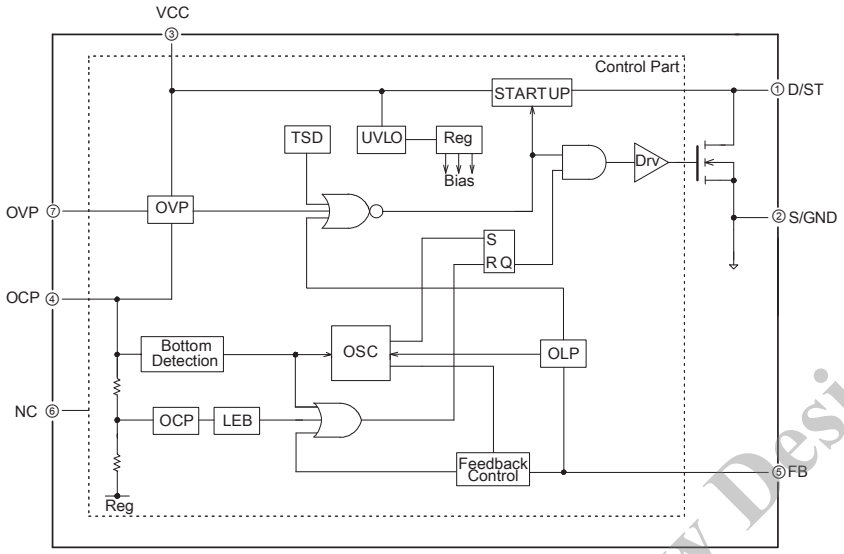
- LED lighting fixtures
- LED light bulbs

The product lineup for the LC5540LF series provides the following options:

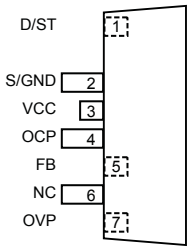
Part Number	MOSFET V_{DSS}(min) (V)	$R_{DS(on)}$ (max) (Ω)	PWM Operation Frequency f_{OSC}(typ) (kHz)	On-Time $t_{ON(MAX)}$(typ) (µs)	P_{OUT}* (W)	
					230 VAC	85 to 265 VAC
LC5546LF	650	1.9	40	17.5	60	40
LC5547LF		1.1			80	55
LC5549LF	800	1.7			60	40

*Based on the thermal rating; the allowable maximum output power can be up to 120% to 140% of this value. However, maximum output power may be limited in such an application with low output voltage or short duty cycle.

Functional Block Diagram



Pin-out Diagram



(LF3051)

Pin List Table

Number	Name	Function
1	D/ST	MOSFET drain pin and input of the startup current
2	S/GND	MOSFET source and GND pin for the Control Part
3	VCC	Supply voltage input and Overvoltage protection (OVP) signal input
4	OCP	Overcurrent Protection, quasi-resonant signal input pin, and Overvoltage Protection (OVP) signal input
5	FB	Feedback signal input and Overload Protection (OLP) signal input
6	NC	No connection
7	OVP	Overvoltage Protection (OVP) signal input

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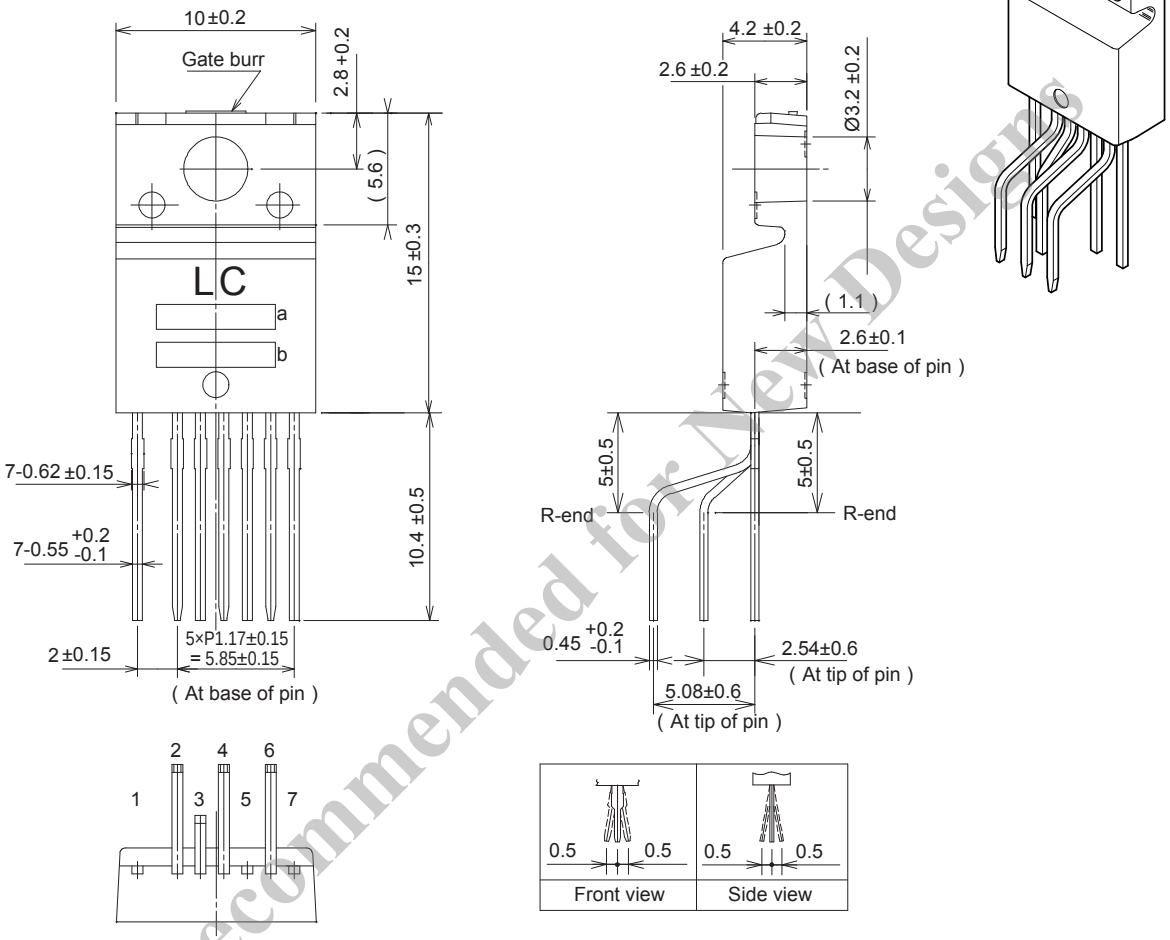
Leadform 3051



Unit: mm
Package: TO-220F-7L

Note: "Gate Burr" shows area where 0.3 mm (max) gate burr may be present.

a: Part # 55xxF
b: Lot number
1st letter: Last digit of year
2nd letter: Month
Jan to September: Numeric
October: O
November: N
December: D
3rd and 4th letter: Date
01 to 31: Numeric
5th letter: Sanken control number

Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Electrical Characteristics

• This section provides electrical characteristic data for each product.

• The polarity value for current specifies a sink as "+ ," and a source as "–," referencing the IC.

• Please refer to the datasheet of each product for additional details.

Absolute Maximum Ratings Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Notes		Pins	Rating	Unit
Drain Current	I_{DPeak}	LC5546LF	Single pulse	1 – 2	9.2	A
		LC5547LF			13.0	A
		LC5549LF			10.5	A
Single Pulse Avalanche Energy	E_{AS}	LC5546LF	I_{LPeak} = 2.9 A, V_{DD} = 99 V, L = 20 mH	1 – 2	99	mJ
		LC5547LF	I_{LPeak} = 4.4 A, V_{DD} = 99 V, L = 20 mH		233	mJ
		LC5549LF	I_{LPeak} = 2.8 A, V_{DD} = 99 V, L = 20 mH		92	mJ
Control Part Input Voltage	V_{CC}			3 – 2	35	V
OCP Pin Voltage	V_{OCP}			4 – 2	−2.0 to 5.0	V
FB Pin Voltage	V_{FB}			5 – 2	−0.3 to 7.0	V
OVP Pin Voltage	V_{OVP}			7 – 2	−0.3 to 5.0	V
Allowable Power Dissipation of MOSFET	P_{D1}	LC5546LF	With infinite heatsink	1 – 2	20.2	W
		LC5547LF			23.6	W
		LC5549LF				
		Without heatsink			1.8	W
Internal Frame Temperature in Operation	T_F			—	−20 to 115	°C
Operating Ambient Temperature	T_{OP}			—	−55 to 115	°C
Storage Temperature	T_{stg}			—	−55 to 125	°C
Channel Temperature	T_{ch}			—	150	°C

Electrical Characteristics of Control Part Unless specifically noted, T_A is 25°C, V_{CC} = 20 V

Characteristic	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Unit
Power Supply Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		3 – 2	13.8	15.1	17.3	V
Operation Stop Voltage*	$V_{CC(OFF)}$		3 – 2	8.4	9.4	10.7	V
Circuit Current in Operation	$I_{CC(ON)}$		3 – 2	–	–	4.7	mA
Startup Circuit Operation Voltage	$V_{STARTUP}$		1 – 2	18	21	24	V
Startup Current	$I_{CC(STARTUP)}$	V_{CC} = 13 V	3 – 2	−8.5	−4.0	−1.5	mA
Startup Current Threshold Biasing Voltage*	$V_{CC(BIAS)}$		3 – 2	9.5	11.0	12.5	V
Normal Operation							
PWM Operation Frequency	f_{OSC}		1 – 2	33	40	47	kHz
Maximum On-Time	$t_{ON(MAX)}$		1 – 2	14	17.5	21	µs
FB Pin Control Minimum Voltage	$V_{FB(MIN)}$		5 – 2	0.50	0.85	1.20	V
Maximum Feedback Current	$I_{FB(MAX)}$		5 – 2	–40	–25	–10	µA
Leading Edge Blanking Time	$t_{ON(LEB)}$		4 – 2	−	600	−	ns
Quasi-Resonant Operation Threshold Voltage-1	$V_{BD(TH1)}$		4 – 2	0.14	0.24	0.34	V
Quasi-Resonant Operation Threshold Voltage-2	$V_{BD(TH2)}$		4 – 2	0.11	0.16	0.21	V
Protection Operation							
OCP Pin Overcurrent Protection (OCP) Threshold Voltage	V_{OCP}		4 – 2	−0.66	−0.60	−0.54	V
OCP Pin Source Current	I_{OCP}		4 – 2	−120	−40	−10	µA
OCP Pin Overvoltage Protection (OVP) Operation Voltage	$V_{BD(OVP)}$		4 – 2	2.2	2.6	3.0	V
Overload Protection (OLP) Threshold Voltage	$V_{FB(OLP)}$		5 – 2	4.1	4.5	4.9	V
OVP Pin OVP Threshold Voltage	$V_{OVP(OVP)}$		7 – 2	1.6	2.0	2.4	V
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		3 – 2	28.5	31.5	34.0	V
Thermal Shutdown Activating Temperature	$T_{J(TSD)}$		—	135	–	–	°C

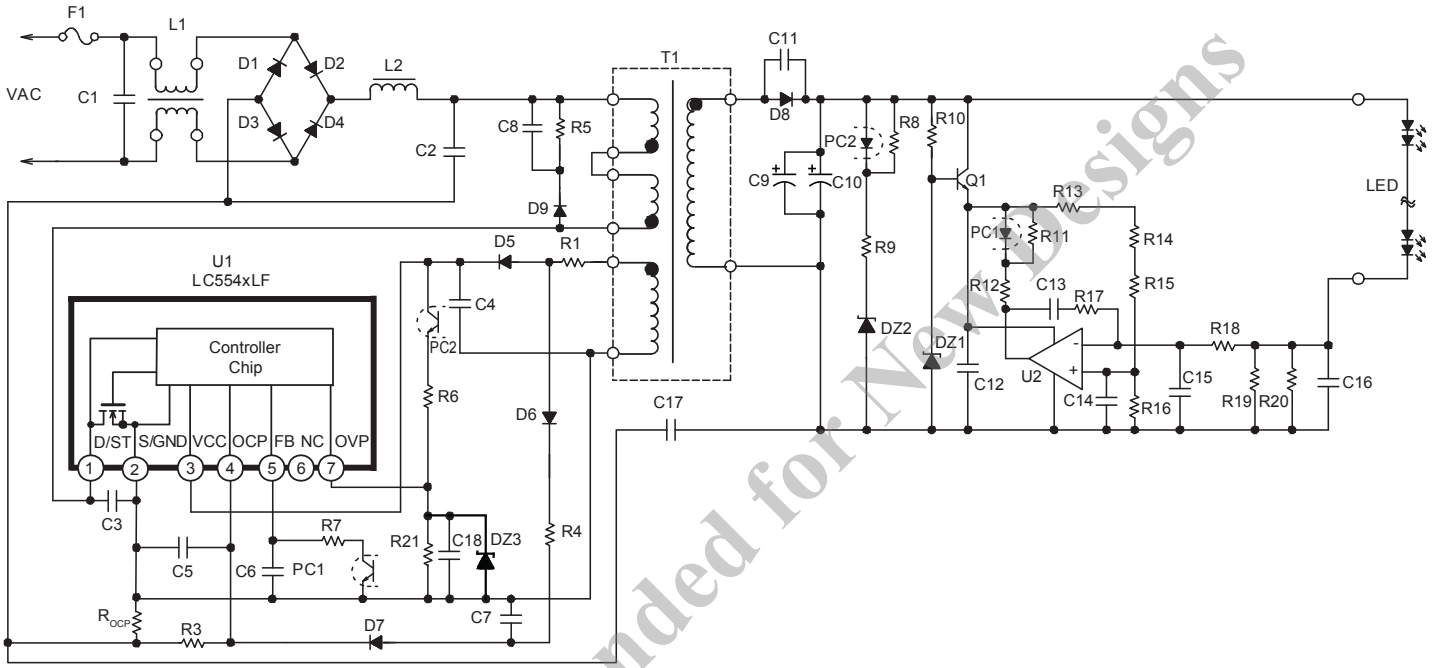
*$V_{CC(BIAS)}$ > $V_{CC(OFF)}$ always.

Electrical Characteristics of MOSFET Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Test Conditions		Pins	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V_{DSS}	LC5546LF LC5547LF		1 – 2	650	—	—	V
		LC5549LF			800	—	—	V
Drain Leakage Current	I_{DSS}			1 – 2	—	—	300	μA
On-Resistance	$R_{DS(on)}$	LC5546LF		1 – 2	—	—	1.9	Ω
		LC5547LF			—	—	1.1	Ω
		LC5549LF			—	—	1.7	Ω
Switching Time	t_f	LC5546LF LC5547LF		1 – 2	—	—	400	ns
		LC5549LF			—	—	300	ns
Thermal Resistance*	$R_{\theta ch\text{-}F}$	LC5546LF		—	—	—	3.1	°C/W
		LC5547LF LC5549LF			—	—	2.2	°C/W

*The thermal resistance between the channels of the MOSFET and the internal frame.

Typical Application Circuit



Power supply circuit example for LED lighting

Functional Description

All of the parameter values used in these descriptions are typical values, according to the LC5546LF specification, unless they are specified as minimum or maximum.

With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

Startup Operation

Startup Period

Figure 2 shows the VCC pin peripheral circuit. The integrated startup circuit is connected to the D/ST pin. When the D/ST pin voltage reaches $V_{STARTUP}$ = 21 V, the startup circuit is activated, and it generates a constant current, $I_{CC(STARTUP)}$ = –4.0 mA, to charge capacitor C4 at the VCC pin. During this process, when the VCC pin voltage reaches $V_{CC(ON)}$ = 15.1V, the IC starts operation. After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

The startup time is determined by the C4 capacitance. A ceramic or film capacitor can be used for C4, and a value of 0.22 to 22 µF is generally recommended. The approximate value of the startup time can be calculated using the following formula:

$$t_{START} \approx C_4 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{CC(STARTUP)}|} \quad (1)$$

where:

t_{START} is the startup time in s, and

$V_{CC(INT)}$ is the initial voltage of the VCC pin in V.

Undervoltage Lockout (UVLO) Circuit

Figure 3 shows the relation of the VCC pin voltage to the circuit current, I_{CC}. When the VCC pin voltage reaches the Operation Start Voltage, $V_{CC(ON)}$ = 15.1 V, the IC starts operation and the circuit current increases. In operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the IC stops operation by UVLO circuit, and reverts to the state before startup.

The voltage from the auxiliary winding (D in figure 2) becomes a power source to the IC in steady state operation. The auxiliary winding voltage should be targeted to be about 20 V, determined by the winding turns of the D winding, in order that the VCC pin voltage should be set within the specifications of the input voltage range and the output load range of the power supply, according to the following formula:

$$V_{CC(BIAS)}(\text{max}) < V_{CC} < V_{CC(OVP)}(\text{min})$$

$$12.5\ (\text{V}) < V_{CC} < 28.5\ (\text{V})$$

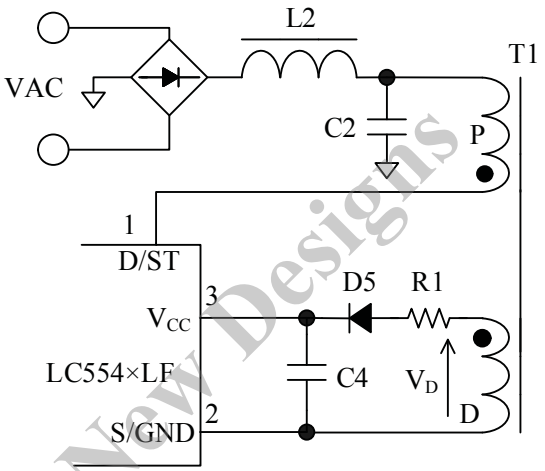


Figure 2. D/ST and VCC pin peripheral circuits

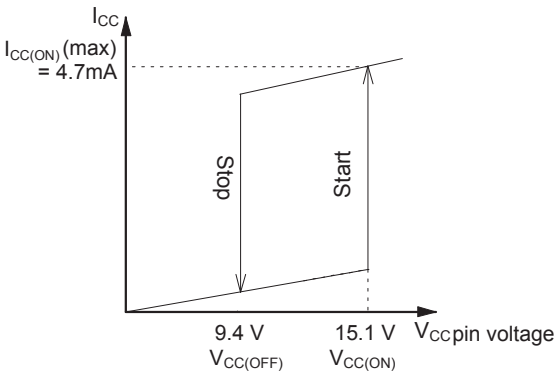


Figure 3. V_{CC} versus I_{CC}

Bias Assist Function

Figure 4 shows the VCC pin voltage behavior during the startup period. If VCC pin voltage decreases enough to reach the Startup Current Threshold Biasing Voltage, $V_{CC(BIAS)}$ = 11.0 V, the Bias Assist function is activated before the voltage decreases to $V_{CC(OFF)}$ = 9.4 V. While the Bias Assist function is operating, any decrease of the VCC pin voltage is counteracted by a supplementary current from the Startup circuit, and thus V_{CC} is kept almost constant.

While the output voltage rises, the VCC pin voltage increases to the target voltage to counterbalance the voltage drop caused by increasing IC current and the increase of the auxiliary winding voltage, V_D, proportional to the output voltage.

Because of the Bias Assist function, the use of a low-value capacitor for C4 (see figure 6) is allowed. Also, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function can also be shortened.

It is necessary to check and adjust the startup process in the application, so that poor starting conditions may be avoided.

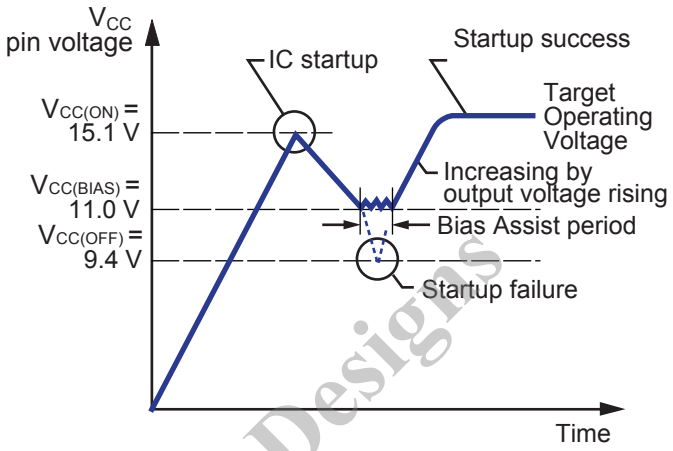


Figure 4. V_{CC} during startup period

Auxiliary Winding

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output of the SMPS (see figure 5). This happens because C4 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C4 peak charging, it is effective to add some value R1, of several tenths of ohms to several ohms, in series with D5 (see figure 6). The optimal value of R1 should be determined using a transformer matching what will be used in the actual application, because the proportion of the VCC pin voltage versus the transformer output voltage differs according to transformer structural design.

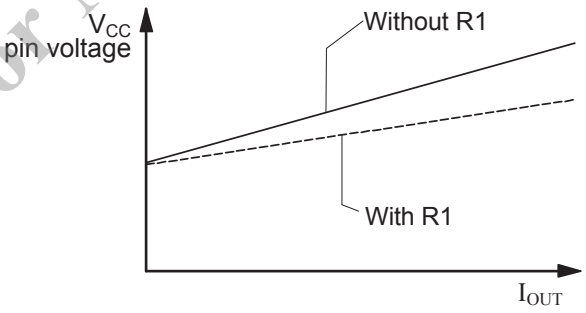


Figure 5. V_{CC} versus I_{OUT} with and without resistor R1

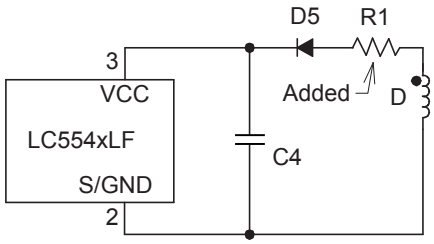


Figure 6. VCC pin peripheral circuit with R1

Fluctuation of V_{CC} by I_{OUT} worsens in the following cases, requiring a transformer designer to pay close attention to the placement of the auxiliary winding D:

- Poor coupling between the primary and secondary windings (this causes high surge voltage and is seen in a design with low output voltage and high output current).
- Poor coupling between the auxiliary winding D and the secondary stabilized output winding where the output line voltage is controlled constant by the output voltage feedback (this is susceptible to surge voltage)

Figure 7 shows two transformer design examples considered the winding location of the auxiliary winding D to minimize impact of V_{CC} surge voltage. Triple insulation wires are used for either the primary or secondary winding, and thus no margin-tape is used:

- Separate the auxiliary winding D from the primary windings P1 and P2 (figure 7 (A)); P1 and P2 are two separated primary windings.
- Place the auxiliary winding D within the secondary winding S1 in order to improve the coupling of those windings (figure 7 (B)); S1 is the secondary output winding.

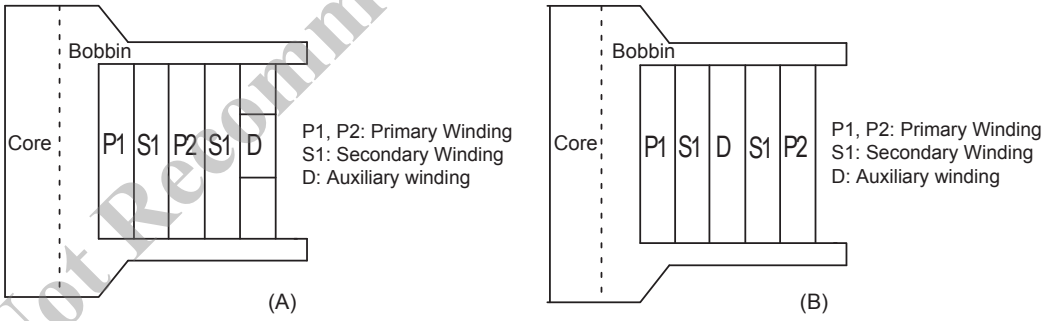


Figure 7. Transformer winding structures

Soft Start Function

Figure 8 shows the operation waveform at startup. The soft start function reduces power stress on the incorporated MOSFET and the secondary rectifier.

The soft start operation begins when the FB pin voltage reaches V_{FB}(min) = 0.85 V, and lasts until the output current becomes constant. During that period, the operation is in PWM operation, at the internally set f_{OSC} = 40 kHz, and the output power gradually increases.

During this period, check the items below:

• Ensure the VCC pin voltage does not drop to the Operation Stop Voltage, $V_{CC(OFF)}$.
• Ensure the output current reaches the target value before the Overload Protection (OLP) function is activated by the FB pin voltage reaching $V_{FB(OLP)}$ = 4.5 V.

Operational Mode at Startup

Figure 8 shows the operation mode at the startup. After the startup, when the FB pin voltage reaches V_{FB}(min) = 0.85 V, the switching operation begins in PWM operation at an operation frequency of f_{OSC} = 40 kHz.

Then, when the output voltage rises, the auxiliary winding voltage will rise, and when the quasi-resonant signal of the positive voltage on OCP pin reaches $V_{BD(TH1)}$ = 0.24 V or more, the quasi-resonant operation will begin.

Figure 9 shows the OCP pin voltage waveform expanded time scale at point A of figure 8.

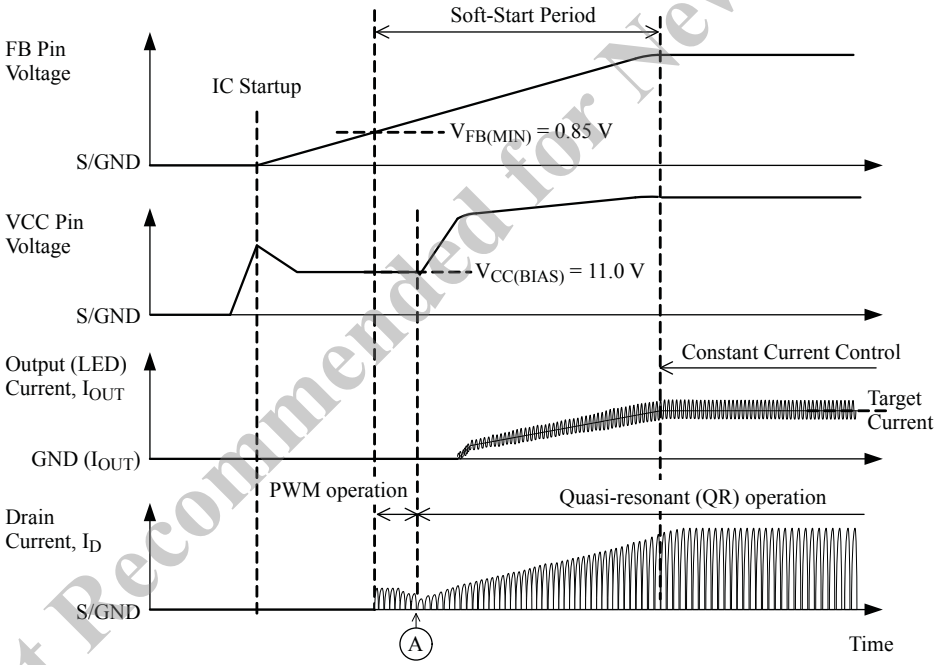


Figure 8. Soft-start operation waveforms at startup

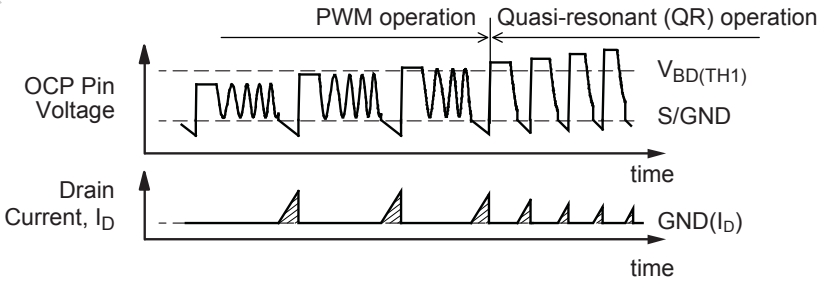


Figure 9. OCP Pin Voltage (with time scale expanded at point A of figure 8)

On-Time Control Operation

Figure 10 shows the peripheral circuit at the FB pin, and figure 11 shows the on-time control. The output control is done by voltage mode control, which controls on-time depending on output load, and average current control.

As shown in figure 11, in the average current control operation, the current detection resistor voltage in secondary side is compared with the reference voltage by the secondary operational amplifier circuit (U2 in the Typical Application Circuit drawing). This output is run through the photo-coupler, PC1, to the FB pin, and its output is averaged at the FB pin.

This averaged voltage at the FB pin is compared with the internal oscillator (OSC) output by the internal FB comparator, and the on-time is controlled. Here, the internal OSC indicates the oscillator circuit, which controls the PWM operation frequency, quasi-resonant oscillation, and the maximum on-time limit. The recommended value of capacitor C6 linked to the FB pin is approximately 2.2 µF.

The constant output current control of the output is done as below:

- When the output load current becomes less than the target value, the current detection resistor voltage in secondary side becomes low, and the feedback current through the PC1 decreases. Because the averaged voltage at the FB pin becomes high, the on-time and the output current increase.
- When the output current becomes greater than the target value, the circuits operate in the opposite way. The feedback current through the PC1 increases. Because the averaged voltage at the FB pin becomes low, the on-time and the output current decrease.

Figure 12 shows the average input current waveform. The averaged FB pin voltage becomes constant, and the duty cycle is controlled according to the E_{IN} voltage (C2 voltage in the Typical Application Circuit drawing). It makes an averaged input current sine waveform which realizes a high power factor.

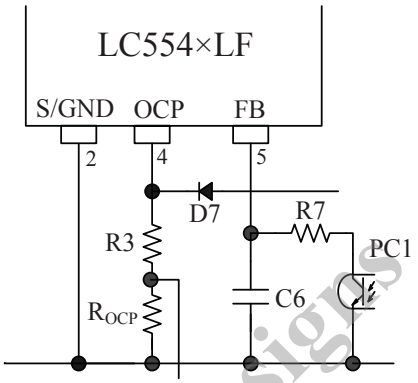


Figure 10. FB pin peripheral circuit

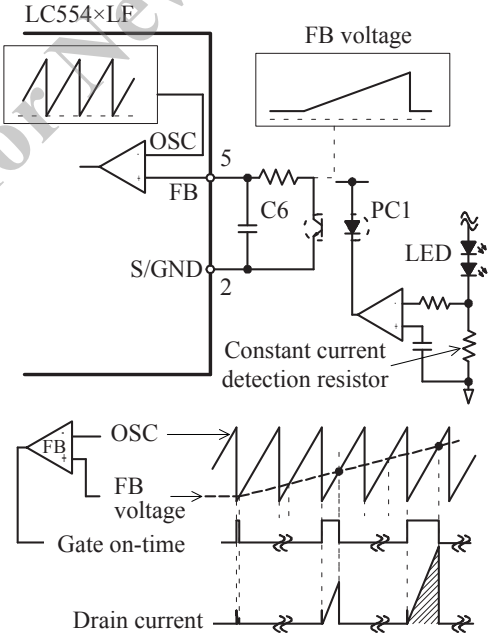


Figure 11. On-time control

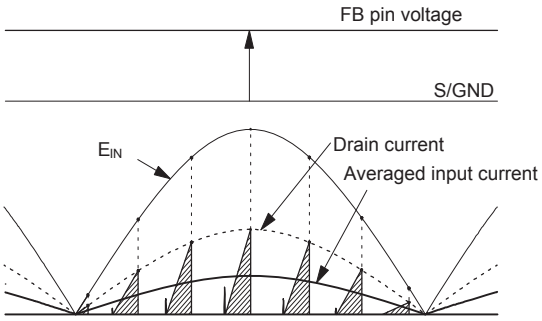


Figure 12. Averaged input current waveform

Quasi-Resonant Operation and Bottom-On Timing

Quasi-Resonant Operation

Figure 13 shows the circuit of a flyback converter. A flyback converter is a system which transfers the energy stored in the transformer to the secondary side when the primary side power MOSFET is turned off. After the energy is completely transferred to the secondary, when the MOSFET keeps turning off, the MOSFET drain node begins free oscillation based on the L_P of the transformer and C_V across the drain and source pins.

The quasi-resonant operation is the V_{DS} bottom-on operation that turns-on the MOSFET at the bottom point of V_{DS} free oscillation.

Figure 14 shows an ideal V_{DS} waveform during bottom-on operation.

Using bottom-on operation, switching loss and switching noise are reduced and it is possible to obtain converters with high efficiency and low noise.

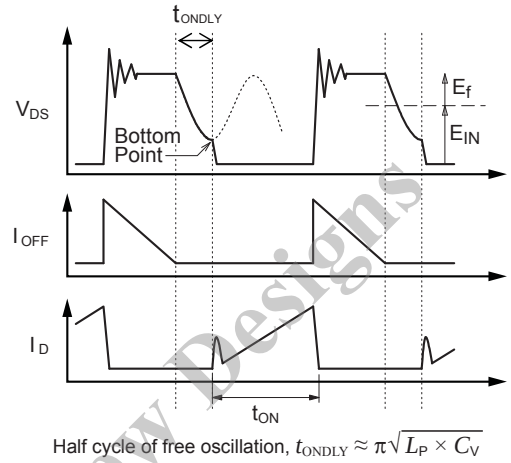


Figure 14. Ideal bottom-on operation waveform (MOSFET turn-on at a bottom point of a V_{DS} waveform)

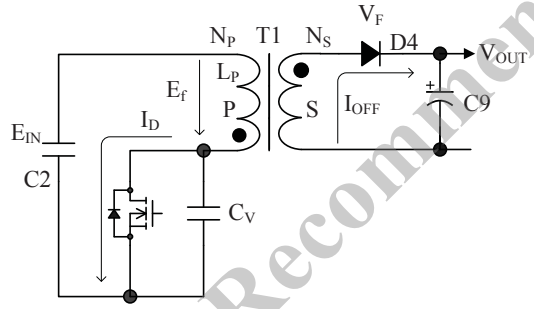


Figure 13. Basic flyback converter circuit

E_{IN}: Input voltage

E_f: Flyback voltage

$$E_f = \frac{N_P}{N_S} \times (V_{OUT} + V_f) \quad (2)$$

N_P: Number of turns in the primary winding
N_S: Number of turns in the secondary winding
V_{OUT}: Output voltage
V_f: Forward voltage of the secondary rectifier
I_D: Drain current of the power MOSFET
I_{OFF}: Current running through the secondary rectifier during the power MOSFET off-period
C_V: Voltage resonant capacitor
L_P: Primary inductance

Bottom-On Timing

Figure 15 shows the voltage waveform of the OCP pin peripheral circuit and auxiliary winding, D.

This delay time, t_{ONLDLY}, for bottom-on, from the start of V_{DS} free oscillation to the timing of turning-on the power MOSFET, is created by exploiting the auxiliary winding voltage, which synchronizes to the drain voltage V_{DS} waveform.

During turning off the power MOSFET, the auxiliary winding voltage is fed through the delay circuit (D6, R4, C7, and D7 of figure 15) to the OCP pin, and the OCP pin is provided the quasi-resonant signal of positive voltage.

After the power MOSFET turns off, the quasi-resonant signal immediately goes up and it exceeds the Quasi-Resonant Operation Threshold Voltage 1, $V_{BD(TH1)}$ = 0.24 V. After this occurs, the power MOSFET remains off until the quasi-resonant signal comes down enough to cross the Quasi-Resonant Operation Threshold Voltage 2, $V_{BD(TH2)}$ = 0.16 V. Then the power MOSFET again turns on. In addition, at this point, the threshold voltage goes up to $V_{BD(TH1)}$ automatically to prevent malfunction of the quasi-resonant operation from noise interference.

R3 and R4 Setup

R3 is recommended to be between 100 and 330 Ω, and C5 to be between 100 and 470 pF.

R4 must set the range for the quasi-resonant signal: greater than or equal to $V_{BD(TH1)}$ under input and output conditions where V_{CC} becomes lowest, but less than the OCP Pin Overvoltage Protection (OVP) Threshold Voltage, $V_{BD(OVP)}$ = 2.6 V, under conditions where V_{CC} becomes highest.

Figure 16 defines the pulse width of the quasi-resonant signal. For initiating quasi-resonant operation, the quasi-resonant signal pulse width between the two points $V_{BD(TH1)}$ and $V_{BD(TH2)}$, t_{QR}, must be equal to 1.2 µs or more. This pulse width must be ensured, while at the same time the OCP pin peak voltage, $V_{BD(PK)}$, is recommended to be between 1.5 and 2.0 V. Both conditions should be satisfied throughout the power supply input and output ranges, over variations in R3 and R4 actual component values.

Because R_{OCP} is much less than R3, the formula below is used to calculate R4:

$$R_4 = \frac{R_3 \times (V_{CC} - V_{BD(PK)} - 2 \times V_f)}{V_{BD(PK)}} \quad (3)$$

given R3 = 220 Ω, $V_{BD(PK)}$ = 1.5 V, V_{CC} = 16 V, and the V_f of D6

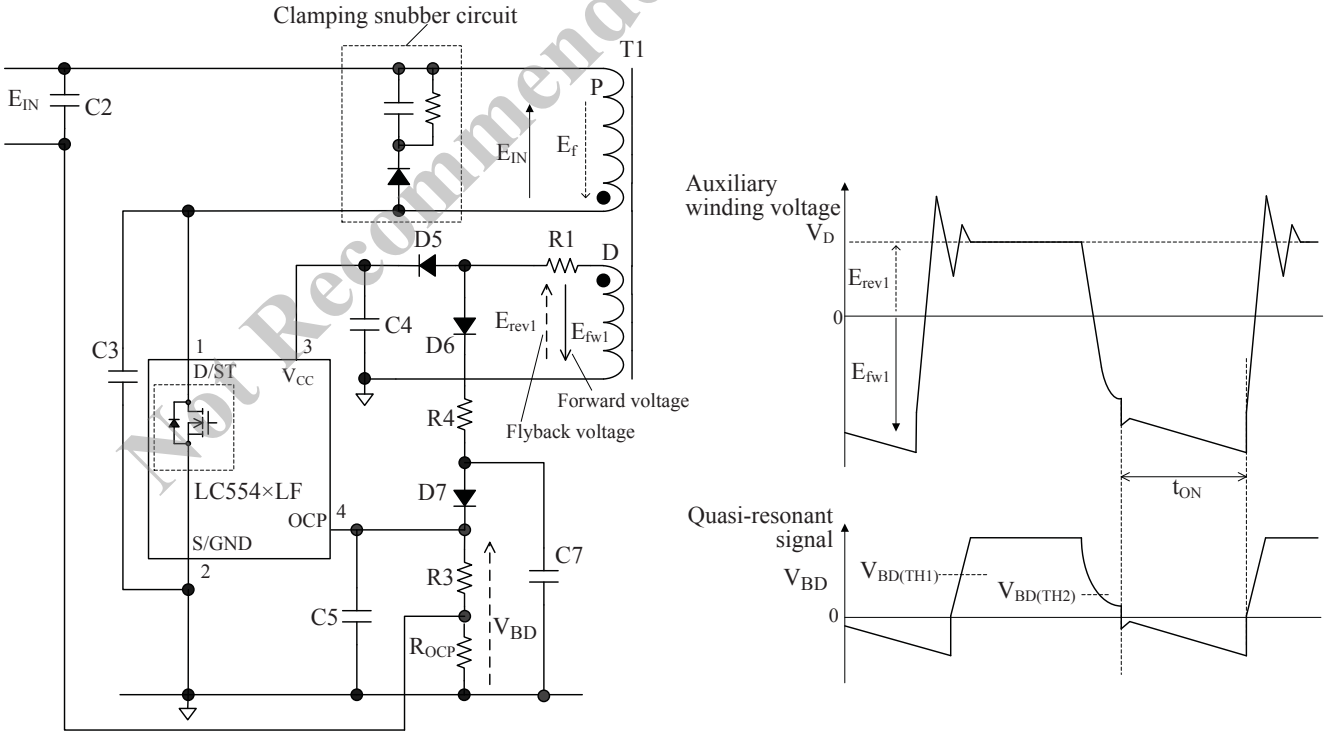


Figure 15. OCP pin peripheral circuit (left) and auxiliary winding voltage and quasi-resonant signal (right)

and D7 = 0.8 V. R4 is approximately 1.89 kΩ, and it is 1.8 kΩ in the E12 series.

If the pulse width is not satisfied, increase R3 or decrease R4, in order to raise $V_{BD(PK)}$. Alternatively, increasing the capacitance of resonant capacitor C3 is also effective because it widens the free oscillation period. However, it causes an additional switching loss increase; therefore, ensure the IC temperature rise is acceptable.

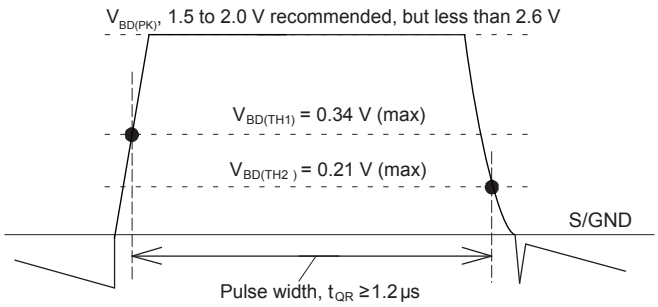


Figure 16. Definition of the pulse width of the quasi-resonant signal

C7 Setup

The delay time, t_{ONDLY}, after which the power MOSFET turns on, is adjusted by the value of C7, so that the power MOSFET turns on at the bottom-on of V_{DS}.

To do so, observe the power MOSFET drain voltage, V_{DS}, the drain currnet, I_D, and the quasi-resonant signal, under the maximum input voltage and the maximum output power, as shown in figure 14.

The following show how to adjust the turn-on point:

- If the turn-on point precedes the bottom of the V_{DS} signal (see figure 17, left panel), it causes higher switching losses. In that situation, after confirming the initial turn-on point, delay the turn-on point by increasing the C7 value gradually, so that the turn-on will match the bottom point of V_{DS}.
- In the converse situation, if the turn-on point lags behind the V_{DS} bottom point (see figure 17, right panel), it causes higher switching losses also. After confirming the initial turn-on point, advance the turn-on point by decreasing the C7 value gradually, so that the turn-on will match the bottom point of V_{DS}.

An initial reference value for C7 is about 1000 pF.

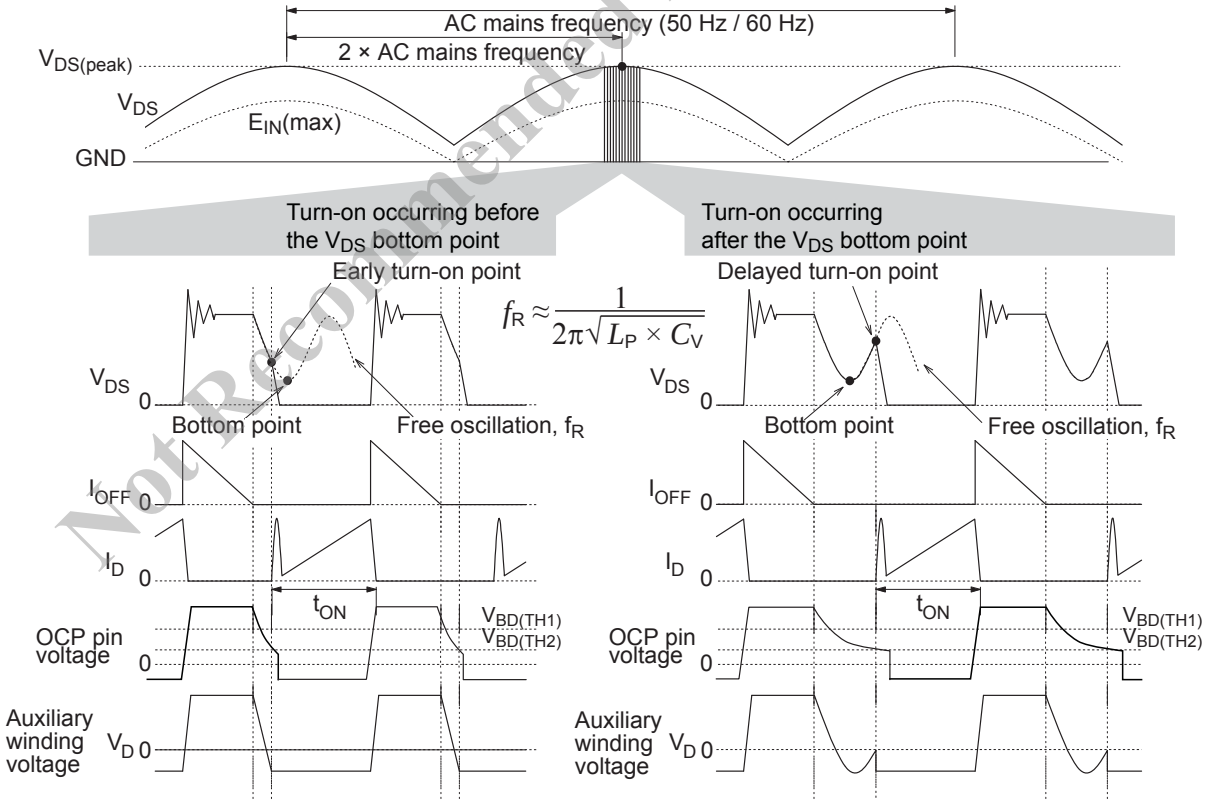


Figure 17. Effects of failure to turn on precisely at the V_{DS} bottom point: (left) turn-on before a bottom point, and (right) turn-on after a bottom point

BD Pin Blanking Time

Figure 18 shows two different OCP pin waveforms, comparing transformer coupling conditions between the primary and secondary winding. The poor coupling tends to happen in a low output voltage transformer design with high N_P/ N_S turns ratio (N_P and N_S indicate the number of turns of the primary winding and secondary winding, respectively), and it results in high leakage inductance. The poor coupling causes high surge voltage ringing at the power MOSFET drain pin when it turns off. That high surge voltage ringing is coupled to the auxiliary winding and then the inappropriate quasi-resonant signal occurs.

The OCP pin has a blanking period of 250 ns (max) to avoid the IC reacting to it, but if the surge voltage continues longer than that period, the IC responds to it and repeatedly turns the power MOSFET on and off at high frequency. This results in an increase of the MOSFET power dissipation and temperature, and it can be damaged.

The following adjustments are required when such high frequency operation occurs:

- C5 must be connected near the OCP pin and the GND pin
- The circuit trace loop between the OCP pin and the GND pin must be separated from any traces carrying high current
- The coupling of the primary winding and the auxiliary winding must be loosened
- The clamping snubber circuit (refer to figure 15) must be adjusted properly.

In addition, the OCP pin waveform during operation should be measured by connecting test probes as short to the OCP pin and the GND pin as possible, in order to measure any surge voltage correctly.

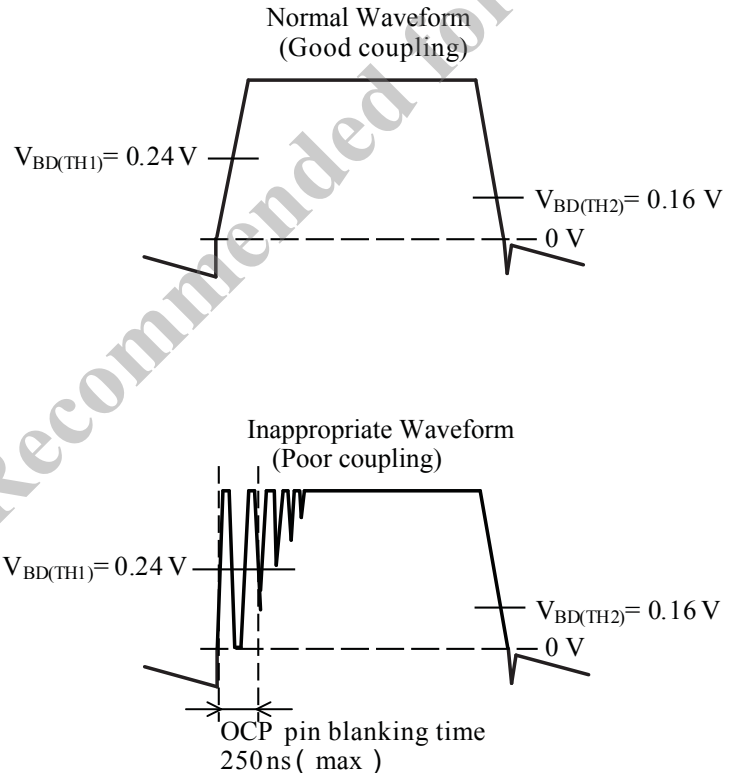


Figure 18. The difference of OCP pin voltage waveform by the coupling condition of the transformer; good coupling (top) versus inappropriate coupling (bottom)

Protection Functions

Latch Function

Overvoltage protection (OVP), Overload protection (OLP), and Thermal shutdown (TSD) protection are latched. After the switching operation stops, the VCC pin voltage will begin to decrease, and when it falls to $V_{CC(BIAS)}$ = 11.0 V, the Bias Assist Function will be activated. When the Bias Assist Function is activated, the startup current is supplied to the VCC pin in order to prevent the VCC pin voltage from decreasing to $V_{CC(OFF)}$ = 9.4 V, and thus the latched state is maintained. Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

Overvoltage Protection (OVP)

The IC has three OVP activation methods: linked to the VCC pin, to the OCP pin, and to the OVP Pin.

• VCC Pin Overvoltage Protection. Figure 19 shows the waveforms of the OVP function on the VCC pin. When the VCC pin voltage with reference to the S/GND pin reaches $V_{CC(OVP)}$ = 31.5 V or more, OVP is activated and the IC stops switching operation in latch mode.

Because VCC pin voltage is proportional to the output voltage, it can be used to detect an output overvoltage event, such as open load condition. In this situation, the detecting voltage, $V_{OUT(OVP)}$, is expressed by the formula below:

$$V_{OUT(OVP)} = \frac{V_{OUT}(\text{normal operation})}{V_{CC}(\text{normal operation})} \times 31.5\ (\text{V}) \quad (4)$$

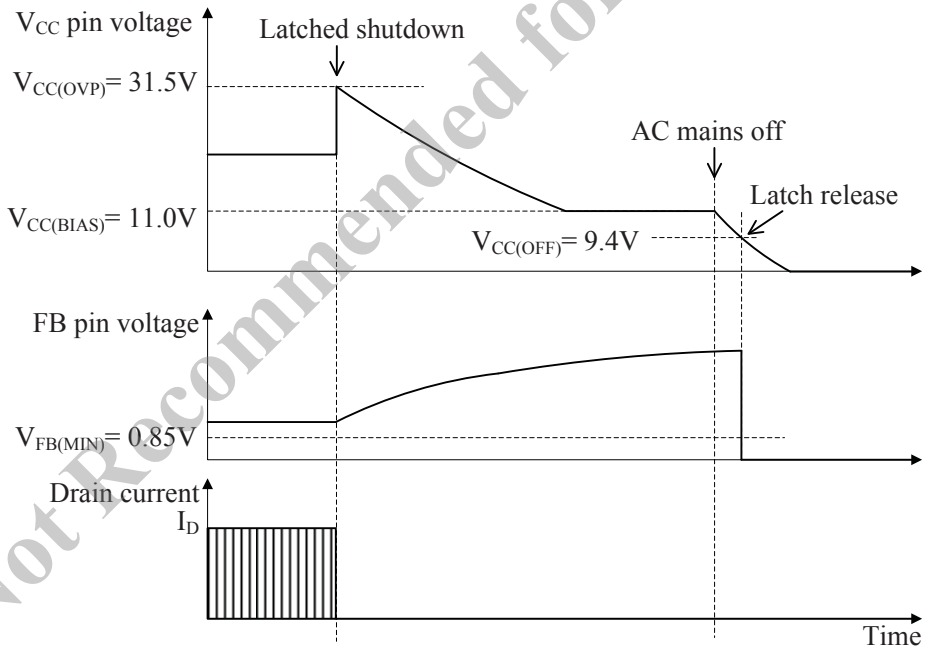


Figure 19. Waveforms when VCC pin OVP function is being activated

• OCP Pin Overvoltage Protection. Figure 20 shows the waveform of the OCP function on the OCP pin. When the OCP pin voltage with reference to the S/GND pin reaches $V_{BD(OVP)}$ = 2.6 V or more, OVP is activated and the IC stops switching operation in latch mode. This input voltage must be less than the absolue maximum rating, 5V.

This can be used as protection in the event that the quasi-resonant signal setup is mistaken or excess load current happens in the use of a poor coupling transformer between the primary and secondary winding.

• OVP Pin Overvoltage Protection. Figure 21 shows the waveform of the OVP function on the OVP pin. When the OVP Pin voltage with reference to the S/GND pin reaches $V_{OVP(OVP)}$ = 2.0 V or more, OVP is activated, and the IC stops switching operation in latch mode. This input voltage must be less than the absolue maximum rating, 5V.

This function can be used through a photocoupler (PC2 as shown in the Typical Application Diagram) to detect an excess output voltage, such as caused by an open load condition, and protect the circuit.

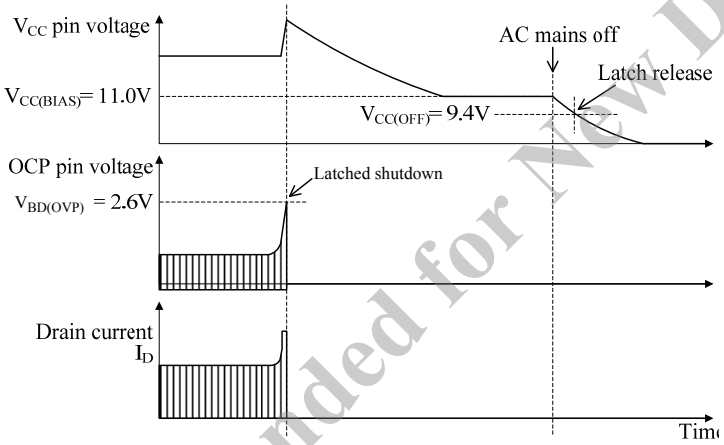


Figure 20. Waveforms when OCP pin OVP function is being activated

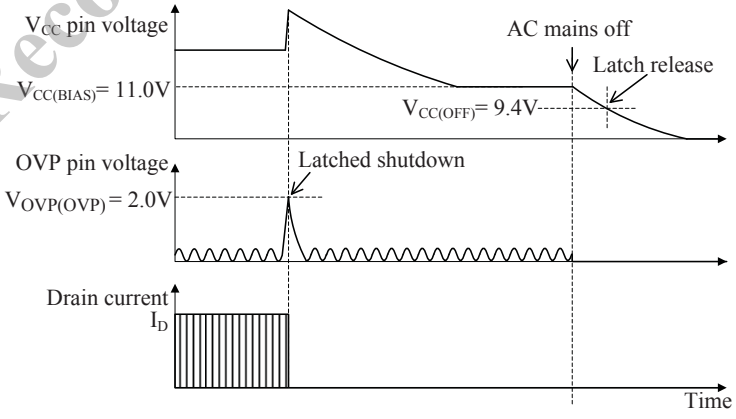


Figure 21. Waveforms when OVP pin OVP function is being activated

Overload Protection (OLP)

The overload protection (OLP) state is a state in which the peak drain current is limited by OCP operation under an overload condition. Figure 22 shows the the waveform of the OLP function on the FB pin. At the overload condition, the VCC pin voltage drops because the output voltage drops. When the VCC pin voltage reaches the Startup Current Threshold Biasing Voltage, $V_{CC(BIAS)}$ = 11.0 V, the Bias Assist Function is activated to avoid the VCC pin voltage from decreasing. Simultaneously, the output voltage decreases so the error amplifier on the secondary side cuts off, and a photo-coupler, PC1, is cut off.

When the error amplifier cuts off, the capacitor C6 connected to the FB pin is charged, and when the FB/OLP pin voltage reaches the OLP Threshold Voltage, $V_{FB(OLP)}$ = 4.5 V, the overload protection circuit will operate and stop switching operation in latch mode. Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

Generally, the target value of capacitor C6 is about 1 to 4.7 µF. If the C6 value is too small, the OLP function may be activated after cycling power to the IC.

The C6 value should be adjusted based on actual operation in the application.

Overcurrent Protection (OCP)

The Overcurrent Protection (OCP) feature monitors the power MOSFET drain current on a pulse-by-pulse basis, in order to limit output power.

OCP Detection Method and Leading Edge Blanking

The drain current of the power MOSFET is detected by the current detection resistor, R_{OCP}, placed between the OCP pin and the S/GND pin, as shown in figure 23.

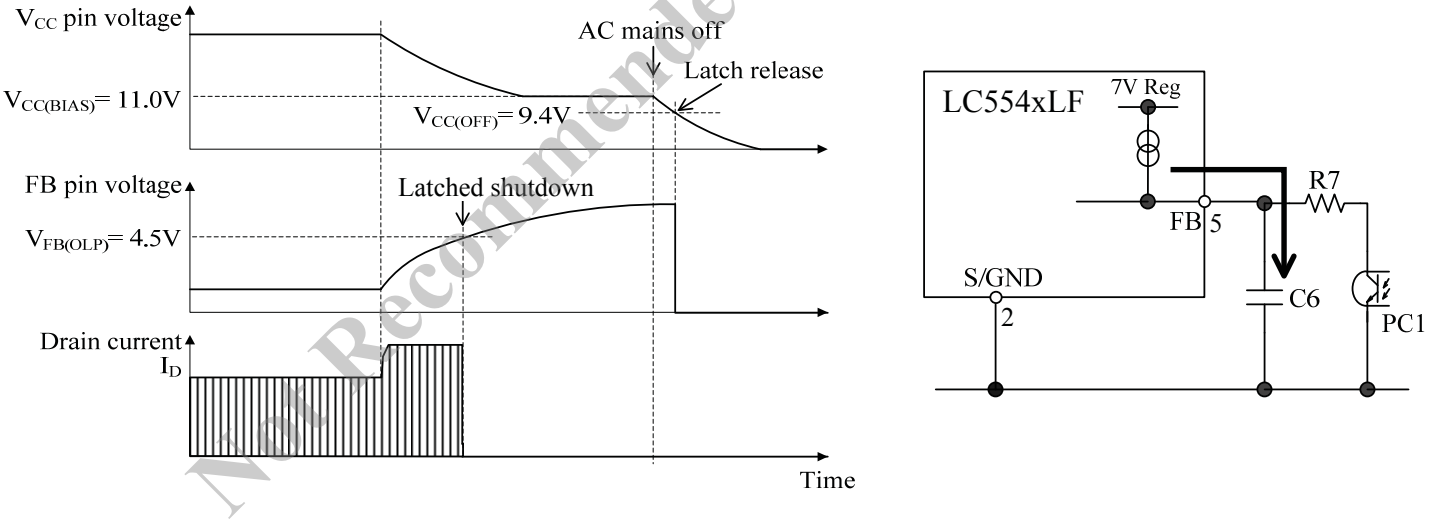


Figure 22. Operation waveform at the time of OLP operation (left) and peripheral circuit (right)

The voltage across R_{OCP}, V_{ROCP}, is fed through R3 to the OCP pin to be detected by it. The turn-off point for the power MOSFET can be determined as that where V_{ROCP} reaches the value of the following equation:

$$V_{ROCP} = -\left(|V_{OCP}| + R_3 \times |I_{OCP}| \right) \quad (5)$$

where

V_{OCP}: OCP threshold voltage (−0.6 V) of the IC,
R_3: R3 resistance, and
I_{OCP}: OCP pin source current (−40 μA) of the IC.

A filter is inserted at the OCP pin in order to prevent malfunction:

• R3 setup. In order to minimize effects of variation in the internal resistor, R3 is recommended to have a value from 100 to 330 Ω.

• C5 setup. C5 is recommended to have a value from 100 to 470 pF, with good temperature characteristics. Selecting larger capacitances for C5 would cause OCP response to become slow, and then it would result in an increase in the peak drain current at transient conditions, such as startup.

Because the OCP function detects a peak current, it can react to the surge voltage at the power MOSFET turn-on edge and thus the power MOSFET might turn off. In order to avoid this, the Leading Edge Blanking Time, $t_{ON(LEB)}$, = 600 ns, is set.

The surge current pulse width must be less than $t_{ON(LEB)}$ as shown in figure 24. In case its width is longer than that, try these measures:

• adjust the turn-on point to the V_{DS} bottom point

• reduce the voltage resonant capacitor C_V (C3 in figure 23) capacitance

• reduce the secondary rectifier snubber capacitor capacitance

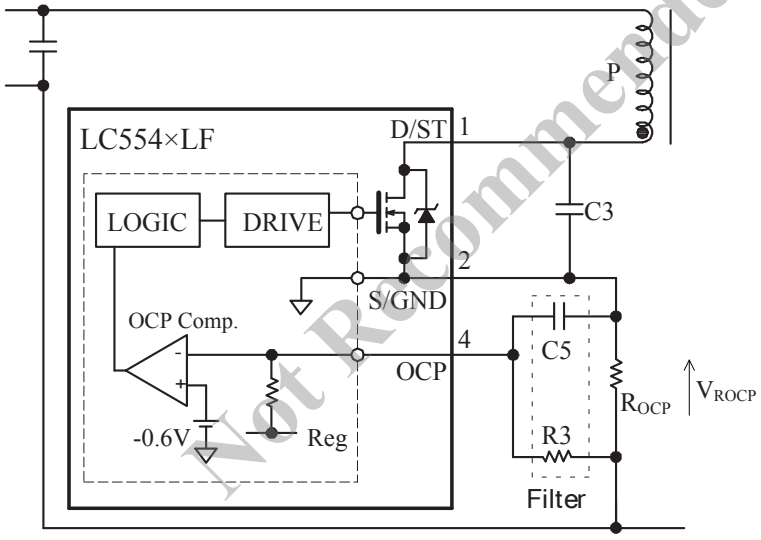


Figure 23. OCP circuit for negative side detect

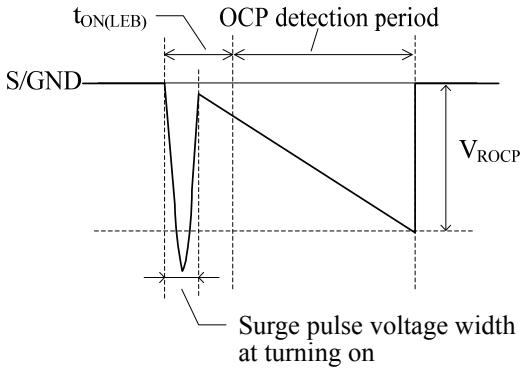


Figure 24. OCP pin voltage (converted from MOSFET drain current by R_{OCP})

OCP Input Compensation Function

This Overcurrent Input Compensation function can compensate the OCP threshold voltage according to the AC input voltage. When using a quasi-resonant converter with universal input (85 to 265 VAC), if the output power is set constant, then because higher input voltages have higher frequency, the MOSFET peak drain current becomes low.

Because R_{OCP} is fixed, the OCP point in the higher input voltage will shift further into the overload area, as shown by curve A in figure 25. In order to suppress this phenomenon, this IC has the Overcurrent Input Compensation function.

As for determining an input compensation value, it is necessary to avoid excessive input compensation for the output current specification, I_{OUT}, as shown in figure 25. When excessive input compensation is applied, $I_{OUT(OCP)}$ may be below I_{OUT} in the situation where the input voltage is high. Therefore, it is necessary to ensure that $I_{OUT(OCP)}$ remains more than I_{OUT} across the input voltage range.

Figure 26 shows an overcurrent input compensation circuit (D_{X1}, DZ_{X1}, R_{X1}).

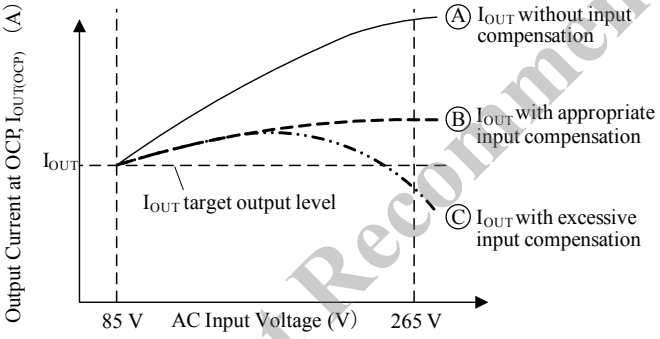


Figure 25. OCP circuit input compensation

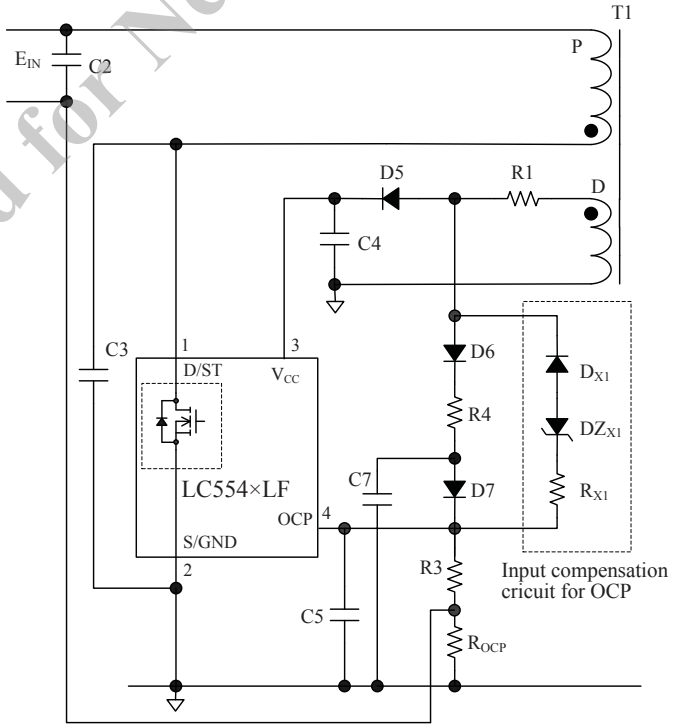


Figure 26. External OCP input compensation circuit

The OCP compensation amount depends on values of the input compensation current, R_{X1}, R3, and R_{OCP} (see figure 27). The input compensation current, I, is expressed by the following equation:

$$I = \frac{E_{fw1} - V_{ZX1} - V_{FX1}}{R_{X1} + R_3 + R_{OCP}} \quad (6)$$

where

I: Input compensation current,
E_{fw1}: Forward voltage of the auxiliary winding D proportional to input voltage,
V_{FX1}: D_{X1} forward voltage, and
V_{ZX1}: DZ_{X1} Zener voltage.

OCP threshold voltage after input compensation, V'_{ROCP}, is expressed by the following equation:

$$V'_{ROCP} = -\left[\left(|V_{OCP}| + |R_3 \times I_{OCP}|\right) - R_3 \times I\right] \quad (7)$$

This input Compensation Current, I, creates the voltage of $R_3 \times I$, and it lowers the absolute value of the compensated OCP threshold voltage to less than the original OCP threshold voltage, V_{OCP} = –0.6 V. This way, when E_{IN} is high, the compensation amount becomes high.

The DZ_{X1} Zener diode is used to set the voltage at which the input compensation begins, so choose the Zener voltage value that is equal to E_{fw1} at the time when input compensation begins.

Optimize the circuit in a way to minimize the difference between the overcurrent points at low and high AC input voltage. Also ensure that the output current meets its target over the entire AC input voltage range, as the curve B in figure 25 (appropriate input compensation). The OCP pin voltage, including surge voltage, must not exceed its absolute maximum rating of –2.0 to 5.0 V at the highest AC input voltage.

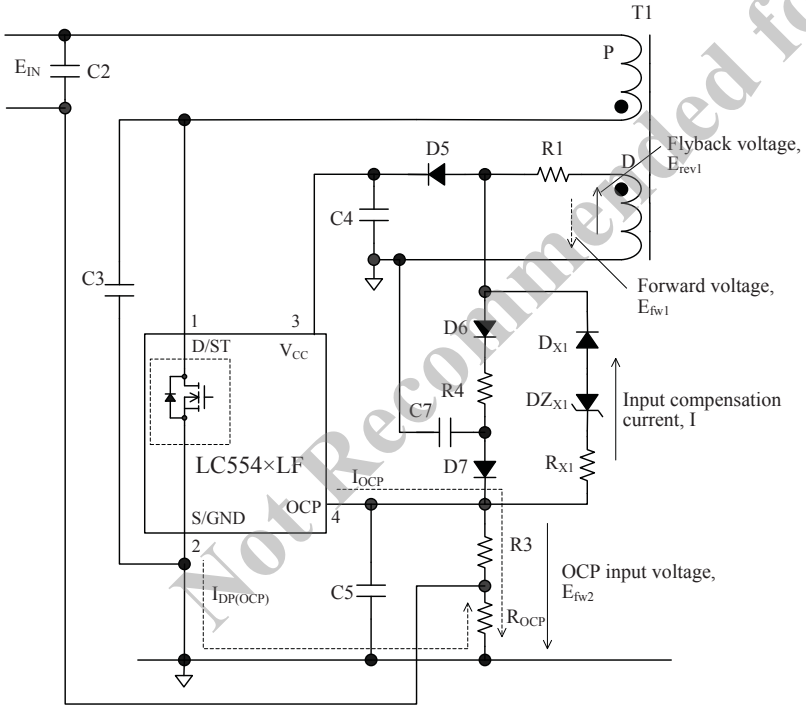


Figure 27. OCP input compensation circuit

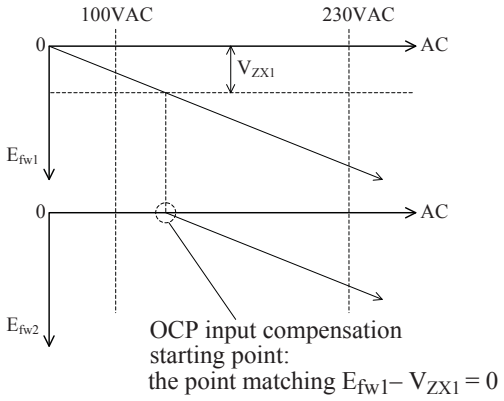


Figure 28. E_{fw1} and E_{fw2} voltage relative to AC input voltage

OCP Threshold Voltage with and without the OCP Input Compensation Circuit

OCP threshold voltage without OCP input compensation circuit, V_{ROCP}, is expressed by equation 8. As shown in figure 29, when V_{ROCP} with reference to the S/GND pin is equal to the sum of the OCP threshold voltage, V_{OCP}, and the voltage across R3 (= R3 × I_{OCP}), then OCP operations will start.

$$V_{ROCP} = -|R_{OCP} \times I_{DP(OCP)}| = -\left(|V_{OCP}| + R_3 \times |I_{OCP}|\right) \quad (8)$$

where

$I_{DP(OCP)}$: Peak drain current during OCP operation,
V_{OCP}: OCP threshold voltage (−0.6 V) of the IC, and
I_{OCP}: OCP pin source current (−40 μA) of the IC.

In the converse situation, with the input compensation circuit, as shown in the figure 30, the overcurrent detecting voltage is equal to the sum of the Overcurrent Protection Threshold Voltage (V_{OCP}), the voltage across R3 (= $R_3 \times I_{OCP}$), and $-R_3 \times I$, then OCP operations will start:

$$V'_{ROCP} = -|R'_{OCP} \times I'_{DP(OCP)}| = -\left[\left(|V_{OCP}| + |R_3 \times I_{OCP}|\right) - R_3 \times I\right] \quad (9)$$

where,

$I'_{DP(OCP)}$: The peak drain current during OCP operation with OCP input compensation circuit,
V_{OCP}: OCP threshold voltage (−0.60 V) of the IC,
I_{OCP}: OCP pin source current (−40 μA), and
I: Input compensation current.

Thus, by adding OCP input compensation circuit, OCP threshold voltage during OCP operation will be changed and the output power is limited.

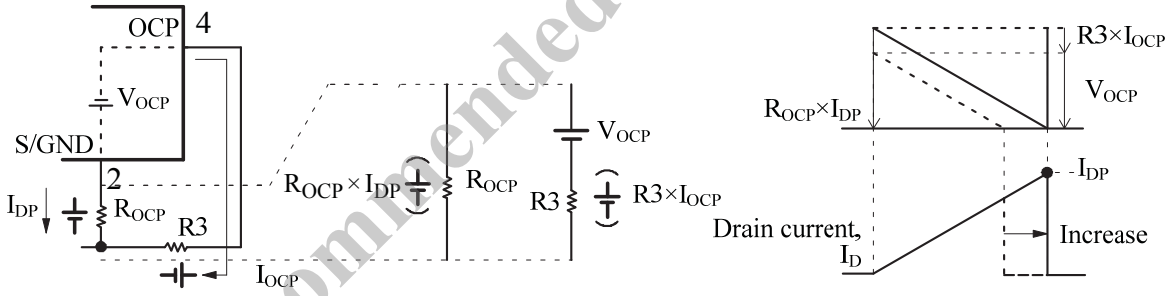


Figure 29. Without OCP input compensation function

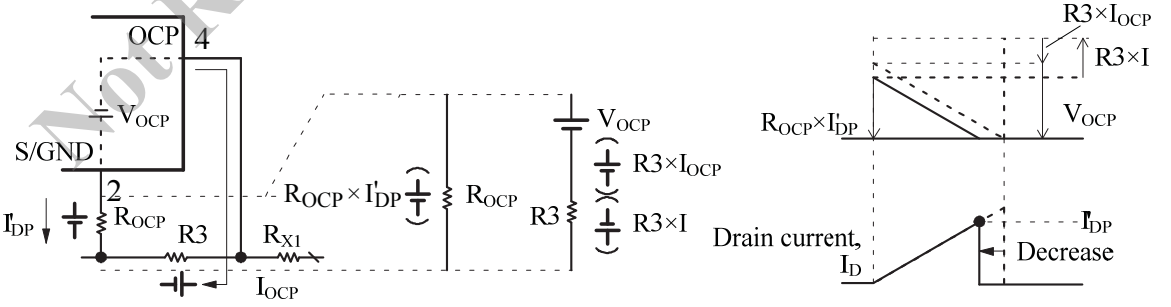


Figure 30. With OCP input compensation function

Determining OCP pin input compensation circuit component values

Given:

I_{DP}, Peak drain current of power MOSFET

V_{FX1}, D_{X1} forward voltage

V_{ZX1}, DZ_{X1} Zener voltage

V_{OCP}, OCP threshold voltage: −0.6 V at the IC

I_{OCP} , OCP pin source current; −40 µA at the IC

I, Input compensation current

Other component numbers, such as resistors, are as referred to in figure 27.

1. The peak drain current during OCP operation without OCP input compensation circuit, $I_{DP(OCP)}$, is expressed by the following equation, derived from equation 8. $I_{DP(OCP)}$ is equal to the drain current limited by OCP threshold voltage without OCP input compensation function at the minimum AC input voltage:

$$|I_{DP(OCP)}| = \frac{|V_{OCP}| + R_3 \times |I_{OCP}|}{R_{OCP}} \quad (10)$$

2. The overcurrent detecting peak drain current with the input compensation circuit, $I'_{DP(OCP)}$, is expressed by the following equation, derived from equation 9. $I'_{DP(OCP)}$ is set to to the peak drain current where the output current is equal to that at the maximum AC input voltage of the curve B in figure 25 (appropriate input compensation):

$$I'_{DP(OCP)} = \frac{|V_{OCP}| + R_3 \times (|I_{OCP}| - I)}{R_{OCP}} \quad (11)$$

3. The input compensation current, I, can be expressed by the following equation, derived from equations 10 and 11:

$$I = (|I_{DP(OCP)}| - |I'_{DP(OCP)}|) \times \frac{R_{OCP}}{R_3} \quad (12)$$

4. The forward voltage, E_{fw1}, at C2 peak voltage $E_{IN(PK)MAX}$ of the maximum AC input voltage is expressed as follows:

$$E_{fw1} = \frac{N_D \times E_{IN(PK)MAX}}{N_P} \quad (13)$$

5. To calculate component values for R_{XI} so that the input compensation circuit provides adequate input compensation current, I, at the maximum AC input voltage, $E_{IN(PK)MAX}$, the following equation is used:

$$I = \frac{E_{fw1} - V_{ZX1} - V_{FX1}}{R_{X1} + R_3 + R_{OCP}} \quad (14)$$

assuming: R3 and $R_{OCP} \ll R_{X1}$, then:

$$R_{X1} = \frac{E_{fw1} - V_{ZX1} - V_{FX1}}{I} \quad (15)$$

and, from equations 13 and 15:

$$R_{X1} = \frac{\frac{N_D \times E_{IN(PK)MAX}}{N_P} - (V_{ZX1} + V_{FX1})}{I} \quad (16)$$

AC input compensation circuit design example with universal input

When the input voltage is universal specification (85 to 265 VAC), the OCP pin input voltage compensation circuit (DZ_{X1}, R_{X1}) rating is calculated as follows, but should also be checked for functional operation in the actual application:

Given:

E_{IN}, AC input voltage: 85 to 265 VAC

P_{OUT}, Output power: 40 W

N_P, Transformer primary winding turns: 40 T

N_D, Transformer auxiliary winding turns: 6 T

R_{OCP}, OCP detection resistor: 0.2 Ω

R3, Filter resistor at the OCP pin: 220 Ω

V_{FX1}, D_{X1} forward voltage: 0.8 V

$I_{DP(OCP)}$, Drain current during OCP operation, measured at E_{IN}(min) of 85 VAC: 3.0 A

$I'_{DP(OCP)}$, Drain current when the output current is equal to that at the maximum AC input voltage of the curve B in figure 25 (appropriate input compensation): 1.9 A

The OCP input compensation startup voltage, $V_{IN(OCP\_ST)}$, should be set in the range of 100 to 130 VAC. Tentatively, for this example, $V_{IN(OCP\_ST)}$ is set to 120 VAC.

1. Calculate DZ_{X1} value. E_{fw1} at 120 VAC input:

$$E_{fw1} = \frac{N_D}{N_P} \times E_{IN(PK)}(\max) \quad (17)$$

$$= \frac{N_D}{N_P} \times V_{IN(OCP\_ST)} \times \sqrt{2}$$

$$= \frac{6\ (T)}{40\ (T)} \times 120\ (VAC) \times \sqrt{2} = 25.5\ V$$

Thus, select 27 V as the Zener value for DZ_{X1}.

2. The compensation current, I, is calculated using equation 12:

$$I = (3.0\ (A) - 1.9\ (A)) \times \frac{0.2\ (\Omega)}{220\ (\Omega)} = 1\ mA$$

3. R_{X1} can be calculated using equation 16:

$$R_{X1} = \frac{\frac{6\ (T) \times 265\ (VAC)\sqrt{2}}{40\ (T)} - (27\ (V) + 0.8\ (V))}{1\ (mA)} = 28.4\ k\Omega$$

Thus, select R_{X1} = 27 kΩ out of the E12 series.

Finally, ensure that the output current limited by OCP operation is similar to that of the curve B in figure 25 (appropriate input compensation), in actual operation throughout AC input voltage ranges. If necessary, re-adjust the rating of DZ_{X1} and R_{X1} by changing the compensation startup voltage $V_{IN(OCP\_ST)}$ for OCP pin input voltage.

Thermal Shutdown Protection

Thermal Shutdown protection is activated when the temperature of the Control Part in the IC reaches $T_{J(TSD)}$ = 135°C(min), and then the IC stops switching operation in latch mode. Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

Maximum On-Time Limiting Function

The maximum on-time, set at $t_{ON(MAX)}$ = 17.5 µs, limits lower side operation frequency (see figure 31), and it minimizes audible noise from the transformer, as well as power stress on the incorporated MOSFET and secondary rectifier at low AC input or during transient periods such as at switching AC input voltage on or off.

Ensure that the actual on-time at the minimum AC input and the maximum load condition does not reach $t_{ON(MAX)}$. If that does happen, redesign the transformer, such as by reducing the primary inductance, L_P, or reducing the duty cycle by lowering the turns ratio of N_P / N_S.

Design Notes

Peripheral Components

Take care to use properly rated and proper type of components.

- Output smoothing capacitor. Consider design margins for ratings of ripple current, voltage, and temperature in selecting the output capacitor. A low impedance capacitor, designed to be tolerant against high ripple current, is recommended.
- Transformer. Consider design margins for temperature rise, resulting from copper losses and core losses, in designing or selecting a transformer.

  Switching current contains a high frequency component that causes the skin effect; therefore, consider a current density of 3 to 4 A/mm^2 and select a wire gauge based on RMS current.

  In the event further temperature measurement is necessary, try the following measures to increase the surface area of the wire:
  - Increase the quantity of parallel wires
  - Use litz wire
  - Increase the diameter of the wires
- Current detection resistor, R_{OCP}. Choose a low equivalent series inductance and high surge tolerant type for the current detection resistor. If a high inductance type is used, it may cause malfunctioning because of the high frequency current running through it.

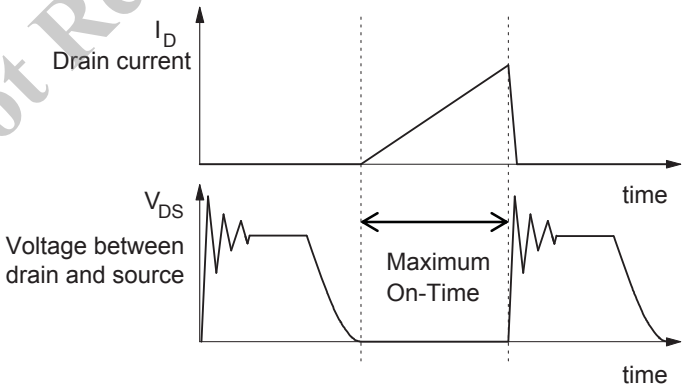


Figure 31. Confirmation of Maximum On-Time

Transformer Design

Figure 32 shows an ideal waveform in average current control relative to a sine wave of AC input voltage. The Average Current Control function controls FB pin voltage at a fixed rate relative to the sine wave of AC input voltage, V_{IN}, at commercial frequencies. Therefore, the envelope curve of the peak drain current, I_{DP}, and the input current, I_{IN} (which is the averaged I_{DP}), shows a sine waveform which is similar to that of the AC input voltage.

To set the fixed FB pin voltage, the value of C6 (connected to the FB pin) and the secondary side current detection resistor must be be adjusted.

The transformer design is the same as for an RCC (ringing choke converter, or self-oscillation flyback converter) transformer design. However, a quasi-resonant operation includes a certain delay to turn-on, so duty cycle must be compensated. Moreover, for input capacitorless applications, the applied voltage of a transformer is the sine wave of the AC input voltage, V_{IN}, at commercial frequencies.

Therefore, the duty cycle compensation for quasi-resonant delay time is added to the basic equation of the RCC topology; moreover, the equation must be changed into the sine wave of the AC input voltage, V_{IN}.

In consideration of quasi-resonant delay time, the primary side inductance, L'_P, applied the sine wave of AC input voltage, is expressed by the following equation:

$$L'_P = \frac{(V_{INRMS(MIN)} \times D_{ON})^2}{\left(\sqrt{\frac{2 \times P_{OUT} \times f_{S(MIN)}}{\eta}} + V_{INRMS(MIN)} \times D_{ON} \times f_{S(MIN)} \times \pi \sqrt{C_V}\right)^2} \quad (18)$$

where

$V_{INRMS(MIN)}$: Effective value (rms) of the sine wave of the minimum AC input voltage,

P_{OUT}: Maximum output power:

$$P_{OUT} = V_{OUT} \times I_{OUT} \quad (19)$$

where V_{OUT} is the output voltage, and I_{OUT} is the maximum output current,

$f_{S(MIN)}$: Operation frequency at the peak voltage of the sine wave of AC input voltage (the minimum operation frequency in quasi-reaonant operation),

η: Efficiency rate: 80% to 90%,

C_V: Voltage resonant capacitor (C3) rating: usually 47 to 470 pF

D_{ON}: Maximum duty cycle, not compensated for the quasi-resonant delay time, at the minimum AC input voltage:

$$D_{ON} = \frac{E_f}{\sqrt{2} \times V_{INRMS(MIN)} + E_f} \quad (20)$$

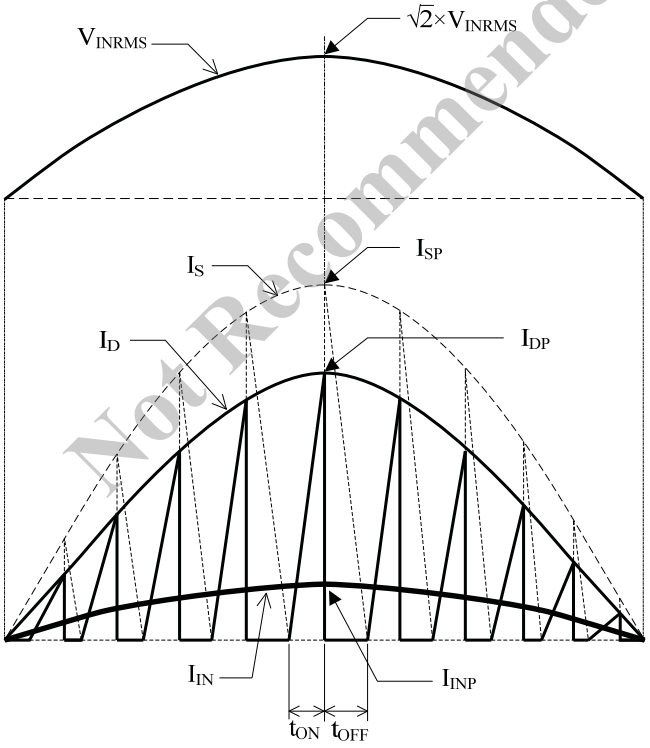


Figure 32. Ideal current waveform

V_{INRMS}: Effective value (RMS) of sine wave of AC input voltage
I_{IN} : Input current
I_{INP} : Peak input current
I_D : Power MOSFET drain current
I_{DP} : Power MOSFET peak drain current
I_S : Forward current of a secondary side rectifier
I_{SP} : Peak forward current of a secondary side rectifier

E_f : Flyback voltage:

$$E_f = (N_P / N_S) \times (V_{OUT} + V_f) \quad (21)$$

where N_P is the number of turns of the primary winding, N_S is the number of turns of the secondary winding, and V_f is the forward voltage of the secondary rectifier, D8, approximately 0.7 V.

E_f is determined by the power MOSFET breakdown voltage and the surge voltage. Because the breakdown voltage of the power MOSFET of this IC is 650 V, when it is used with the specified universal input range, the target voltage of E_f is 100 to 150 V.

Quasi-resonant delay time, t_{ONDLY}:

$$t_{ONDLY} = \pi\sqrt{L'_P \times C_V} \quad (22)$$

Maximum duty cycle, compensated for quasi-resonant delay time (t_{ONDLY}), D'_{ON}:

$$D'_{ON} = (1 - f_{S(MIN)} \times t_{ONDLY}) \times D_{ON} \quad (23)$$

Input rms current of the sine wave of the minimum AC input voltage, $I_{INRMS(MAX)}$:

$$I_{INRMS(MAX)} = \frac{P_{OUT}}{\eta \times V_{INRMS(MIN)}} \quad (24)$$

Peak drain current, compensated for quasi-resonant delay time (t_{ONDLY}), $I_{DP(DLY)}$:

$$I_{DP(DLY)} = \frac{2\sqrt{2} \times P_{OUT}}{\eta \times D'_{ON} \times V_{IN(RMS(MIN)}} \quad (25)$$

In transformer design, the AL-value of the ferrite core should be chosen so the transformer dose not saturate, in consideration of NI-Limit(AT) (= $N_P \times I_{DP(DLY)}$).

When choosing a ferrite core to match the relationship of NI-Limit (AT) versus AL-value, it is recommended to set the calculated NI-Limit value below about 30% from the NI-Limit curve of ferrite core data, as shown in the hatched area containing the design point in figure 33, to provide a design margin in consideration of temperature effects and other variations, as expressed by the formulas below:

$$\text{NI-Limit} \leq N_P \times I_{DP(DLY)} \times 130\% \quad (26)$$

$$N_P = \sqrt{\frac{L'_P}{\text{AL-Value}}} \quad (27)$$

Then, the rest of the winding turns are determined by the formulas below.

$$N_S = \frac{V_{OUT} + V_f}{E_f} \times N_P \quad (28)$$

$$N_D = \frac{V_{CC}}{V_{OUT} + V_f} \times N_S \quad (29)$$

Trace and Component Layout Design

PCB circuit trace design and component layout affect IC functioning during operation. Unless they are proper, malfunction, significant noise, and large power dissipation may occur.

Circuit loop traces flowing high frequency current, as shown in figure 34, should be designed as wide and short as possible to reduce trace impedance.

In addition, earth ground traces affect radiation noise, and thus should be designed as wide and short as possible.

Switching mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layout should be done in compliance with all safety guidelines.

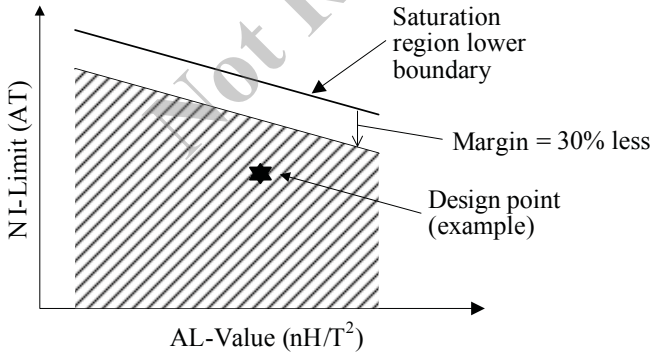


Figure 33. Example of NI-Limit versus AL-Value characteristics

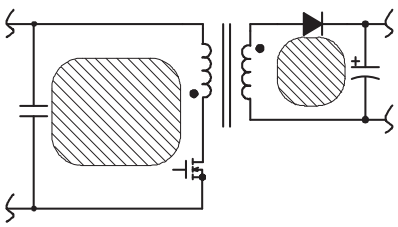


Figure 34. High frequency current loops (hatched portion)

Furthermore, because an integrated power MOSFET is being used as the switching device, take account of the positive thermal coefficient of $R_{DS(on)}$ for thermal design.

Figure 35 shows practical trace design examples and considerations. In addition, observe the following:

• IC peripheral circuit

(1) Traces among S/GND pin, R_{OCP}, C2, T1(primary winding), and D/ST pin

The traces carry the switching current; therefore, widen and shorten them as much as possible.

The input capacitor C2 must be placed close to the IC or the transformer in order to reduce series inductances of the traces against high frequency current.

(2) Traces among S/GND pin, C4(–), T1(auxiliary winding D), R1, D5, C4(+), and VCC pin

This trace is for supplying voltage to the IC. Widen and shorten the traces as much as possible. If the IC and the capacitor C4 are apart, place a film or ceramic capacitor (0.1 to 1.0 μF) as close to the VCC pin and the S/GND pin as possible.

(3) Current Detection Resistor, R_{OCP}:

Place R_{OCP} as close to the S/GND pin as possible. In addition, in order to avoid interference of the switching current with the control circuit, connect the trace of R3 to the base of R_{OCP} at the point A in figure 35.

• Secondary side, traces among T1(secondary winding), D8, and C9

The secondary-side switching current runs through this trace. Widen and shorten the traces as much as possible.

Thin and long traces cause the series inductance to be high and it results in high surge voltage on the power MOSFET when it turns off. Therefore, proper layout pattern design helps to increase the voltage margin of the power MOSFET to its breakdown voltage and to reduce power stress and losses in the clamping snubber circuit.

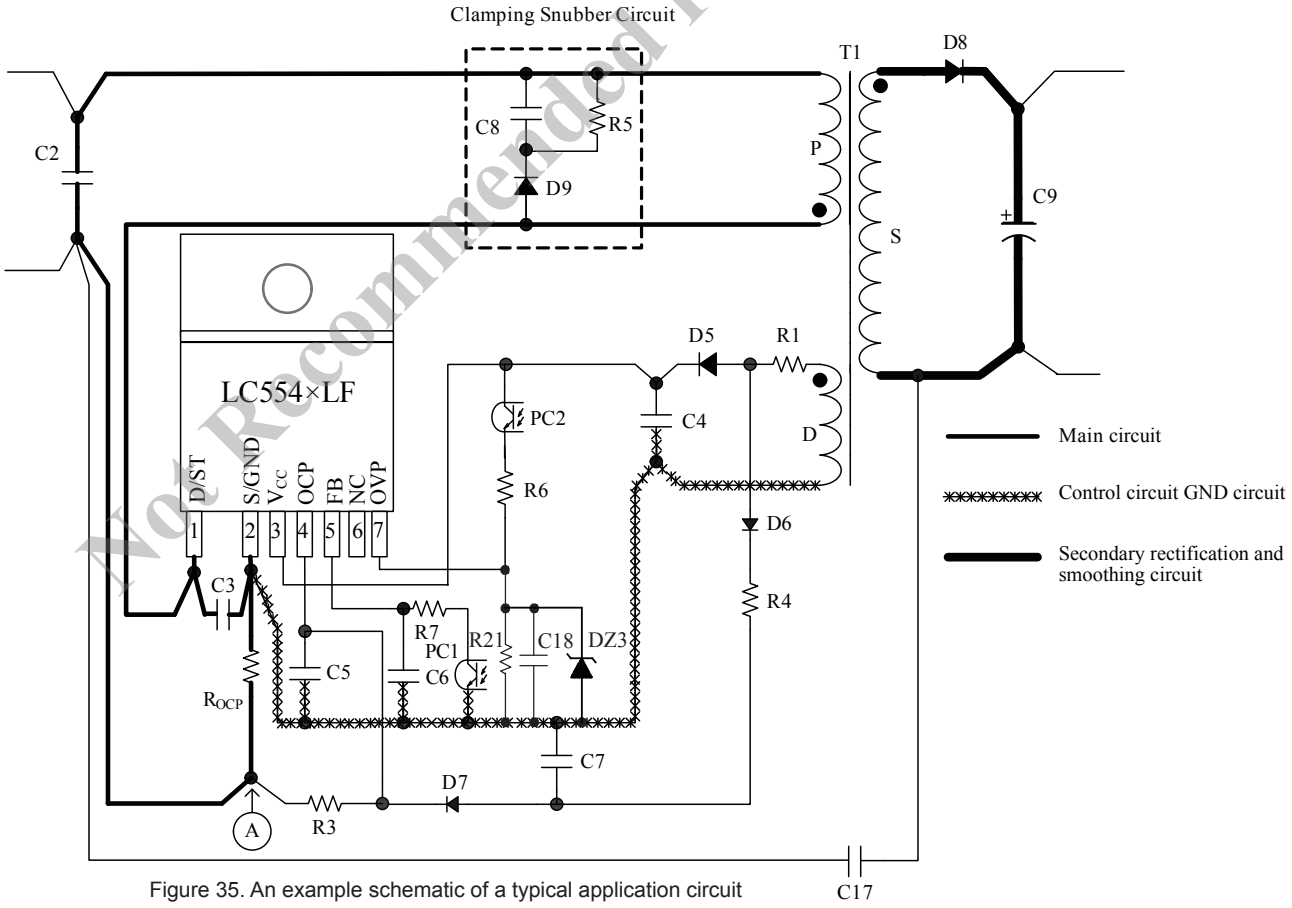


Figure 35. An example schematic of a typical application circuit

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