1 Converter High Power Factor LED Driver ICs

LC5581AS/LS

Data Sheet

Description

The LC5581AS and LC5581LS are quasi-resonant LED driver ICs. The ICs can also operate in PWM mode. The ICs support isolated and non-isolated buck circuits and buck-boost converters.

The ICs provide the systems that can comply with the harmonics standard (IEC61000-3-2 Class C) in all conditions, including a light load condition. These systems, moreover, can be achieved by 1 converter system that requires no input electrolytic capacitor.

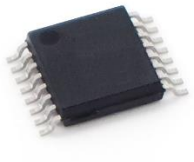
The ICs employ the average current and quasi-resonant controls: the average current control realizes high power factors, whereas the quasi-resonant control contributes to high efficiency and low noise. Having a rich set of protection features, the ICs can provide more cost-effective power supply systems with fewer external components.

Features

- 800 V High Voltage Built-in Startup Circuit
- Analog Dimming Function
- High Power Factor by Average Current Control
- Soft Start Function
- Shorter Time from Startup to LED Lighting
  – COMP Pin Fast Charging Function
  – Bias Assist Function that Includes Two Types that are Activated at Different Voltage Levels (Smaller Capacitance of the VCC Pin)
- Standby Function
- Leading Edge Blanking Function
- Maximum On-time Limitation Function
- Protections
  Overcurrent Protection (OCP): Pulse-by-pulse
  Overload Protection (OLP): Auto-restart
  Overvoltage Protection (OVP): Latched Shutdown/ Auto-restart

Package

VSOP16



Not to scale

Selection Guide

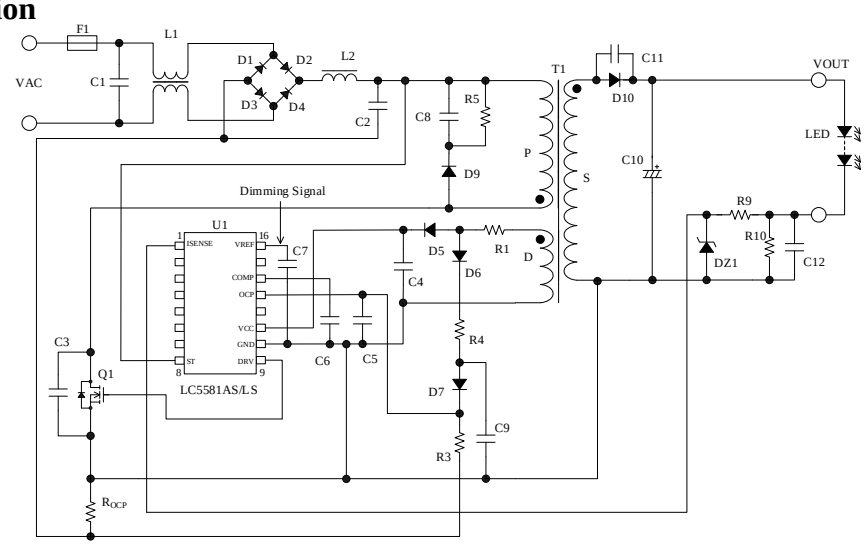
- Specifications
  Gate Drive Output Voltage, V_{DRV} = 8.2 V
  DRV Pin Output Impedance, $R_{DRV(SOURCE)}$ = 45 Ω
  DRV Pin Input Impedance, $R_{DRV(SINK)}$ = 15 Ω
- Protection Operation

Part Number	Protection Operation	
	OLP	OVP
LC5581AS	Auto-restart	Auto-restart
LC5581LS	Auto-restart	Latched shutdown

Applications

- LED Lighting Equipment
- LED Bulbs

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless otherwise specified, T_A = 25 °C.

Surge withstand capability (HBM) of the LC5581AS/LS is guaranteed as follows: 1000 V for pin 8, and 2000 V for the other pins.

Parameter	Symbol	Conditions	Pin	Rating	Unit
OCP Pin Voltage	V_{OCP}		13 – 10	−2.0 to 5.0	V
COMP Pin Voltage	V_{COMP}		14 – 10	−0.3 to 7.0	V
VREF Pin Voltage	V_{REF}		16 – 10	−0.3 to 5.0	V
ISENSE Pin Voltage	V_{ISEN}		1 – 10	−0.3 to 5.0	V
ST Pin Voltage	V_{ST}		8 – 10	−0.3 to 800	V
DRV Pin Voltage	V_{DRV}		9 – 10	−0.3 to V_{DRV} +0.3	V
VCC Pin Voltage	V_{CC}		11 – 10	35	V
Operating Ambient Temperature	T_{OP}		—	−55 to 125	°C
Storage Temperature	T_{STG}		—	−55 to 125	°C
Junction Temperature	T_J		—	150	°C

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit
Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		11 – 10	13.8	15.1	17.3	V
Operation Stop Voltage[1]	$V_{CC(OFF)}$		11 – 10	8.4	9.4	10.7	V
Circuit Current in Operation	$I_{CC(ON)}$		11 – 10	—	—	4.7	mA
Startup Circuit Operation Voltage	$V_{ST(ON)}$		8 – 10	19	22	25	V
Startup Current at VCC Pin Shorted	$I_{CC(ST)\_S}$	V_{CC} = 0 V	11 – 10	−600	−300	−100	µA
Startup Current	$I_{CC(ST)}$	V_{CC} = 13.5 V	11 – 10	−9.5	−6.3	−3.2	mA
Bias Assist Threshold Voltage in Normal Operation [1]	$V_{CC(BIAS\_NOM)}$	I_{CC} = −500 µA	11 – 10	9.5	11.0	12.5	V
Bias Assist Threshold Voltage in Startup [1]	$V_{CC(BIAS\_IN)}$	I_{CC} = −500 µA	11 – 10	14.5	16.0	17.5	V
Bias Assist Release Threshold Voltage in Startup [1]	$V_{CC(BIAS\_OUT)}$	I_{CC} = −500 µA	11 – 10	15.1	16.6	18.1	V

[1] Always in the condition of $V_{CC(OFF)} < V_{CC(BIAS\_NOM)} < V_{CC(BIAS\_IN)} < V_{CC(BIAS\_OUT)}$.

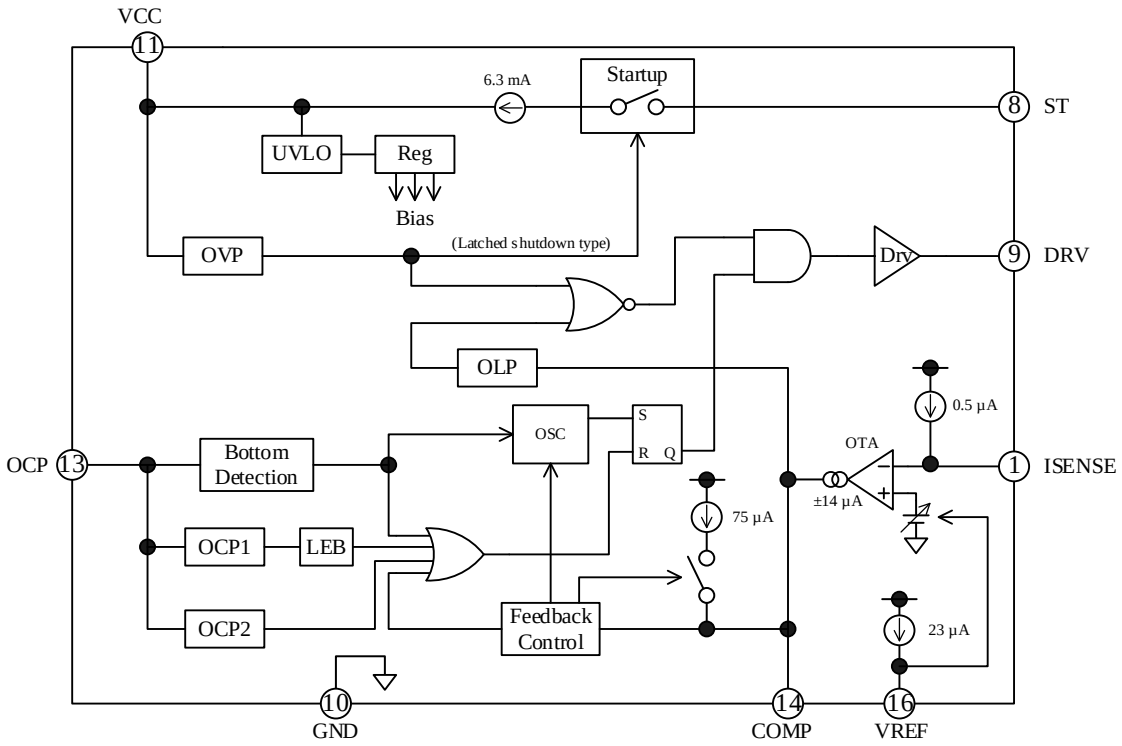
Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit
Normal Operation							
PWM Operation Frequency	f_{OSC}		9 – 10	50	60	70	kHz
Maximum On-time	$t_{ON(MAX)}$		9 – 10	8.0	10.0	13.5	µs
COMP Pin Fast Charging Current	$I_{COMP(CHG)}$		14 – 10	−100	−75	−50	µA
COMP Pin Fast Charging Stop Voltage	$V_{COMP(CHG\_STOP)}$		14 – 10	0.20	0.68	1.00	V
Minimum COMP Pin Control Voltage	$V_{COMP(MIN)}$		14 – 10	0.40	0.85	1.10	V
Error Amplifier Reference Voltage (2)	$V_{ISEN(TH)}$	I_{COMP} = 0 µA	1 – 10	0.285	0.300	0.315	V
Error Amplifier COMP Pin Source Current	$I_{COMP(SOURCE)}$	V_{SENSE} = 0 V	14 – 10	−22	−14	−6	µA
Error Amplifier COMP Pin Sink Current	$I_{COMP(SINK)}$	V_{SENSE} = 0.6 V	14 – 10	6	14	22	µA
VREF Pin Source Current	I_{REF}	V_{REF} = 4.5 V	16 – 10	−33	−23	−13	µA
Quasi-Resonant Operation Threshold Voltage 1	$V_{BD(TH1)}$		13 – 10	0.14	0.24	0.34	V
Quasi-Resonant Operation Threshold Voltage 2	$V_{BD(TH2)}$		13 – 10	0.11	0.16	0.21	V
DRV Output Characteristics							
DRV Pin Output Voltage	V_{DRV}		9 – 10	7.5	8.2	8.9	V
DRV Pin Output Impedance	$R_{DRV(SOURCE)}$		—	—	45	—	Ω
DRV Pin Input Impedance	$R_{DRV(SINK)}$		—	—	15	—	Ω
Protections							
Overcurrent Detection Threshold Voltage 1	V_{OCP1}		13 – 10	−0.66	−0.60	−0.54	V
Overcurrent Detection Threshold Voltage 2	V_{OCP2}		13 – 10	−1.8	−1.6	−1.4	V
OCP Pin Source Current	I_{OCP}		13 – 10	−120	−40	−10	µA
Leading Edge Blanking Time	t_{BW}		9 – 10	350	700	1400	ns
OLP Threshold Voltage	$V_{COMP(OLP)}$		14 – 10	4.15	4.60	5.00	V
ISENSE Pin Source Current	I_{ISEN}		1 – 10	−1.0	−0.5	−0.1	µA
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		11 – 10	28.5	31.5	34.0	V
Thermal Characteristics							
Thermal Resistance (3) (Junction-to-Case)	θ_{J-C}		—	—	—	16	°C/W

3. Mechanical Characteristics

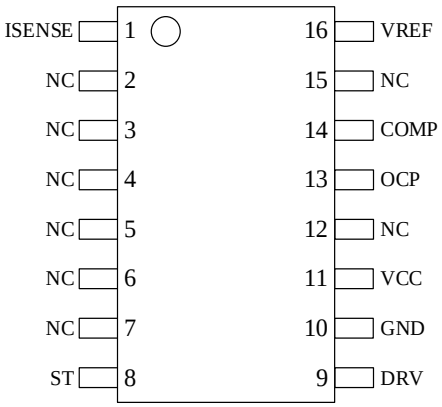
Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.070	—	g

(2) See Figure 9-9. V_{REF} Pin Voltage vs. $V_{ISEN(TH)}$.
(3) Guaranteed by design.

4. Block Diagram



5. Pin Configuration Definitions



Pin Number	Pin Name	Description
1	ISENSE	Feedback current detection
2 to 7	(NC)	No connection
8	ST	Startup current input
9	DRV	Drive output
10	GND	Ground
11	VCC	Power supply voltage input for control part and overvoltage protection signal input
12	(NC)	No connection
13	OCP	Input for overcurrent protection and quasi-resonant signal
14	COMP	Feedback phase compensation
15	(NC)	No connection
16	VREF	Dimming signal input and standby signal input

6. Typical Application

Figure 6-1 and Figure 6-2 show examples of a non-isolated flyback circuit and a non-isolated buck-boost converter circuit for quasi-resonant operation. In power supply specifications with a large surge voltage at the drain pin of the MOSFET, it is recommended to add a CRD clamp snubber circuit (Figure 6-1) between the windings P and a C or RC damper snubber circuit (Figure 6-1 and Figure 6-2) between the drain and source pins. When the IC operates in PWM mode, no detection circuit for the quasi-resonant signal is required. D6, D7, R4, and C9 are not required in Figure 6-1, and D6 and R2 are not required in Figure 6-2.

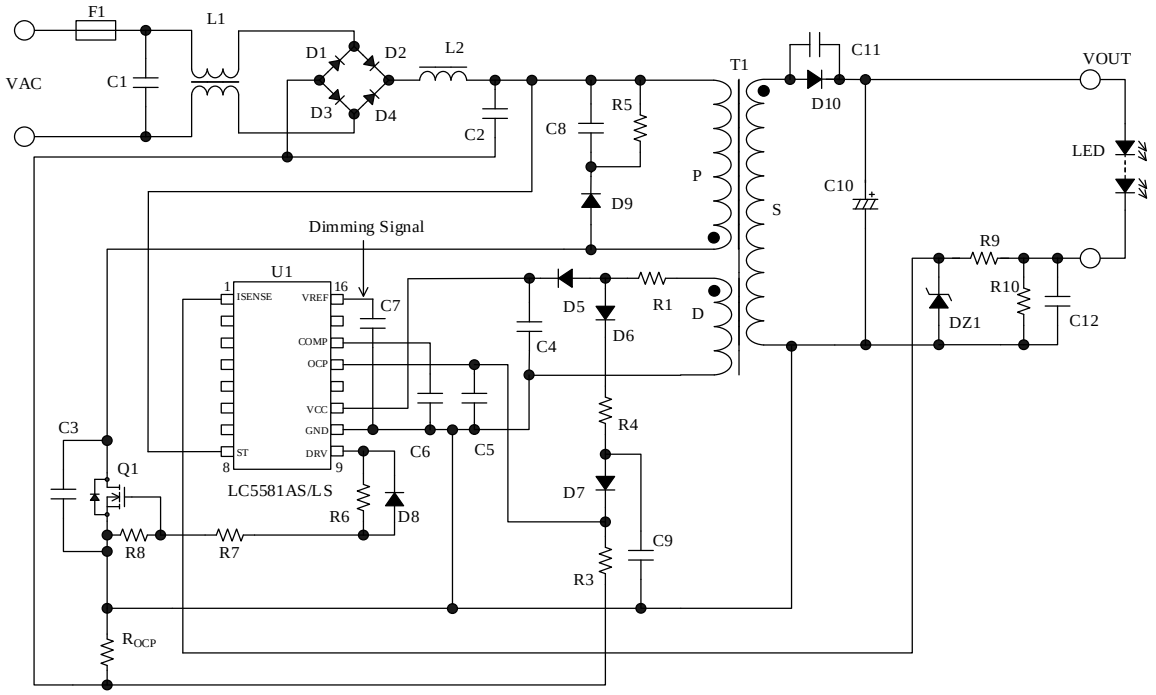


Figure 6-1. Design Example of Non-isolated Flyback Converter (Quasi-resonant Operation)

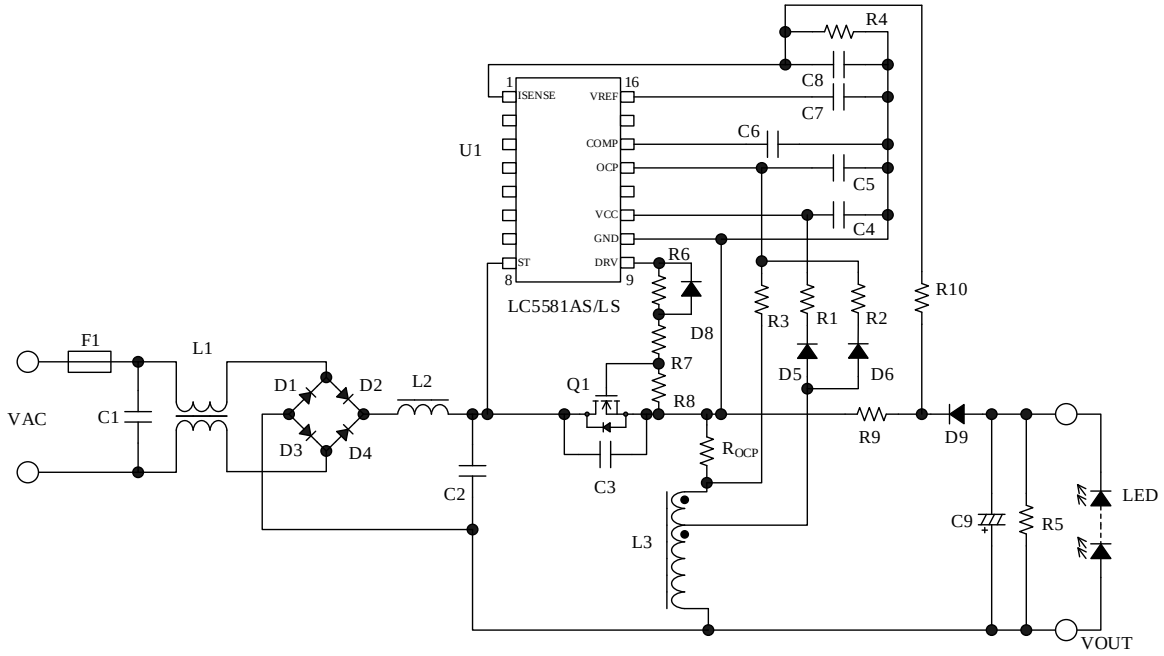
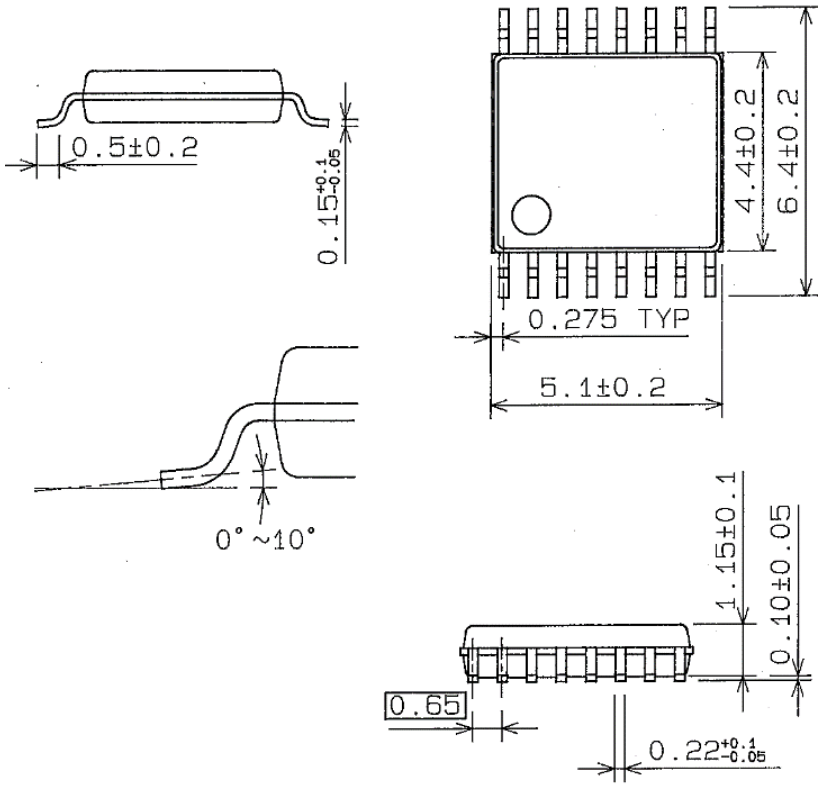


Figure 6-2. Design Example of Non-isolated Buck-boost Converter (Quasi-resonant Operation)

7. Physical Dimensions

● VSOP16

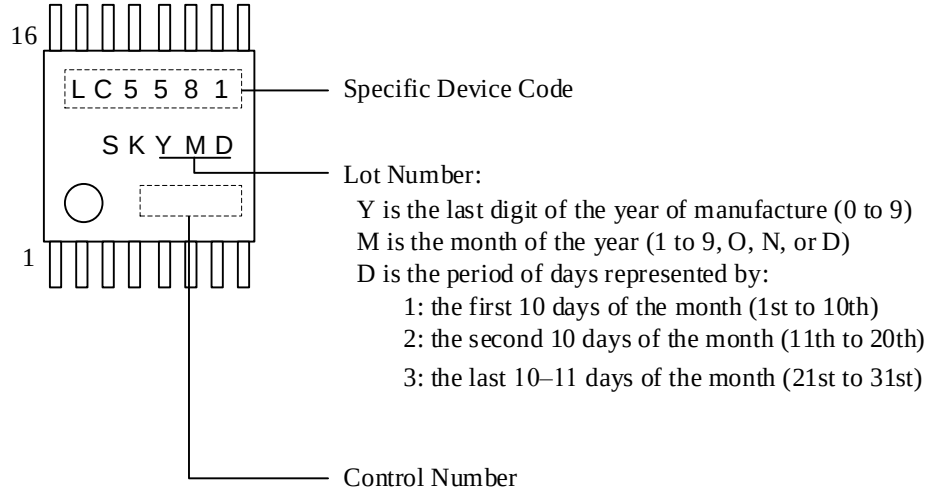


NOTES:

– Dimensions in millimeters
– Pb-free (RoHS compliant)
– When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Soldering Iron: 350 °C / 3.5 s, 1 time

8. Marking Diagram

• **LC5581AS**



• **LC5581LS**

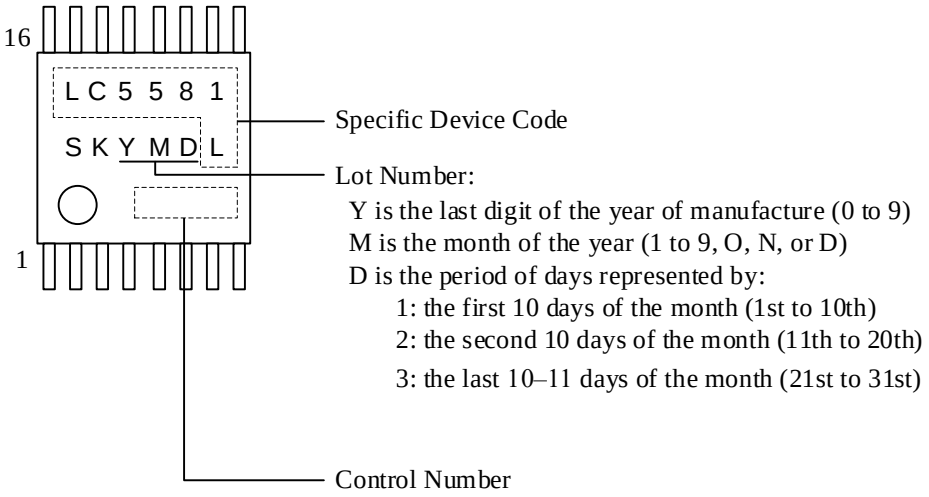


Table 8-1. Specific Device Code

Specific Device Code	Part Number
LC5581	LC5581AS
LC5581L	LC5581LS

9. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). This section describes various functions based on non-isolated flybuck circuit with quasi-resonant operation (Figure 6-1).

9.1. Startup Operation

Figure 9-1 shows the VCC pin and its peripheral circuit. The IC has the startup circuit connected to the ST pin. When the ST pin voltage reaches Startup Circuit Operation Voltage, $V_{ST(ON)}$ = 22 V, the startup circuit starts to operate. During the startup process, the constant current, $I_{CC(ST)}$ = −6.3 mA, charges C4 connected to the VCC pin. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.1 V, the control circuit starts to operate. After the control circuit starts operating, a voltage to be applied on the VCC pin is the rectified auxiliary winding voltage, V_D, as shown in Figure 9-1.

After the power startup sequence ends, the startup circuit turns off automatically to eliminate the power dissipation by itself. The winding turns of the auxiliary winding, D, should be adjusted so that the VCC pin voltage falls within the range defined by Equation (1), in accordance with the power supply specifications giving the variation range of input and output voltages. The reference voltage across an auxiliary winding is about 20 V.

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.}) \quad (1)$$

$$\Rightarrow 12.5\ (\text{V}) < V_{CC} < 28.5\ (\text{V})$$

The startup time of the IC is determined by the capacitance of C4. The approximate startup time, t_{START}, can be calculated by Equation (2):

$$t_{START} = C4 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{CC(ST)}|} \quad (2)$$

Where:
t_{START} is the startup time of the IC (s), and
$V_{CC(INT)}$ is the initial VCC pin voltage (V).

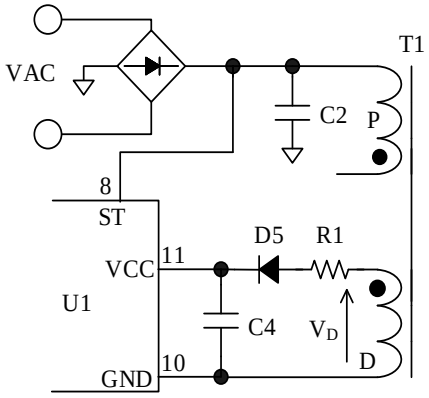


Figure 9-1. VCC Pin and Peripheral Circuit

9.2. Undervoltage Lockout (UVLO)

Figure 9-2 shows the relationship of VCC pin voltage and circuit current, I_{CC}. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the control circuit stops its operation by the undervoltage lockout (UVLO) circuit, and reverts to the state before startup.

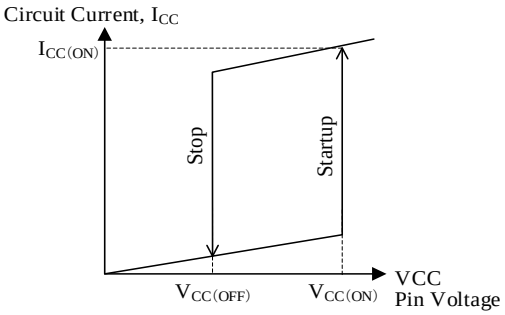


Figure 9-2. VCC Pin Voltage vs. Circuit Current, I_{CC}

9.3. Bias Assist Function

The IC has the bias assist function. While the bias assist function is actuated, a startup current is supplied from the startup circuit. The IC has two types of bias assist functions: at startup and normal operation.

• Startup

Figure 9-3 represents the VCC pin voltage waveform at power-on. After the VCC pin voltage reaches $V_{CC(ON)}$ = 15.1 V, the IC starts operating, resulting in an increased circuit current and a decreased VCC pin voltage. At the same time, the auxiliary winding voltage, V_D, increases in proportion to output voltage. These are all balanced to produce the VCC pin voltage.

The transient surge voltage that occurs at power MOSFET turn-off induces a voltage across the auxiliary winding, D. When the output load at startup is light, this induced voltage may cause the feedback control to reduce

the power sent to the output. Along with the decrease in output voltage, the VCC pin voltage also decreases. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the control circuit may stop, resulting in startup failure. To prevent this, when the VCC pin voltage decreases to $V_{CC(BIAS\_IN)}$ = 16.0 V, the bias assist function is activated to suppress the VCC pin voltage drop by supplying the startup current to the VCC pin through the startup circuit.

Since the threshold $V_{CC(BIAS\_IN)}$ of the bias assist function at startup has a margin against $V_{CC(OFF)}$, a capacitor with small capacitance (a ceramic capacitor of about 4.7 µF) can be used for C4. This results in shortening the startup time at power-on. The response time of the overvoltage protection can also be shortened because the VCC pin voltage rises faster at output overvoltage. To avoid a startup failure, constants should be selected based on the operation performance checked with an actual board.

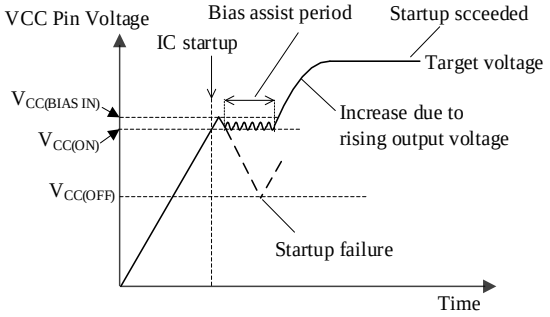


Figure 9-3. VCC Pin Voltage at Startup

• In Normal Operation

After startup of the IC, the VCC pin bias assist threshold voltage switches from $V_{CC(BIAS\_IN)}$ = 16.0 V to $V_{CC(BIAS\_NOM)}$ = 11.0 V under any of the following conditions.

– The VCC pin voltage is ≥$V_{CC(BIAS\_OUT)}$ of 16.6 V.
– COMP pin voltage is ≥0.6 V
– ISENSE pin voltage is ≥0.2 V.

When the VCC pin voltage decreases to $V_{CC(BIAS\_NOM)}$ in normal operation, a startup current is supplied from the startup circuit. As a result, the VCC pin voltage drop is suppressed to regulate the VCC pin voltage.

9.4. Soft Start Function

Figure 9-4 shows the operation waveforms at startup. The soft start function of the IC is activated at power-on. The soft start function reduces the voltage and current stress of the power MOSFET and the secondary rectifier diode at power-on. The soft start operation period is the period from when the COMP pin voltage reaches $V_{COMP(MIN)}$ = 0.85 V to when the output current is controlled to be constant. During that period, the output power gradually increases.

At power-on, it is required to check the following.

- The VCC pin voltage maintains over the Operation Stop Voltage, $V_{CC(OFF)}$.
- The output current reaches the target value before the overload protection (OLP) is activated.
  (At this point, the COMP pin voltage is less than $V_{COMP(OLP)}$ = 4.60 V)

After the IC starts operating, when the COMP pin voltage reaches $V_{COMP(MIN)}$ = 0.85 V, the IC starts a PWM switching. The PWM oscillation frequency, f_{OSC}, is 60 kHz.

When the auxiliary winding voltage rises along with the output voltage, the positive voltage on the OCP pin also rises. When the OCP pin voltage reaches $V_{BD(TH1)}$ = 0.24 V or more, the IC shifts to the quasi-resonant operation (QR). Figure 9-5 shows the OCP pin voltage waveforms on an expanded time scale when the IC shifts to quasi-resonant operation mode from PWM operation (point A in Figure 9-4).

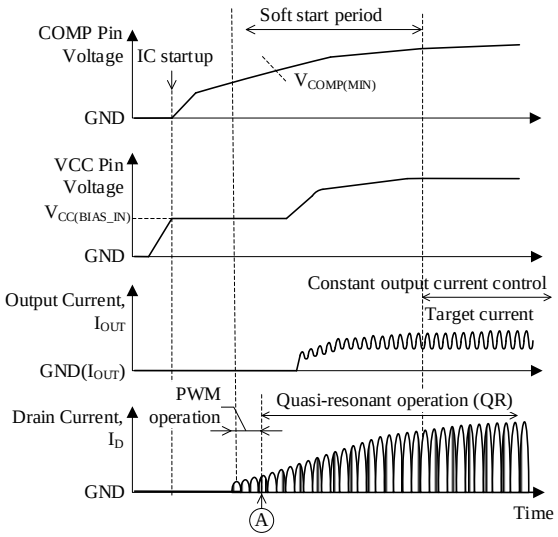


Figure 9-4. Operational Waveforms at Startup

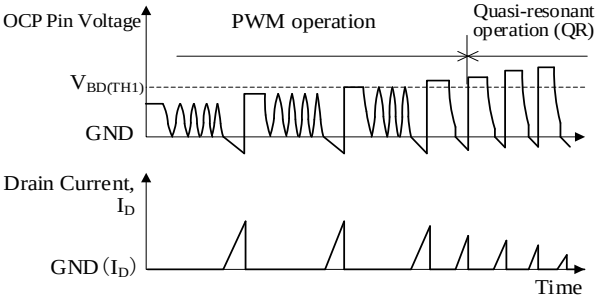


Figure 9-5. OCP Pin Voltage Waveforms on Expanded Time Scale (Point A)

9.5. Standby Function

The IC has the standby function. When the VREF pin voltage is reduced to ≤ 0.7 V by applying an external voltage to the VREF pin, the IC enters standby operation, and then stops oscillating.

When the IC recovers from standby operation, the VREF pin voltage should be set to ≥1.4 V. When the VREF pin voltage reaches ≥1.4 V, the IC starts oscillating in the soft start mode.

9.6. On-time Control Operation

Figure 9-6 shows the peripheral circuit of the COMP pin, whereas Figure 9-7 shows the on-time control. The output is controlled to depend on the output current with the voltage mode which controls an on-time, and average current control.

As shown in Figure 9-7, the average current control of the IC compares the voltage drop of the constant current detection resistor and the internal error amplifier reference voltage, $V_{ISEN(TH)}$ = 0.300 V by the OTA circuit to average the OTA circuit output at C6 connected to the COMP pin. The IC compares the COMP pin voltage with the internal oscillator (OSC) output by the FB comparator to control the on-time. The OSC is the circuit to control operations such as the PWM frequency, the quasi-resonant oscillation, and the maximum on-time limit.

Figure 9-8 shows the averaged input current waveform, $I_{IN(AVG)}$. Since the input capacitor C2 is a low capacitance film capacitor, the voltage across C2, V_{IN} is a sine waveform. When the output load becomes constant, the COMP pin voltage becomes constant and the ON time, t_{ON} is determined. When t_{ON} is constant, the average input current is a sine waveform because the peak drain current I_{DP} is proportional to V_{IN}. As a result, a high power factor is achieved. The capacitance of C6 connected to the COMP pin is approximately 1 μF. The IC controls the constant output current according to loads as follows:

- **When the output current becomes less than the target value**

When the output current decreases to less than the target value, the ISENS pin voltage decreases, and the COMP pin voltage increases. This results in a longer on-time and larger output current.

- **When the output current becomes greater than the target value**

When the output current exceeds the target value, the COMP pin voltage decreases in the opposite of the operation described above. This results in a shorter on-time and a smaller output current.

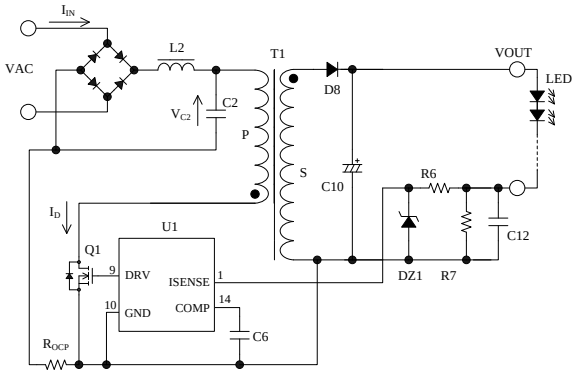


Figure 9-6. COMP Pin Peripheral Circuit

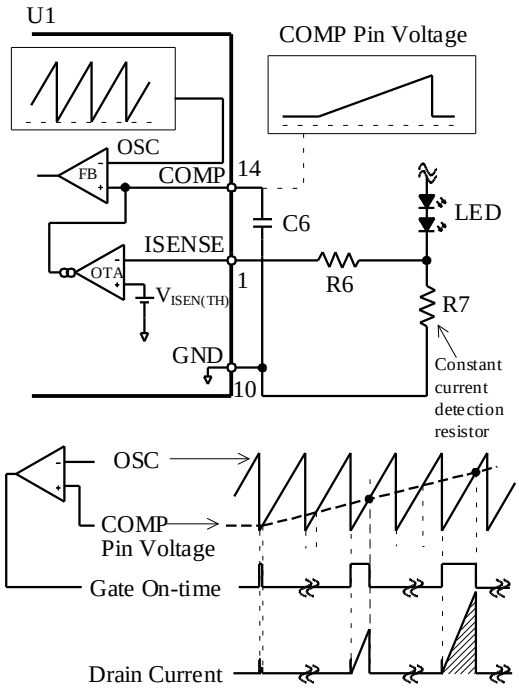


Figure 9-7. On-time Control

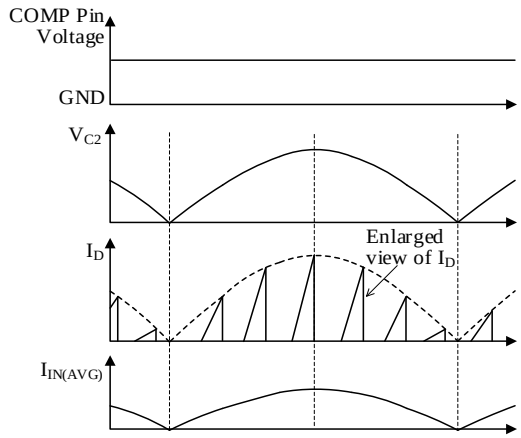


Figure 9-8. Averaged Input Current Waveform

9.7. Analog Dimming Function

The IC has the analog dimming function. When using the dimming function, apply an external voltage to the VREF pin.

In the average current control, the IC compares the voltage drop of the constant current detection resistor and the internal error amplifier reference voltage $V_{ISEN(TH)}$ in the OTA circuit (see Figure 9-7). The relationship between VREF pin and $V_{ISEN(TH)}$ is shown in Figure 9-9, and this characteristic is used for dimming. The applied voltage for dimming is about 1.4 V to 3.8 V.

Note that the IC transits to standby mode when the VREF pin is set to ≤ 0.7 (see Section 9.5).

If the dimming function is not used, it is not required to apply voltages to the VREF pin.

Regardless of the use of the dimming function, connect a ceramic capacitor C7 of about 0.01 μF to the VREF pin for stable operation.

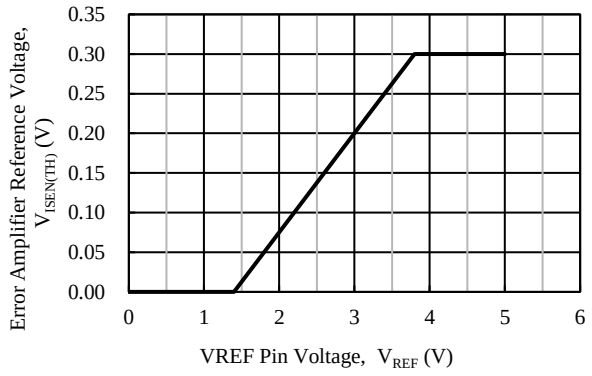


Figure 9-9. V_{REF} Pin Voltage vs. $V_{ISEN(TH)}$

9.8. Quasi-resonant Operation and Bottom-on Timing

Figure 9-10 shows the circuit of a flyback converter. The flyback converter is a system that transfers the energy stored in the transformer to the secondary side when the primary-side power MOSFET is turned off. The MOSFET stays in the off state even after the energy is completely transferred to the secondary side. During the off state, the voltage between the drain and source, V_{DS}, oscillates freely at the frequency based on the primary inductance, L_P, and the capacitance between the drain and source, C_V.

The quasi-resonant operation provides VDS bottom-on operation that the power MOSFET turns on at the lowest voltage point of V_{DS} free oscillation.

Figure 9-11 shows ideal waveforms during the bottom-on operation. The bottom-on operation reduces switching loss and switching noise. This results in a power supply with high efficiency and low noise.

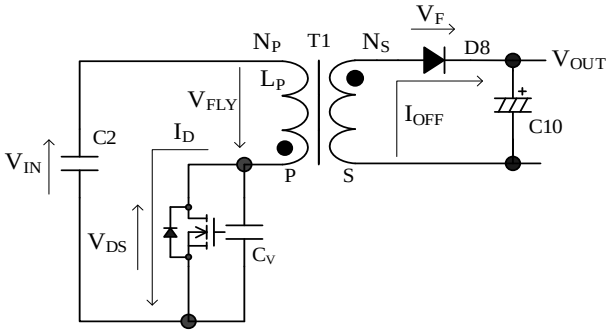


Figure 9-10. Basic Flyback Converter Circuit

The symbols in Figure 9-10 represent as follows:

V_{IN} is the input voltage,
V_{DS} is the voltage between the drain and source of the power MOSFET,
I_D is the drain current of the power MOSFET,
I_{OFF} is the current running through the secondary rectifier diode during the power MOSFET off-period,
C_V is the voltage resonant capacitor,
L_P is the primary side inductance, and
V_{FLY} is the flyback voltage.

$$V_{FLY} = \frac{N_P}{N_S} \times (V_{OUT} + V_F)$$

Where:
N_P is the primary winding,
N_S is the secondary winding,
V_{OUT} is the output voltage, and
V_F is the forward voltage drop of the secondary side rectifier diode.

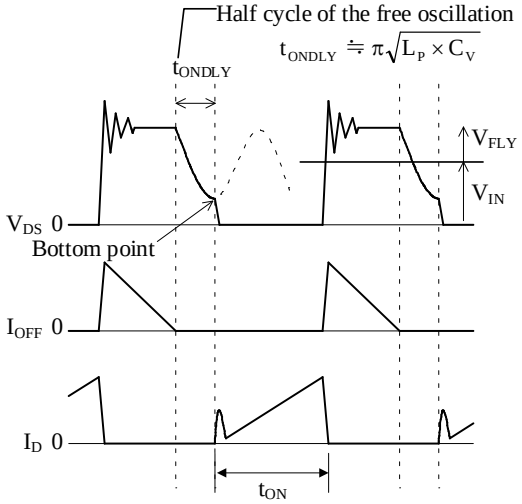


Figure 9-11. Ideal Bottom-on Operation Waveforms (Power MOSFET Turns On at the Lowest Voltage of V_{DS} Waveform)

Figure 9-12 shows an OCP pin peripheral circuit, and Figure 9-13 shows the waveform of an auxiliary winding

voltage.

To control the bottom-on operation, the IC uses the auxiliary winding voltage synchronized with V_{DS}. During the power MOSFET turn-off, the positive voltage is supplied through the delay circuit (D6, R4, C9, and D7 in Figure 9-12) to the OCP pin from auxiliary winding. This input signal to the OCP pin is defined as a quasi-resonant signal, V_{BD}.

The IC detects V_{BD} at the OCP pin and controls the on/off signal of the power MOSFET.

When the V_{BD} increases to the Quasi-resonant Operation Threshold Voltage 1 ($V_{BD(TH1)}$ = 0.24 V) or more after the power MOSFET turns off, the IC maintains the power MOSFET in an off state. When the V_{BD} decreases to the Quasi-resonant Operation Threshold Voltage 2 ($V_{BD(TH2)}$ = 0.16 V), the power MOSFET turns on. When V_{BD} reaches $V_{BD(TH2)}$, the Quasi-resonant Operation Threshold Voltage increases to $V_{BD(TH1)}$. In this way, switching the threshold voltage of the quasi-resonant signal prevents malfunctions caused by the noise added to the OCP pin.

The delay time, t_{ONDLY}, is the period from when V_{DS} free oscillation starts to when the power MOSFET turns on. The delay time, t_{ONDLY} is determined by the constant values of the delay circuit. Therefore, the values of R3 and R4 should be adjusted so that the power MOSFET turns on at the bottom of the V_{DS} waveform.

R3 and R4 should be adjusted so that the peak voltage, $V_{BD(PK)}$ of the quasi-resonant signal is 1.5 V to 2.0 V and the effective pulse width of the quasi-resonant signal, t_{QR} ≥ 1.2 µs within the power supply specifications giving the variation range of input and output voltages. Adjust the values that take the variation of R3 and R4 into account.

t_{QR} is the time from when V_{BD} reaches the maximum $V_{BD(TH1)}$ value of 0.34 V to when V_{BD} decreases to the maximum $V_{BD(TH2)}$ value of 0.21 V (see Figure 9-14).

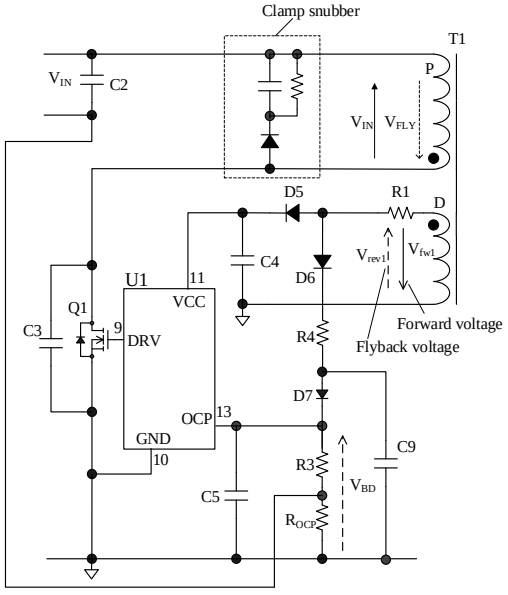


Figure 9-12. OCP Pin Peripheral Circuit

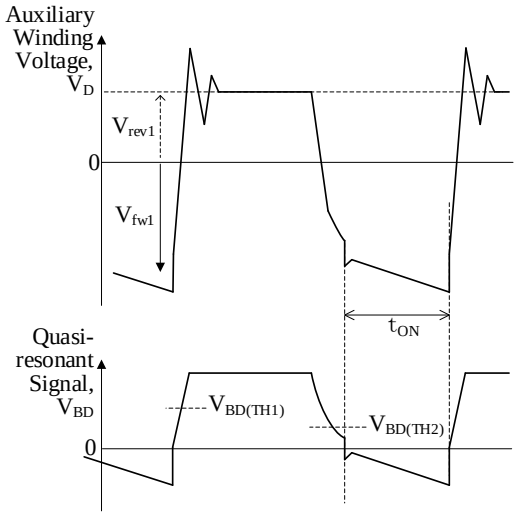


Figure 9-13. Auxiliary Winding Voltage Waveform

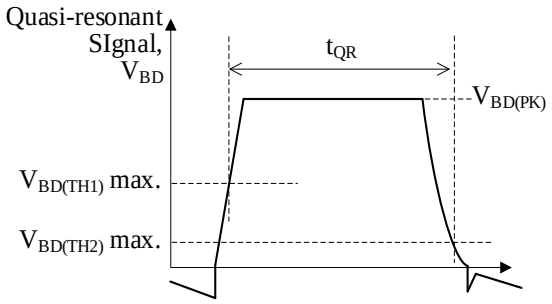


Figure 9-14. The Effective Pulse Width of Quasi-Resonant Signal

The following describes how to set the constants of the delay circuit.

- **Setting of R3**

The recommended value for R3 is about 100 Ω to 330 Ω.

- **Setting of C5**

The recommended value for C5 is about 100 pF to 470 pF.

- **Setting of R4**

R4 should be set so that $V_{BD(PK)} \geq V_{BD(TH1)}$ under the lowest VCC pin voltage condition in the ranges of the input and output specifications.

If R_{OCP} is much smaller than R3 and R_{OCP} is not factored into, R4 is calculated by the following equation.

$$R4 = \frac{\left(V_{CC(MIN)} - V_{BD(PK)} - 2 \times V_F\right) \times R3}{V_{BD(PK)}} \quad (3)$$

Where:

$V_{CC(MIN)}$ is the minimum voltage of the VCC pin within the power supply specification range,
$V_{BD(PK)}$ is the peak voltage of the quasi-resonant signal, and
V_F is the forward voltage drop of D6 and D7.

When $V_{CC(MIN)}$ = 16 V, $V_{BD(PK)}$ = 1.5 V, V_F = 0.8 V, and R3 = 220 Ω, R4 ≈ 1.89 kΩ. Hence, R4 is 1.8 kΩ in E12 series.

If t_{QR} is not long enough, t_{QR} should be adjusted as follows:

– To raise $V_{BD(PK)}$, increase the R3value.
– To raise $V_{BD(PK)}$, reduce the R4 value.
– To increase the free oscillation period, increase the capacitance of the voltage resonant capacitor, C3. (The greater the C3 value, the higher the switching loss at the power MOSFET turn-on; therefore, be sure to check that the power MOSFET temperature ranges within the absolute maximum rating when increasing the C3 value.)

• Setting of C9

t_{ONDLY}, is adjusted by the value of C9. To set the ideal bottom-on of V_{DS} (see Figure 9-11), adjust C9 value as follows with measuring actual waveforms under the maximum AC input voltage and the maximum output power. Measurement waveforms are V_{DS}, I_D, and the OCP pin quasi-resonant signal, V_{BD}. A measurement point is the maximum amplitude of V_{DS} waveform, $V_{DS(PEAK)}$ (see Figure 9-15).

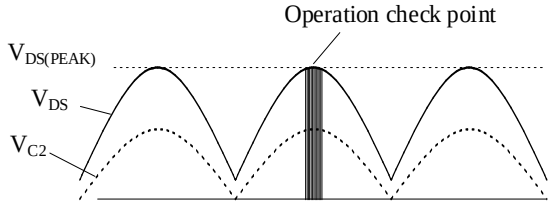


Figure 9-15. Operation Check Point in Setting C9

An initial constant for C9 is about 1000 pF. When the power MOSFET turn-on at the initial constant of C9 is earlier than the free vibration bottom point (see Figure 9-16), gradually increase the value of C9 until the power MOSFET turn-on point matches the free vibration bottom point.

On the other hand, when the power MOSFET turn-on at the initial constant of C9 is later than the free vibration bottom point (see Figure 9-17), gradually decrease the value of C9 until the power MOSFET turn-on point matches the free vibration bottom point.

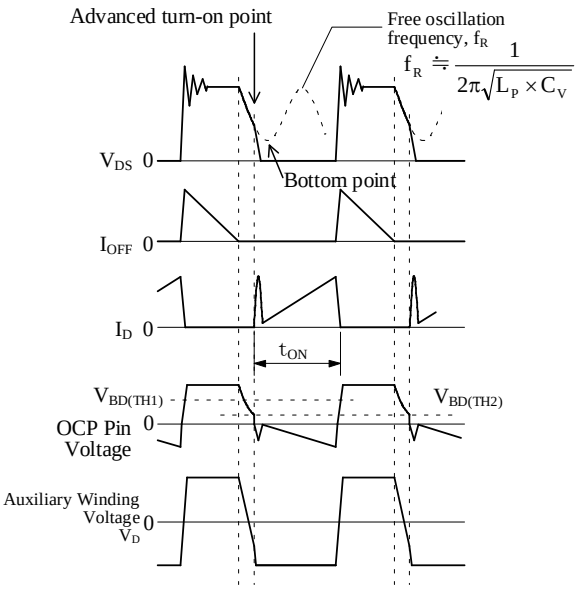


Figure 9-16. When the power MOSFET turn-on is earlier than the free vibration bottom point

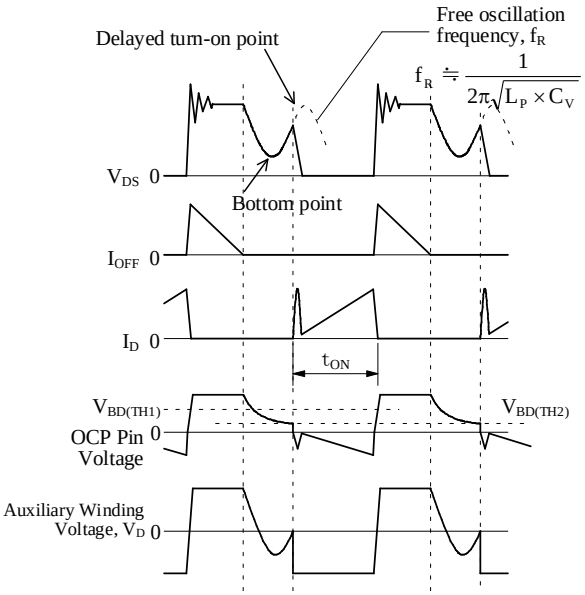


Figure 9-17. When the power MOSFET turn-on is later than the free vibration bottom point

9.8.1. BD Blanking Time

Figure 9-18 shows the normal and inappropriate waveforms of the OCP pin voltage. An inappropriate operation is caused by poor coupling between the primary winding and the secondary winding of the transformer. A transformer with $N_P >> N_S$ (e.g., low output power design) has poor coupling.

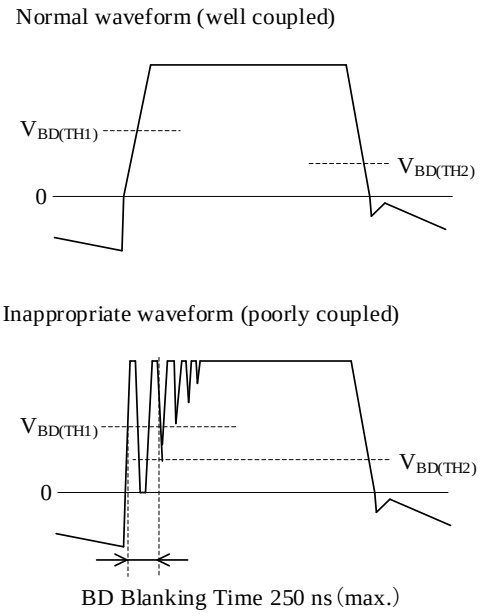


Figure 9-18. Voltage Waveforms of OCP Pin

Large inductance causes high surge voltage ringing at the OCP pin through the auxiliary winding when the power MOSFET turns off. The OCP pin has a blanking period of 250 ns (max.). In this period, the IC does not detect the OCP pin input signal (i.e., quasi-resonant signal). If the period when a surge voltage is being added to the OCP pin becomes longer than the blanking period, the power MOSFET may switch at a high frequency because the IC responds to the surge. As a result, when the power dissipation in the internal power MOSFET exceeds, and then the junction temperature increases to the absolute maximum rating value, or more, the power MOSFET can be damaged. When such a high frequency switching operation occurs, the following adjustments are required:

– Connect the capacitor C5 connected to the OCP pin close to the OCP and GND pins
– Redesign the PCB so that the trace of the OCP pin to the GND pin is separated from large current traces.
– Redesign the transform so that the coupling of the primary and auxiliary windings is poor.
– Adjust the value of a clamping snubber circuit.

To correctly measure any surge voltage waveform on the OCP pin, connect a test probe as short as possible to the OCP and GND pins.

9.9. Maximum On-time Limitation Function

When the input voltage is low or in a transient state (e.g., at which the input voltage turns on or off), the IC limits the on-time of the internal power MOSFET to the Maximum On-time, $t_{ON(MAX)}$ = 10.0 µs. This reduces audible noise from the transformer and stress on the devices such as internal power MOSFET and secondary rectifier.

Make sure that the actual on-time is < $t_{ON(MAX)}$ in the minimum AC input voltage and the maximum load. If your application uses a transformer whose on-time is ≥$t_{ON(MAX)}$, the output power decreases due to the on-time of the power MOSFET limited to $t_{ON(MAX)}$ in the condition of the minimum AC input voltage. In this case, redesign the transformer that takes the following into account:

– Decrease the inductance of the transformer, L_P, to increase the switching frequency and reduce the on-time.
– Decrease the N_P/N_S, which is the turn ratio of the primary side and the secondary side to reduce the duty cycle.

9.10. Overcurrent Protection (OCP)

9.10.1. OCP Detection Method

The overcurrent protection (OCP) turns off the power MOSFET to limit the output power when the drain peak current of the power MOSFET reaches the OCP threshold voltage (pulse-by-pulse basis).

The drain current of the power MOSFET is detected by the current detection resistor, R_{OCP}, placed between the OCP and GND pins, as shown in Figure 9-19. The detection signals, VROCP, are fed through R3 to the OCP pin.

The power MOSFET turns off when V_{ROCP} reaches the value obtained by Equation (4), below:

$$V_{ROCP} = -\left|R_{OCP} \times I_{DP(OCP)}\right|$$

$$= -|V_{OCP}| + R3 \times |I_{OCP}| \quad (4)$$

Where:
R_{OCP} is the value of R_{OCP},
$I_{DP(OCP)}$ is the peak drain current during OCP operation,
V_{OCP} is the overcurrent detection threshold voltage (−0.60 V),
R3 is the value of R3, and
I_{OCP} is OCP pin source current (−40 µA).

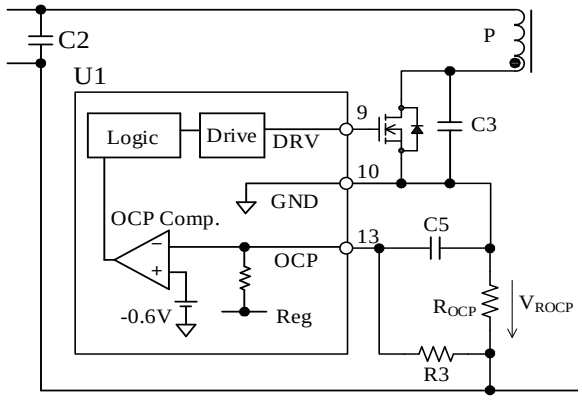


Figure 9-19. OCP Circuit for Negative Side Detect

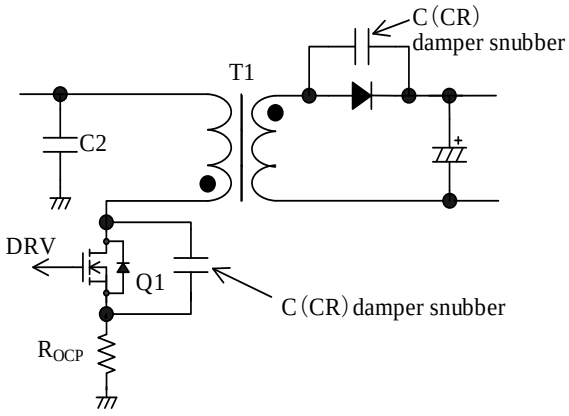


Figure 9-21. Damper Snubber

9.10.2. Leading Edge Blanking Function

For the constant current control of the output voltage, the IC uses a peak current mode control. In the peak-current-mode control, the overcurrent protection circuit responds to a steep surge generated when the power MOSFET is turned on, and then the power MOSFET may be turned off. As a prevention against such operation, the IC has the leading edge blanking time (t_{BW} = 700 ns), which starts immediately after the power MOSFET turn-on. During t_{BW}, the OCP is controlled not to respond to the drain current surge at turn-on.

When the power MOSFET turns on, the width of surge voltage on the OCP pin should be less than t_{BW}, as shown in Figure 9-20. To reduce surge voltages, extreme care should be taken for the R_{OCP} layout (see Section 10.3).

If the turn-on timing of the MOSFET does not match the bottom point of free oscillation of V_{DS}, adjust t_{ONDLY} (see Section 9.8). In addition, when a damper snubber in Figure 9-21 is used, reduce the capacitance of damper snubber.

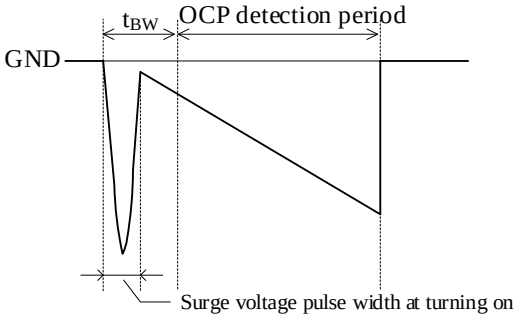


Figure 9-20. Voltage Waveform of OCP Pin Voltage

9.10.3. Input Compensation Function

The IC has the input compensation function that compensates the Overcurrent Detection Threshold Voltage, V_{OCP}, according to AC input voltages. In an application using a quasi-resonant converter with universal input (85 VAC to 265 VAC), the peak drain current of the power MOSFET decreases due to a higher operation frequency caused by an increased input voltage under a condition of constant output power. When the overcurrent detection threshold voltage is fixed and adjusted with the maximum load taken into consideration, the higher the $I_{OUT(OCP)}$, the higher the AC input voltage as shown in "without OCP input compensation" in Figure 9-22.

To regulate $I_{OUT(OCP)}$ at the maximum AC input voltage, add the OCP input compensation circuit (D_{X1}, DZ_{X1}, R_{X1}) as shown in Figure 9-23. Thus, the overcurrent detection threshold voltage is changed to limit the output power.

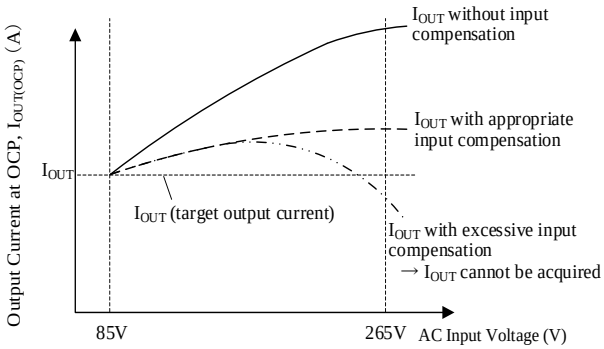


Figure 9-22. AC Input Voltage vs. Output Current at OCP (with or without OCP Input Compensation Function)

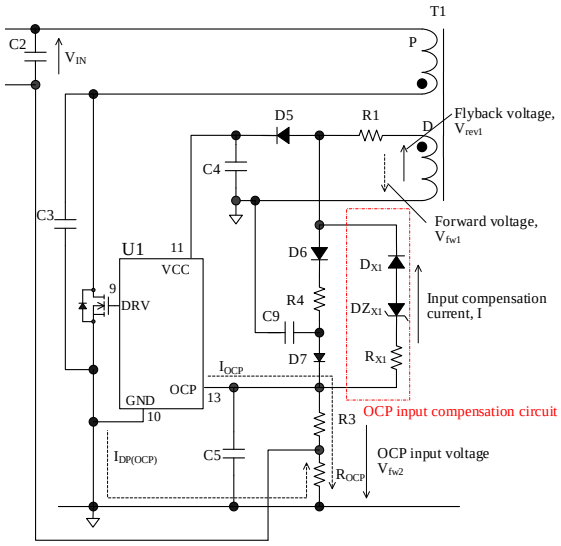


Figure 9-23. External OCP Input Compensation Circuit

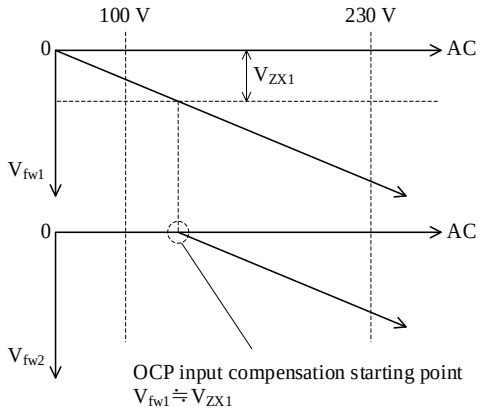


Figure 9-24. V_{fw1} and V_{fw2} vs. AC Input Voltages

The compensation amount of VOCP depends on values of the input compensation current, I, R_{X1}, R3, and R_{OCP}. The input compensation current, I, is calculated by the following equation:

$$I = \frac{V_{fw1} - V_{ZX1} - V_{FX1}}{R_{X1} + R3 + R_{OCP}} \quad (5)$$

Where:
I is the input compensation current,
V_{fw1} is the forward voltage of the auxiliary winding, D, and proportional to input voltage,
V_{FX1} is the forward voltage of the rectifier diode D_{X1}, and
V_{ZX1} is the Zener voltage of the Zener diode DZ_{X1}.

The Overcurrent Detection Threshold Voltage, V_{ROCP}' applied with OCP input compensation is calculated by the following equation:

$$V_{ROCP}' = -\left|R_{OCP} \times I_{DP(OCP)}'\right|$$

$$= -(|V_{OCP}| - |R3 \times I_{OCP}| - R3 \times I) \quad (6)$$

Where:
R_{OCP} is the value of R_{OCP},
$I_{DP(OCP)}'$ is the peak drain current during OCP operation with OCP input compensation circuit,
I is the input compensation current,
R3 is the value of R3,
V_{OCP} is the overcurrent detection threshold voltage (−0.60 V), and
I_{OCP} is the OCP pin source current (−40 μA).

As the input voltage, V_{IN}, increases, the voltage drop by the input compensation current, I, (i.e., R3 × I) increases. Then, the input compensation amount also increases, and the absolute value of V_{ROCP}' decreases.

The compensation start voltage of the OCP input voltage is determined by the Zener voltage (V_{ZX1}) of the Zener diode (D_{ZX1}). Set V_{ZX1} to the same voltage as V_{fw1} at the OCP input compensation starting point.

V_{ROCP}' reduces the difference in $I_{OUT(OCP)}$ at the maximum and minimum AC input voltage range so that $I_{OUT(OCP)}$ at the maximum AC input voltage is adjusted to the target current, I_{OUT} or higher as shown in Figure 9-22.

The OCP pin voltage, including surge voltage, must be regulated within the rated voltages (−2.0 V to 5.0 V) under a condition of the maximum AC input voltage.

9.10.4. Determining OCP Input Compensation Circuit Component Values

The calculation symbols used in this section are represented as follows:

V_{FX1} is the forward voltage of the rectifier diode D_{X1},
V_{ZX1} is the Zener voltage of the Zener diode DZ_{X1},
V_{OCP} is the overcurrent detection threshold voltage V_{OCP} = −0.60 V, and
I_{OCP} is the OCP pin source current, I_{OCP} = −40 μA.

For other component numbers, such as resistors, see Figure 9-23.

The peak drain current during OCP operation without OCP input compensation circuit, $I_{DP(OCP)}$, is calculated by Equation (7). $I_{DP(OCP)}$ is equal to the peak drain current limited by overcurrent detection threshold voltage without OCP input compensation in the minimum AC input voltage condition.

$$R_{OCP} \times |I_{DP(OCP)}| = |V_{OCP}| - R3 \times |I_{OCP}|$$

$$\Rightarrow |I_{DP(OCP)}| = \frac{|V_{OCP}| - R3 \times |I_{OCP}|}{R_{OCP}} \quad (7)$$

The peak drain current during OCP operation with OCP input compensation circuit, $I_{DP(OCP)}'$, is calculated by Equation (8).

$$R_{OCP} \times |I_{DP(OCP)}'| = |V_{OCP}| - R3 \times |I_{OCP}| - R3 \times I$$

$$\Rightarrow |I_{DP(OCP)}'| = \frac{|V_{OCP}| - R3 \times (|I_{OCP}| + I)}{R_{OCP}} \quad (8)$$

$I_{DP(OCP)}'$ in the maximum AC input voltage should be set to the drain current where the output current is equal to "I_{OUT} with appropriate input compensation" in Figure 9-22.

From Equations (7) and (8), the input compensation current, I, is calculated by the following equation:

$$I = \left(|I_{DP(OCP)}| - |I_{DP(OCP)}'|\right) \times \frac{R_{OCP}}{R3} \quad (9)$$

The forward voltage, V_{fw1}, at C2 peak voltage $V_{IN(PK)MAX}$ in the maximum AC input voltage is expressed as follows:

$$V_{fw1} = \frac{N_D \times V_{IN(PK)MAX}}{N_P} \quad (10)$$

Set to flow at the maximum AC input voltage, the input compensation current, I is calculated by the following equation.

$$I = \frac{V_{fw1} - V_{ZX1} - V_{FX1}}{R_{X1} + R3 + R_{OCP}} \quad (11)$$

Assuming R3 << R_{X1} and R_{OCP} << R_{X1}, the R_{X1} is calculated as follows:

$$R_{X1} = \frac{V_{fw1} - V_{ZX1} - V_{FX1}}{I} \quad (12)$$

Substituting Equation (10) for Equation (12), R_{X1} is calculated as follows:

$$R_{X1} = \frac{\frac{N_D \times V_{IN(PK)MAX}}{N_P} - (V_{ZX1} + V_{FX1})}{I} \quad (13)$$

9.10.5. Reference Design for OCP Input Compensation Circuit with Universal Input

A constant of the OCP input compensation circuit (DZ_{X1}, R_{X1}) that supports universal input specifications (85 VAC to 265 VAC) should be determined based on the actual performance in your application as follows:

1) Tentatively, set the OCP input compensation start voltage.
   The tentatively set value of compensation start voltage, $V_{IN(OCP\_ST)}$ is about 100 VAC to 130 VAC.
   In this reference design, $V_{IN(OCP\_ST)}$ = 120 VAC.
2) Set the circuit constants as shown in Table 9-1.

Table 9-1. Reference Circuit Constant

Parameter	Symbol	Constant
AC Input Voltage	V_{IN}	85 VAC to 265 VAC
Output Power	P_{OUT}	40 W
Transformer Primary Winding Turns	N_P	40 T
Transformer Auxiliary Winding Turns	N_D	6 T
OCP Detection Resistor	R_{OCP}	0.2 Ω
OCP Pin Filter Resistance	R3	220 Ω
D_{X1} Forward Voltage Drop	V_{FX1}	0.8 V

3) In the minimum AC input voltage (85 VAC) condition, measure the peak drain current during OCP operation, $I_{DP(OCP)}$.
4) In the maximum AC input voltage (265 VAC) condition, measure the drain current, $I_{DP(OCP)'}$, when the output current, $I_{OUT(OCP)}$, becomes the "I_{OUT} with appropriate input compensation" in Figure 9-22.
5) Set the component constants for the OCP input voltage compensation circuit based on the results in Table 9-1 and 3) and 4). The following shows the component constants setting.

• Setting of D_{ZX1}

Based on Equation (10), when $V_{IN(OCP\_ST)}$ = 120 VAC, V_{fw1} is calculated as follows:

$$V_{fw1} = \frac{N_D}{N_P} \times V_{IN(PK)MAX}$$

$$= \frac{N_D}{N_P} \times V_{IN(OCP\_ST)} \times \sqrt{2}$$

$$= \frac{6\ T}{40\ T} \times 120\ VAC \times \sqrt{2} = 25.5\ V$$

For the setting example, select 27 V for the Zener voltage V_{ZX1} of the Zener diode DZ_{X1}.

• **Calculation of input compensation current, I**

If the results of 3) and 4) are $I_{DP(OCP)}$ = 3.0 A and $I_{DP(OCP)}'$ = 1.9 A, respectively, I is calculated as follows based on Equation (9):

$$I = \left(\left|I_{DP(OCP)}\right| - \left|I_{DP(OCP)}'\right|\right) \times \frac{R_{OCP}}{R3}$$

$$= (3.0\ A - 1.9\ A) \times \frac{0.2\ \Omega}{220\ \Omega} = 1\ mA$$

• **Setting of R_{X1}**

Based on Equation (13),

$$R_{X1} = \frac{\frac{N_D \times V_{IN(PK)MAX}}{N_P} - (V_{ZX1} + V_{FX1})}{I}$$

$$= \frac{\frac{6\ T \times 265\ VAC \times \sqrt{2}}{40\ T} - (27\ V + 0.8\ V)}{1\ mA}$$

$$= 28.4\ k\Omega$$

Thus, select R_{X1} = 27 kΩ of the E12 series.

6) Confirm that the output current during OCP operation, $I_{OUT(OCP)}$, is similar to "I_{OUT} with appropriate input compensation" in Figure 9-22, in an actual operation throughout AC input voltage ranges with the constants set in 5). If $I_{OUT(OCP)}$ is not appropriate, be sure to adjust the constants of D_{ZX1} and R_{X1} by changing the compensation startup voltage, $V_{IN(OCP\_ST)}$.

9.11. Overload Protection (OLP)

Figure 9-25 and Figure 9-26 show the COMP pin peripheral circuit and the waveforms during the OLP operation, respectively. In the overload condition where the drain peak current is limited by the overcurrent operation, the VCC pin voltage drops along with the output voltage drop. When the VCC pin voltage reaches $V_{CC(BIAS\_NOM)}$ = 11.0 V, the bias assist function is activated to suppress a reduction in the VCC pin voltage. In addition, the ISENSE pin voltage also decreases. When the ISENSE pin voltage drops to the internal error amplifier reference voltage $V_{ISEN(TH)}$ = 0.300 V, the OTA circuit output inside the IC turns off. Therefore, C6 connected to the COMP pin is charged by the constant current source inside the COMP pin. When the COMP pin voltage reaches $V_{COMP(OLP)}$= 4.60 V, the overvoltage protection (OVP) is activated to stop the switching operation. After the switching operations stops, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the startup circuit is activated and the IC restarts. At this time, the IC discharges C6 and the COMP pin voltage decreases. When the startup circuit raises the VCC pin voltage to $V_{CC(ON)}$ =15.1 V, the IC starts operating. At the same time, the startup circuit turns off and the VCC pin voltage decreases. The bias assist function is activated to regulate the VCC pin voltage at startup. When the control circuit starts operating, C6 is charged again if the causes of the overload condition have not been eliminated. As a result, the COMP pin voltage increases to reach the COMP pin control minimum voltage, $V_{COMP(MIN)}$ = 0.85 V, the IC starts oscillating again. After that, the IC operates in the intermittent oscillation that repeats oscillation stop and restart until the causes are eliminated.

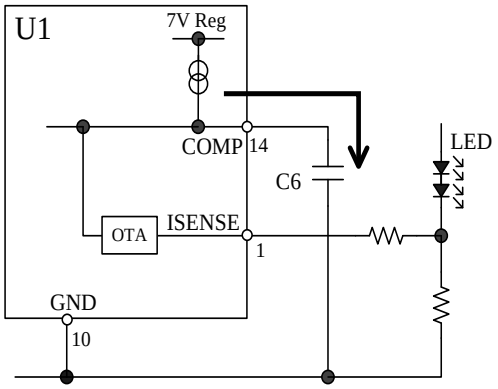


Figure 9-25. COMP Pin Peripheral Circuit

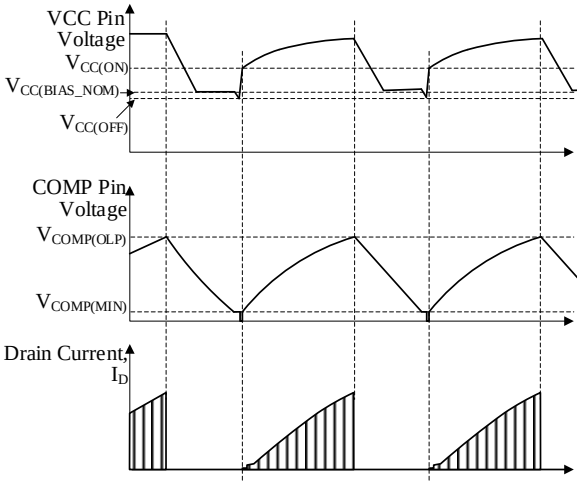


Figure 9-26. OLP Operational Waveforms

9.12. Overvoltage Protection (OVP)

When the voltage between the VCC and GND pins increases to $V_{CC(OVP)}$ = 31.5 V or more, the overvoltage protection (OVP) is activated. The operation after the OVP detection is different in the latch type (LC5581LS) and the auto-restart type (LC5581AS).

Because the VCC pin voltage is proportional to the output voltage, an output overvoltage event such as an open load condition can be detected. The approximate value of the output voltage, $V_{OUT(OVP)}$, at the OVP activation can be calculated by the following equation.

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 31.5 \text{ (V)} \qquad (14)$$

9.12.1. Latch Type (LC5581LS)

When the OVP is activated, the IC stops switching operation in a latched state. After the switching operation stops, the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS\_NOM)}$, the bias assist function operates. As a result, the VCC pin voltage is kept at $V_{CC(OFF)}$ or more. This keeps the IC in a latched state.

To release the latched state, turn off the supply voltage to decrease the VCC pin voltage to $V_{CC(OFF)}$ or less.

9.12.2. Auto-restart Type (LC5581AS)

When the OVP is activated, the IC stops switching operation. During the OVP operation, the bias assist function is disabled, and the intermittent operation by the VCC_UVLO is repeated. When the causes of the overvoltage condition are eliminated, the power supply IC automatically returns to its normal operation.

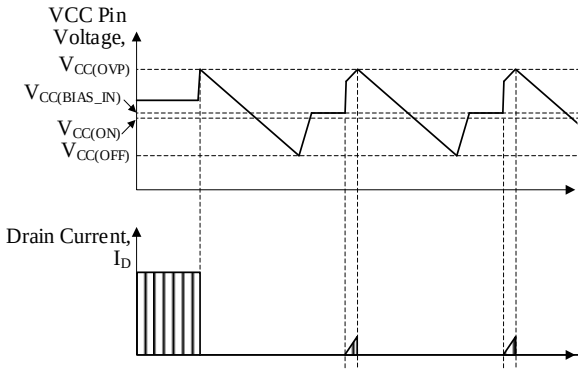


Figure 9-27. VCC_OVP Operational Waveforms (Auto-restart Type)

10. Design Notes

10.1. External Components

Components fit for the use condition should be used. Figure 10-1 shows the IC peripheral circuit.

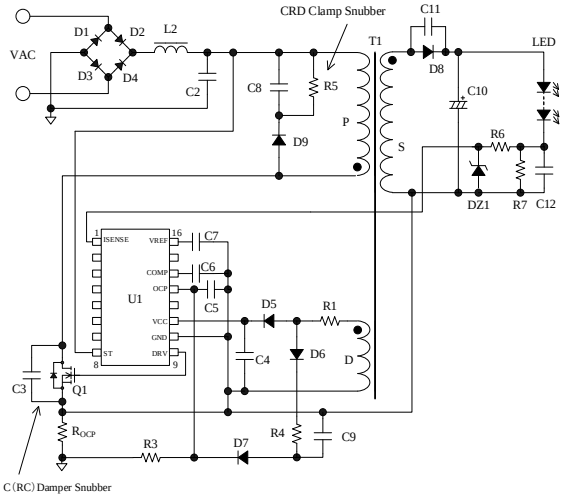


Figure 10-1. IC Peripheral Circuit

• Output Smoothing Electrolytic Capacitor

Apply proper design margin to ripple current, ripple voltage, and temperature rise. A low-ESR capacitor is recommended to reduce ripple voltage, in terms of designing switch-mode power supplies.

• OCP Pin Peripheral Circuit

R_{OCP} in is the resistor for the current detection. It is required to use a resistor with low internal inductance because high-frequency switching current will flow through R_{OCP}. In addition, choose a resistor with allowable power dissipation according to your application.

R3 and C5 to be connected to the OCP pin are for the noise reduction filter. To minimize the effects of a variation in the internal resistor, set R3 value to about 100 Ω to 330 Ω. C5 should have a capacitance of about 100 pF to 470 pF with good temperature characteristics. If the C5 value is too large, a response time of the OCP function may become slow. This causes the peak drain current to be increased in transient conditions such as a startup.

• COMP Pin Peripheral Circuit

The reference capacitance of C6 is about 0.47 µF to 2.2 µF. If the capacitance is too small, the OLP function may be activated when the IC restarts. C6 should be adjusted based on actual operations in your application.

• VCC Pin and Its Peripheral Circuit

Generally, the approximate value of C4 capacitance is

4.7 µF to 22 µF. Care must be taken in setting the value of C4 because it affects the startup time (see Section 9.1).

In actual power supply circuits, the overvoltage protection (OVP) may be activated due to fluctuation of the VCC pin voltage in proportion to the output current, I_{OUT} (see Figure 10-2). This happens because the transient surge voltage that occurs at power MOSFET turn-off induces a voltage across the auxiliary winding, D and C4 is charged at the peak of the induced voltage. To prevent the C4 peak charging, add R1 with a value ranging from several ohms to several ten ohms, in series with D5 (see Figure 10-1). The optimal value of R1 should be determined with a transformer set for an actual application, because the variation of the VCC pin voltage depends on the transformer's structural design.

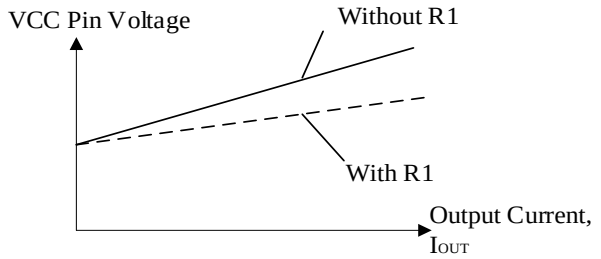


Figure 10-2. I_{OUT} vs. VCC with or without R1

• Snubber Circuit

When the surge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 10-1);

– A clamp snubber circuit of a capacitor-resistor- diode (CRD) combination should be added on the primary winding P.
– A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the darin and source pins of the power MOSFET. When the damper snubber circuit is added, the components should be connected close to the drain and source pins.

• Transformer

Apply proper design margin to temperature rise due to core loss and copper loss. Because the switching currents contain high frequency currents, the skin effect may become a consideration. For this reason, the wire diameter of a transformer winding should be selected by taking the RMS of the operating current into account, and the current density should be 3 A/mm^2 to 4 A/mm^2. If the measures to further reductions in temperature are still necessary, the following should be taken into account to increase the total surface area of the wiring:

– Increase the number of wires in parallel.
– Use litz wires.
– Thicken the wire gauge.

Care must be taken in the placement of the auxiliary winding, D, when designing your transformer because the VCC pin voltage is more susceptible to the effect of I_{OUT} in the following cases.

– When poor coupling between the primary and secondary windings causes high surge voltage in the conditions such as low output voltage and high output current.
– When poor coupling between the auxiliary winding, D, and the secondary winding causes the auxiliary winding voltage to be susceptible to the effect of surge voltage variation.

Figure 10-3 shows two transformer design examples for minimizing the impact of VCC surge voltage, with consideration given to the placement of the auxiliary winding, D.

<Winding Structural Example (a)>

Separate the auxiliary winding, D, from the primary windings, P1 and P2 (P1 and P2 are two separated primary windings).

<Winding Structural Example (b)>

The structure to improve the coupling between the secondary winding, S1, and the auxiliary winding, D

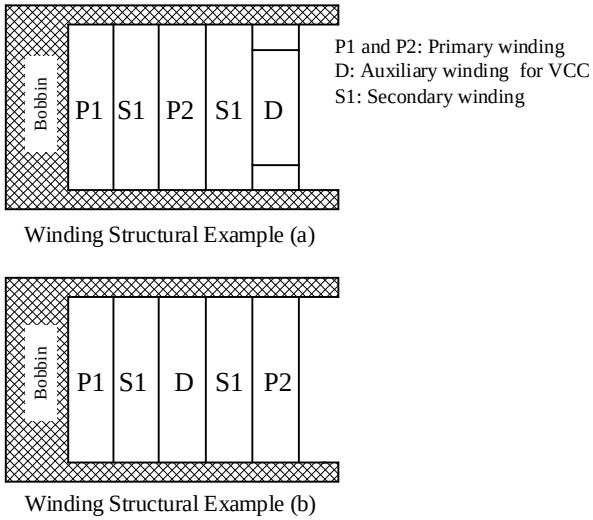


Figure 10-3. Winding Structural Examples

10.2. Transformer Design

Figure 10-4 shows an ideal waveform of a sine wave of AC input voltage in the average current control. The symbols in Figure 10-4 are represented as follows:

V_{INRMS} is the effective value (RMS) of a sine wave of AC input voltage,

I_{IN} is the input current,

I_{INP} is the peak input current,

I_D is the power MOSFET drain current,

I_{DP} is the power MOSFET peak drain current,

I_S is the forward current of a secondary rectifier diode, and

I_{SP} is the peak forward current of a secondary rectifier diode.

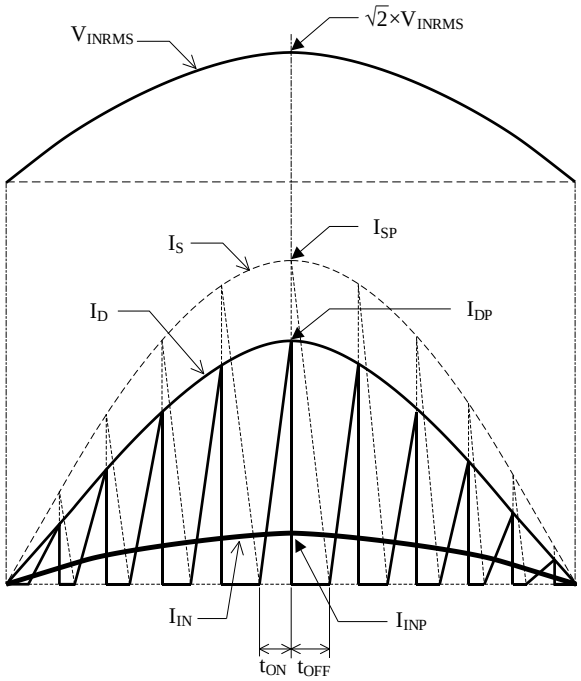


Figure 10-4. Ideal Current Waveform

In the average current control, the IC controls the COMP pin voltage to be constant over the AC input voltage, V_{IN}, which is the sine wave of a commercial frequency. Therefore, the envelope curve of the peak drain current, I_{DP}, and the input current, I_{IN} (i.e., average of I_{DP}), becomes sinusoidal, similar to that of the AC input voltage. The values of C6 connected to the COMP pin and the secondary current detection resistor are adjusted so that the COMP pin voltage remains constant.

Designing a transformer for the flyback circuit used for the IC employs the method for designing ringing choke converter (RCC) transformers. However, a quasi-resonant operation includes a certain delay to a turn-on timing, so duty cycles change. Moreover, as the input capacitor uses no electrolytic capacitor, the applied voltage of a transformer results in a sine wave of the AC input voltage, V_{IN}, at commercial frequencies.

Therefore, the duty cycle compensation for quasi-resonant delay time is added to the basic equation of the RCC topology; moreover, the equation must be changed into the sine wave of the AC input voltage, V_{IN}.

Thus, the primary-side inductance, L_P', with quasi-resonant delay time considered and the sine-wave AC input voltage applied is expressed as Equation (15).

$$L_P' = \frac{\left(V_{INRMS(MIN)} \times D_{ON}\right)^2}{\left(\sqrt{\frac{2 \times P_{OUT} \times f_{S(MIN)}}{\eta}} + V_{INRMS(MIN)} \times D_{ON} \times f_{S(MIN)} \times \pi\sqrt{C_V}\right)^2} \quad (15)$$

Where:
$V_{INRMS(MIN)}$ is the effective value (RMS) of the sine wave of the minimum AC input voltage,
P_{OUT} is the maximum output power calculated by Equation (16),
$f_{S(MIN)}$ is the operation frequency at the peak voltage of the sine wave of the AC input voltage (i.e., minimum operation frequency),
η is the efficiency, ranging from 80% to 90%,
C_V is the capacitance of the voltage resonant capacitor (C3), typically rated at between 47 pF and 470 pF, and
D_{ON} is the maximum duty cycle not compensated for the quasi-resonant delay time at the sine wave of the minimum AC input voltage, given by Equation (17).

$$P_{OUT} = V_{OUT} \times I_{OUT} \quad (16)$$

Where:
V_{OUT} is the output voltage, and
I_{OUT} is the maximum output current.

$$D_{ON} = \frac{V_{FLY}}{\sqrt{2} \times V_{INRMS(MIN)} + V_{FLY}} \quad (17)$$

Where:
$V_{INRMS(MIN)}$ is the effective value (RMS) of the sine wave of the minimum AC input voltage, and
V_{FLY} is the flyback voltage calculated by Equation (18).

The flyback voltage is determined by the power MOSFET breakdown voltage and the surge voltage. When the power MOSFET breakdown voltage is 650 V for universal input specifications, the target voltage of V_{FLY} is 100 V to 150 V.

$$V_{FLY} = \frac{N_P}{N_S} \times (V_{OUT} + V_F) \quad (18)$$

Where:
N_P is the primary winding,
N_S is the secondary winding, and
V_F is the forward voltage of the secondary rectifier diode, D10 ($V_F \approx 0.7$ V).

The quasi-resonant delay time, t_{ONDLY} is calculated by the following equation.

$$t_{ONDLY} = \pi\sqrt{L_P' \times C_V} \quad (19)$$

The compensated maximum duty cycle, D_{ON}', which includes a quasi-resonant delay time (t_{ONDLY}) is expressed as:

$$D_{ON}' = \left(1 - f_{S(MIN)} \times t_{ONDLY}\right) \times D_{ON} \quad (20)$$

The RMS input current of the sine wave of the minimum AC input voltage, $I_{INRSM(MAX)}$, is defined as:

$$I_{INRMS(MAX)} = \frac{P_{OUT}}{\eta \times V_{INRMS(MIN)}} \quad (21)$$

The peak drain current, $I_{DP(DLY)}$, which includes a quasi-resonant delay time (t_{ONDLY}) is expressed as:

$$I_{DP(DLY)} = \frac{2\sqrt{2} \times P_{OUT}}{\eta \times D_{ON}' \times V_{INRMS(MIN)}} \quad (22)$$

For proper transformer designing, the following should be taken in to account when you choose the AL-value of a ferrite core used in your transformer to avoid transformer saturation: the value of NI-Limit(AT) (= $N_P \times I_{DP(DLY)}$) calculated from the primary winding, N_P, and the peak drain current, $I_{DP(DLY)}$.

To select a ferrite core that satisfies the relationship between NI-Limit and AL-value, set a design margin for variations such as temperature as follows. Set the calculated NI-Limit value within the NI-Limit vs. AL-value characteristic curve (hatched area) in Figure 10-5 where the magnetic saturation margin is about 30% lower than the core data NI-Limit.

$$\text{NI-Limit} \leq N_P \times I_{DP(DLY)} \times 130\% \quad (23)$$

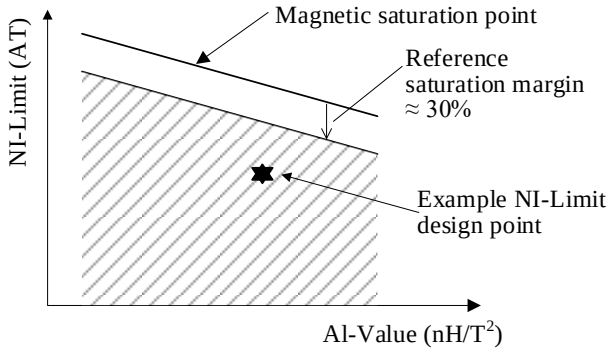


Figure 10-5. Example of NI-Limit vs. AL-value Characteristics

The primary winding (N_P), the secondary winding (N_S), and the auxiliary winding (N_D) are expressed as follows:

$$N_P = \sqrt{\frac{L_P'}{\text{AL-value}}} \quad (24)$$

$$N_S = \frac{V_{OUT} + V_F}{V_{FLY}} \times N_P \quad (25)$$

$$N_D = \frac{V_{CC}}{V_{OUT} + V_F} \times N_S \quad (26)$$

10.3. PCB Layout

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state.

In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

In addition, the following considerations should be taken into account in designing pattern layouts for your application.

Figure 10-6 is a peripheral circuit example of the IC.

(1) Main Circuit Trace Layout

This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible. To reduce the impedance of high-frequency current loops, place an input capacitor, C2, close to the transformer.

(2) Logic Ground Trace Layout

If a large current flows through a logic ground, the IC malfunction may be caused. Therefore, connect the control ground as close and short as possible to the R_{OCP} pin at a single-point ground (point A in Figure 10-6) that is separated from the power ground.

(3) Peripheral Connections to VCC Pin

Traces connected to the VCC pin should be looped small as possible because the pin supplies power to the IC. If the IC and the capacitor C4 are distant from each other, connect the film capacitor C_f (about 0.1 µF to 1.0 µF) between the VCC and GND pins with a minimal length of traces.

(4) Peripheral Connections to R_{OCP}

R_{OCP} should be placed as close as possible to the source pin and the OCP pin.

The peripheral components of the OCP pin should be connected to the root of R_{OCP} with dedicated pattern.

(5) Peripheral Components of the IC

The components for control connected to the IC should be placed as close as possible to the IC with a minimal length of traces.

(6) Secondary Rectifier Smoothing Circuit

The switching current flows through these traces. Since the secondary-side switching current flows through these traces, they should be as wide and short as possible.

Lowering the impedance of this pattern can reduce the surge voltage at the power MOSFET turn-off. Therefore, a proper rectifier smoothing trace layout permits your application to have an increased margin to the power MOSFET breakdown voltage and reduced component stress and loss in the clamp snubber circuit.

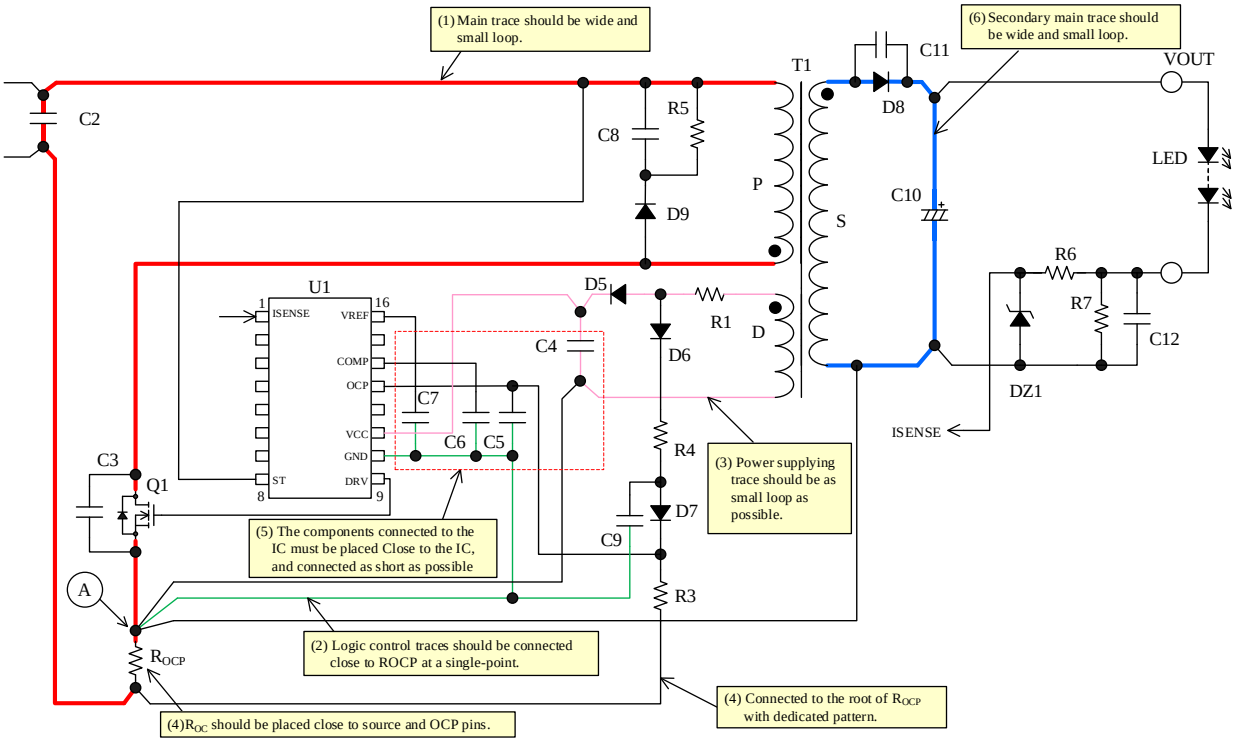


Figure 10-6. Peripheral Circuit Example around IC

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