LC5830K
DATA SHEET Rev.1.0

SANKEN ELECTRIC CO., LTD.
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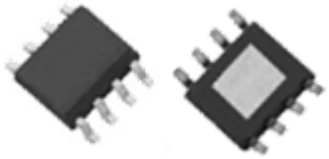
Description:

The LC5830K is a single IC switching regulator that provides constant-current output to drive high-power LEDs. It integrates a high-side N-channel DMOS switch for DC-to-DC step- down (buck) conversion.
A true average current is output using a cycle-by-cycle, controlled on-time method.
Output current is user-selectable by an external current sense resistor. Output voltage is automatically adjusted to drive various numbers of LEDs in a single string. This ensures the optimal system efficiency.
LED dimming is accomplished by a direct logic input pulse width modulation (PWM) signal at the enable pin.
The device is provided in a compact 8-pin narrow SOIC package with exposed pad for enhanced thermal dissipation.It is lead (Pb) free, with 100% matte tin leadframe plating.

Package:

eSOIC8(Exposed SOIC8)



Features and Benefits:

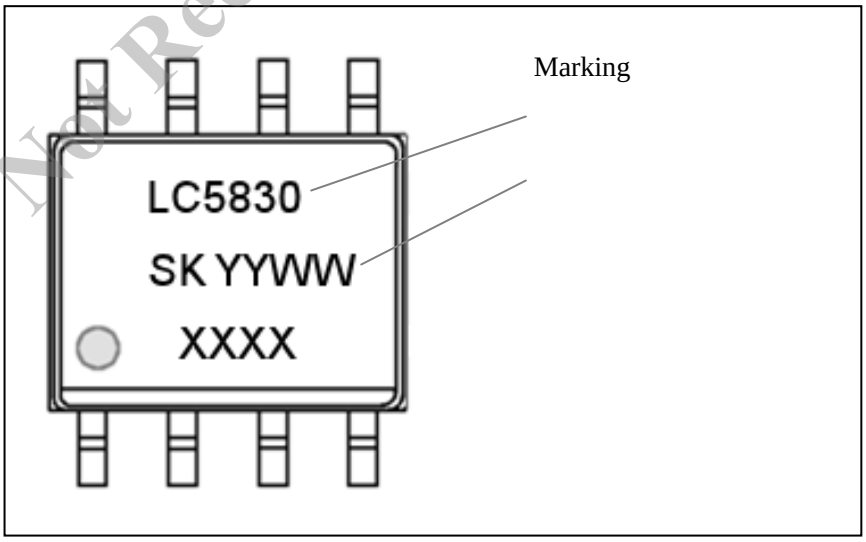
- Supply voltage 6 to 48 V
- True average output current control
- 3.0 A maximum output over operating temperature range
- Cycle-by-cycle current limit
- Integrated MOSFET switch
- PWM Dimming Freqency: 100 to 2000Hz
- Internal control loop compensation
- Undervoltage lockout (UVLO) and thermal shutdown protection
- Low power shutdown (1 μA typical)

Electrical Characteristics

Range of the Input Voltage: 6V(MIN) - 48V(MAX)
Internal MOSFET $R_{DS(ON)}$:250mΩ(TYP)
Io (i_{LED})=3A

Applications

- General Illumination
- Scanners and multi-function printers (light bars)
- Architectural lighting
- Industrial Lighting
- Display case lighting / MR16



1. Absolute maximum ratings

- Refer to a specification for contents of details.
- The polarity of the electric current value prescribes "sink = +" and "source = -" based on the IC.
- A condition Ta= 25℃ of the case without special mention.

Table.1

Characteristic	Symbol	Ratings	Units	Remarks
Input Supply Voltage	V_{IN}	−0.3～50	V	
Bootstrap Drive Voltage	V_{BOOT}	−0.3～V_{IN}+8	V	
Switching Voltage	V_{SW}	−1.5～V_{IN}+0.3	V	
Linear Regulator Terminal	V_{CC}	-0.3～14	V	Vcc – GND
Enable and TON Voltage	V_{EN}, V_{TON}	−0.3～V_{IN}+0.3	V	
Current Sense Voltage	V_{CS}	−0.3～7	V	
Allowable Power Dissipation	PD	2.85	W	
Operating Ambient Temperature	T_A	−40～105	ºC	
Maximum Junction Temperature	$T_{j(MAX)}$	150	ºC	
Storage Temperature	T_{stg}	−55～150	ºC	
Thermal Resistance (Junction –Air)	R θ ja	35	ºC/W	4-layer PCB based on JEDEC standard
Thermal Resistance (Junction – Pad)	R θ jp	2	ºC/W	

(1) But, it is restricted by Junction temperature.
(2) But, thermal protection detection temperature is about 165℃.
(3) You must use it within Thermal Derating Curve of the fig1.

* Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

2. Recommended Operation Conditions

- Recommended Operation Conditions are the required operating conditions to maintain the normal circuit functions described in the electrical characteristics. In actual operation, it should be within these conditions.
- The polarity value for current specifies a sink as "+" and a source as "−" referencing the IC.
- Unless specifically noted, Ta is 25°C

Table.2

Characteristic		Symbol	Ratings MIN	Ratings MAX	Units	Remarks
Range of VIN Pin Voltage		V_{IN}	6	48	V	
Range of Output Current	(4)	I_O	0	3	A	
Inductor ripple current ⊿IL／Io		ΔIL／Io	0.1	0.3	—	
Operating Ambient Temperature	(4)	T_{OP}	–40	105	℃	

(4) You must use it within Thermal Derating Curve of the fig1.

3. Electrical Characteristics

- Refer to a specification for contents of details.
- The polarity of the electric current value prescribes "sink = +" and "source = -" based on the IC.

Electrical Characteristics of Control Part (MIC)

Valid at V_{IN} = 24 V, T_A = –40°C to 125°C, typical values at T_A = 25°C; unless otherwise noted

Table.3

Items	Symbol	Ratings			Units	Conditions
		MIN	TYP	MAX		
Input Supply Voltage	V_{IN}	6	-	48	V	T_A=25°C
VIN Undervoltage Lockout Threshold	V_{UVLO}	-	5.3	-	V	V_{IN} increasing
VIN Undervoltage Lockout Hysteresis	$V_{UVLOHYS}$	-	150	-	mV	V_{IN} decreasing
VIN Pin Supply Current	I_{IN}	-	5	-	mA	V_{CS}=0.5V, EN="H"
VIN Pin Shutdown Current	I_{INSD}	-	1	10	μA	EN shorted to GND
Buck Switch Current Limit Threshold	I_{SWLIM}	3.0	4.0	5.0	A	
Buck Switch On-Resistance	$R_{DB(on)}$	-	0.25	0.4	Ω	V_{BOOT}=V_{IN}+4.3V, T_A=25°C, I_{SW}=1A
BOOT Undervoltage Lockout Threshold	V_{BOOTUV}	1.7	2.9	4.3	V	V_{BOOT} to V_{SW} increasing
BOOT Undervoltage Lockout Hysteresis	$V_{BOOTHYS}$	-	370	-	mV	V_{BOOT} to V_{SW} decreasing
Switching Minimum Off-Time	t_{OFFmin}	-	110	150	ns	V_{CS}=0V
Switching Minimum On-TIme	$t_{SWONTIME}$		110	150	ns	
Selected On-Time	t_{ON}	800	1000	1200	ns	V_{IN}=24V, V_{OUT}=12V, R_{ON}=137 kΩ
Load Current Sense Regulation Threshold	V_{CSREG}	187.5	200	210	mV	V_{CS} decreasing, SW turns on
Load Current Sense Bias Current	I_{CSBIAS}	-	0.9	-	μA	V_{CS}=0.2V, EN=low
VCC Regulated Output	V_{CC}	5.0	5.3	5.6	V	0mA<I_{CC}<5mA, V_{IN}>6V
VCC Current Limit*	I_{CCLIM}	5	20	-	mA	V_{IN}=24V, V_{CC}=0V
Logic High Voltage	V_{IH}	1.8	-	-	V	V_{EN} increasing
Logic Low Voltage	V_{IL}	-	-	0.4	V	V_{EN} decreasing
EN Pin Pull-down Resistance	R_{ENPD}	-	100	-	kΩ	V_{EN}=5V
Maximum PWM Dimming Off-Time	t_{PWML}	10	17	-	ms	Measured while EN = low, during dimming control, and internal references are powered-on (exceeding tPWML results in shutdown)
Thermal Shutdown activation temperature	T_{SD}	–	165	–	°C	
Thermal Shutdown Hysteresis temperature	T_{SDHYS}	–	25	–	°C	

* The internal linear regulator is not designed to drive an external load.

Allowable package power dissipation

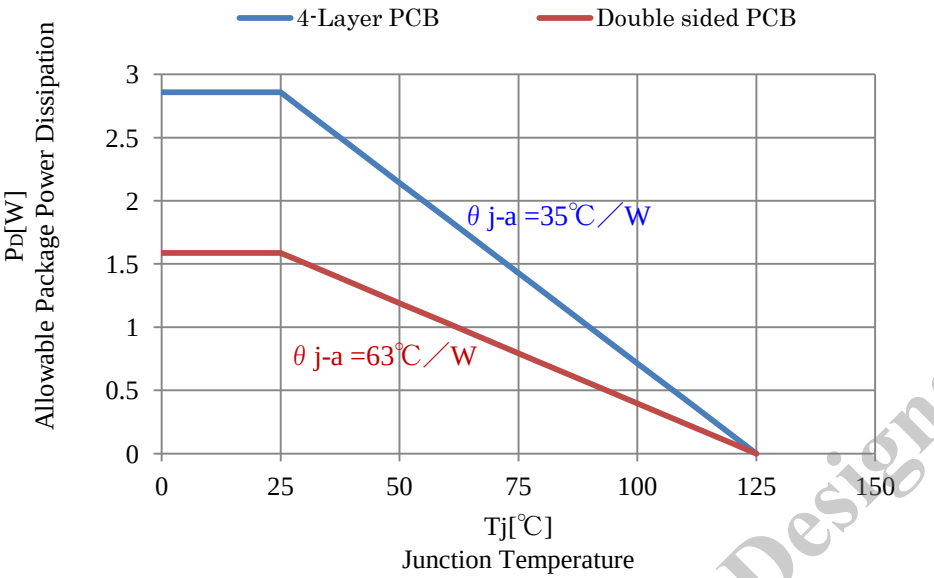


fig.1 LC5830K Thermal Derating Curve

Note1: 4-layer PCB based on JEDEC standard.
Copper area: 1inch × 1inch =1inch^2 (645.16mm^2) /Layer ,4-layer PCB with via connection(Blue line)
Copper area: 1inch × 1inch =1inch^2 (645.16mm^2) /Layer ,Double sided PCB with via connection(Red line)
* θ j-a grows big when the areas of the radiation pattern in total decrease.

Note2: As for the "Thermal-Derating-Curve" of the fig1, it is calculated in consideration of the printed-circuit-board temperature limit = 130℃ to use most in less Junction-temperature Tj= 125℃.

Note3: P_D can be calculated with the following equation.

$$P_D=(VIN\times I_{IN})-(V_{OUT}\times i_{LED})-(i_{LED}^2\times DCR)-\{V_F\times i_{LED}\times(1-Duty)\}-(V_{CS}^2/R_{SENSE}) \quad \cdots(1)$$

VIN: Input Voltage(V), I_{IN}: Input Current(A), i_{LED}: Average Current of LED(A),
V_F: The forward voltage of Flyweel-Diode (V), DCR: DC-resistance of Inductor winding(Ω),
Duty: V_{OUT}／VIN (V_{OUT}=LED String voltage＋V_{CS}), V_{CS}=0.2(V), R_{SENSE}=Current detection resistance(Ω)
* It is based on the measurement circuit of the fig2.

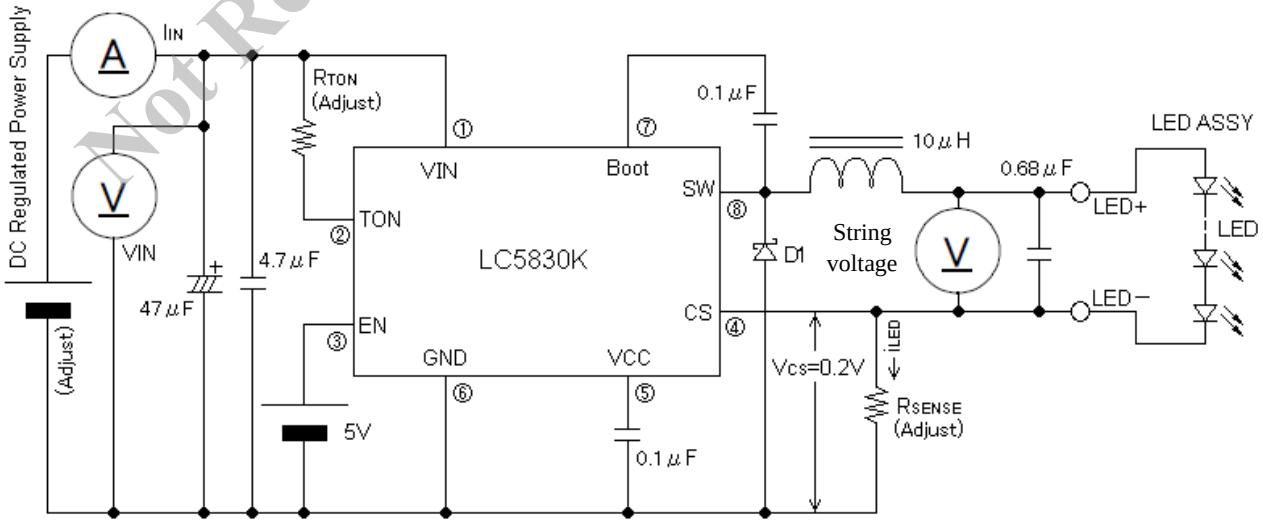


fig2. Measurement circuit of Power dissipation

4. Functional Block Diagram

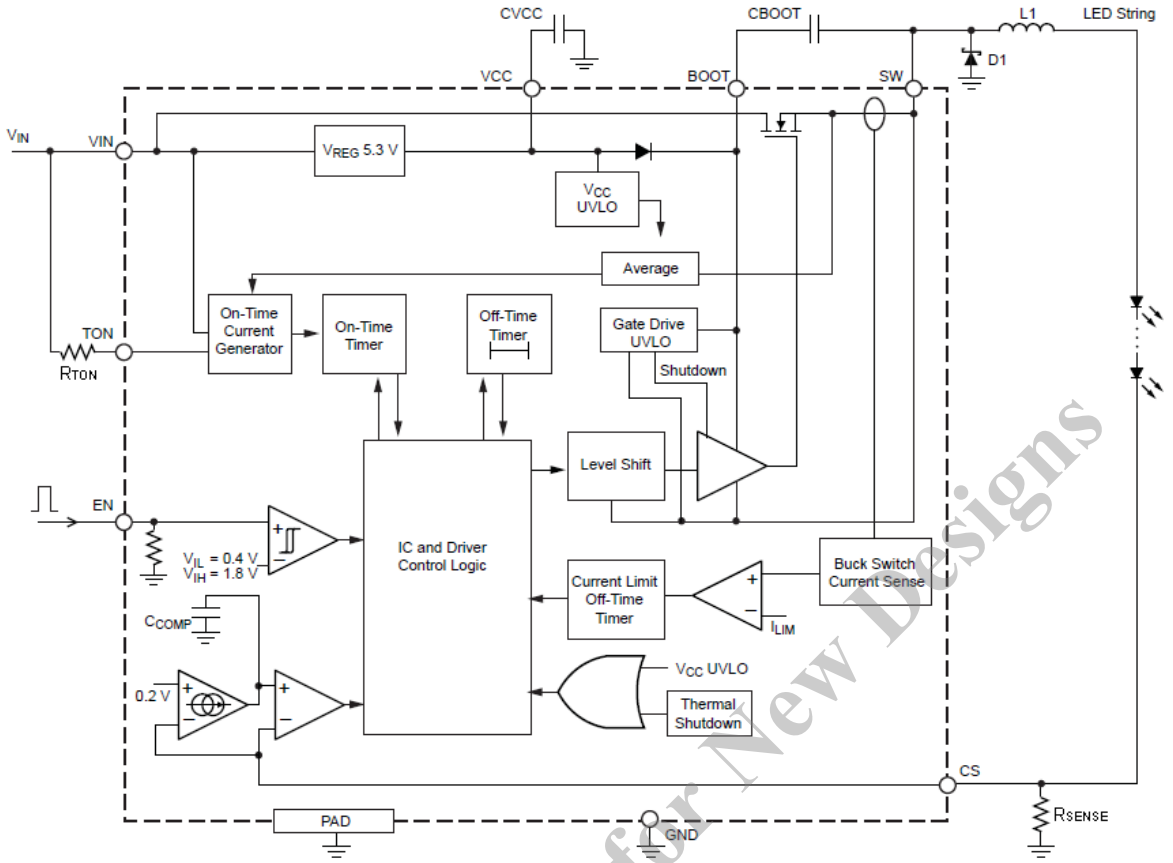


fig3. Function Block Diagram

5. Pin Assignment & Functions

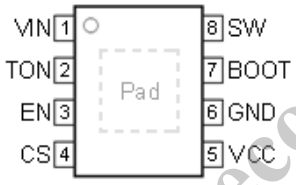


fig.4 Pin Assignment

Table.4

Pin No.	Symbol	Functions
1	VIN	Supply voltage input terminals
2	TON	Regulator on-time setting resistor terminal
3	EN	Logic input for Enable and PWM dimming
4	CS	Drive output current sense feedback
5	VCC	Internal linear regulator output
6	GND	Ground terminal
7	BOOT	DMOS gate driver bootstrap terminal
8	SW	Switched output terminals
Pad	-	Exposed pad for enhanced thermal dissipation;connect to GND

6. Typical Application Circuit

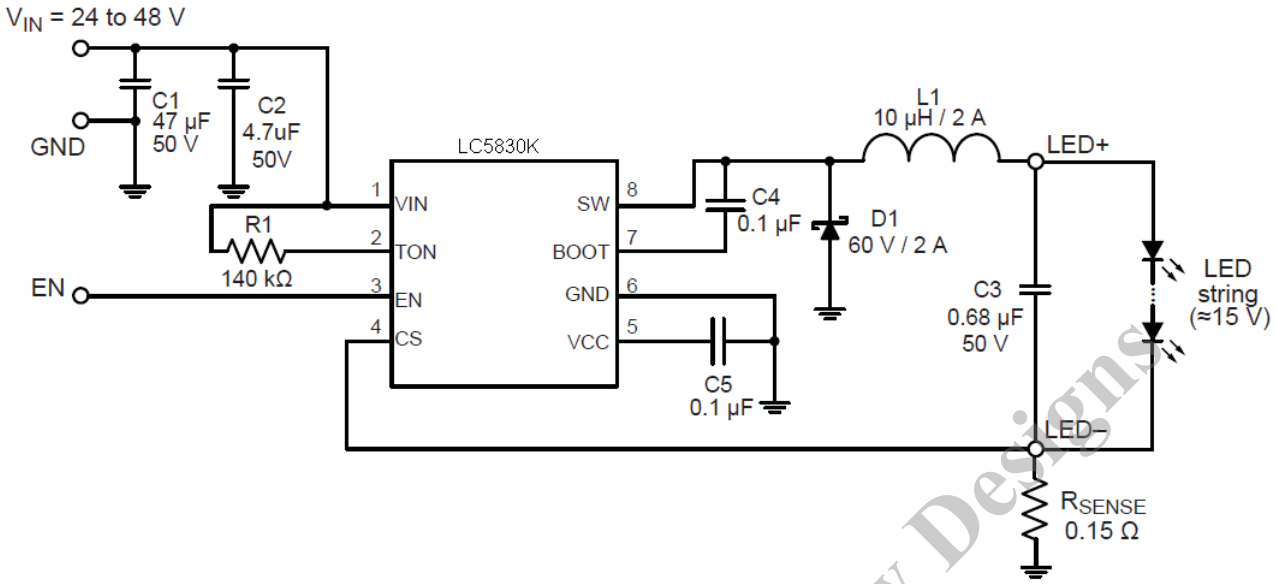


fig5. LC5830K Application Circuit

The application circuit in fig5 shows a design for driving a 15 V LED string at 1.3 A (set by RSENSE). The switching frequency is 500 kHz, as set by R1. As for the C_{OUT}, a 0.68 µF ceramic capacitor is added across the LED string to reduce the ripple current through the LEDs (as shown in figure 17B).

*Refer to “9.2 demonstration board circuit diagram” for the circuit diagram of the demonstration board.

7. Package Information

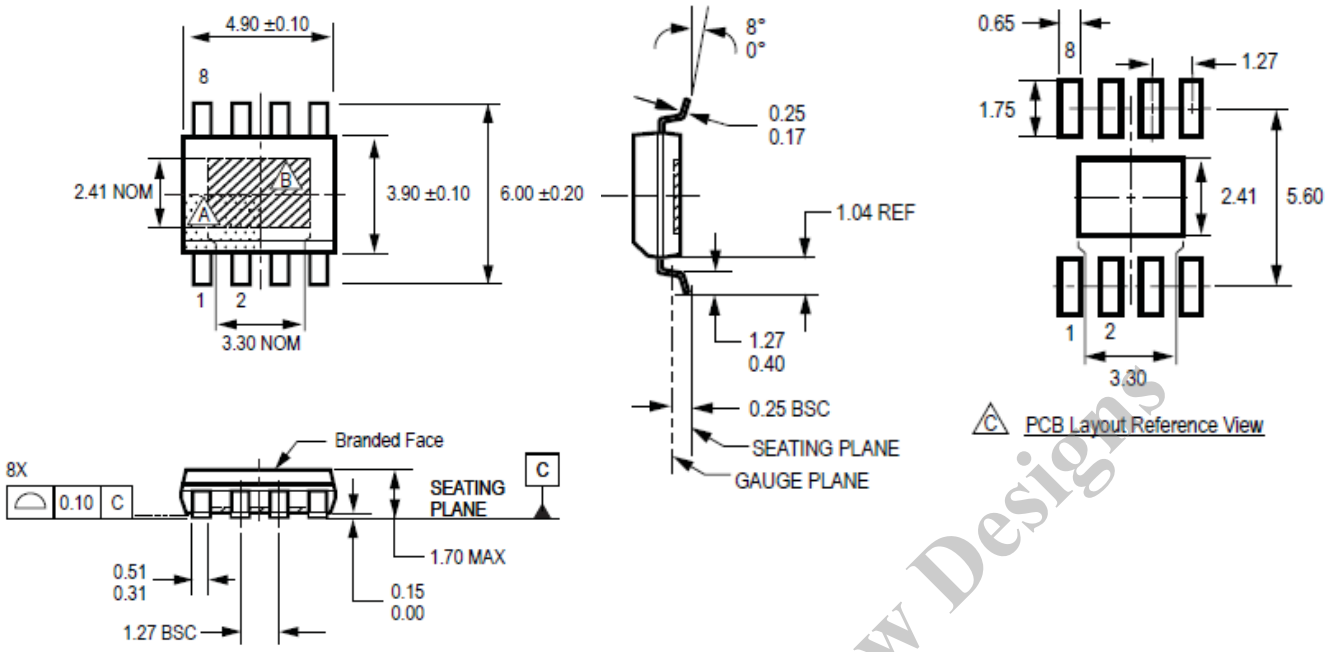


fig6. package outline

Units : Dimensions in mm

A Mark of Pin No.1

B Exposed Thermal Pad(Bottom Surface)

C Foot-printing reference (Adjust it corresponding to the application.)

For Reference Only; not for tooling use (reference MS-012BA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351SOP65P640X120-29CM);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirementsand PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

8. Functional Description

The LC5830K is a buck regulator designed for driving a high-current LED string. It utilizes average current mode control to maintain constant LED current and consistent brightness. The LED current level is easily programmable by selection of an external sense resistor, valued as follows:

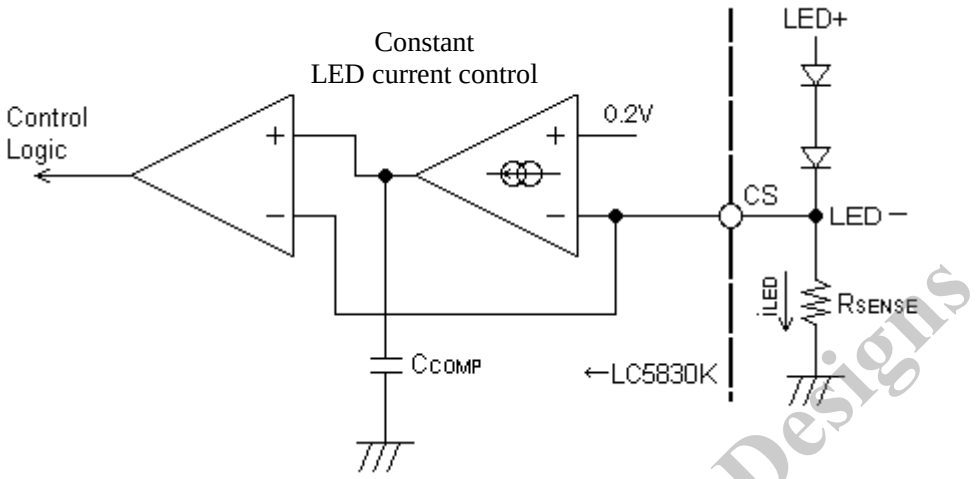


fig.7 Constant LED current control

$i_{LED} = V_{CSREG} / R_{SENSE}$ ･･･(2) where ,V_{CSREG} = 0.2V typical.

In other words, by detecting "Voltage between both ends" of the "LED current detection resistor R_{SENSE}" that is series connection to LED with the CS terminal, it is controlled so that "Voltage between both ends" of R_{SENSE} may become a constant (0.2V).

8.1 Settlement of frequency

The LC5830K operates in fixed on-time mode during switching. The on-time (and hence switching frequency) is programmed using an external resistor connected between the VIN and T_{ON} pins, as given by the following equation:

$t_{ON} = k \times (R_{TON} + R_{INT}) \times (V_{OUT} / V_{IN})$ ･･･(3)

$f_{SW} = 1 / [k \times (R_{TON} + R_{INT})]$ ･･･(4)

where, k = 0.013, with f_{SW} in MHz, t_{ON} in μs and R_{TON} in kΩ, R_{INT}=5kΩ（Refer to fig8.）

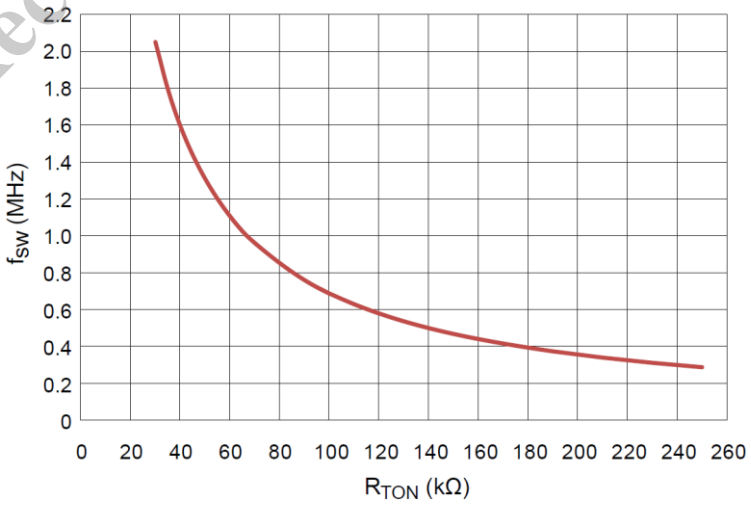


fig.8 Switching Frequency versus R_{TON} Resistance

8.2 Enable and Dimming

·Enable terminal

The IC is activated when a logic high signal is applied to the EN (enable) pin. The buck converter ramps up the LED current to a target level set by RSENSE. When the EN pin is forced from high to low, the buck converter is turned off, but the IC remains in standby mode for up to 10 ms. If EN goes high again within this period, the LED current is turned on immediately. Active dimming of the LED is achieved by sending a PWM (pulse-width modulation) signal to the EN pin. The resulting LED brightness is proportional to the duty cycle (T_{ON} / Period) of the PWM signal. A practical range for PWM dimming frequency is between 100 Hz (Period = 10 ms) and 2 kHz. At a 200 Hz PWM frequency, the dimming duty cycle can be varied from 100% down to 1% or lower.

If EN is low for more than 17 ms, the IC enters shutdown mode to reduce power consumption. The next high signal on EN will initialize a full startup sequence, which includes a startup delay of approximately 130 µs. This startup delay is not present during PWM operation. The EN pin is high-voltage tolerant and can be directly connected to a power supply. However, if EN is higher than the V_{IN} voltageat any time, a series resistor (1 kΩ) is required to limit the current flowing into the EN pin. This series resistor is not necessary if EN is driven from a logic input.

·PWM Dimming Ratio

The brightness of the LED string can be reduced by adjusting the PWM duty cycle at the EN pin as follows:
Dimming ratio = PWM on-time / PWM period.
For example, by selecting a PWM period of 5 ms (200 Hz PWM frequency) and a PWM on-time of 50 µs, a dimming ratio of 1% can be achieved. In an actual application, the minimum dimming ratio is determined by various system parameters, including: V_{IN}, V_{OUT}, inductance, LED current, switching frequency, and PWM frequency. As a general guideline, the minimum PWM on-time should be kept at 50 µs or longer. A shorter PWM on-time is acceptable under more favorable operating conditions.

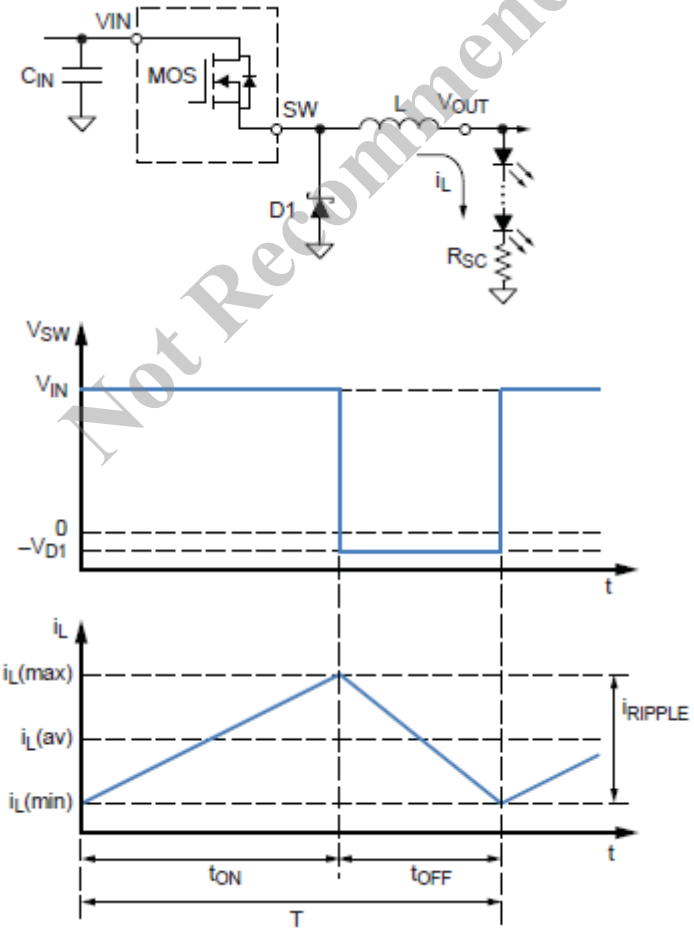
8.3 Range of Output Voltage

fig9 provides simplified equations for approximating output voltage. Essentially, the output voltage of a buck converter is approximately given as

$$V_{OUT} = V_{IN} \times D - V_{D1} \times (1 - D) \approx V_{IN} \times D, \text{ if } V_{D1} << VIN \quad \cdots(5)$$

$$D = t_{ON} / (t_{ON} + t_{OFF}) \quad \cdots(6)$$

where D is the duty cycle, and VD1 is the forward drop of the Schottky diode D1 (typically under 0.5 V).



·During SW on-time:

$$i_{RIPPLE} = [(V_{IN} - V_{OUT}) / L] \times t_{ON} \quad \cdots(7)$$
$$= [(V_{IN} - V_{OUT}) / L] \times T \times D$$
where, $D = t_{ON} / T \quad \cdots(7)$

·During SW off-time:

$$i_{RIPPLE} = [(V_{OUT} - V_{D1}) / L] \times t_{OFF} \quad \cdots(8)$$
$$= [(V_{OUT} - V_{D1}) / L] \times T \times (1 - D)$$

Therefore (simplified equation for Output Voltage):

$$V_{OUT} = V_{IN} \times D - V_{D1} \times (1 - D) \quad \cdots(9)$$

If $V_{D1} << V_{OUT}$,
then V_{OUT} is $\cdots$ $V_{OUT} \approx V_{IN} \times D. \cdots(10)$

More precisely $\cdots$

$$V_{OUT} = (V_{IN} - Iav \times R_{DS(on)}) \times D$$
$$- V_D \times (1 - D) - R_L \times Iav \quad \cdots(11)$$

where, R_L is the resistance fo the inductor.

fig.9 Simplified buck controller equations

For a given input voltage, the maximum output voltage depends on the switching frequency and minimum t_{OFF} . For example, if t_{OFF}(min) = 150ns and f_{SW} = 1 MHz, then the maximum duty cycle is 85%. So for a 24V input, the maximum output is 20.3V. This means up to 6 LEDs can be operated in series, assuming Vf = 3.3V or less for each LED.

The minimum output voltage depends on minimum t_{ON} and switching frequency. For example, if the minimum t_{ON} = 150ns and f_{SW} = 1 MHz, then the minimum duty cycle is 15%. That means with V_{IN} = 24V, the minimum V_{OUT} = 3.2V (one LED). Switching at lower frequency allows a wider range of V_{OUT}, hence more flexible LED configurations. This is shown in fig10.

As a general rule, switching at lower frequencies allows a wider range of V_{OUT} , and hence more flexible LED configurations. This is shown in fig10. fig11 shows how the minimum and maximum output voltages vary with LED current (assuming RDS(on) = 0.4 Ω, inductor DCR = 0.1 Ω, and diode Vf = 0.6 V).

If the required output voltage is lower than that permitted by the minimum t_{ON} , the controller will automatically extend the t_{OFF} , in order to maintain the correct duty cycle. This means that the switching frequency will drop lower when necessary, while the LED current is kept in regulation at all times.

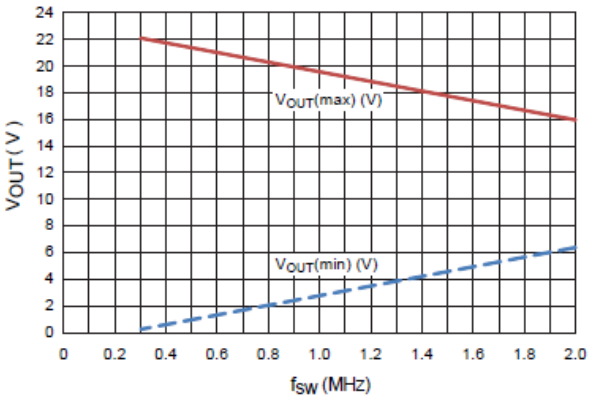


fig.10 Minimum and Maximum Output Voltage versus Switching Frequency
(VIN = 24 V, minimum tON and tOFF = 150 ns)

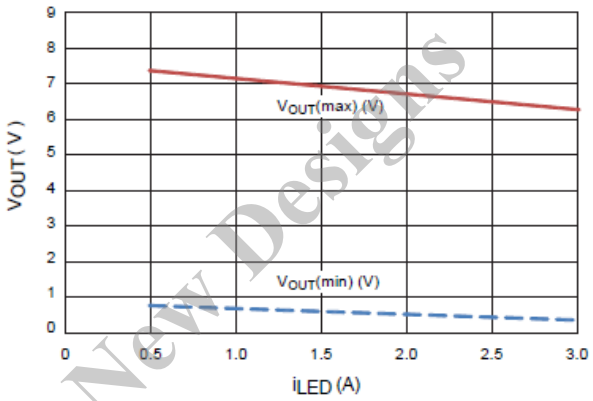


fig.11 Minimum and Maximum Output Voltage versus iLED current
(VIN = 9 V, f_{SW} = 1 MHz, minimum t_{ON} and t_{OFF} = 150 ns)

8.3.1 The number of LED's that it can be driven with LC5830K

Now, the CS terminal voltage =0.2V is taken. When a V_F of LED to connect is set at 3.5V (Max), The number of serial LED's of the string which can be driven, they are shown such as a fig12 and a fig13.

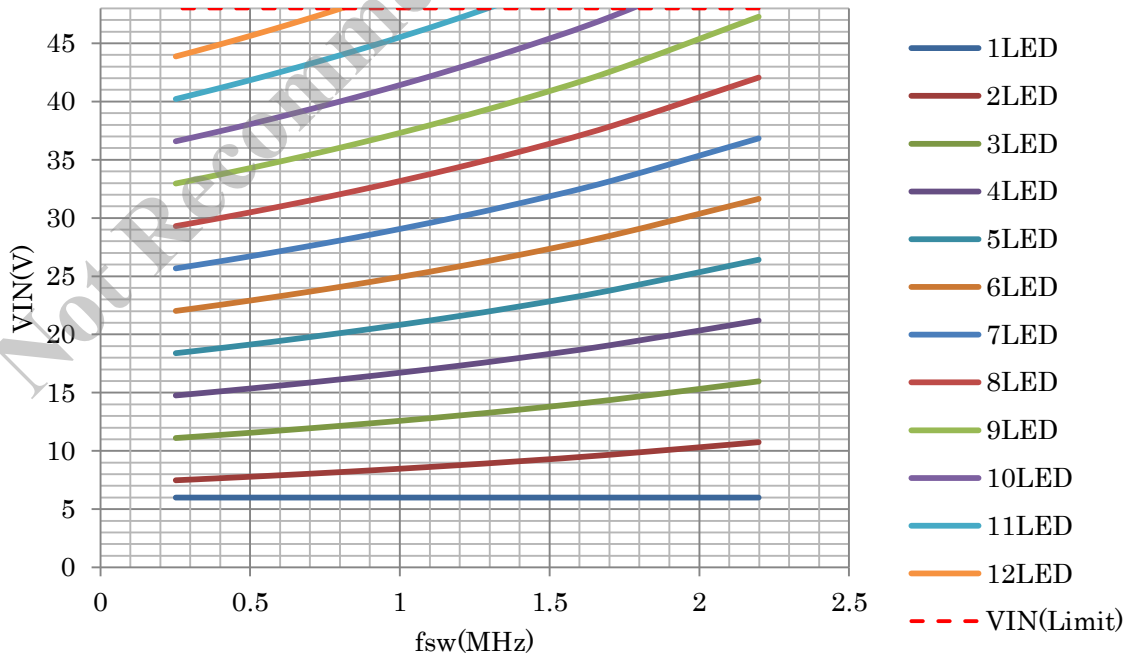


fig.12 The limitation of VIN at t_{OFF}(Min)=150nsec

When a difference in voltage of the "output voltage VOUT" and the "input voltage VIN" becomes small, a fig12 shows the condition of VIN that the "switching-off-period" reaches t_{OFF} (Min) =150nsec.You must avoid the condition which reaches t_{OFF} (Min) =150nsec fundamentally.
If the switching-frequency rises more, you must make ON-Duty decrease and VIN increase.
But,the recommended operating conditions is VIN≦48V.
Therefore from the figure 12, the number of LED serial connection, 9 LEDs are the limit in the whole area of the frequency which can be set up with R_{TON}. If the frequency can be lowered, it is possible to use 10-12 LEDs serial connection.
Then you must set it up, the available VIN ranges which is between "allowable min Vin and 48V.

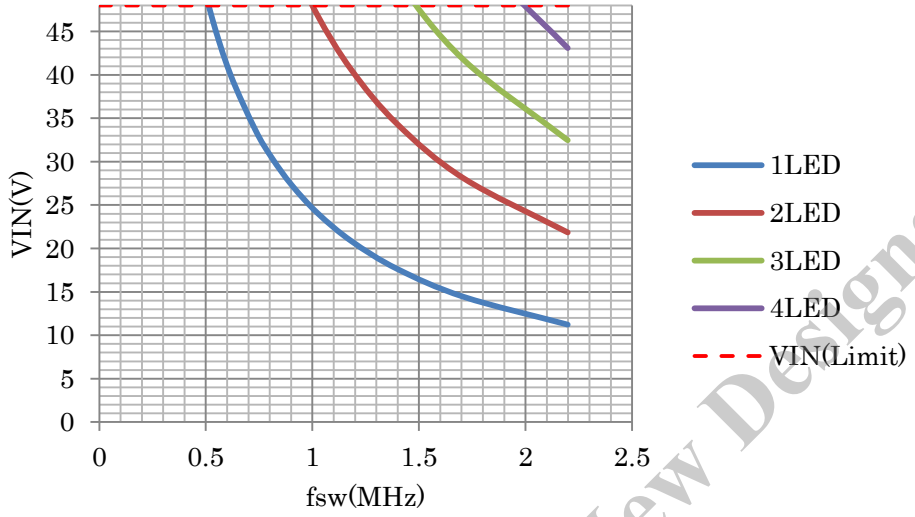


fig.13 When the input voltage is high using a few LED's, the limitation of VIN by "tON (Min) =150nsec".

A fig13 shows the condition that the "switching-ON-period" reaches t_{ON} (Min) =150nsec ,when the VIN is high and using a few LED's. Because it is V_{OUT}<<VIN as a movement condition of the IC, the control Duty-cycle becomes small.
This case, because the control margin becomes narrow when the frequency increases, you must set up VIN that is lower than the "VIN value on each curve" of the fig13.
And, be careful, because it is VIN≦48V as well as the fig12 by the recommended operating condition.

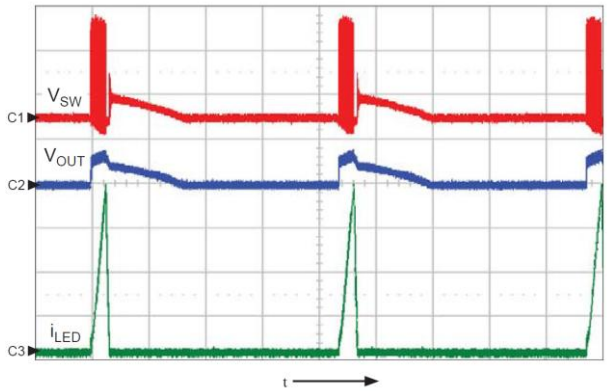
From the above, It seems that the "switching on period" reaches the t_{ON} (Min) condition when the switching frequency was deviated to the tendency that it decreases to against the setup by R_{TON}. And, when the phenomenon that Output-voltage V_{OUT} decreases, the "switching off period" has the possibility to reach the condition of t_{OFF} (Min). Reconsider the setup "range of VIN" or "switching frequency", because V_{OUT} depends on the number of LED serial connection.

8.4 Thermal Budgeting

The LC5830K is capable of supplying a 3.0A current through its high-side switch. However, depending on the duty cycle, the conduction loss in the high-side switch may cause the package to overheat. Therefore care must be taken to ensure the total power loss of package is within budget. For example, if the maximum temperature rise allowed is $\Delta T = 50K$ at the device case surface, then the maximum power dissipation of the IC is 1.4W. Assuming the maximum $R_{DS(on)} = 0.4\Omega$ and a duty cycle of 85%, then the maximum LED current is limited to 2.0A approximately. At a lower duty cycle, the LED current can be higher.

8.5 Over Current Protection(OCP)

The waveform in fig14 illustrates how the LC5830K responds in the case in which the current sense resistor or the CS pin is shorted to GND. Note that the SW pin overcurrent protection is tripped at around 3.75 A, and the part shuts down immediately. The part then goes through startup retry after approximately 380 µs of cool-down period. It becomes a hiccup mode like a fig14.Also LC5830K is tripped at 3.75Atyp.



swtich node V_{SW} (ch1, 10 V/div.),

output voltage,V_{OUT} (ch2, 10 V/div.),

LED current, iLED (ch3, 1 A/div.), t = 100 µs/div

fig.14 LC5830K overcurrent protection tripped in the case of a fault caused by the sense resistor pin shorted to ground.

8.6 Component Selections(Peripheral parts)

The inductor is often the most critical component in a buck converter. Follow the procedure below to derive the correct parameters for the inductor.

8.6.1 Selection of Inductor

1) Determine the saturation current of the inductor.
This can be done by simply adding 20% to the average LED current:

$$i_{SAT} > i_{LED} \times 1.2 \quad \cdots(12)$$

2) Determine the ripple current amplitude (peak-to-peak value).
As a general rule, ripple current should be kept between 10% and 30% of the average LED current:

$$0.1 < \triangle IL / i_{LED} < 0.3 \quad \cdots(13)$$

3) Calculate the inductance based on the following equations:

$$L = (V_{IN} - V_{OUT}) \times D \times T / \triangle IL \quad \cdots(14)$$

$$D = (V_{OUT} + V_{D1}) / (V_{IN} + V_{D1}) \quad \cdots(15)$$

Where D is the duty cycle, T is the period $1/f_{SW}$, and V_{D1} is the forward voltage drop of the Schottky diode D1.(Refer to fig9)

4) Inductor Selection Chart

The chart in fig15 summarizes the relationship between LED current, switching frequency, and inductor value. Based on this chart: Assuming LED current = 2 A and fSW =1 MHz, then the minimum inductance required is L = 10 µH in order to keep the ripple current at 30% or lower. (Note: $V_{OUT} = V_{IN} / 2$ is the worst case for ripple current). If the switching frequency is lower, then either a larger inductance must be used, or the ripple current requirement has to be relaxed.

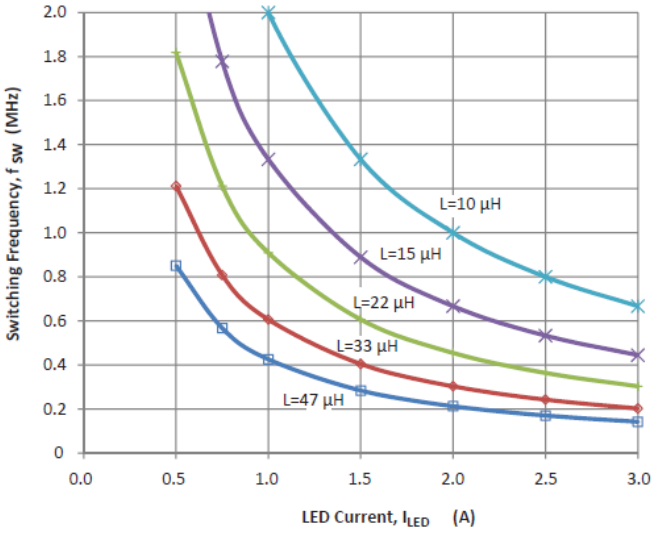


fig.15 Inductance selection based on I_{LED} and fsw ;

V_{IN} = 24 V, V_{OUT} = 12 V, ⊿IL／Io(i_{LED} ave) = 30%

8.6.2The attention in selection of Inductor.

1) For stability, as for the rate (⊿ IL/iLED) of Inductor ripple current, 10%-30 % is recommended. Select Inductor and switching frequency on the minimum VIN condition so that the rate of Inductor ripple current may go into this range. And, as a general value in the Buck-type, as a setup of Inductor, '⊿ IL/iLED=20%-30 %' is said as the 'A cost performance is the best.'

2) There is no hard limit on the highest ripple current percentage allowed. But, in this IC, the continuous current mode that is a DC superposed is recommended, it isn't the discontinuous current mode,the critical current mode. Generally, it is possible that Inductance is made small when the rate of ⊿ IL/iLED is enlarged. But, when Inductance is lowered too much, the peak of Inductor current may reach OCP threshould value. In this case, this IC can't do a normal operation.

3) Obtain the data sheet of Inductor manufacturer. And, select a part after you confirm that it isn't saturated by the current value when OCP activates.

4) Generally, if Inductance is the same, heat-generation of the winding-wire in Inductor is lower whose contour is big. It is because a thicker wire can wind it in the window frame of the core. This means that DC resistance is lowered by the large section product of the winding-wire.

5) As for the structure of a Inductor, in case of structure of open-magnetic-loop like a drum type, it is afraid of a bad influence that is given to EMI and so on. The low leakage flux type Inductor which has the structure of closed-magnetic-loop is recommended.

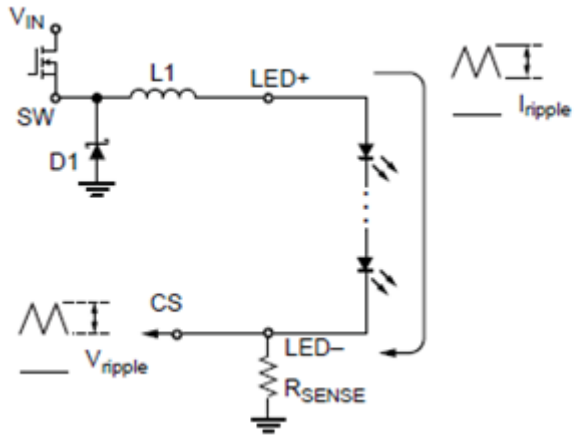
8.6.3 Output Filter Capacitor

The LC5830K is designed to operate without an output filter capacitor, in order to save cost. Adding a large output capacitor is not recommended. In some applications, it may be required to add a small filter capacitor (up to several µF) across the LED string (between LED+ and LED-) to reduce output ripple voltage and current. It is important to note that:

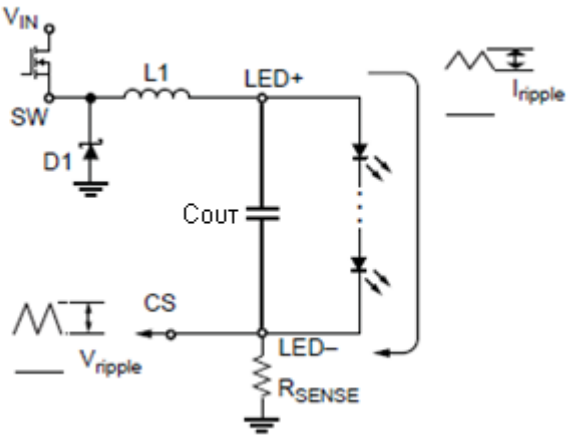
- When the large ripple current is flowing to the pattern, a C_{OUT} capacitor avoids unstable condition of the IC's GND electrical potential.(decoupling capacitor)

- The addition of this filter capacitor introduces a longer delay in LED current during PWM dimming operation. Therefore the maximum PWM dimming ratio is reduced.

- The filter capacitor should NOT be connected between LED+ and GND. Doing so may create instability because the control loop must detect a certain amount of ripple current at the CS pin for regulation.



(A)Without C_{OUT}:
Ripple current through LED string is proportional to ripple voltage at CS pin.



(B) With a C_{OUT} across LED string:
Ripple current through LED string is reduced, while ripple voltage at CS pin remains high.

fig.16 About the difference in the use of a C_{OUT} and the un-use (Ripple Current and Ripple Voltage)

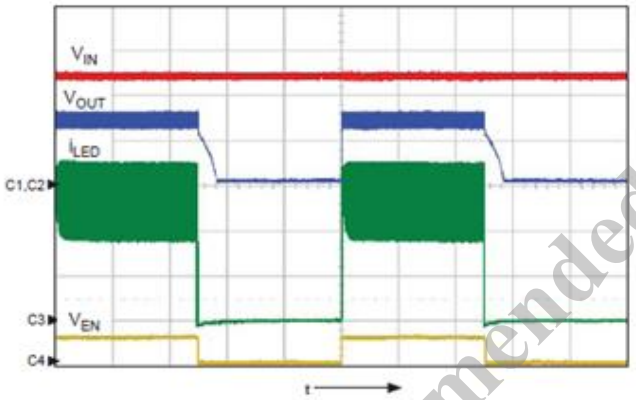


fig.17A Operation without using any output capacitor connected across the LED string

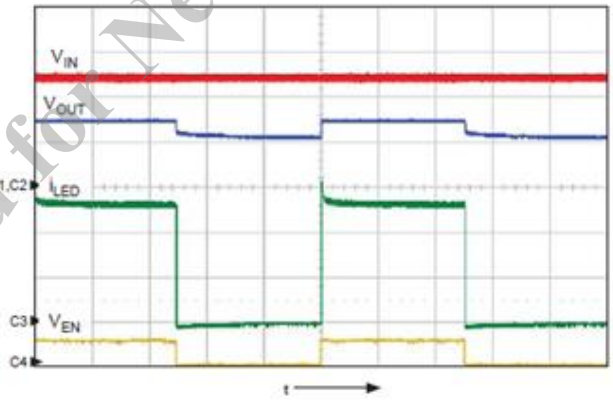


fig.17B Operation with a 0.68 µF ceramic Capacitor(as a C_{OUT}) across the LED string

Operating condition: 200 Hz, V_{IN} = 24 V, V_{OUT} = 15 V, f_{SW} = 500 kHz, L = 10 µH, duty cycle = 50%
CH1 (Red) = VIN (10 V/div), CH2 (Blue) = V_{OUT} (10 V/div),
CH3 (Green) = i_{LED} (500 mA/div), CH4 (Yellow) = Enable (5 V/div), time scale = 1 ms/div

9. Component Placement and PCB Layout Guidelines

9.1 Printing pattern drawing(Our company's circuit board for demonstration)

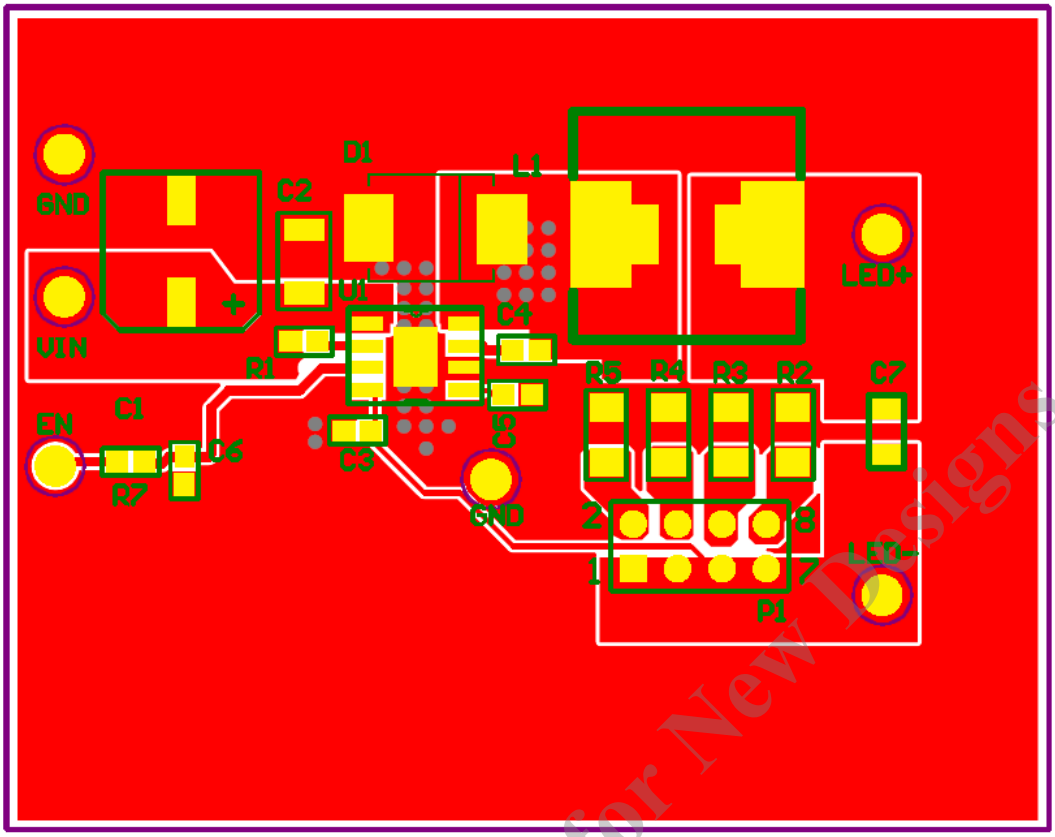


fig.18A Pattern layout of Demo-board(Double sided PCB／Parts mounting side)

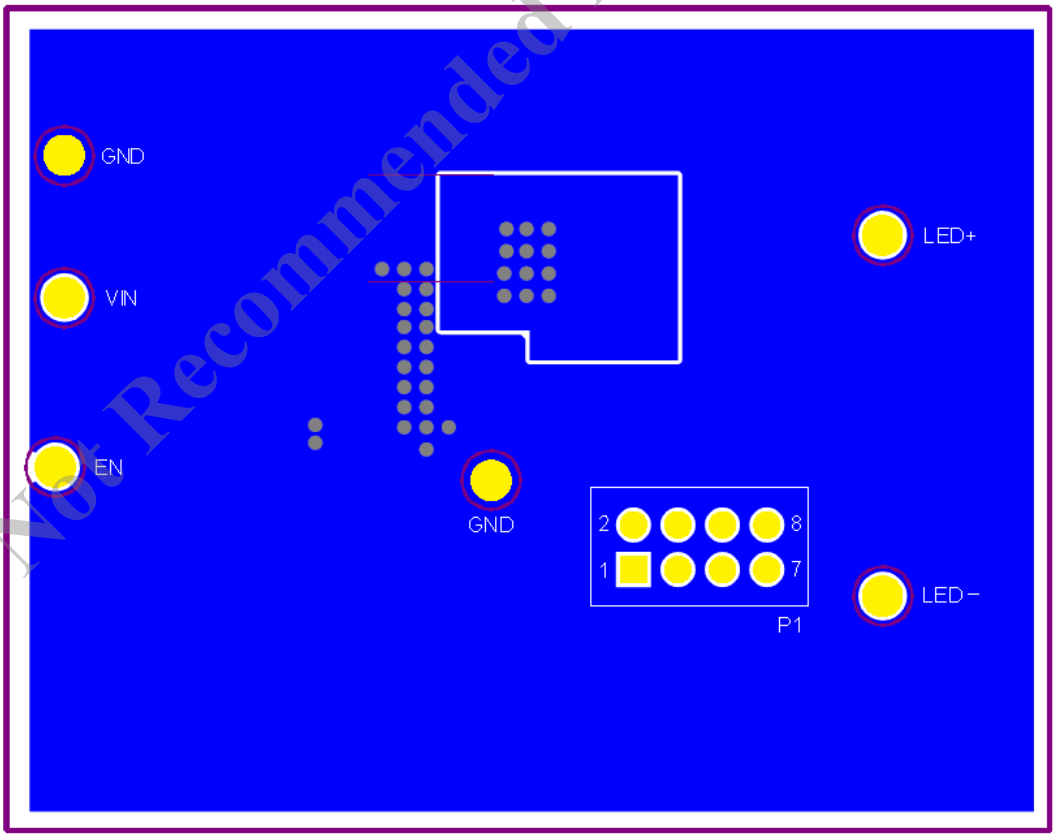


fig.18B Pattern layout of Demo-board(Double sided PCB／Back side)

Double sided PCB(Copper foil thickness：35 μ m、Base material thickness：1.6mm、Contour ：60mm×47mm)
●：via hole(ϕ 0.3)

9.2The circuit diagram of Demo-board

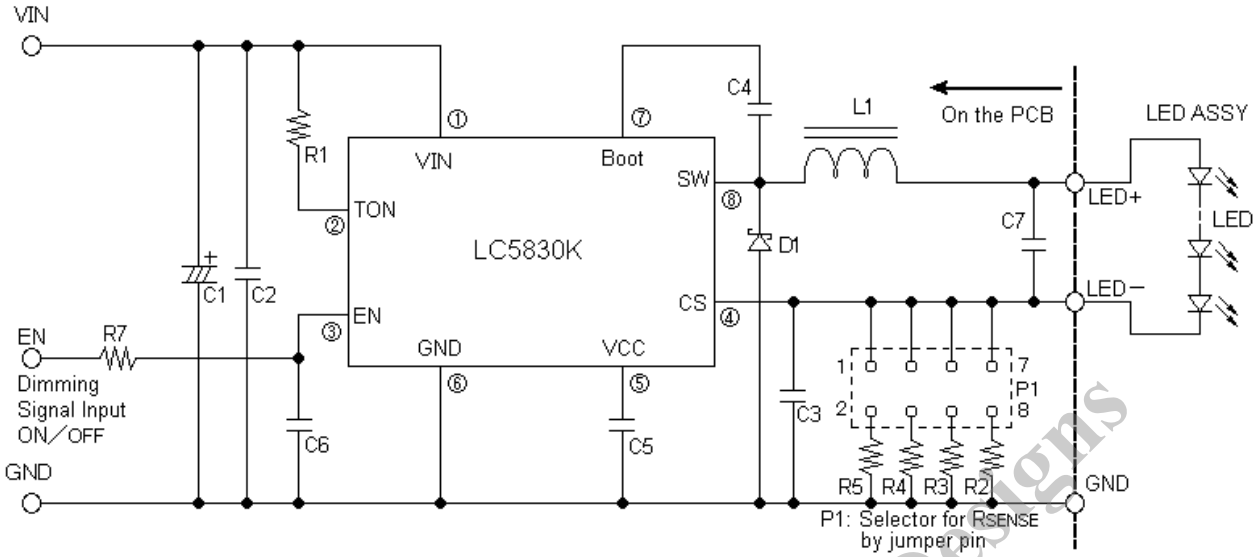


fig.19 LC5830K The circuit diagram of Demo-board

VIN=6～48V，LED string voltage≒15V， Fsw≒1MHz
C1：47μF／50V C2：4.7μF／50V C4：0.1μF／50V C5：0.1μF／50V L1：10μH
D1：SJPB-L6／Sanken-electric co.,LTD.
R1：140kΩ R2：130mΩ R3：200mΩ R4：390mΩ R5：750mΩ･･･R2－R5 can be selected with a jumper pin of P1.

Note ：An optional part for the experiment = C3，C6，C7，R7
*1：R7／C6 →The speed adjustment of dimming pulse ･･･ For the experiment.
*2：C7→It is made to decrease ripple current that is flowing to LED.･･･For the experiment.
*3：C3→For the noise filter of the CS terminal - GND terminal･･･For the experiment.
C3, C6, C7 and R7 are handled as the delay elements against inputted dimming-pulse.

PCB layout is critical in designing any switching regulator. A good layout reduces emitted noise from the switching device, and ensures better thermal performance and higher efficiency. The following guidelines help to obtain a high quality PCB layout. fig18A,fig18B show an example for components placement. fig20 shows the three critical current loops that should be minimized and connected by relatively wide traces.

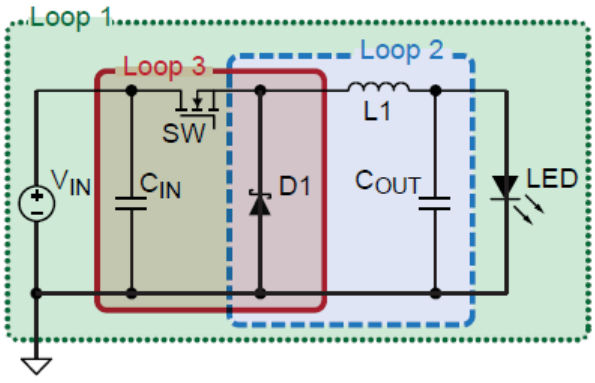


fig.20 Three different current loops in a buck converter

1) When the upper FET (integrated inside the LC5830K) is on, current flows from the input supply/capacitors, through the upper FET, into the load via the output inductor, and back to ground as shown in loop 1. This loop should have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane.

2) When the upper FET is off, free-wheeling current flows from ground through the asynchronous diode D1, into the load via the output inductor, and back to ground as shown in loop 2. This loop should also be minimized and have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane.

3) The highest di/dt occurs at the instant the upper FET turns on and the asynchronous diode D1 undergoes reverse recovery as shown in loop 3. The input capacitors C_{IN} must deliver this high instantaneous current. C1 (fig19 /electrolytic capacitor) should not be too far off C2(fig19 /ceramic capacitor). Therefore, the loop from the ceramic input capacitor C2 through the upper FET and asynchronous diode to ground should be minimized. Ideally this connection is made on both the top (component) layer and via the ground plane.

4) The voltage on the SW node (pin 8) transitions from 0 V to VIN very quickly and may cause noise issues. It is best to place the asynchronous diode and output inductor close to the LC5830K to minimize the size of the SW polygon.

5) Keep sensitive analog signals (CS, and R1/fig19 of switching frequency setting) away from the SW polygon.

6) For accurate current sensing, the LED current sense resistor R_{SENSE}(R2 – R5/fig19) should be placed close to the IC.

7) Place the boot strap capacitor C4(fig19) near the BOOT node (pin 7) and keep the routing to this capacitor short.

8) When routing the input and output capacitors (C1, C2, and C7/fig19 if used), use multiple vias to the ground plane and place the vias as close as possible to the LC5830K pads.

9) To minimize PCB losses and improve system efficiency, the input (VIN) and output (V_{OUT}) traces should be wide and duplicated on multiple layers, if possible.

10) To improve thermal performance, use multiple layers for GND. Place as many vias as possible to the ground plane around the anode of the asynchronous diode.

11) The thermal pad under the LC5830K must connect to the ground plane using multiple vias. More vias will insure lower operating temperature and higher efficiency.

9.3 Optimizing Thermal Layout

The features of the printed circuit board, including heat conduction and adjacent thermal sources such as other components, have a very significant effect on the thermal performance of the device.

To optimize thermal performance, the following should be taken into account:

- The device exposed thermal pad should be connected to as much copper area as is available.
- Copper thickness should be as high as possible (for example, 2 oz. or greater for higher power applications).
- The greater the quantity of thermal vias, the better the dissipation. If the expense of vias is a concern, studies have shown that concentrating the vias directly under the device in a tight pattern, as shown in fig21, has the greatest effect.
- Additional exposed copper area on the opposite side of the board should be connected by means of the thermal vias. The copper should cover as much area as possible.
- Other thermal sources should be placed as remote from the device as possible
- Place as many vias as possible to the ground plane around the anode of the asynchronous diode.

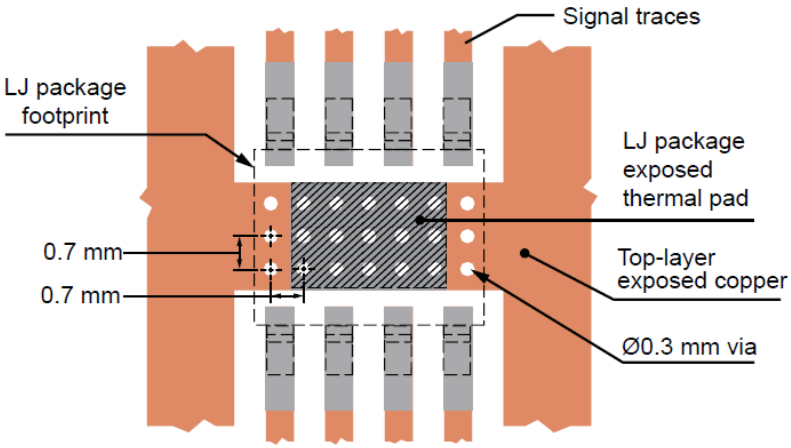


fig.21 Suggested PCB layout for thermal optimization(maximum available bottom-layer copper recommended)

10. Typical characteristics (Ta=25°C)

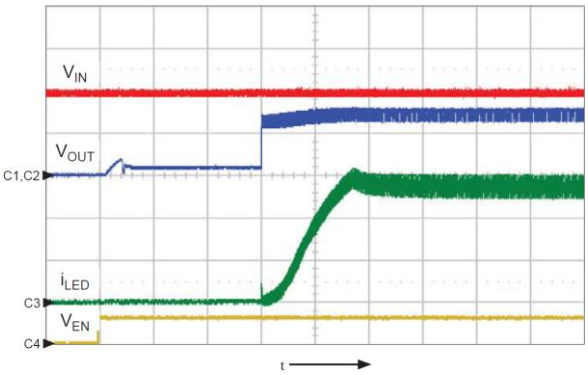


fig.22A Startup waveforms V_{IN} = 19V

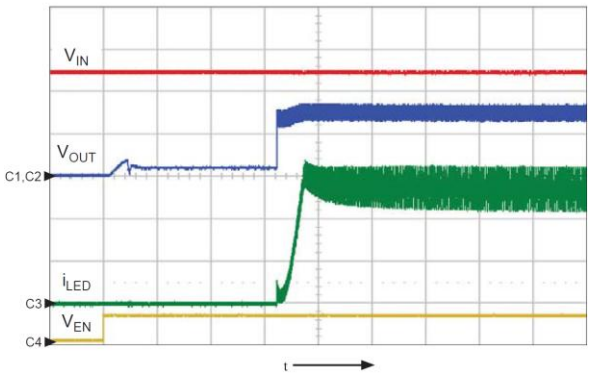


fig.22B Startup waveforms V_{IN} = 24V

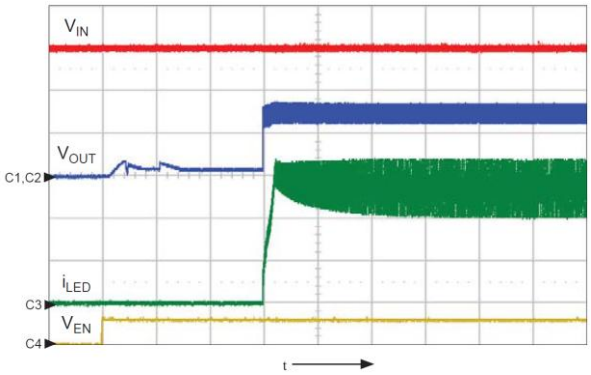


fig.22C Startup waveforms V_{IN} = 30V

*Operating condition : LEDstring voltage = 15V,
LED current = 1.3A, R_1 = 63.4kΩ
(Switching frequency = 1MHz)、
V_{IN} = 19V(fig.22A)、
V_{IN} = 24V(fig.22B)、
V_{IN} = 30V(fig.22C)
Oscilloscope settings:
CH1 (Red) = VIN (10 V/div),
CH2 (Blue) = VOUT (10 V/div),
CH3 (Green) = iLED (500mA/div),
CH4 (Yellow) = Enable (5 V/div),
Time : 50 µs/div

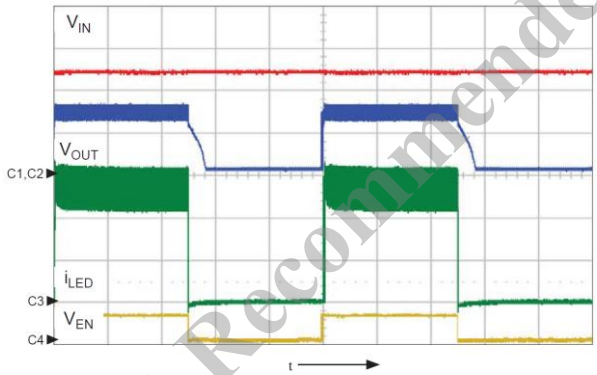


fig.23A PWM dimming waveforms Duty=50%

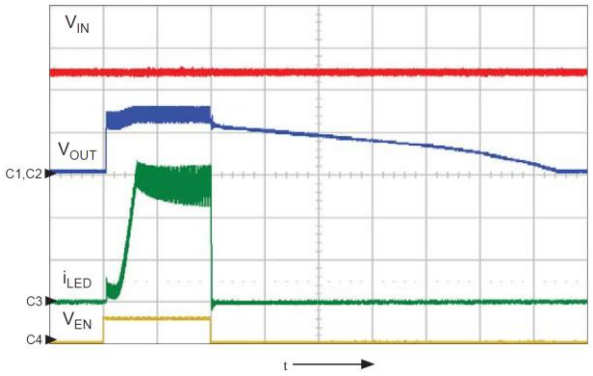


fig.23B PWM dimming waveforms Duty=2%

*Operating condition : 200Hz, V_{IN} = 24 V, V_{OUT} = 15 V, R1 = 63.4 kΩ, duty cycle = 50%
fig23A Duty=50%, fig.23B Duty=2%

Oscilloscope settings:
CH1 (Red) = VIN (10 V/div),
CH2 (Blue) = VOUT (10 V/div),
CH3 (Green) = iLED (500 mA/div),
CH4 (Yellow) = Enable (5 V/div),
Time : 1 ms/div (fig.23A)
50 µs/div (fig.23B)
fig23A,fig23B PWM operation at various duty cycles; note that there is no startup delay during PWM dimming operation
*C3, C6, C7, R6 : Open

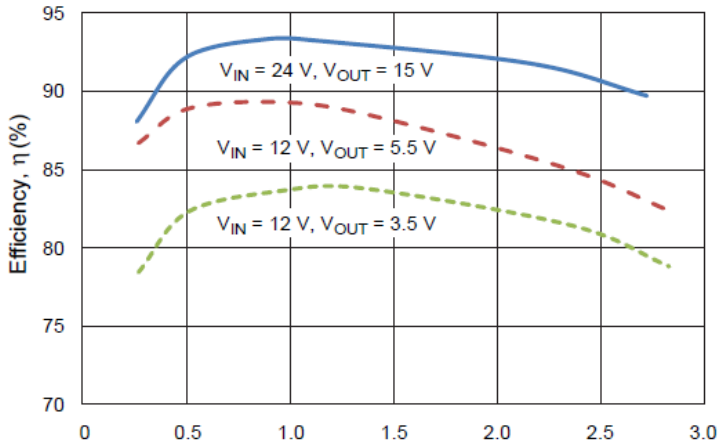


fig.24 Efficiency versus LED Current at various LED voltages Operating conditions:fsw=1MHz

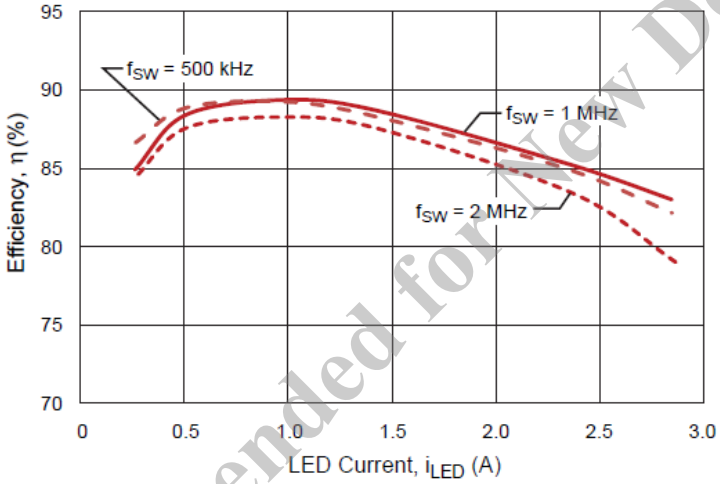


fig.25 Efficiency versus LED Current at various switching frequenciesOperating conditions: VIN = 12 V, VOUT = 5.5 V

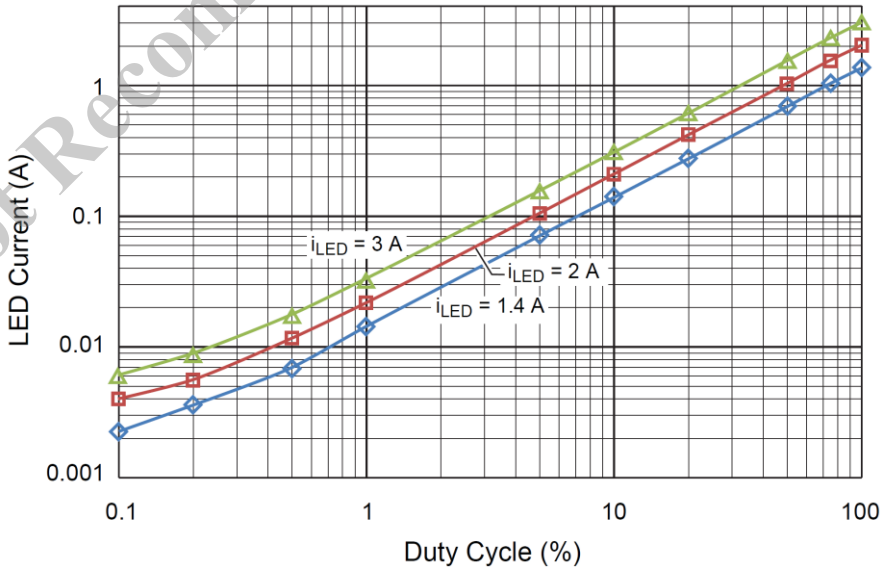


fig.26 Average LED Current versus PWM dimming percentage
Operating conditions: VIN = 12 V, VOUT = 3.5 V, fSW = 1 MHz, fPWM = 200 Hz, L = 10 µH

11. The contents of packing specification.

1) Reel packing figure (Refer to fig25)

   Emboss tape + Reel

2) Inner packing figure

   The material of packing : cardboard

   The number of parts : 3000pcs / reel

3) Outer packing figure

   The material of packing : cardboard

   The number of inner boxes : 1-9 inner boxes / box

4) Outer box

   The material of packing : cardboard

   The number of inner boxes: 3,6 or 9inner boxes/box

5) Remarks

   *It is processed so that the vibration and the shock at the time of transportation and handling of freight may be borne enough and damage may not be done to a product.

   * Be protected to the dust under transportation or storage.

6) Packing list

   *Packing list is appended to the outside of each outer box.

   Contents: Parts number, Order number, Parts name, Quantity

   *Lot number is specified on the product.

11.1 Reel drawing

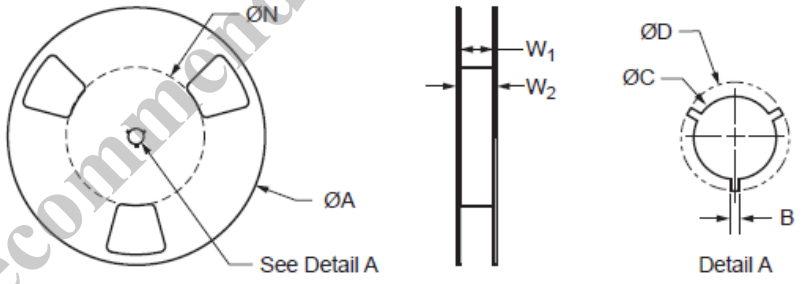


Table.5 Dimmensions of Reel(Units：mm)

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	$13^{+0.5}_{-0.2}$	20.2 (Min)	102 (Nom)
W_1 (inside, at Hub)			12.4 (Min)		
W_2 (outside, at Hub)			18.4 (Max)		

Reference EIA 481

fig.27 Reel Drawing

11.2 Emboss tape drawing

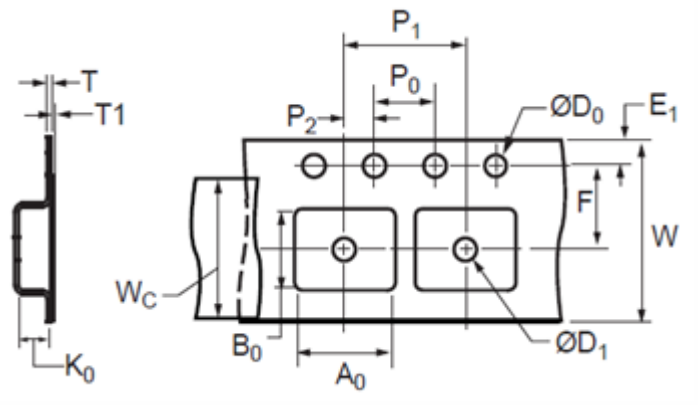


Table.6 Dimmension of Emboss tape

Dimensions in mm

Carrier Tape			Cover Tape
W: 12.00 E_1: 1.75 F: 5.5 T: 0.30	D_0: 1.50 P_0: 4.00 P_1: 8.00 P_2: 2.00	A_0: 6.70 B_0: 5.40 K_0: 2.10 D_1: 1.5	W_C: 9.3 T_1: 0.061

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3 mm above bottom of pocket.
3. Reference EIA 481.

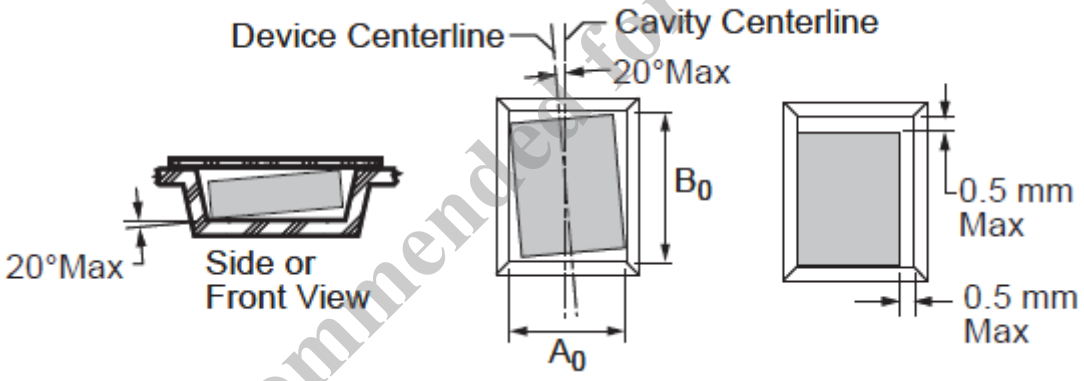


fig.28 Emboss tape drawing

11.3 Reel packing drawing

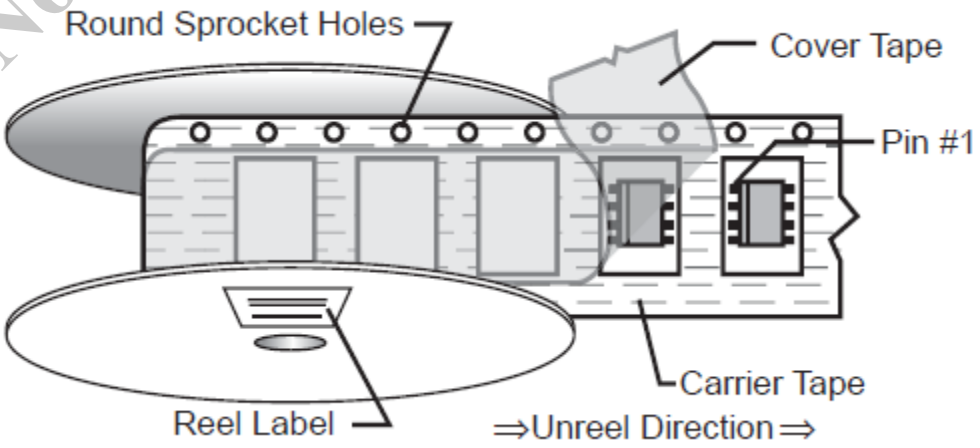


fig.29 Reel packing drawing

Table.7 pin 1 index location

Package	Carrier tape width	Parts per reel	Min Trailer pockets	Min Leader pockets	Cover tape width
eSOIC-8	12 mm	3000	15	50	9.3 mm

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