

Scope

Affected Document	Document Number	Date of Issue
MD6602 Data Sheet	MD6602-DSE Rev.1.0	Aug. 11, 2015

List of Corrections

No.	Location		Description		Errata Rev.
	Page	Chapter	Reads	Should Read	
1	8-10	GPIO	Pin Data Direction for GPIO4 (PDD5)	Pin Data Direction for GPIO5 (PDD5)	1.0a
2	15-3	Watch Dog Timer	Deleted TM_SCAN, TM and OR circuit in Figure 15-2.		1.0a
3	15-3	Watch Dog Timer	Deleted TM and NOT circuit in Figure 15-3.		1.0a
4	16-27	16 bit Timer	TCNTH/L will be cleared at next TNCT cycle when TCNT and COMPB are matched.	TCNTH/L will be cleared at next TCNT cycle when TCNT and COMPB are matched.	1.0a
5	16-27	16 bit Timer	are generated when CMAF and /or CMBF are set/	are generated when CMAF and /or CMBF are set.	1.0a
6	16-27	16 bit Timer	The enable/disable of the interrupt and event are set by TCMRn register.	The enable/disable of the interrupt and event are set by TMCRn register	1.0a
7	12-1	FLASH Memory Control	Added The following explanation. Table 12-1 Feature of FLC Item: Flash memory Description : Times for programming erasure durability : 20000 times		1.0a
8	16-26	16 bit Timer	If TMECSRn.TICCLRS=1b,	If TMECRn.TICCLRS=1b,	1.0a
9	16-24	16 bit Timer	Also the Interrupt output TMINT_N asserts if CMPAIEN and / or CMPBIEN are enable.	Also the Interrupt output TMINT_N asserts if CMAIEN and / or CMBIEN are enable.	1.0a
10	16-26	16 bit Timer	There are two same figures in Figure 16-3	Delete one figure	1.0a
11	32-2	Packaging	Deleted the Thermal size in map of LQFP64.		1.0a
12	13-26	Tiny DSP	Section 13.10.13 DSPn Control Register (DSPnCTRL2) Bit2 LDEN: 0: LDR function and LDD instruction enable 1: LDR function and LDD instruction disable	Section 13.10.13 DSPn Control Register (DSPnCTRL2) Bit2 LDEN: 0: LDR function and LDD instruction disable 1: LDR function and LDD instruction enable	1.0a
13	22-2	12bitADC	(M samples per second)	(million samples per second)	1.0a

Errata Revision History

Revision	Date of Issue
1.0a	May 13, 2016

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DSGN-CEZ-16001