Light Load High Efficiency
Synchronous Rectification Buck Converter IC

NR263S

Data Sheet

Description

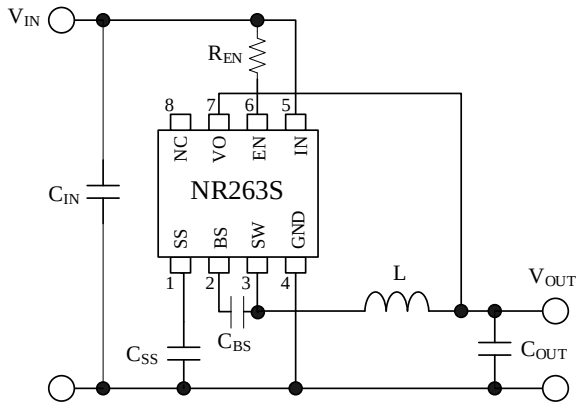
The NR263S is synchronous rectification buck converter IC with built-in power MOSFET. In light load, the IC operates with the pulse skip mode to improve the efficiency. By using the peak current control method, the IC stably operates with a low ESR capacitor such as a ceramic capacitor. The IC has the various protections such as the overcurrent protection, the undervoltage lockout, and the thermal shutdown.

The IC achieves the switching regulator circuit with few components and small mounting area.

Features

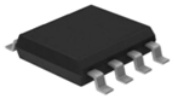
- Synchronous Rectification
- Operation Modes:
  Normal Load: Current Mode PWM Control
  Light Load: Pulse Skip Operation
- Maximum Efficiency (V_{IN} = 12 V, V_{OUT} = 5 V)
  Normal Load: 94%
  Light Load (I_{OUT} = 10 mA): 86%
- Stable with a Low ESR Ceramic Output Capacitor
- Few External Component Counts
  (Fixed Output Voltage of 5 V)
- Soft-start Period Adjustment by External Capacitor
- Enable Function
- Protections:
  Overcurrent Protection (OCP): Drooping Type, Auto-restart
  Thermal Shutdown (TSD): Auto-restart
  Undervoltage Lockout (UVLO)
  Output Short Circuit Protection: Burst Oscillation Operation (Hiccup)

Typical Application



Package

SOP8



Not to scale

Specifications

- Input Voltage, V_{IN}: 8.0 V to 31 V
- Fixed Output Voltage, V_{OUT}: 5 V
- Output Current, I_{OUT}: 1 A
- Fixed Operating Frequency: 500 kHz

Applications

- White Goods
- Audio Visual Equipment
- Office Automation Equipment
- Other Switched Mode Power Supply (SMPS)

Contents

Description ---- 1
Contents ---- 2
1. Absolute Maximum Ratings ---- 3
2. Recommended Operating Conditions ---- 3
3. Electrical Characteristics ---- 4
4. Block Diagram ---- 5
5. Pin Configuration Definitions ---- 5
6. Typical Application ---- 6
7. Physical Dimensions ---- 7
8. Marking Diagram ---- 8
9. Operational Descriptions ---- 8
9.1 PWM Output Control ---- 9
9.2 Enable Function ---- 9
9.3 Soft-start Function ---- 9
9.4 Thermal Shutdown ---- 10
9.5 Overcurrent Protection and Output Short Circuit Protection ---- 11
9.6 Pulse Skip Mode ---- 12
10. Design Notes ---- 13
10.1 Thermal Derating ---- 13
10.2 External Components ---- 13
10.2.1 Inductor ---- 13
10.2.2 Input/Output Capacitor ---- 14
10.3 Spike Noise Reduction Methods ---- 15
10.4 For Applications Where Output Voltage Is Higher than Input Voltage ---- 15
10.5 For Applications Inserting/Removing Load Wire in Power Supply Operation ---- 15
10.6 PCB Layout ---- 16
10.7 Using Bead-core ---- 16
11. Pattern Layout Example ---- 17
12. Typical Characteristics ---- 19
Important Notes ---- 21

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Ratings	Unit
Input Voltage	V_{IN}		−0.3 to 35	V
BS Pin Voltage	V_{BS}		−0.3 to 40.5	V
Voltage between BS and SW Pins	V_{BS-SW}	DC	−0.3 to 5.5	V
		Pulse width ≤10 ns	8	V
SW Pin Voltage	V_{SW}	DC	−1 to 35	V
		Pulse width ≤100 ns	−2 to 35	
		Pulse width ≤10 ns	−6 to 35	
VO Pin Voltage	V_O		−0.3 to 6	V
EN Pin Voltage	V_{EN}		−0.3 to 35	V
SS Pin Voltage	V_{SS}		−0.3 to 7.0	V
SS Pin Sink Current	I_{SSB}		5.0	mA
Power Dissipation(1)	P_D	Mounted on the board (see Section 11), T_J = 150 °C	1.56	W
Junction Temperature(2)	T_J		−40 to 150	°C
Storage Temperature	T_{stg}		−40 to 150	°C
Junction-to-Lead(3) Thermal Resistance	θ_{J-L}		60	°C/W
Junction-to-Ambient Thermal Resistance	θ_{J-A}	Mounted on the board (see Section 11)	80	°C/W

(1) Limited by thermal shutdown.
(2) The temperature detection of thermal shutdown is about 165 °C.
(3) The lead temperature is measured at pin 4.

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input Voltage	V_{IN}		8	31	V
Output Current*	I_{OUT}	L = 6.8 µH	0	1.0	A
Operating Ambient Temperature*	T_A		−40	85	°C
Operating Junction Temperature*	T_J		−40	125	°C

* Must be used in the range of thermal derating (see Section 10.1).

3. Electrical Characteristics

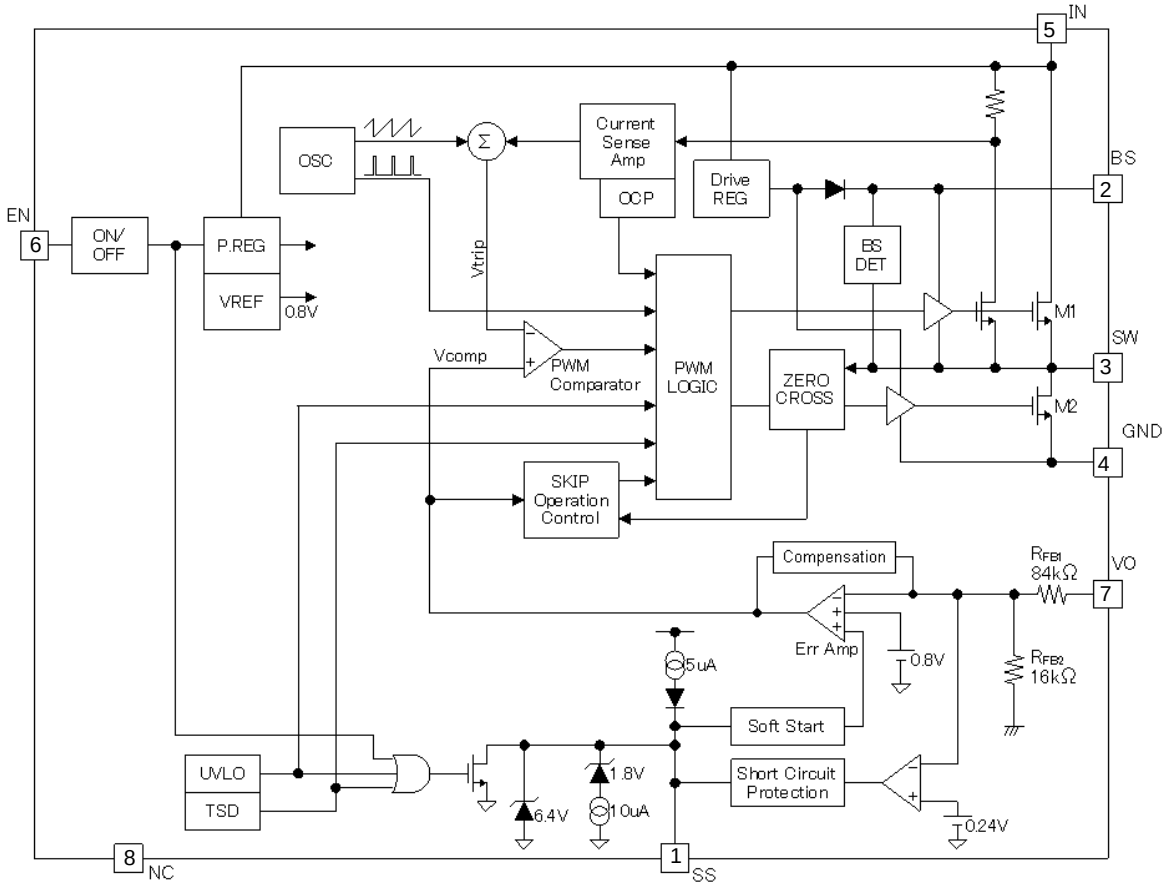
Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C.

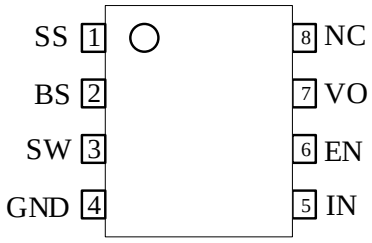
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Output Voltage	V_{OUT}	V_{IN} = 12 V, I_{OUT} = 0.5 A	4.85	5.00	5.15	V
Output Voltage Temperature Coefficient	$\Delta V_{OUT}/\Delta T$	V_{IN} = 12 V, I_{OUT} = 0.5 A, −40 °C to 85 °C	—	±0.3	—	mV/°C
Operating Frequency	f_O	V_{IN} = 12 V, V_{OUT} = 5.0 V, I_{OUT} = 0.5 A	−30%	500	30%	kHz
Line Regulation*	V_{LINE}	V_{IN} = 8 V to 31 V, V_{OUT} = 5.0 V, I_{OUT} = 0.5 A	—	50	—	mV
Load Regulation*	V_{LOAD}	V_{IN} = 12 V, V_{OUT} = 5.0 V I_{OUT} = 0.1 A to 1.0 A	—	50	—	mV
Overcurrent Protection Start Current	I_S	V_{IN} = 12 V, V_{OUT} = 5.0 V	−2.6	−1.5	−1.1	A
Operating Circuit Current	I_{IN}	V_{IN} = 12 V, V_{EN} = 12 V, I_O = 0 mA	—	250	—	µA
Quiescent Circuit Current	$I_{IN(OFF)}$	V_{IN} = 12 V,V_{EN} = 0 V	—	1.2	10	µA
UVLO Threshold Voltage	V_{UVLO}	V_{IN} increases	5	6	7	V
UVLO Hysteresis Voltage	V_{UVLO_HYS}	UVLO on to UVLO off	—	0.55	—	V
SS Pin Capacitor Charge Current	I_{SS}	V_{SS} = 0 V, V_{IN} = 12 V	−8.5	−5.0	−2.5	µA
EN Pin Sink Current	I_{EN}	V_{EN} = 12 V, V_{IN} = 12 V	—	14	30	µA
EN Pin On Threshold Voltage	V_{EN}	V_{IN} =12 V	0.8	1.1	2.1	V
EN Pin Hysteresis Voltage	V_{EN_HYS}	V_{IN} =12 V	—	0.15	—	V
Maximum Duty Cycle*	D_{MAX}	V_{IN} = 12 V	—	85	—	%
Minimum On-time*	$t_{ON(MIN)}$	V_{IN} = 12 V	—	200	—	ns
Thermal Shutdown Operation Temperature *	T_{SD}	V_{IN} = 12 V	151	165	—	°C
Thermal Shutdown Restart Hysteresis*	T_{SD_HYS}	V_{IN} = 12 V	—	15	—	°C
High-side Power MOSFET On-resistance*	R_{ONH}	V_{IN} = 12 V	—	250	—	mΩ
Low-side Power MOSFET On-resistance*	R_{ONL}	V_{IN} = 12 V	—	200	—	mΩ

* Guaranteed by design.

4. Block Diagram



5. Pin Configuration Definitions



Pin Number	Pin Name	Description
1	SS	Soft-start period setting pin. Capacitor for soft-start period setting is connected between the SS and GND pins.
2	BS	Power supply pin for the high-side MOSFET drive circuit. Connect a capacitor between the SW and BS pins.
3	SW	Output pin. The LC filter for the output is connected to the SW pin.
4	GND	Ground
5	IN	Power supply input pin of the IC
6	EN	Enable signal input pin. When the EN pin input is high level, the regulator is enabled. When it is low level, the regulator is disabled.
7	VO	Feedback pin, which compares the reference voltage (5 V) with output voltage. The VO pin is directly connected to the output voltage.
8	NC	No connection

6. Typical Application

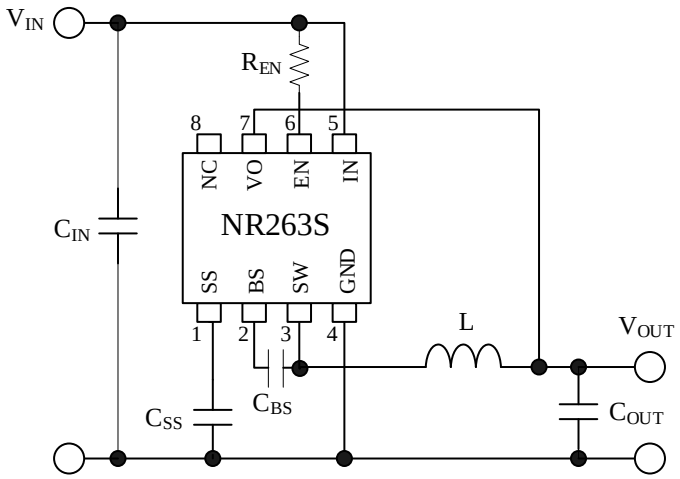


Figure 6-1. Typical Application

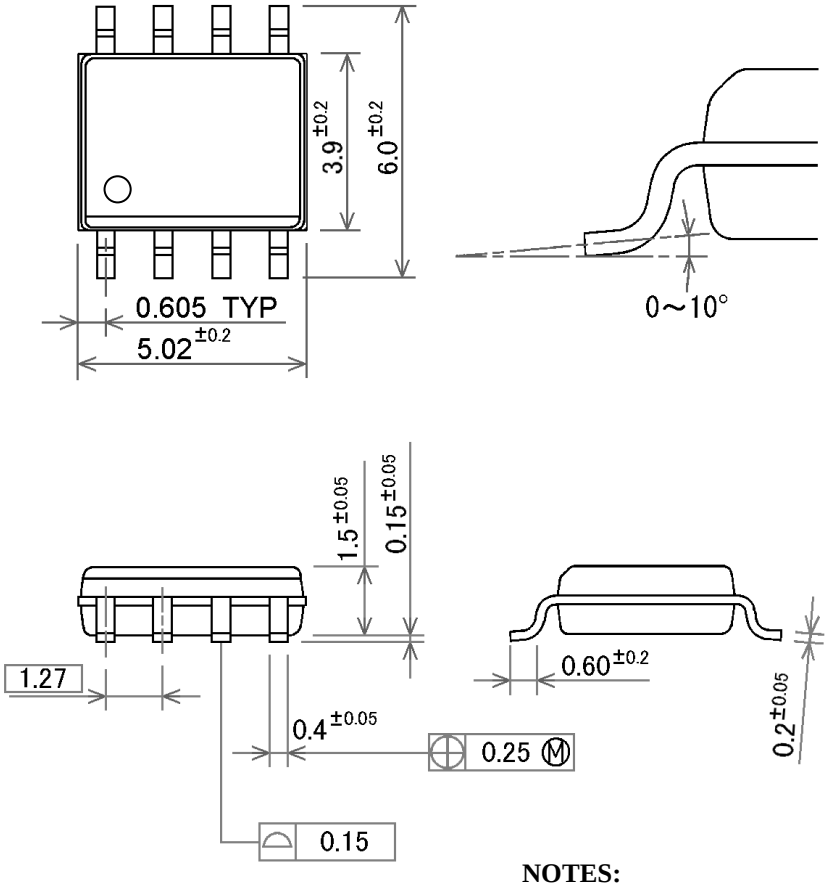
Table 6-1. Reference Value (V_{IN} = 12 V)

Symbol	Reference Value
C_{IN}	10 µF, 25 V
C_{OUT}	22 µF, 16 V
C_{BS}	0.1 µF
C_{SS}	0.1 µF
L	6.8 µH*
R_{EN}	100 kΩ

* Minimum value of inductor when the control duty cycle is set less than 0.5. When ΔI_L is decreased, the required inductance is increased.

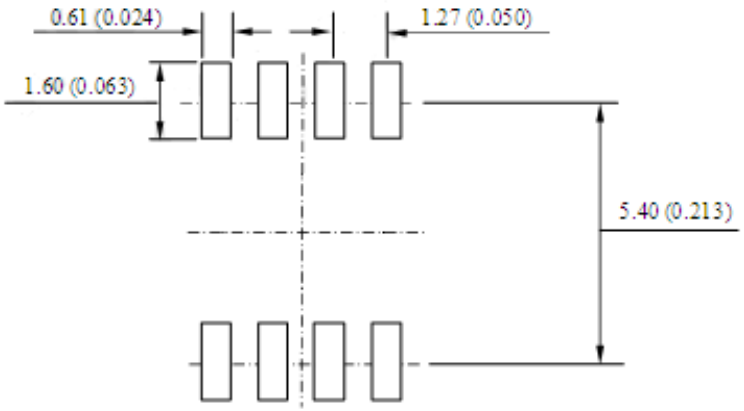
7. Physical Dimensions

● **SOP8 Package**

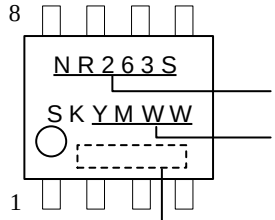


NOTES:
- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)

● **SOP8 Land Pattern Example**



8. Marking Diagram



Part Number

Lot Number:

Y is the last digit of the year of manufacture (0 to 9)

M is the month of the year (1 to 9, O, N, or D)

D is the period of days represented by:

1: the first 10 days of the month (1st to 10th)

2: the second 10 days of the month (11th to 20th)

3: the last 10–11 days of the month (21st to 31st)

Control Number

9. Operational Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

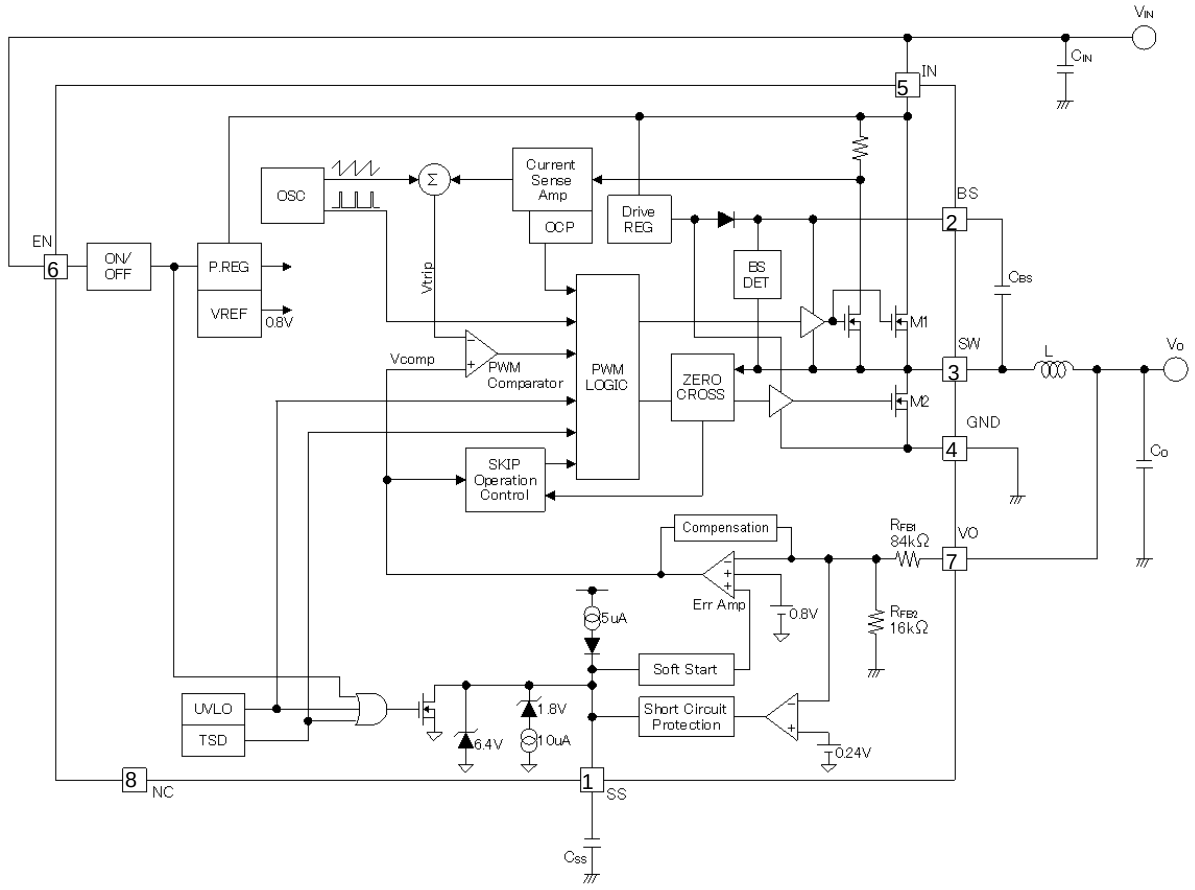


Figure 9-1. Basic Structure of Buck Regulator with PWM Control by Current Mode Control

9.1 PWM Output Control

The PWM control circuit of the IC consists of the current detection amplifier, the error amplifier, the PWM comparator, and the slope superimposed circuit. The duty cycle is controlled by comparing with V_{TRIP} and V_{COMP} in the PWM comparator. V_{TRIP} is the drain current feedback signal detected by the current detection amplifier. V_{COMP} is the error amplification signal generated by the error amplifier with the output voltage and the reference voltage.

The slope superimposed circuit is for avoiding the sub-harmonic oscillation that is generated at the duty cycle of 50% or more. The slope signal is superimposed to the feedback signal, V_{TRIP}.

C_{BS} in Figure 9-1 is the boost capacitor that is a power supply for driving the high-side circuit in the IC and the high-side switch (M1). The power is supplied to the output by the high-side MOSFET (M1) and the low-side MOSFET (M2).

When the IN pin voltage becomes the UVLO Threshold Voltage, V_{UVLO} = 6 V, or more, and the EN pin voltage increases threshold voltage or more, the SS pin voltage increases. M2 is turned on to change C_{BS} before the SS pin voltage reaches 0.6 V. After that, when the SS pin voltage increases 0.6 V or more, the IC starts the switching operation. M1 and M2 repeat on and off alternately. When M1 is turned on, the current of inductor, L, is increased, and the output of current detection amplifier is also increased. In the PWM comparator, when V_{TRIP} exceeds V_{COMP}, the IC turns off M1 and turns on M2. The regenerative current of inductor flows via M2 from the GND pin. After that, M1 is turned on again when receiving a set signal from the oscillator, OSC.

9.2 Enable Function

Figure 9-2 shows the EN pin peripheral circuit. The signal is input to the EN pin using switching transistors. When both of the following conditions are satisfied, the regulator is enabled and starts the switching operation: the IN pin voltage increases to UVLO Threshold Voltage, V_{UVLO} = 6 V, or more, and the EN pin voltage increases to the On Threshold Voltage, V_{EN} = 1.1 V, or more. When the EN pin voltage decreases to $V_{EN} - V_{EN\_HYS}$ or less, the regulator is disabled, and stops the switching operation even if the IN pin voltage is V_{UVLO} or more. When not using the enable function, the EN pin is pulled up to the IN pin as shown in Figure 9-3. The value of the pull-up resistor, R_{EN}, is about 100 kΩ.

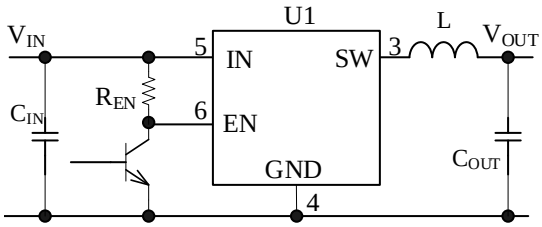


Figure 9-2. EN Pin Peripheral Circuit

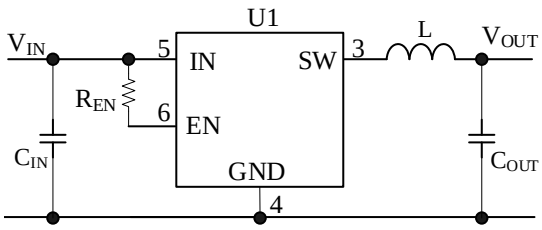


Figure 9-3. EN Pin Peripheral Circuit
(Not Using Enable Function)

9.3 Soft-start Function

Figure 9-4 and Figure 9-5 show the soft-start operational waveform without the enable function and with the enable function, respectively. The soft-start period is set by the value of capacitor, C_{SS}, connected between the SS and GND pins. The output voltage, V_{OUT}, increases according to the SS pin voltage. C_{SS} is charged by the constant current supplied from the SS pin, I_{SS} = −5.0 μA. Thus, the SS pin voltage, V_{SS}, increases linearly. During the soft-start period, the IC controls the output rising period by controlling the off period of PWM signal. The delay time, i.e., from enabling the IC to starting the output voltage rising, is defined as t_{DELAY}. The soft-start period, t_{SS}, of the output voltage is the range of V_{SS} = 0.6 V to 1.4 V.

The approximate values of t_{DELAY} and t_{SS} are calculated by the following equations.

$$t_{DELAY} = \frac{0.6 \times C_{SS}}{|I_{SS}|} \quad (1)$$

$$t_{SS} = \frac{0.8 \times C_{SS}}{|I_{SS}|} \quad (2)$$

Where, I_{SS} is charge current of the capacitor connected to the SS pin (−5.0 μA).

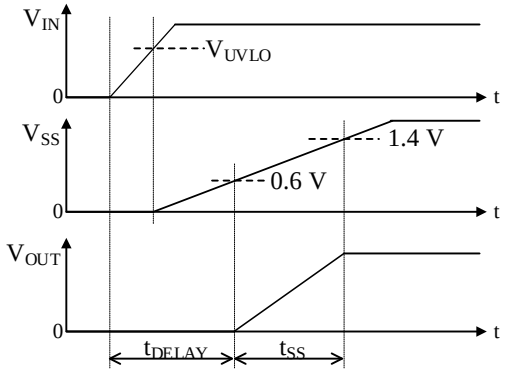


Figure 9-4. Soft-start Operational Waveform
(Not Using Enable Function)

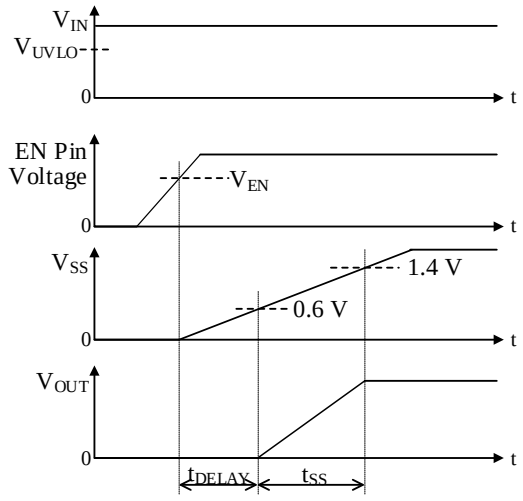


Figure 9-5. Soft-start Operational Waveform
(Using Enable Function)

Be sure to confirm the output rising waveform with the actual operation, and adjust the soft-start period. If t_{SS} is too short, the soft-start period ends before the constant voltage control follows, and the output voltage may overshoot excessively (see Figure 9-6). If t_{SS} is long, the overshoot is reduced, but the startup period becomes long.

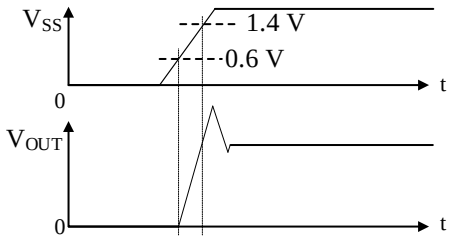


Figure 9-6. Soft-start Operational Waveform
(Soft-start Period is Too Short)

When the IC is restarted with the high SS pin voltage (e.g., input voltage variation, high-speed switching of the EN pin signal), a forced discharge circuit in the IC operates. Then, the SS pin voltage is decreased to 0.6 V by the forced discharge circuit. After that, the soft-start operation is started (see Figure 9-7). The value of internal impedance at discharging is about 600 Ω.

When the IC is restarted with the high SS pin voltage, V_{SS}, the required period until the output voltage becomes constant after the period on-signal is input to the EN pin is t_{DIS} + t_{SS}. For applications that perform consecutive on/off operation, this forced discharge period also must be taken into account.

In steady operation, V_{SS}, i.e., the voltage across C_{SS}, increases to the internal regulator voltage (1.8 V). When discharging C_{SS} from 1.8 V, V_{SS} in arbitrary time, t, is calculated by Equation (3). The period until V_{SS} decreases to 0.6 V, t_{DIS}, is calculated by Equation (4).

$$V_{SS} = 1.8\ \text{V} \times \text{EXP}\left(\frac{-t \times 600}{C_{SS}}\right) \quad (3)$$

$$t_{DIS} = -C_{SS} \times 600 \times \ln\left(\frac{0.6}{1.8}\right) \quad (4)$$

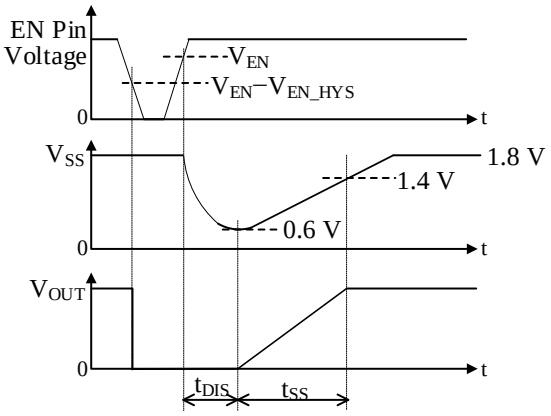


Figure 9-7. C_{SS} Forced Discharge and Soft-start Operational Waveform
(Using Enable Function)

9.4 Thermal Shutdown

When the junction temperature of the IC increases to the Thermal Shutdown Operation Temperature, T_{SD} = 165 °C, or more, the thermal shutdown (TSD) operates, and the IC stops the oscillation. TSD has the Thermal Shutdown Restart Hysteresis, T_{SD_HYS} = 15 °C. When the IC temperature decreases to $T_{SD} - T_{SD\_HYS}$ or less, the IC returns the normal operation automatically.

The purpose of TSD is to protect the IC when the loss of the IC increases due to the abnormal conditions such as an instantaneous short-circuit of the SW pin. TSD

does not guarantee the operation including the IC reliability in the short-circuit state for long period or the state where the heat generation continues.

9.5 Overcurrent Protection and Output Short Circuit Protection

The IC has the overcurrent protection (OCP) circuit with drooping characteristics as shown in Figure 9-8. The OCP circuit detects the peak current flowing to the power MOSFET in the IC by pulse-by-pulse. When this peak current exceeds the OCP threshold value, on-period of the power MOSFET is forcibly terminated. Thus, the output voltage is decreased, and the output current is limited.

As shown in Figure 9-9, when the VO pin voltage decreases from the setting value of 5 V, and reaches 3.50 V (70%), the IC transits to the switching frequency reduction mode. This improves the drooping characteristics.

Moreover, when the VO pin voltage decreases to 1.50 V (30%), the IC charges the soft-start capacitor, C_{SS} of the SS pin by I_{SS} = −5.0 µA. When the SS pin voltage, V_{SS}, increases to 2.2 V or more, the output short circuit protection is started. When the output short circuit protection is started, the IC discharges C_{SS} by current of 2.5 µA, and stops the switching operation until V_{SS} decreases to 0.23 V. When V_{SS} decreases to 0.23 V, the soft-start operation is restarted.

As described above, while the output short circuit protection is operated, intermittent operation (hiccup) is repeated. This intermittent operation reduces the stress of parts such as heat generation. When the overcurrent state is released, the output voltage returns automatically.

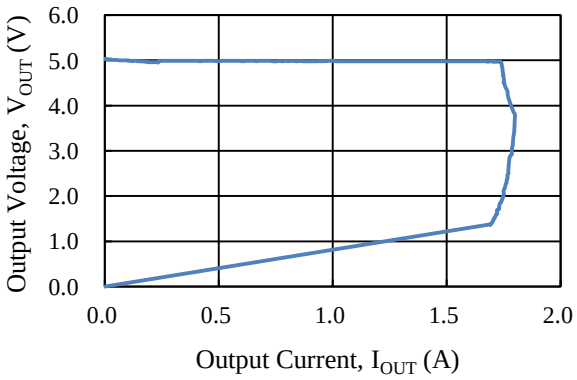


Figure 9-8. Overcurrent Protection Characteristic Example (V_{IN} = 12 V)

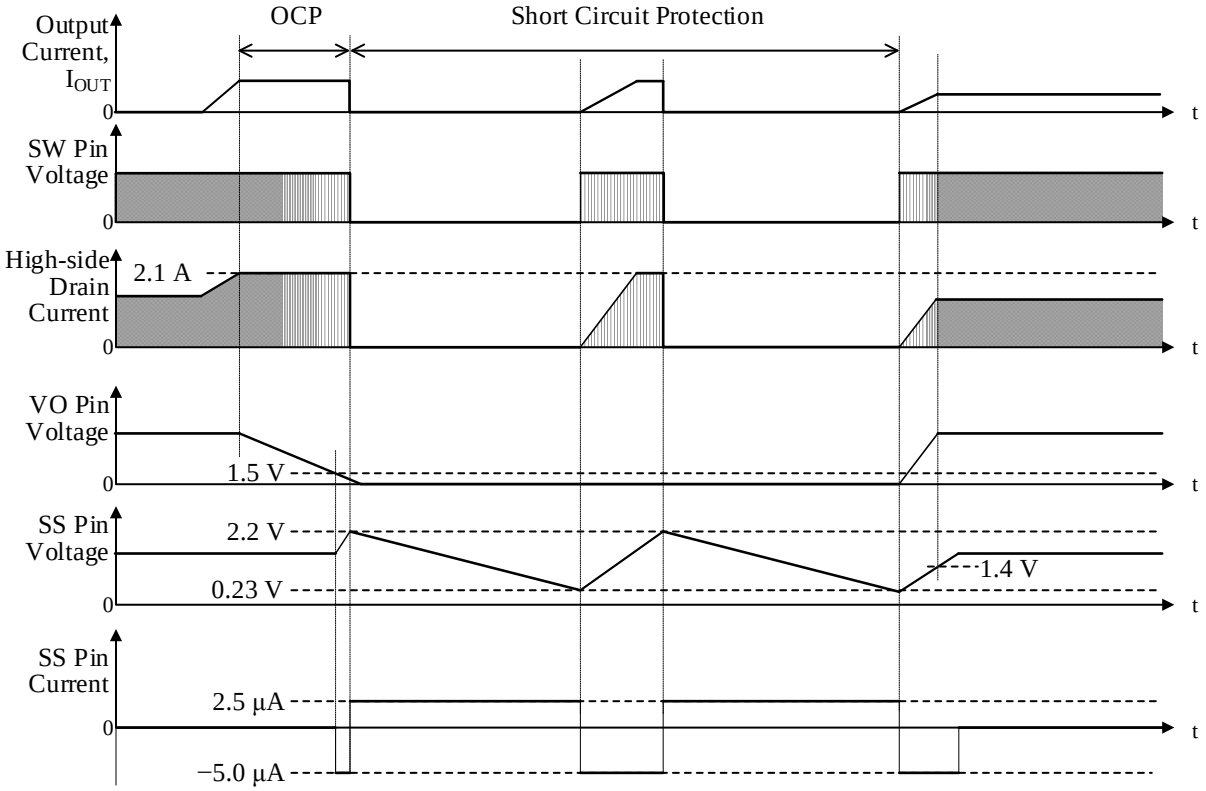


Figure 9-9. Operational Waveforms of Overcurrent Protection and Output Short Circuit Protection

9.6 Pulse Skip Mode

The IC has the pulse skip mode to improve the efficiency in light load. The pulse skip mode cannot be disabled by the external signal.

When the load current decreases, the IC controls so as to decrease the output voltage of error amplifier, V_{COMP} (see Section 4). V_{COMP} cannot be checked directly from the outside of the IC. When the state where V_{COMP} is low continues for a certain period, the IC switches the pulse skip mode. In the pulse skip mode, the drain current peak value that flows the high-side MOSFET in the IC, I_{LP}, is limited to the constant value. This limit value is determined by the input voltage, V_{IN}, and the inductance of the used inductor, L. The pulse skip frequency is varied according to the load. When the state where V_{COMP} is increased continues for a certain period by increasing the load current, the IC returns to the normal PWM operation.

Thus, the switching losses of high-side and low-side MOSFETs in the IC are reduced by decreasing the pulse skip frequency in light load.

When the pulse skip frequency decreases to the audible frequency (20 kHz or less), note that the audible noise may be generated in the actual operation. In this case, adjust the inductor value with reference to Equation (5).

The approximate pulse skip frequency, f_{SKIP}, is calculated by Equation (5).

$$f_{SKIP} \approx \frac{2 \times I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{{I_{LP}}^2 \times L \times V_{IN}} \quad (5)$$

Where:

I_{OUT} is the output current (A),

V_{OUT} is the output voltage (fixed to 5 V internally),

V_{IN} is the input voltage,

L is the inductance, and

I_{LP} is the high-side drain current peak value in pulse skip operation (Since I_{LP} depends on the input voltage, read the value of I_{LP} from Figure 9-10, and substitute it. The values in Figure 9-10 are reference, and are not guaranteed under the conditions requiring accuracy.)

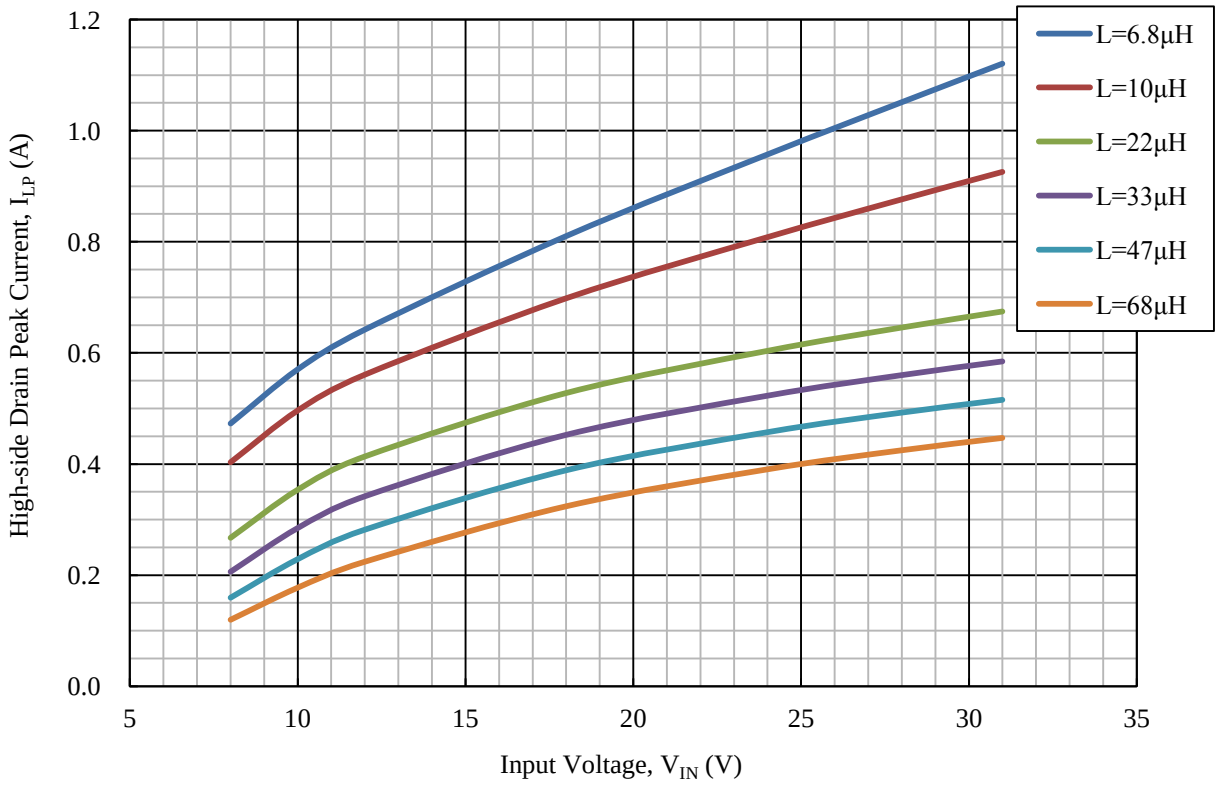


Figure 9-10. I_{LP} Input Dependence (Reference Value)

10. Design Notes

10.1 Thermal Derating

Figure 10-1 shows the IC derating when mounting on the board described in Section 11. When using the IC, ensure enough margins.

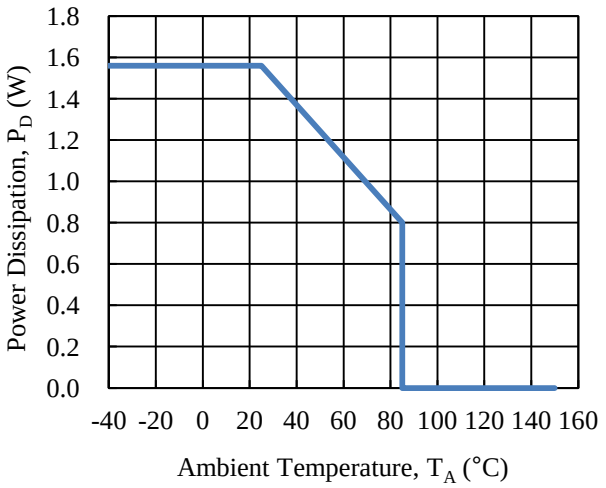


Figure 10-1. Thermal Derating Curve

The IC loss is calculated by Equation (6). Since the efficiency, ηx, is varied depending on the input and output voltages, substitute the appropriate value according to the power supply specifications (see Figure 12-1).

$$P_D = V_{OUT} \times I_{OUT} \left(\frac{100}{\eta x} - 1 \right) \quad (6)$$

Where:
V_{OUT} is the output voltage,
V_{IN} is the input voltage,
I_{OUT} is the output current, and
ηx is the efficiency (%).

10.2 External Components

Each part suitable for the usage condition should be used.

10.2.1 Inductor

For the regulator stable operation, it is required to avoid saturating the inductor and self-heating excessively. When choosing an inductor, care should be taken for the following contents.

- **Inductor Type**

Be sure to choose an inductor for a switching regulator. Using an inductor for noise filter is prohibited because the loss is large. For suppressing the noise effect to the peripheral circuit, it is recommended to use the inductor that a low leakage flux core (structure) is used. In the open magnetic circuit core such as drum type, the peripheral circuit may be damaged by noise because the magnetic flux passes outside the coil. For details, contact inductor manufacturer.

- **DC Superimposed Characteristic**

The inductance has the DC superimposed characteristic (i.e., the characteristic the inductance decreases as DC increases). Be sure to check the maximum value of the actual flowing current whether the inductance is significantly decreased from the design value. The saturation point and the DC superimposed characteristic should be confirmed after obtaining the characteristics of the inductor to be used from the inductor manufacturer.

For example, when the maximum load is I_{OUT} = 1 A, a coil with a saturation point of 0.5 A cannot be used. Moreover, care should be taken when the inductor characteristic with the inductance of 10 µH at no load is 5 µH at 1 A.

- **Inductor Temperature**

Self-heating of an inductor depends on the DC resistance, DCR, of the winding. Reducing the winding diameter increases the DC resistance (DCR) and causes the inductor temperature rising. Generally, there are the following limitations depending on the inductor type:

– Automotive grade product: 150 °C
– Highly reliable product: 125 °C
– General product: 85 °C to 100 °C

The inductor temperature is varied according to the heat dissipation conditions. Be sure to check the inductor temperature including self-heating and temperature rise by heat generation of surrounding parts. Appropriate inductor should be selected taking into account the usage conditions, mounting conditions, and heat dissipation conditions.

- **$\Delta I_L/I_{OUT}$ Setting**

When $\Delta I_L/I_{OUT}$, which is the ratio of the inductor ripple current (ΔI_L) and the output current (I_{OUT}), are large, the inductance decreases, but the output ripple voltage increases. Decreasing $\Delta I_L/I_{OUT}$ increases the inductance, and also increases the inductor size. In general, the value of $\Delta I_L/I_{OUT}$ is set to about 0.2 to 0.3.

● **Inductance Calculation**

The IC adopts the peak detection current control method. In this method, the problem of sub-harmonic oscillation occurs in principle. The sub-harmonic oscillation is a phenomenon that the inductor current fluctuates with a cycle at an integral multiple of the switching frequency. The sub-harmonic oscillation may occur when the duty cycle reaches 0.5 or more in the continuous current mode. In order to avoid the sub-harmonic oscillation, the slope compensation is performed inside the IC. However, since the slope compensation amount is fixed inside the IC, the slope compensation is not performed perfectly for rapid current change. Therefore, the inductance must be set so that the slope of the inductor current is small. As shown in Equation (7) and Equation (8), the inductor ripple current, ΔI_L, and the inductor peak current, I_{LP}, increase as the inductance is small, and the slope of the current waveform also increases.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f_{SW}} \quad (7)$$

$$I_{LP} = \frac{\Delta I_L}{2} + I_{OUT} \quad (8)$$

Where:
V_{IN} is the input voltage,
V_{OUT} is the output voltage (fixed to 5 V internally),
L is the inductance,
f_{SW} is the switching frequency, and
I_{OUT} is the output current (A).

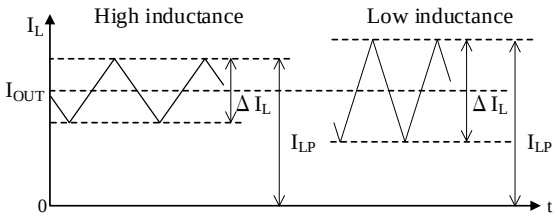


Figure 10-2 Relationship between Inductance and Ripple Current

The inductance is set in the range of Equation (9).

The ripple current, ΔI_L, in Equation (9) must be set according to the duty cycle to avoid the sub-harmonic oscillation (see Table 10-1). The duty cycle is determined by V_{OUT}/V_{IN}, which is the ratio of the output voltage (V_{OUT}) and the input voltage (V_{IN}). Since the output voltage of the IC is 5 V, the duty cycle reaches 0.5 or more when the input voltage is decreased to 10 V or less. The inductance must be set to prevent the inductor from being magnetically saturated even during overload or short-circuit load condition.

$$L \geq \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f_{SW}} \quad (9)$$

Where:
L is the inductance,
V_{IN} is the input voltage,
V_{OUT} is the output voltage (fixed to 5 V internally),
ΔI_L is the ripple current (see Table 10-1), and
f_{SW} is the switching frequency.

Table 10-1. ΔI_L Setting Value

Duty Cycle	Ripple Current, ΔI_L
More than 0.5	Less than 0.2 A
Less than 0.5	More than 0.2 A, less than 1 A

10.2.2 Input/Output Capacitor

To operate the IC stably, the input capacitor, C_{IN}, must be used a ceramic capacitor to decrease the input impedance. In addition, C_{IN} must be placed close to the IC, and be connected to the IN and GND pins with a minimum length of traces. Even when there is a smoothing capacitor for the rectifier circuit placed at the input side of the IC, C_{IN} is required to connect near the IC.

The output capacitor, C_{OUT}, is for smoothing of the switching output. An LC low-pass filter consists of C_{OUT} and inductor. The inductor ripple current, ΔI_L, flows to C_{OUT}. A low ESR ceramic capacitor can be used for C_{OUT}. Conventionally, an electric capacitor with large capacitance is required for the output to compensate the second delay of the LC filter. However, the mounting area can be greatly reduced because the ceramic capacitor for the output can be used in the IC with the current control method.

The ceramic capacitor has the equivalent series resistor, ESR. The output ripple voltage, $V_{ORIPPLE}$, is calculated by the following equation.

$$V_{ORIPPLE} = ESR(C_{OUT}) \times \Delta I_L \quad (10)$$

Where:
$ESR(C_{OUT})$ is the equivalent series resistor of the output capacitor, and
ΔI_L is the inductor ripple current.

When the output ripple voltage is set less than $V_{ORIPPLE}$, the ESR requirements for ceramic capacitors are as follows:

$$ESR(C_{OUT}) < \frac{V_{ORIPPLE}}{\Delta I_L} \quad (11)$$

As shown in Equation (11), when ΔI_L is large, the output ripple voltage, $V_{ORIPPLE}$, becomes relatively large. To decrease ESR, the workaround such as connecting the ceramic capacitors in parallel is required.

For the input capacitor, C_{IN}, and the output capacitor, C_{OUT}, must be selected the appropriate capacitor taking into account enough margins for the usage, mounting, and heat dissipation conditions. Especially, care should be taken for the following contents (for details, contact capacitor manufacturer).

- The breakdown voltage of the capacitor is sufficient for the voltage range to be used.
- Change in capacitance is small in the voltage range to be used.
- Change in capacitance is small in the temperature range to be used.
- The capacitor temperature including a self-heating and an ambient temperature is within the maximum operating temperature range of the capacitor.
  (When the ripple current flows to the ceramic capacitor, the capacitor temperature increases due to ESR.)
- The impedance of the capacitor is sufficiently low under the frequency and temperature conditions to be used.

10.3 Spike Noise Reduction Methods

When measuring spike noises with an oscilloscope, the spike noises may be measured larger than the actual value because the probe ground lead wire behaves as an antenna. To suppress this, connect the ground lead wire of the probe as short as possible, and connect it to the root of the output capacitor.

The spike noise reduction methods are described as follows. Note that the circuit efficiency is decreased in either method.

- **Adding R_{BS}**

To slow down a turn-on switching speed of the internal power MOSFET, add a resistor, R_{BS}, between the BS and SW pins (see Figure 10-3). This reduces the spike noises. R_{BS} should be set 10 Ω or less. If the value of R_{BS} is too high, the startup failure or the damage by under drive state of the power MOSFET may be caused.

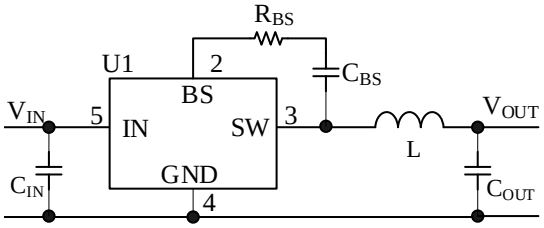


Figure 10-3. Adding Series Resistor

- **Adding Snubber Circuit**

To compensate the output waveform and the diode recovery time, add a resistor and a capacitor (RC snubber) between the SW and GND pins (see Figure 10-4). This reduces the spike noise.

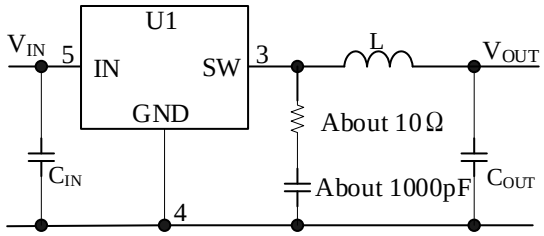


Figure 10-4. Adding Snubber Circuit

10.4 For Applications Where Output Voltage Is Higher than Input Voltage

For the applications where the SW pin voltage is higher than the IN pin voltage (e.g., battery charger), add a diode for reverse bias protection between the IN and SW pins.

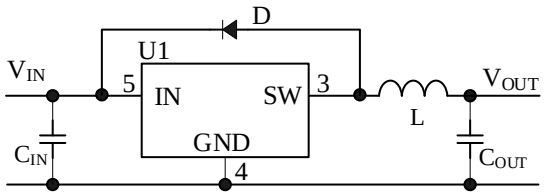


Figure 10-5. Adding Reverse Bias Protection Diode

10.5 For Applications Hot Swapping Load Wire in Power Supply Operation

For applications where active wires such as load line connectors connected to the output circuit are inserted and removed while the switching regulator circuit is operating (i.e., hot swapping), add R_{VO} so that the surge voltage by hot swapping does not exceed the absolute maximum rating (6 V) of the VO pin (see Figure 10-6). R_{VO} reference value is 100 Ω. Note that the output voltage (5 V) increases when adding R_{VO} (e.g., the

output voltage increases by about 5 mV when R_{VO} = 100 Ω).

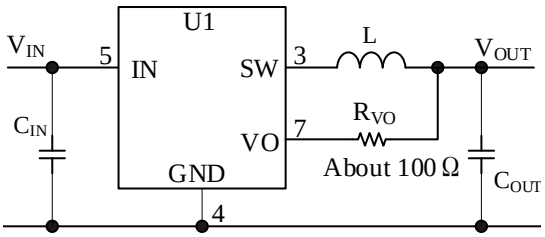


Figure 10-6. Adding VO Pin Thermal Shutdown Resistor, R_{VO}

10.6 PCB Layout

Since a large current flows to the bold line in Figure 10-7, the trace should be wide and short. Also, the control ground must be separated from the ground where the large current flows, and should be connected to the root of the output capacitor at a single point.

Since the ripple current flows to C_{IN} and C_{OUT}, the impedance of the trace between these capacitor electrodes should be small. Therefore, the input capacitor, C_{IN}, and the output capacitor, C_{OUT}, must be placed as close as possible to the IC, and be connected to each pin as short as possible with thick trace (see Figure 10-8).

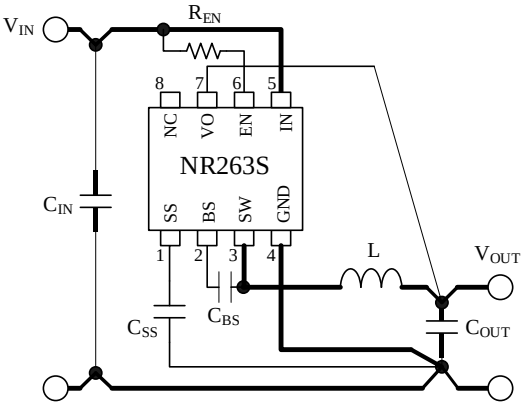


Figure 10-7. Large Current Pattern

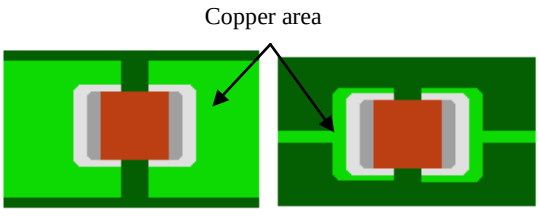


Figure 10-8. Peripheral Layout Example of C_{IN} and C_{OUT}

10.7 Using Bead-core

To operate the IC safety, a parasitic inductance of wiring should be minimized. When inserting the bear-core such as ferrite bead in the shaded area of Figure 10-9, the bead-core inductance is added to the parasitic inductance of traces. The surge voltage generated by the inductance on these traces may cause malfunction of the IC, and in the worst case, critical damage to the IC. Therefore, do not insert the bead-core on the wiring in the shaded area of Figure 10-9.

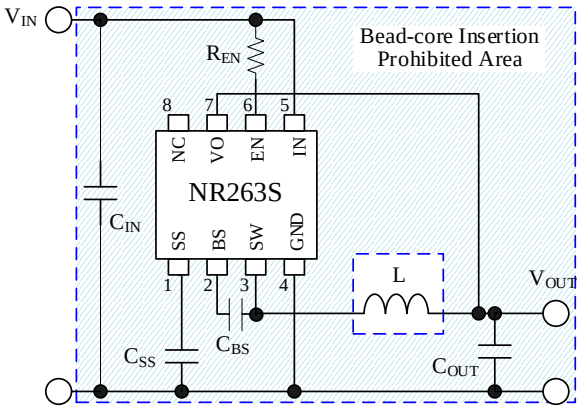
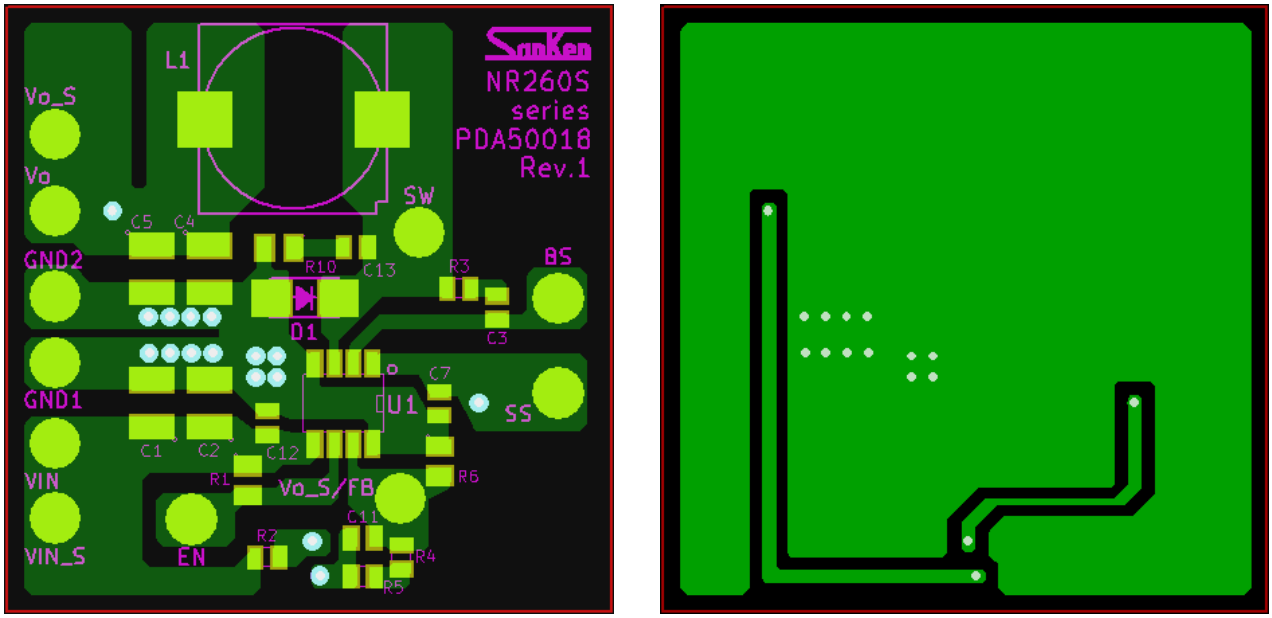


Figure 10-9. Bead-core Insertion Prohibited Area

11. Pattern Layout Example

Size: 40 mm × 40 mm
Thickness of the board: 1.6 mm
Copper thickness: 35 µm



(A) Top View (B) Bottom View

Figure 11-1. Pattern Layout Example

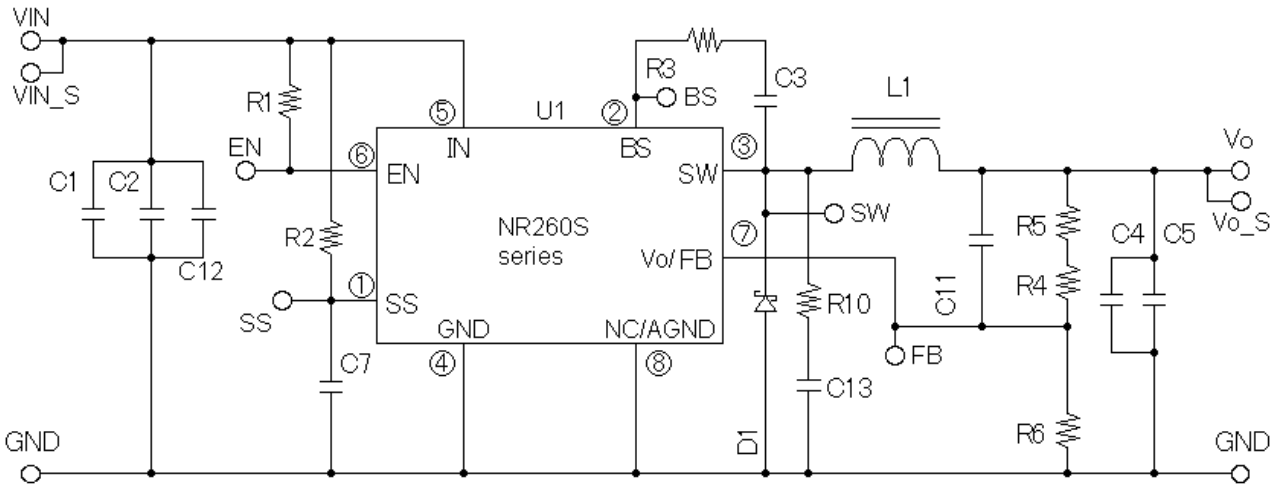


Figure 11-2. Circuit Diagram of Pattern Layout Example

Table 11-1. Reference Value (V_{IN} = 12 V)

Symbol	Part	Reference Value	Remarks
C1	Chip ceramic capacitor, 3225	10 μF, 25 V	
C2	Chip ceramic capacitor, 3225	10 μF, 25 V	
C3	Chip ceramic capacitor, 3225	0.1 μF	
C4	Chip ceramic capacitor, 3225	22 μF, 16 V	
C5	Chip ceramic capacitor, 3225	22 μF, 16 V	
C7	Chip ceramic capacitor, 3225	0.047 μF	
C11*	Chip ceramic capacitor, 3225	Open	Phase advance capacitor
C12*	Chip ceramic capacitor, 3225	Open	Bypass capacitor
C13*	Chip ceramic capacitor, 3225	Open	Capacitor for snubber circuit
D1*	Schottky diode	Open	Diode for efficiency improvement
L	Inductor	6.8 μH	
R1	Chip resistor, 1608	100 kΩ	
R2*	Chip resistor, 1608	Open	Not used for the IC
R3*	Chip resistor, 1608	0 Ω	For spike noise reduction (10 Ω or less)
R4	Chip resistor, 1608	0 Ω	
R5	Chip resistor, 1608	0 Ω	
R6	Chip resistor, 1608	Open	
R10*	Chip resistor, 1608	Open	For snubber circuit
U1	IC	NR263S	

* Refers to a part that requires the adjustment on the actual operation.

12. Typical Characteristics

Unless otherwise specified, T_A = 25 °C.

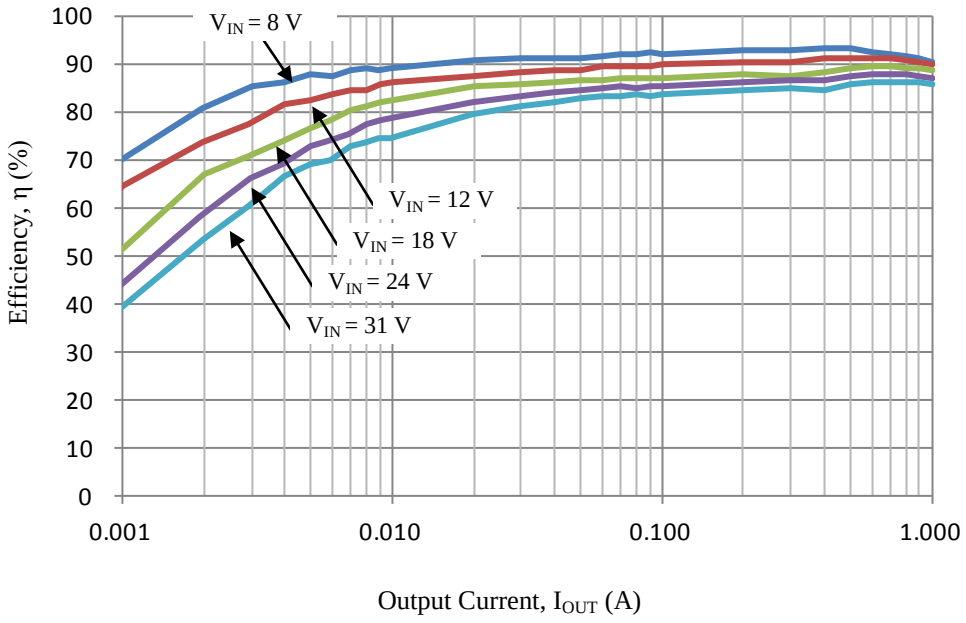


Figure 12-1. Efficiency Curves

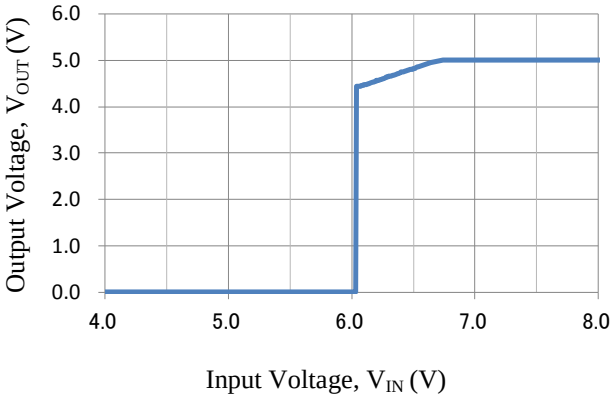


Figure 12-2. Output Voltage Rising (I_{OUT} = 1 A)

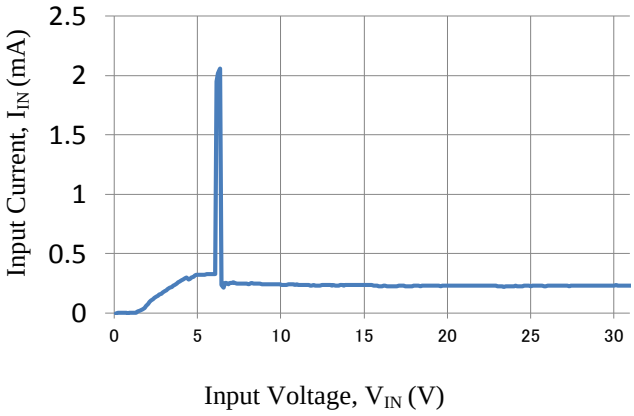


Figure 12-3. Input Current, I_{IN}

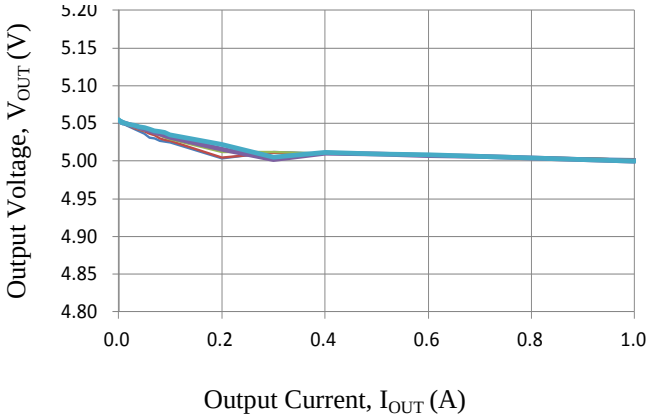


Figure 12-4. Load Regulation

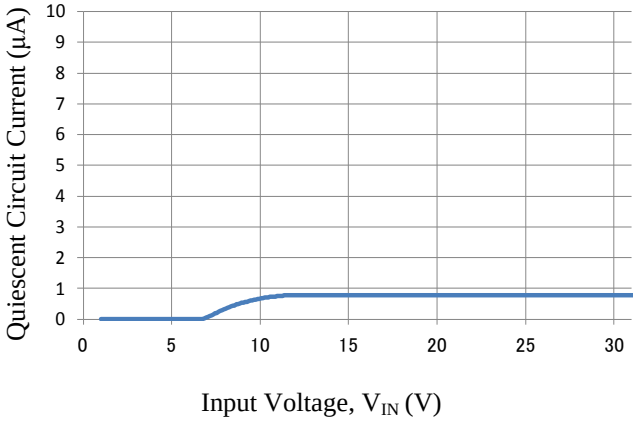


Figure 12-5. Quiescent Circuit Current

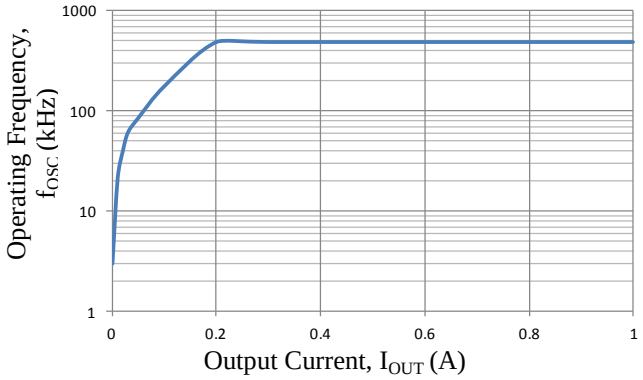


Figure 12-6. Operating Frequency

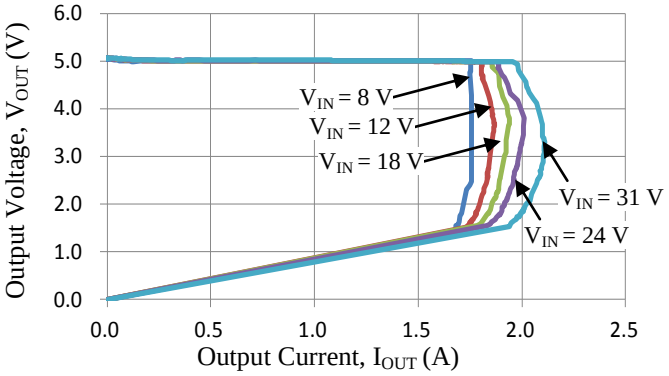


Figure 12-7. Overcurrent Protection Characteristics

Important Notes

- All data, illustrations, graphs, tables and any other information included in this document (the "Information") as to Sanken's products listed herein (the "Sanken Products") are current as of the date this document is issued. The Information is subject to any change without notice due to improvement of the Sanken Products, etc. Please make sure to confirm with a Sanken sales representative that the contents set forth in this document reflect the latest revisions before use.
- The Sanken Products are intended for use as components of general purpose electronic equipment or apparatus (such as home appliances, office equipment, telecommunication equipment, measuring equipment, etc.). Prior to use of the Sanken Products, please put your signature, or affix your name and seal, on the specification documents of the Sanken Products and return them to Sanken. When considering use of the Sanken Products for any applications that require higher reliability (such as transportation equipment and its control systems, traffic signal control systems or equipment, disaster/crime alarm systems, various safety devices, etc.), you must contact a Sanken sales representative to discuss the suitability of such use and put your signature, or affix your name and seal, on the specification documents of the Sanken Products and return them to Sanken, prior to the use of the Sanken Products. The Sanken Products are not intended for use in any applications that require extremely high reliability such as: aerospace equipment; nuclear power control systems; and medical equipment or systems, whose failure or malfunction may result in death or serious injury to people, i.e., medical devices in Class III or a higher class as defined by relevant laws of Japan (collectively, the "Specific Applications"). Sanken assumes no liability or responsibility whatsoever for any and all damages and losses that may be suffered by you, users or any third party, resulting from the use of the Sanken Products in the Specific Applications or in manner not in compliance with the instructions set forth herein.
- In the event of using the Sanken Products by either (i) combining other products or materials or both therewith or (ii) physically, chemically or otherwise processing or treating or both the same, you must duly consider all possible risks that may result from all such uses in advance and proceed therewith at your own responsibility.
- Although Sanken is making efforts to enhance the quality and reliability of its products, it is impossible to completely avoid the occurrence of any failure or defect or both in semiconductor products at a certain rate. You must take, at your own responsibility, preventative measures including using a sufficient safety design and confirming safety of any equipment or systems in/for which the Sanken Products are used, upon due consideration of a failure occurrence rate and derating, etc., in order not to cause any human injury or death, fire accident or social harm which may result from any failure or malfunction of the Sanken Products. Please refer to the relevant specification documents and Sanken's official website in relation to derating.
- No anti-radioactive ray design has been adopted for the Sanken Products.
- The circuit constant, operation examples, circuit examples, pattern layout examples, design examples, recommended examples, all information and evaluation results based thereon, etc., described in this document are presented for the sole purpose of reference of use of the Sanken Products.
- Sanken assumes no responsibility whatsoever for any and all damages and losses that may be suffered by you, users or any third party, or any possible infringement of any and all property rights including intellectual property rights and any other rights of you, users or any third party, resulting from the Information.
- No information in this document can be transcribed or copied or both without Sanken's prior written consent.
- Regarding the Information, no license, express, implied or otherwise, is granted hereby under any intellectual property rights and any other rights of Sanken.
- Unless otherwise agreed in writing between Sanken and you, Sanken makes no warranty of any kind, whether express or implied, including, without limitation, any warranty (i) as to the quality or performance of the Sanken Products (such as implied warranty of merchantability, and implied warranty of fitness for a particular purpose or special environment), (ii) that any Sanken Product is delivered free of claims of third parties by way of infringement or the like, (iii) that may arise from course of performance, course of dealing or usage of trade, and (iv) as to the Information (including its accuracy, usefulness, and reliability).
- In the event of using the Sanken Products, you must use the same after carefully examining all applicable environmental laws and regulations that regulate the inclusion or use or both of any particular controlled substances, including, but not limited to, the EU RoHS Directive, so as to be in strict compliance with such applicable laws and regulations.
- You must not use the Sanken Products or the Information for the purpose of any military applications or use, including but not limited to the development of weapons of mass destruction. In the event of exporting the Sanken Products or the Information, or providing them for non-residents, you must comply with all applicable export control laws and regulations in each country including the U.S. Export Administration Regulations (EAR) and the Foreign Exchange and Foreign Trade Act of Japan, and follow the procedures required by such applicable laws and regulations.
- Sanken assumes no responsibility for any troubles, which may occur during the transportation of the Sanken Products including the falling thereof, out of Sanken's distribution network.
- Although Sanken has prepared this document with its due care to pursue the accuracy thereof, Sanken does not warrant that it is error free and Sanken assumes no liability whatsoever for any and all damages and losses which may be suffered by you resulting from any possible errors or omissions in connection with the Information.
- Please refer to our official website in relation to general instructions and directions for using the Sanken Products, and refer to the relevant specification documents in relation to particular precautions when using the Sanken Products.
- All rights and title in and to any specific trademark or tradename belong to Sanken and such original right holder(s).

DSGN-CEZ-16003