# *NR887D*
# *Application Note Rev.4.0*



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## General Descriptions

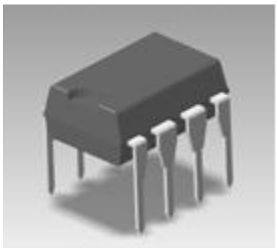
The NR887D is synchronous buck regulator ICs integrates High-side and Low-side power MOSFETs. With the current mode control, ultra low ESR capacitors such as ceramic capacitors can be used. The ICs have protection functions such as Over-Current Protection (OCP), Under-Voltage Lockout (UVLO) and Thermal Shutdown (TSD). An adjustable Soft-Start by an external capacitor prevents the excessive inrush current at turn-on. The ICs integrate phase compensation circuit which reduces the number of external components and simplifies the design of customer application. The ON/OFF pin (EN Pin) turns the regulator on or off and helps to achieve low power consumption requirements. The NR887D is available in an 8-pin DIP package.

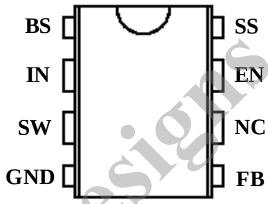
## Features & Benefits

- Current mode PWM control
- Up to 95% efficiency
- Stable with low ESR ceramic output capacitors
- Built-in protection function
  Over Current Protection (OCP)
  Thermal Shutdown (TSD)
  Under Voltage Lockout (UVLO)
- Built-in phase compensation
- Adjustable Soft-Start with an external capacitor
- Turn ON/OF the regulator function

## Package

- DIP 8






## Electrical Characteristics

- 2A Continuous output current
- Operating input range $V_{IN}$ = 4.5V～18V
- Output adjustable $V_O$= 0.8V～14V
- Fixed 500kHz frequency

## Applications

- LCD TV / Blu-Ray / Set top box
- Green Electronic products
- Other power supply

## Series Lineup

| Product No. | $f_O$ | $V_{IN}$ | | $V_O$ | | $I_{OUT}$ |
|---|---|---|---|---|---|---|
| NR887D | 500kHz | 4.5V to 18V | (1) | 0.8V to 14V | (2) | 2A |

(1) The minimum input voltage shall be either of 4.5V or $V_O$+3V, whichever is higher.
(2) The I/O condition is limited by the Minimum on-time ($T_{ON(MIN)}$).

# 1. Electrical Characteristics

## 1.1 Absolute Maximum Ratings

Table 1 Absolute maximum rating of NR887D

| Parameter | | Symbol | Ratings | Units | Remarks |
|---|---|---|---|---|---|
| DC input voltage | | $V_{IN}$ | 20 | V | |
| Power dissipation | (3) | Pd | 1.85 | W | Glass-epoxy board mounting in a 70mm×60mm. (copper area in a 1310mm$^2$) Max Tj =150°C |
| Junction temperature | (4) | $T_j$ | −40 to 150 | °C | |
| Storage temperature | | $T_{stg}$ | −40 to 150 | °C | |
| Thermal resistance (junction- Pin No. 4) | | $\theta_{j-c}$ | 25 | °C /W | |
| Thermal resistance (junction-ambient air) | | $\theta_{j-a}$ | 67 | °C /W | Glass-epoxy board mounting in a 70mm×60mm. (copper area in a 1310mm$^2$) |

(3) Limited by thermal shutdown.
(4) The temperature detection of thermal shutdown is about 160°C

## 1.2 Recommended Operating Conditions

Operating IC in recommended operating conditions is required for normal operating of circuit functions shown in Table 3 Electrical characteristics of NR887D.

Table 2 Recommended operating conditions of NR887D

| Parameter | | Symbol | Ratings | | Units | Remarks |
|---|---|---|---|---|---|---|
| | | | MIN | MAX | | |
| DC input voltage | (5) | $V_{IN}$ | $V_O$+3 | 18 | V | |
| DC output current | (6) (7) | $I_{OUT}$ | 0 | 2.0 | A | |
| Output voltage | | $V_O$ | 0.8 | 14 | V | |
| Ambient operating temperature | (7) | $T_{OP}$ | −40 | 85 | °C | |

(5) The minimum value of input voltage is taken as the larger one of either 4.5V or $V_O$ +3V.
In the case of $V_{IN}=V_O+1 \sim V_O+3$V, it is set to $I_{OUT}$=1A MAX and it is possible to apply the controlled $V_{IN}$ by the Max-on-duty. Refer the following equation. $V_{IN} = V_O / 0.9$(typ)

(6) Recommended circuit refers to Typical Application Circuit (fig.4).
(7) To be used within the allowable package power dissipation characteristics (fig. 5)

## 1.3 Electrical Characteristics

Electrical characteristics indicate specific limits, which are guaranteed when IC is operated under the measurement conditions shown in the circuit diagram (fig. 1)

Table 3 Electrical characteristics of NR887D series (Ta=25°C)

| Parameter | | | Symbol | Ratings MIN | TYP | MAX | Units | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Reference voltage | | | $V_{REF}$ | 0.784 | 0.800 | 0.816 | V | $V_{IN}$ = 12V, $I_O$ = 1.0A |
| Output voltage temperature coefficient | | | $\Delta V_{REF}/\Delta T$ | — | ±0.05 | — | mV/°C | $V_{IN}$ = 12V, $I_O$ = 1.0A –40°C to +85°C |
| Efficiency | | (8) | $\eta$ | — | 90 | — | % | $V_{IN}$=12V, $V_O$=3.3V, $I_O$=1A |
| Operating frequency | | | $f_O$ | 400 | 500 | 600 | kHz | $V_{IN}$ =12V, $V_O$=3.3V, $I_O$=1A |
| Line regulation | | (9) | $V_{Line}$ | — | 50 | — | mV | $V_{IN}$ = 6.3V～18V, $V_O$ = 3.3V, $I_O$ = 1A |
| Load regulation | | (9) | $V_{Load}$ | — | 50 | — | mV | $V_{IN}$ = 12V, $V_O$ = 3.3V, $I_O$ = 0.1A～2.0A |
| Over current protection starting current | | | $I_S$ | 3.1 | — | 6.0 | A | $V_{IN}$ = 12V, $V_O$ = 3.3V |
| Quiescent current 1 | | | $I_{IN}$ | — | 6 | — | mA | $V_{IN}$= 12V $V_{EN}$=10kΩ pull up to $V_{IN}$ |
| Quiescent current 2 | | | $I_{IN(off)}$ | 0 | — | 10 | µA | $V_{IN}$=12V, $I_O$=0A, $V_{EN}$=0V |
| SS Pin | Flow-out current at low level voltage | | $I_{EN/SS}$ | 6 | 10 | 14 | µA | $V_{SS}$=0V, $V_{IN}$=12V |
| | High level voltage | | $V_{SSH}$ | — | 3.0 | — | V | $V_{IN}$=12V |
| EN Pin | Sink current | | $I_{EN}$ | | 50 | 100 | µA | $V_{EN}$= 10V |
| | Threshold voltage | | $V_{C/EH}$ | 0.7 | 1.4 | 2.1 | V | $V_{IN}$=12V |
| Max on-duty | | (9) | $D_{MAX}$ | — | 90 | — | % | |
| Minimum on-time | | (9) | $T_{ON(MIN)}$ | — | 150 | — | nsec | |
| Thermal shutdown threshold temperature | | (9) | TSD | 151 | 165 | — | °C | |
| Thermal shutdown restart hysteresis of temperature | | (9) | TSD_hys | — | 20 | — | °C | |

(8) Efficiency is calculated by the following equation.

$$\eta\ (\%) = \frac{V_O \cdot I_O}{V_{IN} \cdot I_{IN}} \times 100$$

(9) Guaranteed by design,not tested.

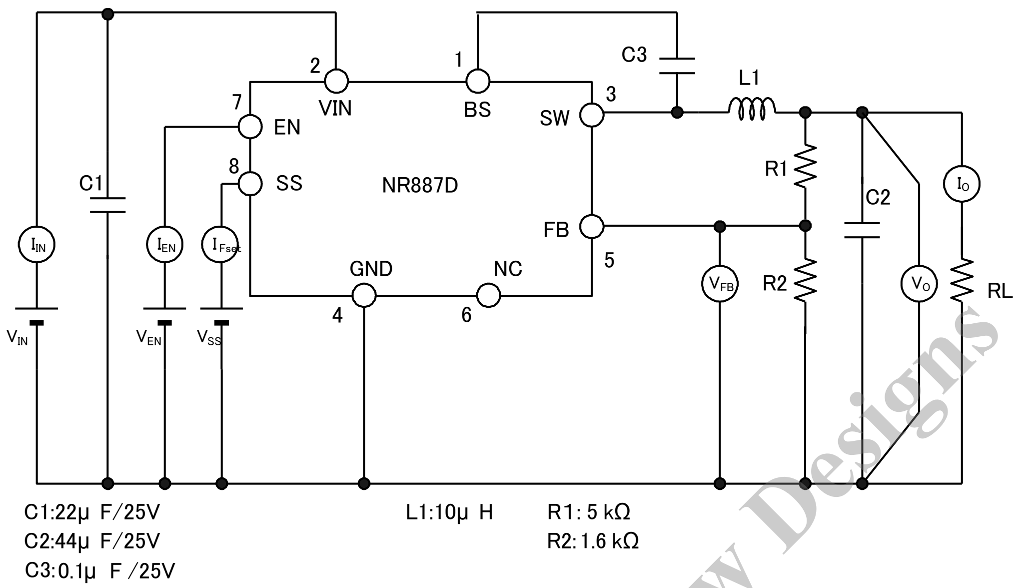



fig.1 Measurement circuit diagram

## 2. Block Diagram & Pin Functions
## 2.1 Functional Block Diagram

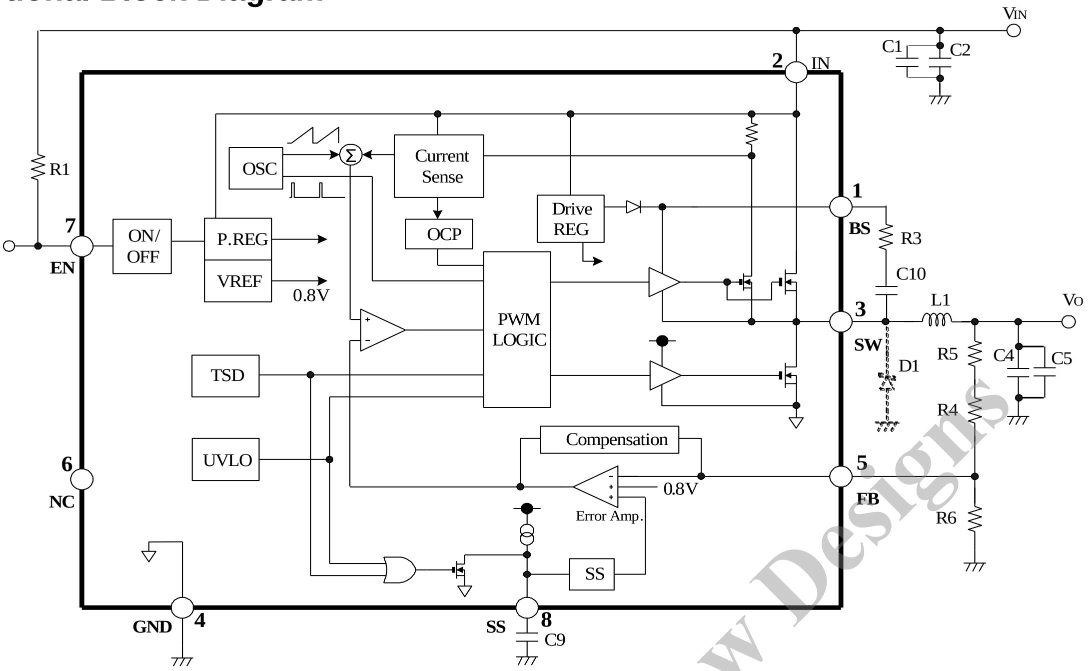



fig.2 Block diagram of NR887D

## 2.2 Pin Asignments & Functions

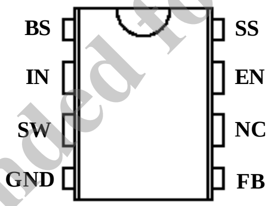



fig.3 Pin Assignments

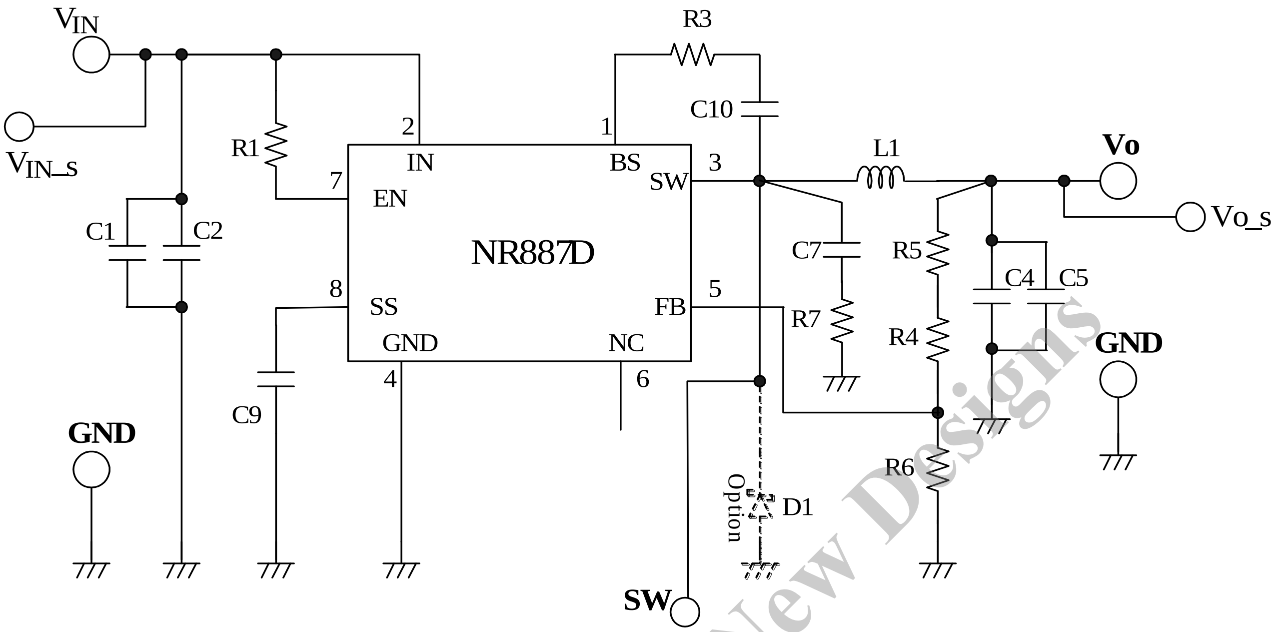
Table4 Pin functions of NR887D

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | BS | High-side Boost input.<br>BS supplies the drive for High-side Nch-MOSFET switch.<br>Connect a capacitor and a resistor between SW to BS. |
| 2 | IN | Power input. VIN supplies the power to the IC.as well as the regulator switches |
| 3 | SW | Power switching output.<br>SW supplies power to the output.<br>Connect the LC filter from SW to the output.<br>Note that a capacitor is required from SW to BS to supply the power the High-side switch |
| 4 | GND | Ground<br>Connect the exposed pad to Pin No.4 |
| 5 | FB | Feedback input Pin to compare Reference Voltage.The feedback threshold is 0.8V.<br>To set the output voltage, FB Pin is required to connect between resistive voltage divider R4 and R6. |
| 6 | NC | No Connection. |
| 7 | EN | Enable input.<br>Drive EN Pin high to turn on the regulator, low to turn it off. |
| 8 | SS | Soft-Start control input.<br>To set the soft-start period, connect to a capacitor between GND. |

## 3. Example Application Circuit

Each ground of all components is connected as close as possible to the Pin No.1 at one point.

To help heat dissipation, connect a large copper plane to exposed pad on the back side of the package. The copper plane is required for GND




C1, C2: 10 μ F / 25V R1: 100kΩ L1: 10 μ H
C4, C5: 22 μ F / 16V R3: 22Ω
C7: 1000pF R4: 1.1kΩ, R5: 3.9kΩ (Vo=3.3V)
C9: 0.1 μ F R6: 1.6kΩ
C10: 0.1 μ F R7: 10Ω

fig. 4 Typical Application Circuit of NR887D

## 4. Allowable package power dissipation

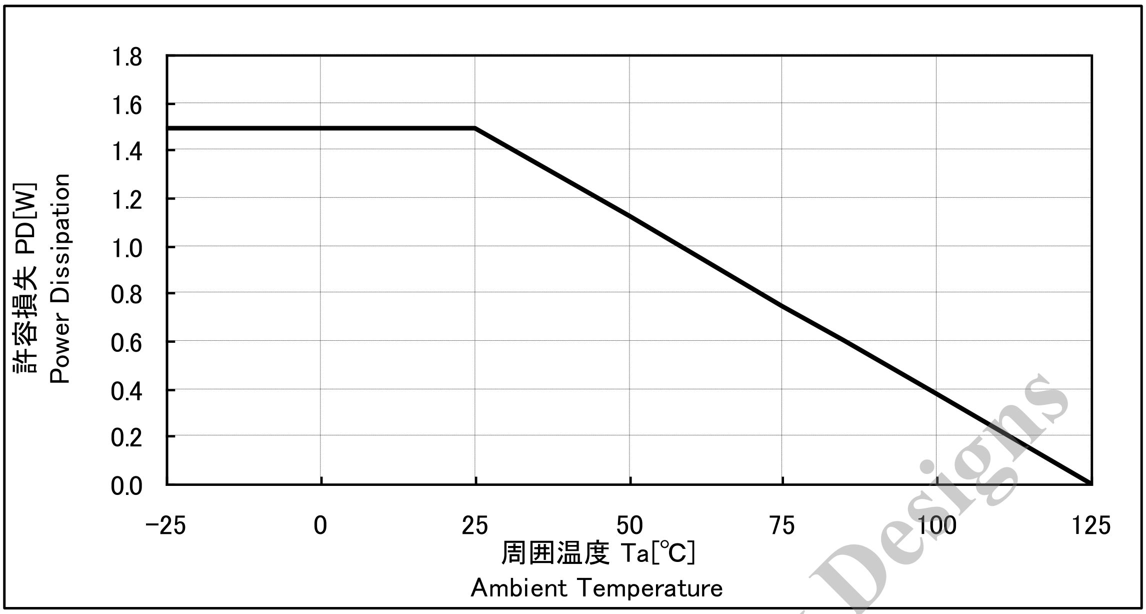



fig. 5 Allowable package powe disspation of NR887D



NOTES:

1) Glass-epoxy board mounting in a 70mm × 60mm
2) copper area : 1310mm$^2$
3) The power dissipation is calculated at the junction temperature 125 °C
4) Losses can be calculated by the following equation.
   As the efficiency is subject to the input voltage and output current, it shall be obtained from the efficiency curve and substituted in percent.
5) Thermal design for D1 shall be made separately.

$$P_d = V_O \times I_O\left(\frac{100}{\eta x} - 1\right)$$

$V_{O:}$ Output voltage

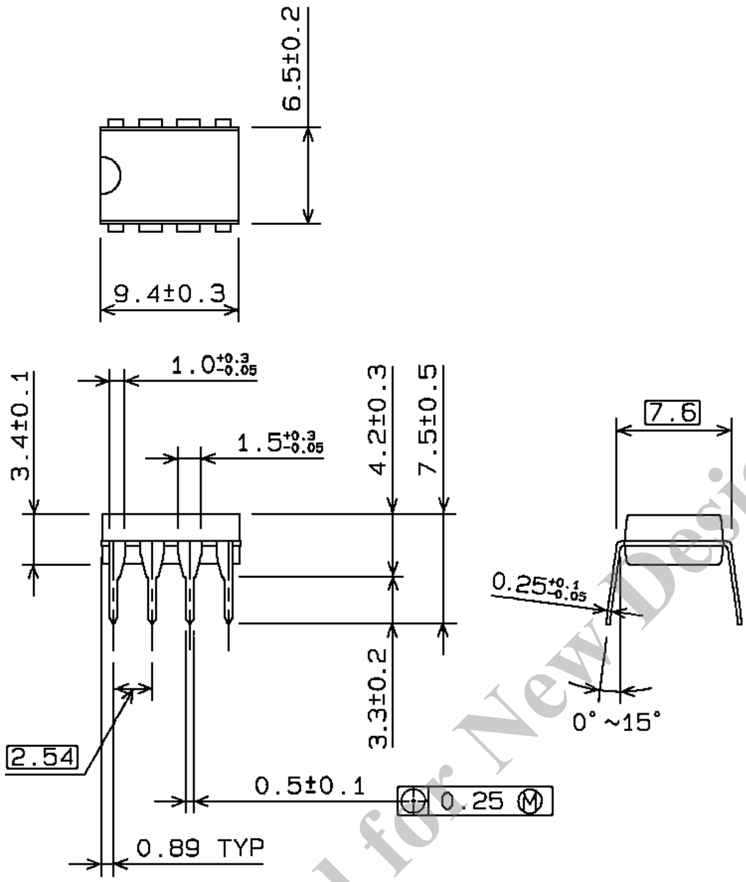
$V_{IN:}$ Input voltage

$I_{O:}$ Output current

$\eta$ x : Efficiency (%)

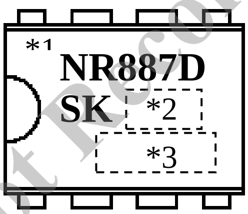
## 5. Package Outline

- DIP8




Notes:
1) Dimension is in millimeters.
2) Drawing is not to scale.

fig.6 Package outline




*1. Product number
*2. Lot number (three digit)
1st letter : The last digit of the year
2nd letter : Month
January to September : 1 to 9
October : O
November : N
December : D
3rd letter : manufacturing week
First week to 5th week : 01 to 05
*3. Control number (four digit)

fig.7 Marking of NR887D

# 6. Operational Descriptions

## 6.1 PWM (Pulse Width Modulation) Output Control

The NR887D consists of three blocks; two feedback loops (voltage control and current control) and one slope compensation. The PWM is controlled with the current mode control by calculating the voltage feedback control, and the current feedback control and the slope compensation signals (fig.8). For the voltage feedback control, the output voltage feed back to the PWM control. The error amplifier compares the output voltage divided by resistors with the reference voltage $V_{REF}$ = 0.8V. For the current feedback control, the inductor current feed back to the PWM control. The inductor current divided by Sense-MOSFET is detected with the current sense amplifier. To prevent sub-harmonic oscillations, which is characteristic in current mode control, the slope of current control is compensated.

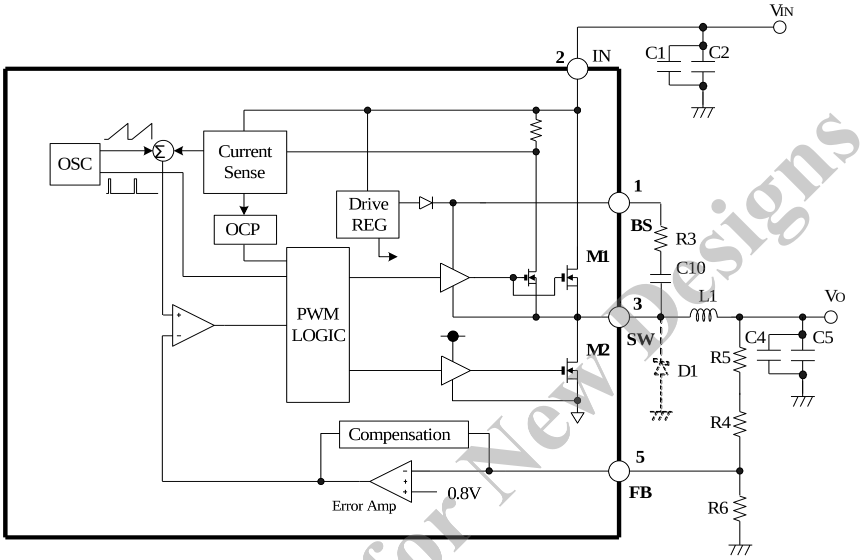



fig.8 Basic Structure of Chopper Type Regulator with PWM Control by Current Control

The NR887D starts the switching operation when UVLO is released, or EN or SS Pin voltage exceeds the threshold. Initially, it operates switching with minimum ON duty or maximum ON duty. The high-side switch (M1) is the switching MOSFET that supplies output power. At first, the low-side switch (M2) turns ON and charges the boost capacitor C10 that drives M1. When M1 is ON, as the inductor current is increased by applying voltage to SW Pin and the inductor, the output of inductor current sense amplifier is also increased. Sum of the current sense amplifier output and slope compensation signal is compared with the error amplifier output. When the summed signal exceeds the error amplifier (Error Amp.) output voltage, the current comparator output becomes “High” and the RS flip-flop is reset. When M1 turns OFF and M2 turns ON, the regenerative current flows through M2. In the case that an external SBD (D1) is connected, the current also flows through D1.

In the NR887D, the set signal is generated in each cycle and RS flip-flop is set. In the case that the summed signal does not exceed the error amplifier (Error Amp.) output voltage, RS flip-flop is reset without fail by the signal from OFF duty circuit.

## 6.2 Power Supply Stability

The phase characteristics of chopper type regulator are the synthesis of the internal phase characteristics of regulator IC, the combination of output capacitor C4 (C5) and load resistance Rout. The internal phase characteristics of regulator IC are generally determined by the delay time of control block and the phase characteristics of output error amplifier. The phase delay due to the delay time of control block is very small and not problem in actual use. As the built-in phase compensation for output error amplifier, in order to ensure stable operation, refer to “**7.1.3 Output Capacitor C4 (C5)**” and “**7.1.4 Output Voltage Set-up (FB Pin)**” for setting the output voltage and output capacitor,

## 6.3 Over Current Protection (OCP)

The NR887D integrates the drooping type over-current protection circuit. The peak current of switching transistor is detected. When the peak current exceeds rated value, the over-current protection limits the current by forcibly shortening the ON time of transistor and decreasing the output voltage. It prevents the current increment at low output voltage by decreasing the switching frequency, if the output voltage drops lower. When the over-current state is released, the output voltage automatically returns.

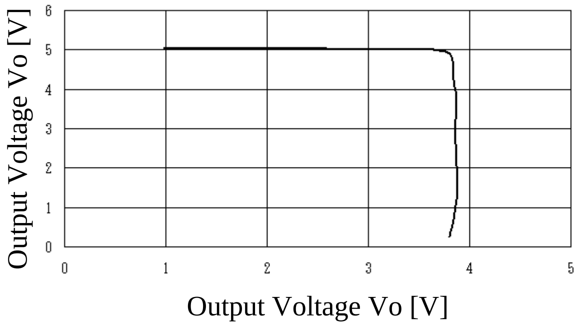



fig.9 OCP Characteristics of NR887D

## 6.4 Thermal Shutdown (TSD)

The thermal shutdown circuit detects the IC junction temperature. When the junction temperature exceeds the rated value (around 160°C), it shuts-down the output transistor and turns the output OFF. If the junction temperature falls below the thermal shutdown rated value by around 20°C, the operation returns automatically.

* (Thermal Shutdown Characteristics) Notes

The circuit protects the IC against temporary heat generation. It does not guarantee the operation including reliabilities under the continuous heat generation conditions, such as short circuit for a long time.

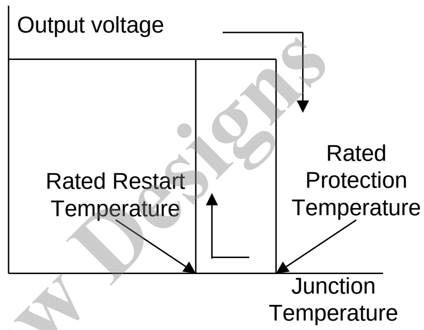



fig.10 TSD Characteristics of NR887D

## 6.5 Soft-Start

By connecting a capacitor between Pin No.8 (SS) and Pin No.4 (GND), Soft-Start operates when the power is supplied to the IC. Output Voltage (Vo) is ramped up by the charge voltage level of Css.

Time of Soft-Start can be calculated from the time constant of charging Css.

A capacitor Css controls OFF period of PWM and then the rise time is determined. The rise time t_ss and the delay time t_delay are calculated in following equations.

In the case of operating IC without using Soft-Start function, Pin No.4 is required for open.

$t_{SS} = C_{SS} \times (V_{SS2} - V_{SS1}) / (I_{SS} \times V_{SS1})$

$V_{SS1}$ (0.9V) < SS Pin voltage < $V_{SS2}$ (1.79V)

$t\_delay = C_{SS} \times V_{SS1} / I_{SS}$

SS Pin voltage < $V_{SS1}$(th) = $V_{SS1}$ (0.9V)

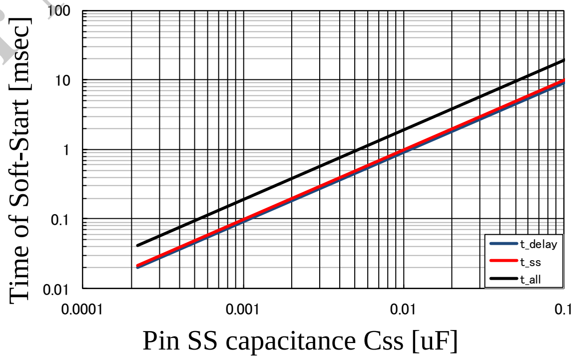



fig.11 SS Pin capacitance $C_{SS}$ VS Soft-Start

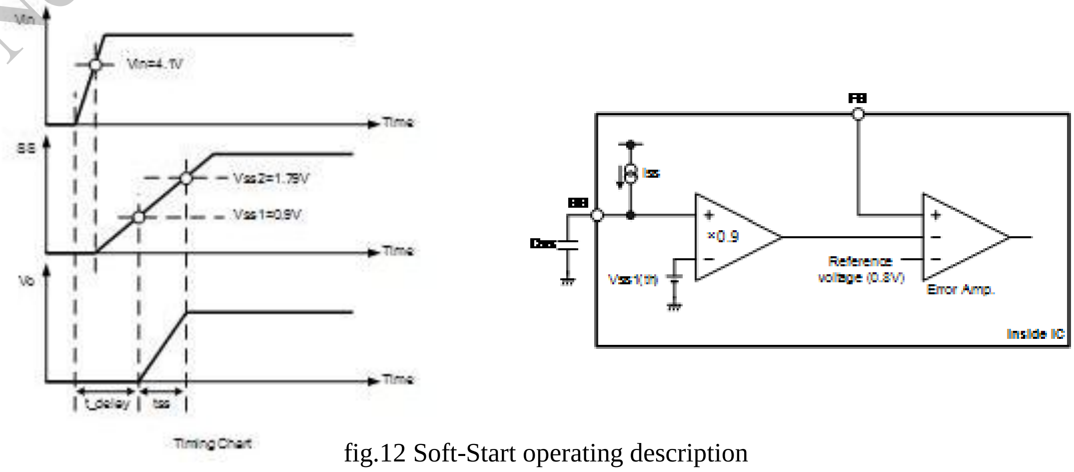



fig.12 Soft-Start operating description

In the case of without or too small Css, IC starts up at the time constant that output current limited by Is charges output capacitor C4 (C5).
Following equation shows the time constant of start up by the output capacitor C4 (C5) at no load.

$t = (C_O \times V_O) / I_S$

*At the start up with a load, load current is detracted from Is.

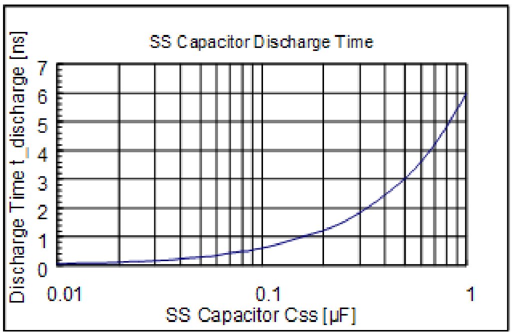



fig.13 Discharge time of SS capacitor

Pin SS Open Voltage: 3V
SS Discharge Capability: 500μA
The left graph shows the SS Pin voltage changing time from 3V to 0V.

## 6.6 ON and OFF the Regulator (Enable)

EN Pin (Pin No.7) turns the regulator ON or OFF. When drive EN under 1.4V ($V_{ENL}$), output is turned OFF (fig.14). 1.4V ($V_{ENL}$) can be achieved by connecting a bipolar transistor in an open collector configuration.
When the external ON/OFF function isn't used, connect only Pull-up resistor of 100kΩ between IN and EN, and use it as the fig15.It starts when a $V_{IN}$ voltage is inputted.

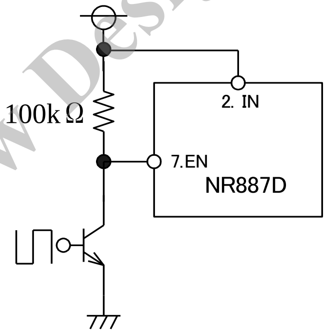



fig. 14 ON / OFF Control 1

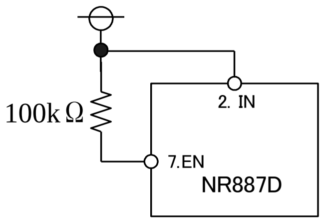



fig. 15 ON / OFF Control 2

# 7. Design Notes

## 7.1 External Components

All components are required for matching to the condition of use.

### 7.1.1 Choke Coil L1

The choke coil L1 is one of the most important components in the chopper type switching regulators. In order to maintain the stabilized regulator operation, the coil should be carefully selected so it must not enter saturation or over heat excessively at any conditions. The selection points of choke coil are as follows:

a) The coil type is only required for switching regulator.
It is recommended not to use a coil for noise filer since it causes high heat generation due to high power dissipation.

b) The sub-harmonic oscillations should be prevented.
Under the peak detection current control, the inductor current may fluctuate at a frequency that is an integer multiple of switching operation frequency. This phenomenon is the known as sub-harmonic oscillation and this phenomenon theoretically occurs in the peak detection current control mode. In order to stabilize the operation, the inductor current compensation is made internally. The inductance corresponding to the output voltage should be selected.

From fig.16 shows the selection range of inductance L to prevent the sub-harmonic oscillations. As for the upper limit of inductance L, the value is for reference, because it may vary depending on input/output conditions and load current.

The ripple portion of choke coil current ΔIL and the peak current ILp are calculated from the following equations:

$$\Delta IL = \frac{(V_{IN} - V_O) \cdot V_O}{L \cdot V_{IN} \cdot f} \quad \text{------ (1)}$$

$$IL_P = \frac{\Delta IL}{2} + I_O \quad \text{------ (2)}$$

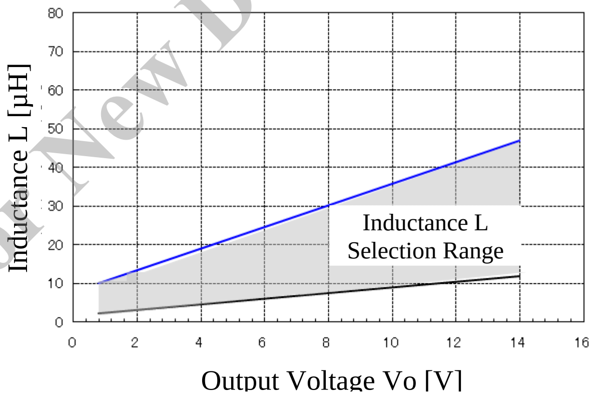



fig.16 Selection Range of Inductance L in NR887D

The ΔIL and ILp increase when the inductance of the choke coil L becomes smaller.
If the inductance is too small, the regulator operation may be unstable because the choke coil current fluctuates largely. It is necessary to give attention to decreasing of the inductance due to the magnetic saturation such as in overload and load shortage.

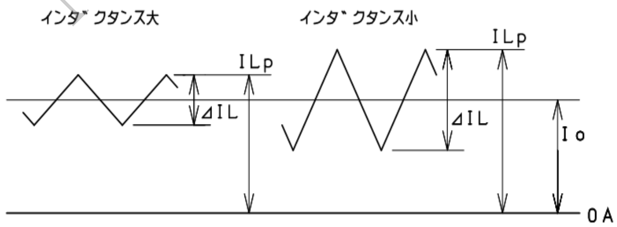



fig.17 Relationship between inductance and ripple current

c) The coil should be of proper rated current.
The rated current of the choke coil should be higher than the maximum load current used. If the load current exceeds the rated current of coil, the inductance decreases drastically and eventually enters into the saturation state. In this status, it is necessary to give attention because the high-frequency impedance decreases and the excess current runs.

d) The magnetic noise should be minimized.
The open magnetic circuit type core like a drum type may generate noise in peripheral circuit due to the magnetic flux passing outside of coil. Coils of closed magnetic circuit type core, such as toroidal type, EI type and EE type are preferable.

### 7.1.2 Input Capacitor C1 (C2)

The input capacitor operates as a bypass capacitor of input circuit. It supplies the short current pulses to the regulator during switching and compensates the input voltage drop. It should be connected close to the regulator IC. Even if the rectifying capacitor of AC rectifier circuit is in input circuit, the input capacitor cannot be used as a rectifying capacitor unless it is connected near IC.

The selection points of C1 (C2) are as follows:
a) The capacitor should be of proper breakdown voltage rating
b) The capacitor should have sufficient allowable ripple current rating

If the input capacitor C1 (C2) is used under the conditions of excessive breakdown voltage or allowable ripple current, or without derating, the regulator may become unstable and the capacitor’s lifetime may be greatly reduced. The selection of the capacitor C1 (C2) is required for the sufficient margins to the ripple current. The effective value of ripple current Irms that flows across the input capacitor is calculated from the equation (3):

$$\mathrm{Irms} \approx 1.2 \times \frac{\mathrm{Vo}}{\mathrm{Vin}} \times \mathrm{Io} \quad \text{------ (3)}$$

In the case of $V_{IN}$ = 20V, $I_o$ = 3A, $V_o$ = 5V,

$$\mathrm{Irms} \approx 1.2 \times \frac{5}{20} \times 3 = 0.9\mathrm{A}$$

The capacitor is required for the allowable ripple current of 0.9A or higher.

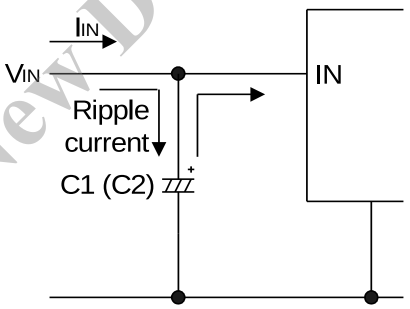



fig. 18 C1 (C2) Current path

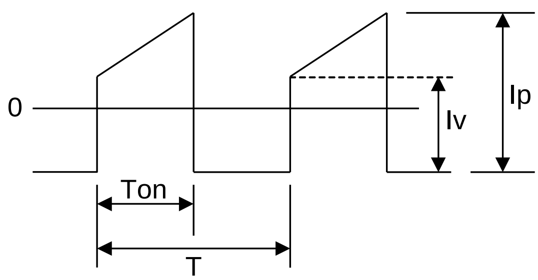



fig.19 C1 (C2) Current Waveform

### 7.1.3 Output Capacitor C4 (C5)

In the current control mode, the feedback loop which detects the inductor current is added to the voltage control mode. The stable operation is achieved by adding inductor current to the feedback loop without considering the effect of secondary delay factor of LC filter. It is possible to reduce the capacitance of LC filter that is needed to make compensations for the secondary delay, and the stable operation is achieved even by using the low ESR capacitor (ceramic capacitor).
The output capacitor C4 (C5) comprises the LC low-pass filter with choke coil L1 and works as the rectifying capacitor of switching output. The current equal to ripple portion ΔIL of choke coil current charges and discharges the output capacitor. In the same way as the input capacitor, the breakdown voltage and the allowable ripple current should be met with sufficient margins.

The ripple current effective value of output capacitor is calculated from the equation (4):

$$\mathrm{Irms} = \frac{\Delta \mathrm{IL}}{2\sqrt{3}} \text{ ------ (4)}$$

When ΔIL = 0.5A,

$$\mathrm{Irms} = \frac{0.5}{2\sqrt{3}} \fallingdotseq 0.14\mathrm{A}$$

Therefore a capacitor with the allowable ripple current of 0.14A or higher is needed.

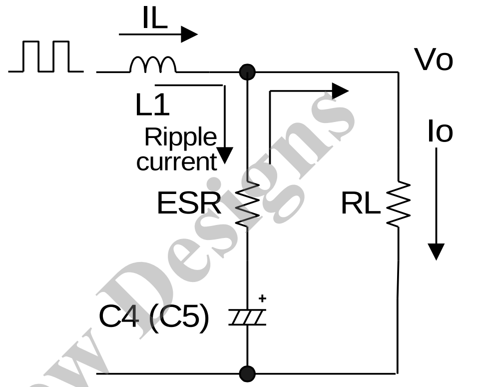



fig. 20 C4 (C5) Current path

The output ripple voltage of regulator Vrip is determined by the product of choke current ripple portion ΔIL (= C4 (C5) discharge and charge current) and output capacitor C4 (C5) equivalent series resistance ESR.

$$\mathrm{Vrip} = \Delta \mathrm{IL} \cdot \mathrm{C4}_{\mathrm{ESR}} \text{ ------ (5)}$$

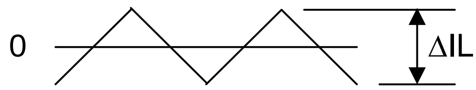



fig. 21 C4 (C5） Current Waveform

It is necessary to select a capacitor with low equivalent series resistance ESR in order to lower the output ripple voltage. As for general electrolytic capacitors of same product series, the ESR shall be lower for products of higher capacitance with same breakdown voltage, or of higher breakdown voltage with same capacitance.

When ΔIL = 0.5A, Vrip = 40mV,

$$\mathrm{C4}_{\mathrm{ESR}} = 40 \div 0.5 = 80\mathrm{m}\Omega$$

A capacitor with ESR of 80mΩ or lower should be selected. Since the ESR varies with temperature and increases at low temperature, it is required to check the ESR at the actual operating temperatures. It is recommended to contact capacitor manufacturers for the ESR value since it is peculiar to every capacitor series.

### 7.1.4 Output Voltage Set-up ( FB Pin )

The FB Pin is the feedback detection Pin that controls the output voltage. It is recommended to connect close to the output capacitor C4 (C5). If they are not close, the abnormal oscillations may be caused by the poor regulation and the increased switching ripple.

The setting of output voltage is achieved by connecting between resistive voltage divider R4 (R5) and R6. Setting the $I_{FB}$ to about 0.5mA is recommended.

(The target of $I_{FB}$ lower limit is 0.5mA, and the upper limit is not defined. However, it is necessary to consider that the circuit current shall increase according to the $I_{FB}$ value.)

R4 (R5), R6 and the output voltage $V_O$ are calculated from the following equations:

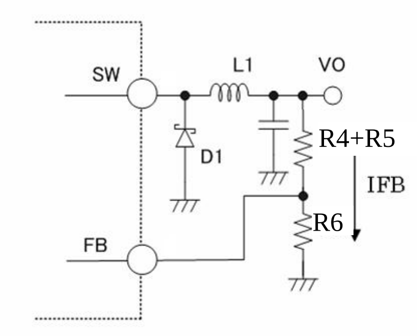



fig. 22 Detection and setting of output voltage

$I_{FB} = V_{FB} / R6$ *$V_{FB} = 0.8V \pm 2\%$

$R4 + R5 = ( V_O - VFB ) / I_{FB}$

$R6 = V_{FB} / I_{FB}$

$V_O = ( R4 + R5 ) \times ( VFB / R6 ) + VFB$

R6 is required to connect for the stable operation when set to $V_O = 0.8V$.

Regarding the relation of input / output voltages, it is recommended that setting of the ON width of the SW Pin is more than 200nsec

The PCB circuit traces of FB Pin, R4 (R5) and R6 are required for not parallel to the flywheel diode. The switching noise may affect the detection voltage and the abnormal oscillation may be caused. Especially, it is recommended to design the circuit trace short from FB Pin to R6.

### 7.1.5 External Bootstrap Diode for Low Input

Although the NR887D will work with input voltages lower than 6V, it is recommended to connect a diode between IN Pin and BS Pin in order to enhance the efficiency (fig.23). Alternatively an external voltage source can be connected through a diode to the BS Pin (fig.24).

NOTES:

1) The external voltage is required to be set from 5V to 6V.

2) In the case that the input voltage $V_{IN}$ is higher than 6V, the Bootstrap Diode must not be connected.

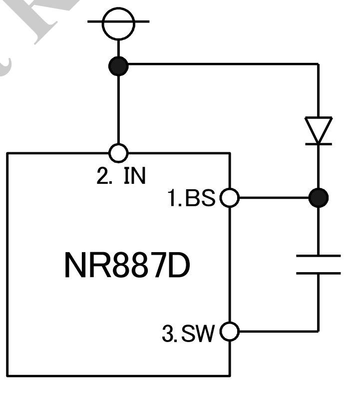



fig.23 Bootstrap Diode Connection 1

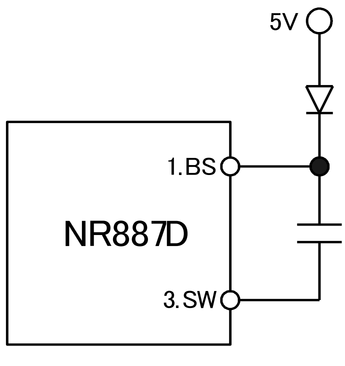



fig.24 Bootstrap Diode Connection 2

### 7.1.6 Flywheel Diode D1

A flywheel diode can be connected to enhance the efficiency.

The flywheel diode D1 is for releasing the energy stored in the choke coil at switching OFF. It is required to use a Schottky barrier diode for flywheel diode. If a general rectifying diode or a fast recovery diode is used, the IC may fail to operate properly becase of applying reverse voltage due to the recovery and ON voltage. Since the output voltage from the SW Pin (Pin No. 3) is almost equal to the input voltage, it is required to use the flywheel diode with the reverse breakdown voltage of equal or higher than the input voltage.

It is recommended not to use ferrite beads for flywheel diode.

### 7.1.7 Output Voltage $V_O$ and Output Capacitor C4 (C5)

From Table 6 shows the comparison of output voltage and output capacitor, for maintaining the IC stable operations, for reference.

ESR of Electrolytic Capacitor is required from 100m Ω to 200mΩ.

Regarding the inductance L, it is recommended to select it according to **7.1.1 Choke Coil L1**.

Table 6 NR887D ($f_{SW}$ =500kHz) $V_O$ and C4 (C5) Comparison

| $V_O$(V) | C4 (C5) (μF) | |
|---|---|---|
| | Ceramic Capacitor | Electrolytic Capacitor (ESR≒100mΩ) |
| 1.2 | 22 to 100 | 47 to 330 |
| 1.8 | 10 to 68 | 33 to 220 |
| 3.3 | 6.8 to 68 | 10 to 100 |
| 5 | 4.7 to 47 | 6.8 to 100 |
| 9 | 2.2 to 33 | 3.3 to 33 |
| 12 | 2.2 to 22 | 2.2 to 22 |
| 14 | 2.2 to 22 | 2.2 to 22 |

## 7.2 Pattern Design

### 7.2.1 High Current Line

High current paths in the circuit are marked as bold lines in the circuit diagram below. These paths are required for wide and short trace as possible.

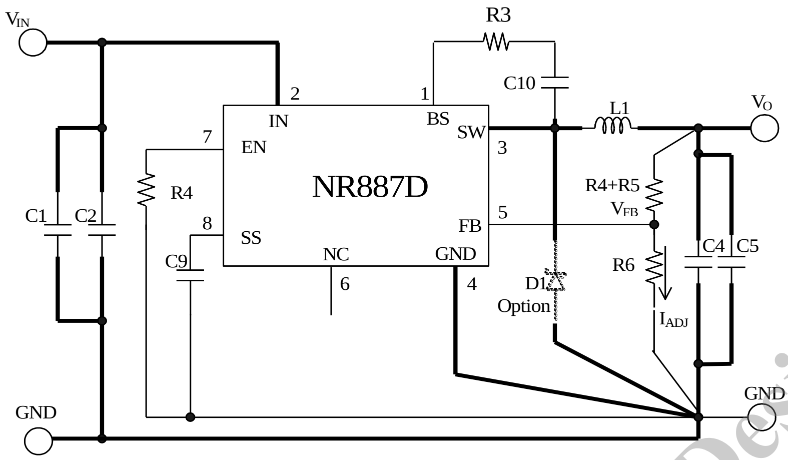



fig.25 Circuit Diagram

### 7.2.2 Input / Output Capacitors

The input capacitor C1 (C2) and the output capacitor C4 (C5) are required to connect to the IC as short as possible. If the rectifying capacitor for AC rectifier circuit is in the input side, it can be also used as an input capacitor. However, if it is not close to the IC, the input capacitor is required to be connected in addition to the rectifying capacitor. Since the high current is discharged and charged with high speed through the leads of input / output capacitors, make the current paths as short as possible. A similar care should be taken when designing pattern for other capacitors.

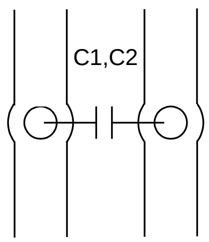



fig. 26 Recommended Pattern example

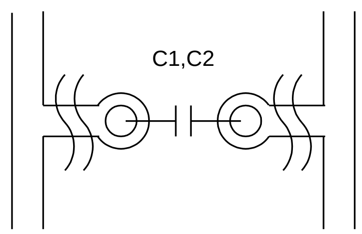
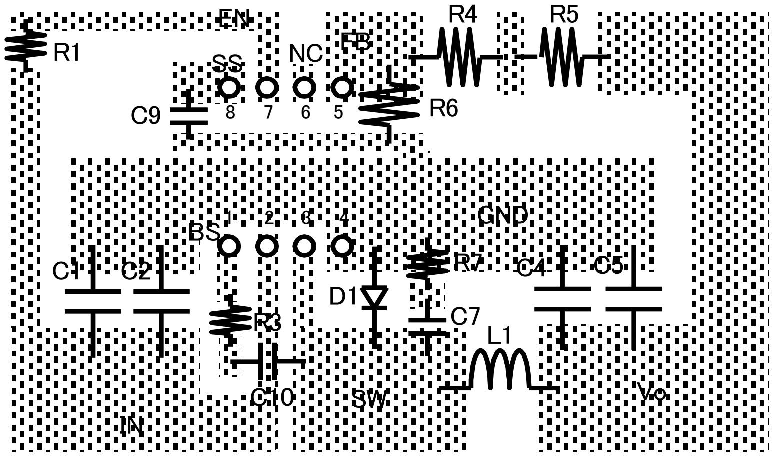



fig. 27 No good pattern example

### 7.2.3 PCB Layout




NOTES:
Drawing is not to scale.

fig.28 Recommended PCB Layout

## 7.3 Applied Design

### 7.3.1 Spike Noise Reduction(1)

・The addition of the BS serial resistor

The “turn-on switching speed” of the internal Power-MOSFET can be slowed down by inserting $R_{BS}$ (option) of the fig29.It is tendency that Spike noise becomes small by reducing the switching-speed. Set up 22-ohm as an upper limit when you use $R_{BS}$.

*Attention

1) When the resistance value of $R_{BS}$ is enlarged by mistake too much, the internal power-MOSFET becomes an under-drive, it may be damaged worst.

2) The “defective starting-up” is caused when the resistance value of RBS is too big.

*The BS serial resistor $R_{BS}$ is R3 in the Demonstration Board.

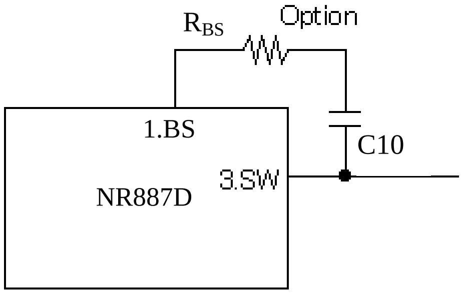



fig.29 The addition of the BS serial resistor

### 7.3.2 Spike Noise Reduction(2)

・The addition of the Snubber circuit

In order to reduce the spike noise, it is possible to compensate the output waveform and the recovery time of diode by connecting a capacitor and resistor parallel to the freewheel diode (snubber method). This method however may slightly reduce the efficiency.

* For observing the spike noise with an oscilloscope, the probe lead (GND) should be as short as possible and connected to the root of output capacitor. If the probe GND lead is too long, the lead may act like an antenna and the observed spike noise may be much higher and may not show the real values.

*The snubber circuit parts are C7 and R7.

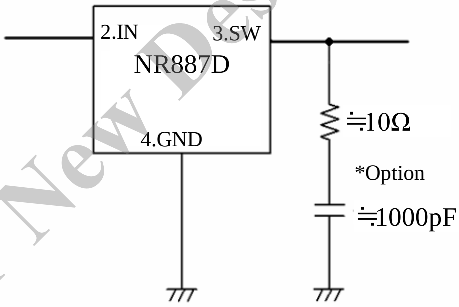



fig.30 The addition of the Snubber circuit

### 7.3.3 Attention about the insertion of the bead-core

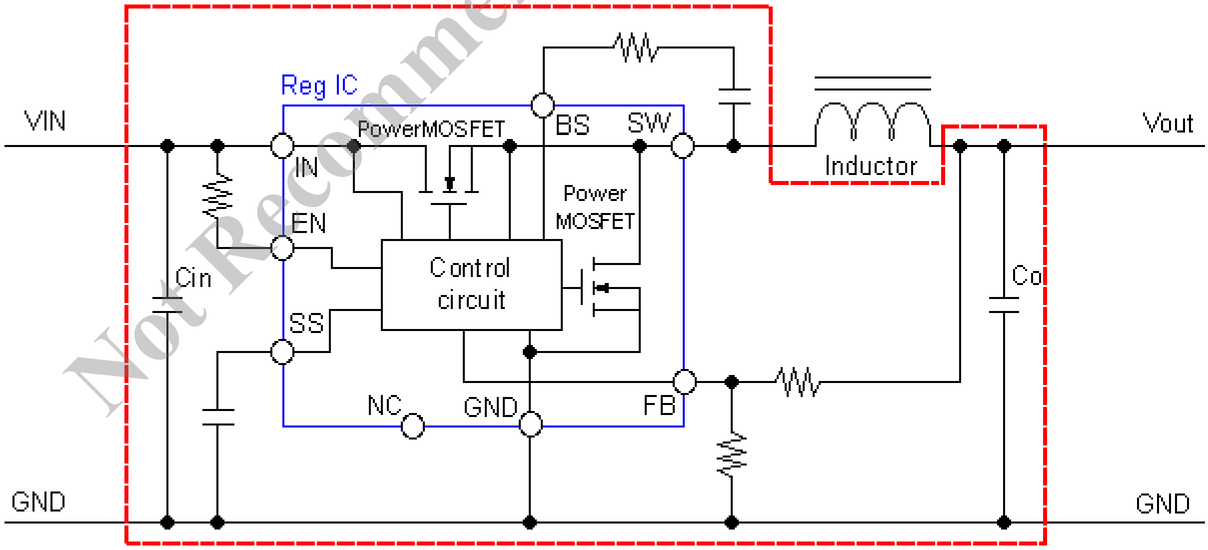



fig.31

In the area surrounded by the red dotted line within the fig31, don't insert the bead-core such as Ferrite-bead.

As for the pattern-design of printed-circuit-board, it is recommended that the parasitic-inductance of wiring-pattern is made small for the safety and the stability.

When bead-core was inserted, the inductance of the bead-core is added to parasitic-inductance of the wiring-pattern. By this influence, the surge-voltage occurs often, or , GND of IC becomes unstable, and also, negative voltage occurs often. Because of this, faulty operation occurs in the IC. The IC has the possibility of damage in the worst case.

About the Noise-reduction, fundamentally, Cope by "The addition of CR snubber circuit" and "The addition of BS serial resistor".

### 7.3.4 Reverse Bias Protection

A diode for reverse bias protection may be required between input and output in case the output voltage is expected to be higher than the input Pin voltage (a common case in battery charger applications).

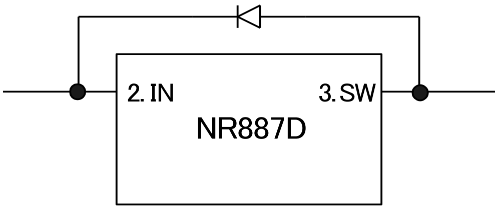



fig.32 Reverse bias protection diode

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