SFA0002

Description

The SFA0002 is the switching power supply IC for flyback circuit and has high accuracy error amplifier.

When the load of the power supply circuit becomes light, the operation of IC becomes the burst oscillation mode in order to improve the circuit efficiency.

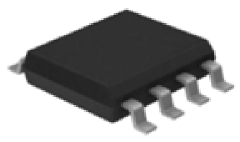
By employing the primary-side regulation, the IC realizes low component counts and design-friendliness, leading to downsizing and standardization of the power supply circuit.

Features

- AEC-Q100 Qualified
- Current Mode Type PWM Control
  (Switching frequency can be adjusted by external capacitor)
- Reducing External Component Count by Primary-side Regulation
- Built-in High Accuracy Error Amplifier
  (V_{FB} = 2.5 V ± 2%, −40°C to 125°C)
- Operation Mode
  Normal Operation: PWM Mode
  Light Load Operation: Burst Oscillation
- Soft Start Function
  (Startup time can be adjusted by external capacitor)
- Drive Output Stop Function
- Protections:
  Overcurrent Protection (OCP): Pulse-by-Pulse
  Overload Protection (OLP): Auto-restart
  Thermal Shutdown Protection (TSD) with Hysteresis: Auto-restart

Package

SOP8



Not to scale

Specifications

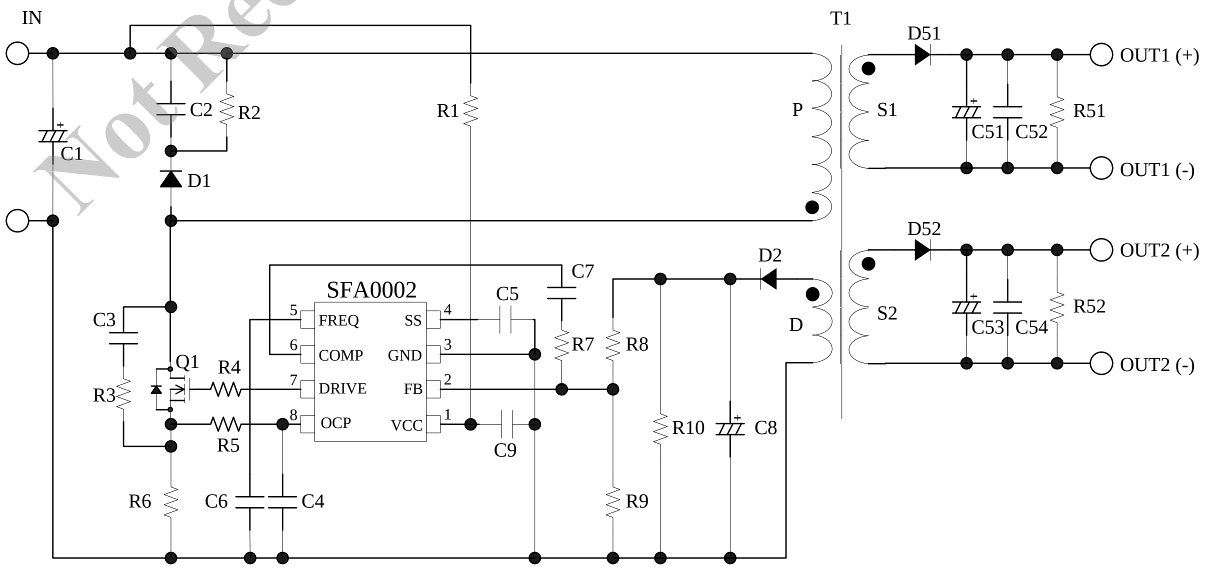
- Maximum Power Supply Voltage, V_{CC} 36 V
- Adjustable Switching Frequency (20 kHz to 200 kHz)

Applications

For following Isolation auxiliary power supply:

- Inverter
- On-board Charger (OBC)
- Battery Management System (BMS)

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
OCP Pin Voltage	V_{OCP}		−5 to 5	V	
SS Pin Voltage	V_{SS}		−0.3 to 9	V	
FB Pin Voltage	V_{FB}		−0.3 to 5	V	
VCC Pin Voltage	V_{CC}		0 to 36	V	
COMP Pin Voltage	V_{COMP}		−0.3 to 5	V	
FREQ Pin Voltage	V_{FREQ}		−0.3 to 5	V	
DRIVE Pin Peak Current	$I_{DRV(PEAK)}$		−270 to 540	mA	
DRIVE Pin DC Current	$I_{DRV(DC)}$		−90 to 180	mA	
Power Dissipation	P_D	* Mounting on PCB	1.2	W	
Junction Temperature	T_J		−40 to 150	°C	
Storage Temperature	T_{stg}		−40 to 150	°C	

* PCB: 42 mm × 32 mm in size, 1 mm in thickness

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
VCC Pin Voltage	V_{CC}		6	—	24	V	
Switching Frequency	f_{OSC}		20	—	200	kHz	

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = −40 °C to 125 °C, VCC = 14 V, and FB = SS = OCP = 0 V.

The following electrical characteristics in T_A = −40 °C to 125 °C are guaranteed by design. The shipping test temperature of the products is −30 °C, 25 °C, and 125 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		4.9	5.1	5.3	V	
Operation Stop Voltage	$V_{CC(OFF)}$		4.4	4.6	4.8	V	
Circuit Current in Operation	$I_{CC(ON)}$		1.0	2.0	3.2	mA	
Circuit Current in Non-operation	$I_{CC(OFF)}$	VCC = 4.8 V	0.3	0.5	1.0	mA	
Normal Operation							
SS Pin High Threshold Voltage of OLP Operation	V_{HSS}		1.9	2.0	2.1	V	
SS Pin Low Threshold Voltage of OLP Operation	V_{LSS}		0.9	1.0	1.1	V	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SS Pin Voltage Hysteresis of OLP Operation	ΔV_{SS}	$V_{HSS} - V_{LSS}$	0.9	1.0	1.1	V	
SS Pin Source Current	$I_{SRC(SS)}$	SS = 0.9 V	−19	−15	−11	µA	
SS Pin Sink Current	$I_{SNK(SS)}$	SS = 2.1 V	13	17	21	µA	
Switching Frequency	$f_{OSC(200p)}$	FREQ = 200 pF	85	100	115	kHz	
FREQ Pin Source Current	$I_{SRC(FREQ)}$	FREQ = 0.9 V	−33	−30	−27	µA	
FREQ Pin Sink Current	$I_{SNK(FREQ)}$	FREQ = 2.1 V	75	85	95	µA	
Oscillation Circuit High Threshold Voltage	V_{HF}		1.9	2.0	2.1	V	
Oscillation Circuit Low Threshold Voltage	V_{LF}		0.9	1.0	1.1	V	
Maximum Duty Cycle	D_{MAX}	FREQ = 200pF	70	74	78	%	
Slope Compensation Rate	SLP		2.1	2.5	2.9	mV/%	
Feedback Voltage	V_{FB}		2.45	2.50	2.55	V	
Burst Operation Threshold Voltage	V_{BURST}	FREQ = 200pF, COMP pin voltage increases from 0 V.	—	0.18	—	V	
Drive Voltage	V_{DRIVE}	FREQ = 3 V, 1 pulse	7.6	8.3	9.0	V	
Minimum Drive Voltage	$V_{DRIVE(MIN)}$	VCC ≥ 6 V, FREQ = 3 V, 1 pulse	4	—	—	V	
Minimum On-time	$t_{ON(MIN)}$	OCP = 1 V, DRIVE = 680 pF	—	170	—	ns	
Protection Function							
Leading Edge Blanking Time*	t_{BW}		—	100	—	ns	
OCP Threshold Voltage	V_{OCP}		0.46	0.50	0.54	V	
OLP Delay Time	t_{OLP}	SS = 10 nF	32	42	52	ms	
Drive Stop Threshold Voltage	V_{ST}		3.5	4.0	4.5	V	
Thermal Shutdown Operating Temperature*	$T_{JH(TSD)}$		150	165	—	°C	
Thermal Shutdown Release Temperature*	$T_{JL(TSD)}$		—	150	—	°C	

* Guaranteed by design.

4. Performance Curves

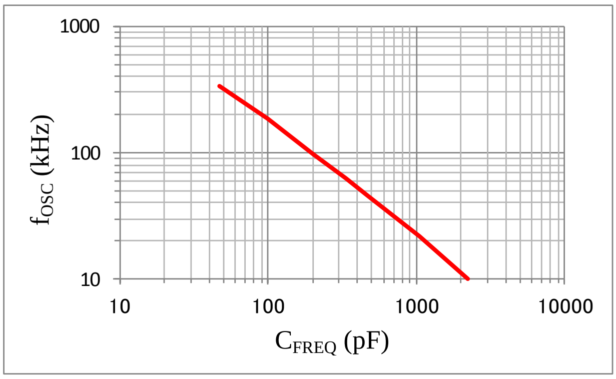


Figure 4-1. Switching Frequency, f_{OSC}, vs. FREQ Pin Capacitor, C_{FREQ}

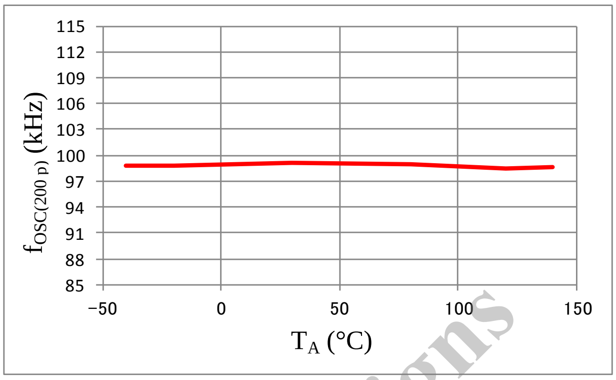


Figure 4-2. Switching Frequency (FREQ = 200 pF) Temperature Characteristics

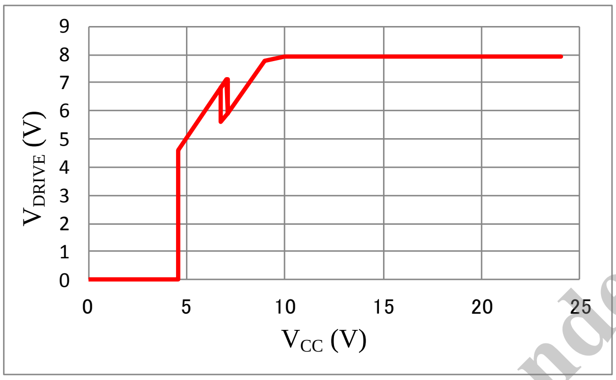


Figure 4-3. DRV Pin Voltage, V_{DRIVE}, vs. VCC Pin Voltage, V_{CC}

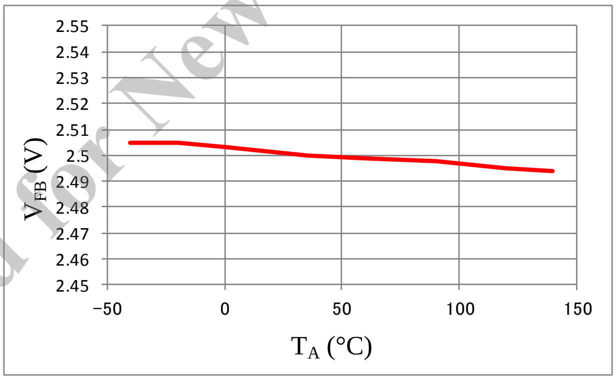


Figure 4-4. Feedback Voltage, V_{FB}, Temperature Characteristics

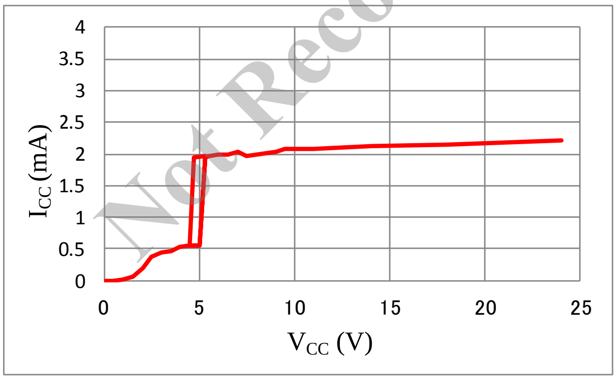
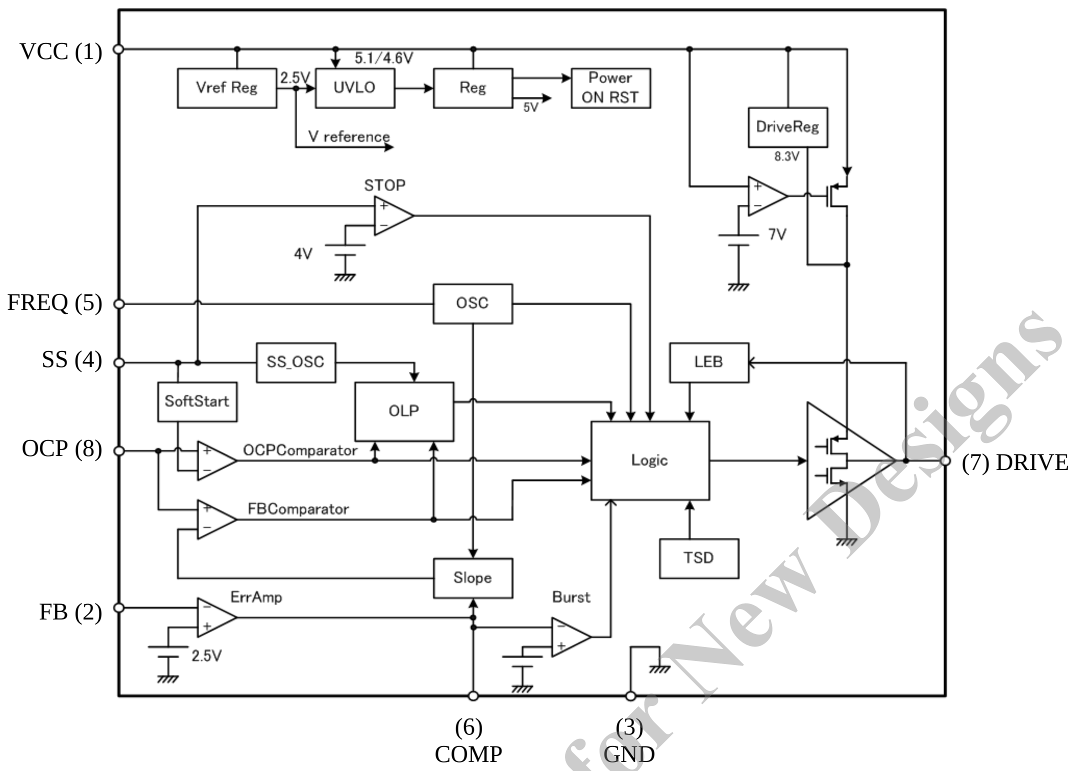
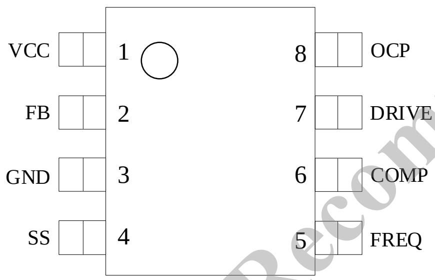


Figure 4-5. VCC Pin Current, I_{CC}, vs. VCC Pin Voltage ,V_{CC}

5. Block Diagram



6. Pin Configuration and Definitions



Pin No.	Pin Name	Function
1	VCC	Power supply voltage input
2	FB	Constant voltage control signal input
3	GND	Ground
4	SS	Connecting capacitor for soft-start time and OLP delay time setting, and the DRIVE pin stop signal input
5	FREQ	Connecting capacitor for switching frequency setting
6	COMP	Connecting capacitor for phase compensation
7	DRIVE	Gate drive output
8	OCP	Overcurrent detection signal input

7. Typical Application

In applications having a power supply specified such that the drain pin of external power MOSFET has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (C2, R2, and D1) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor or a resistor-capacitor (C3 and R3) combination should be added between the drain pin and the source pin.

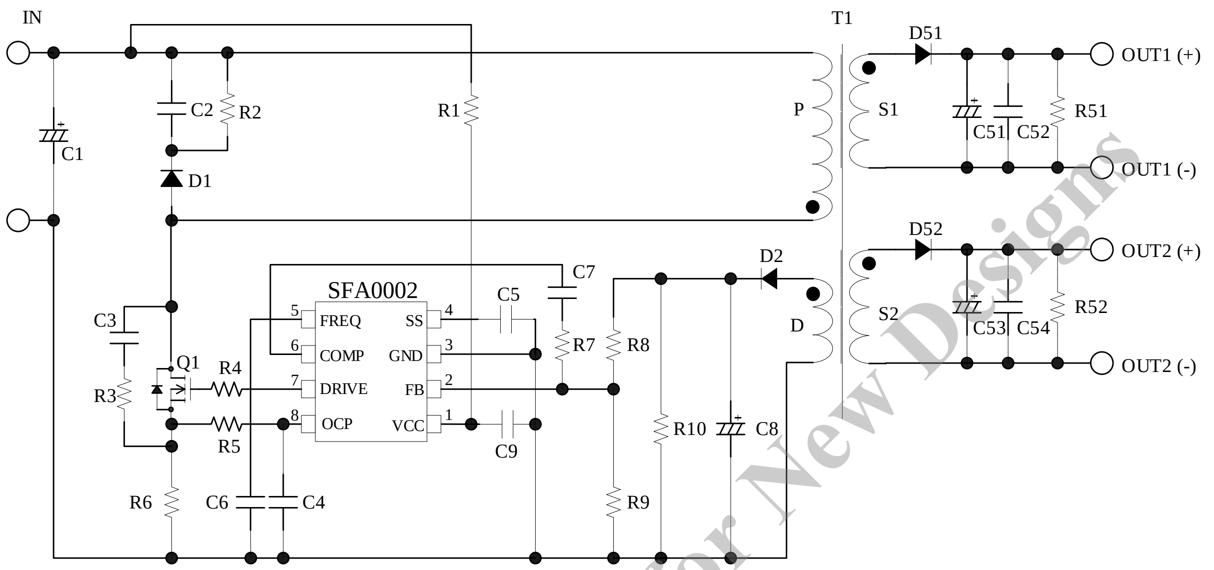


Figure 7-1. Flyback Step-up/ Step-down Converter (Primary-side Detection)

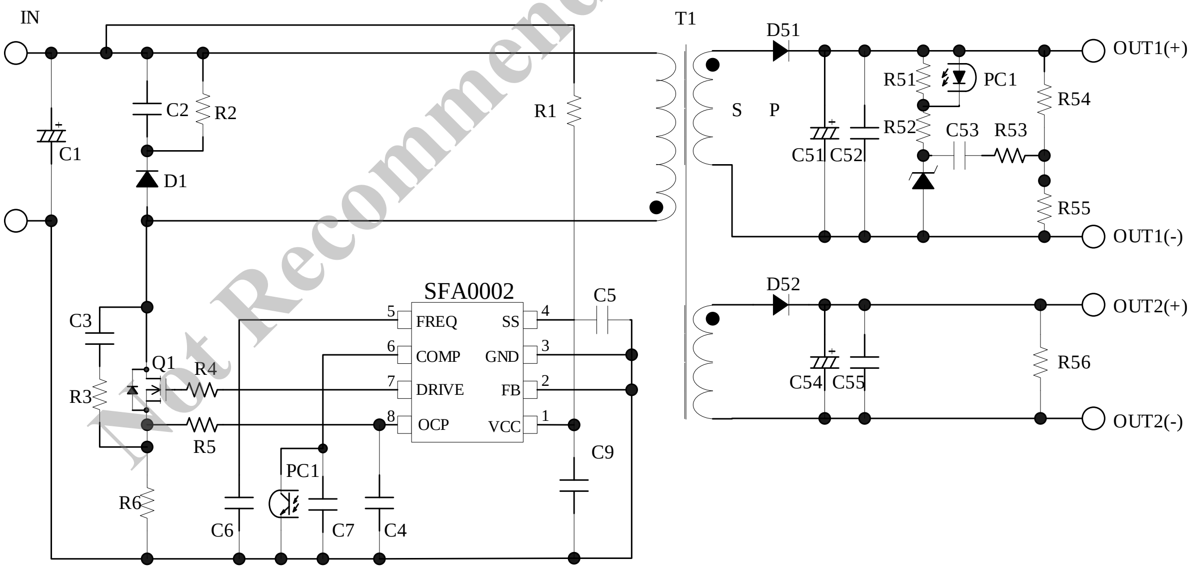
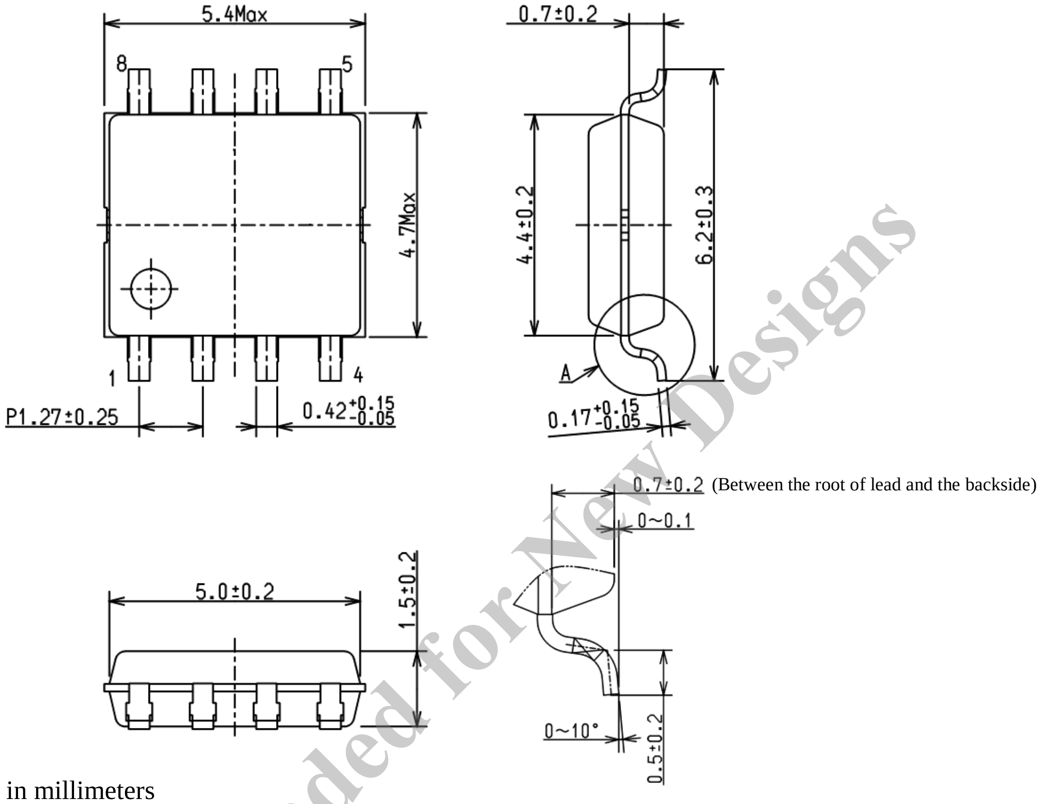


Figure 7-2. Flyback Step-up/ Step-down Converter (Secondary-side Detection)

8. Physical Dimensions

- **SOP8**

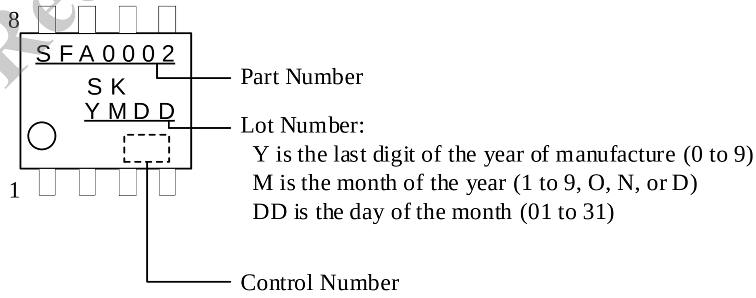


Enlarged View of A

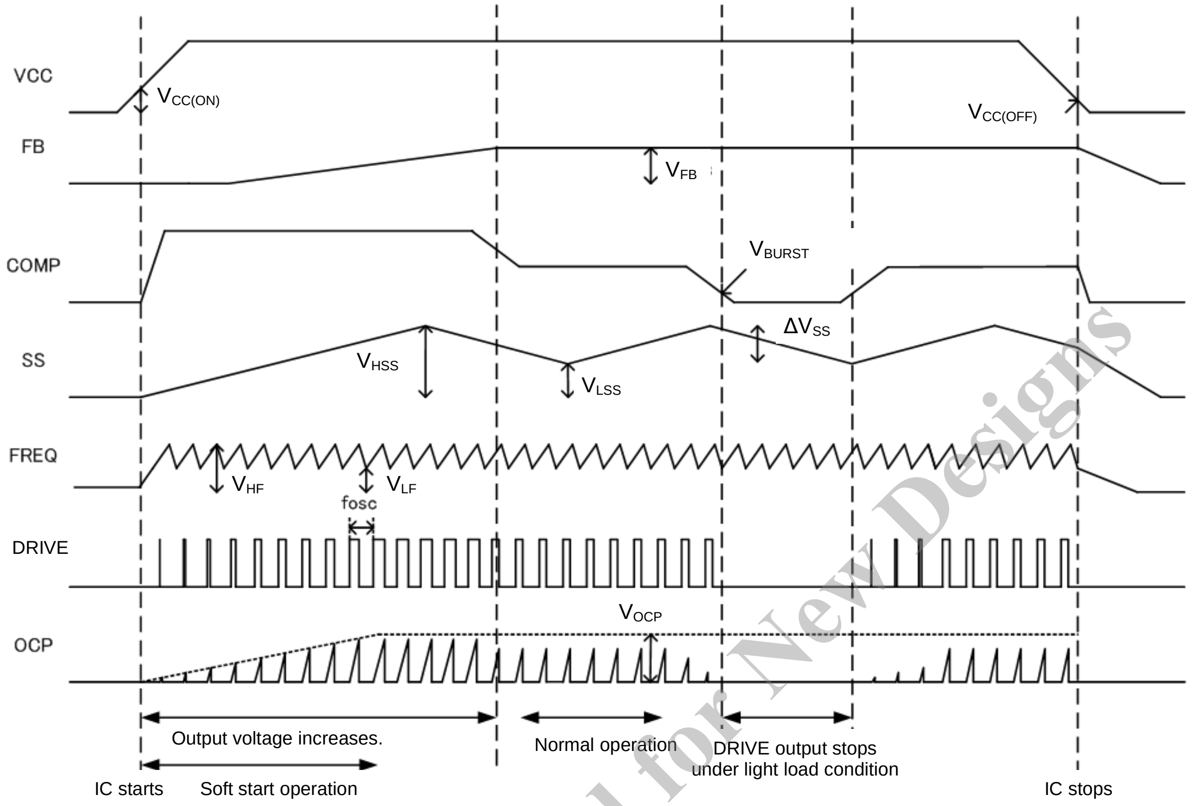
NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)

9. Marking Diagram



10. Timing Chart



When the COMP pin voltage decreases to V_{BURST} or less, the IC operation becomes into burst oscillation mode. The on-time and the intermittent cycle depend on the specification of typical application circuit.

Figure 10-1. Normal Operation

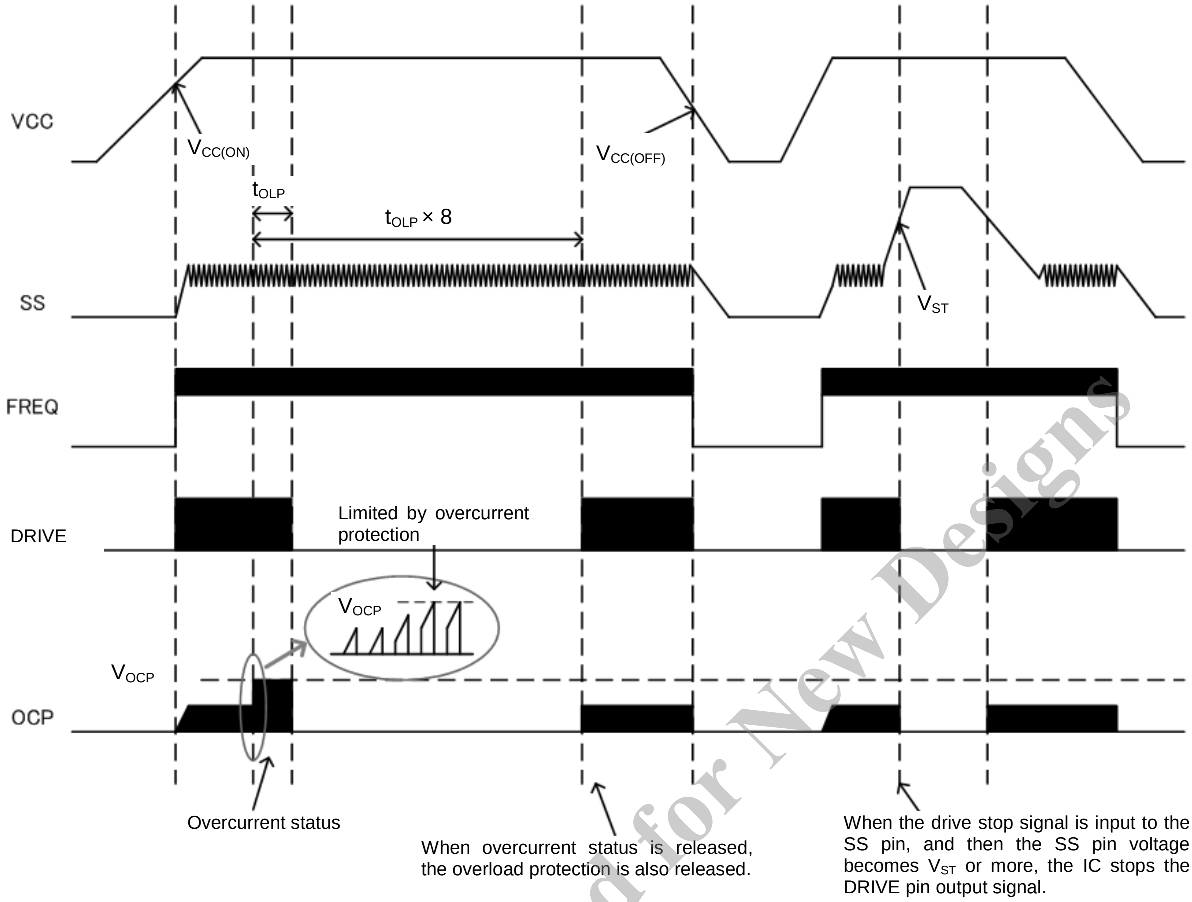


Figure 10-2. Protection Function

11. Operational Description

Unless otherwise specified, the characteristics values are shown in typical value. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

11.1. Pin Descriptions

11.1.1. VCC

The VCC pin is the power input pin of the IC.

When the VCC pin voltage fluctuates greatly, the IC may malfunction. When the impedance of power supply line is high, it is required to add resistors and capacitors to the VCC pin in order to suppress the VCC pin voltage fluctuation.

11.1.2. FB

The FB pin is the input of the output voltage of a feedback signal. The IC controls the FB pin voltage to V_{FB} = 2.50 V (see Section 11.4).

11.1.3. GND

The GND pin is the IC control ground pin. Since the fluctuation of the ground pin potential may cause the IC malfunction, the control ground trace should be separated from power ground and connected to the GND pin as short as possible. Please pay attention to design of the control ground trace to avoid the effect from the high frequency current line.

11.1.4. SS

The SS pin has three functions as follows:

- Setting the soft start time (see Section 11.3)
- Stopping the drive (see Section 11.7)
- Setting the OLP (Over Load Protection) delay time (see Section 11.9)

The capacitor, C_{SS}, for setting the soft start time and the OLP delay time is connected to the SS pin. These both functions should be taken into account in setting the value of C_{SS}.

In normal operation, the waveform of CSS pin voltage is triangular. The SS pin charges the C_{SS} by $I_{SRC(SS)}$ = −15 µA and discharges the C_{SS} by $I_{SNK(SS)}$ = 17 µA when the SS pin voltage reaches V_{HSS} = 2.0 V. The SS pin starts to charge again when the SS pin voltage decreases to V_{LSS} = 1.0 V.

11.1.5. FREQ

The FREQ pin is connected to the capacitor, C_{FREQ}, for setting the oscillation frequency of the DRV pin output. For the setting of oscillation frequency, see Section 11.6.

11.1.6. COMP

The COMP pin is the output pin of an internal error amplifier. The capacitor for phase compensation is connected to the COMP pin. The capacitance is set according to the actual operation.

When the secondary output voltage is controlled using an optocoupler, an optocoupler is connected to the COMP pin as shown in Figure 7-2.

11.1.7. DRV

The gate of the power MOSFET is connected to the DRV pin. The power of the DRV pin is supplied by the VCC pin via the internal regulator. The relation between the VCC pin voltage and the DRV pin voltage is shown in Figure 11-1. The DRV pin voltage is clamped at V_{DRIVE} = 8.3 V. The internal regulator is switched by VCC pin voltage of around 7 V and suppresses the drive voltage drop at the VCC pin voltage drop.

The source potential of the power MOSFET is increased by about 0.5 V due to a drain current detection resistor. Therefore, it is required to select the power MOSFET with the gate threshold voltage that is lower enough than the minimum drive voltage, 4 V (min.).

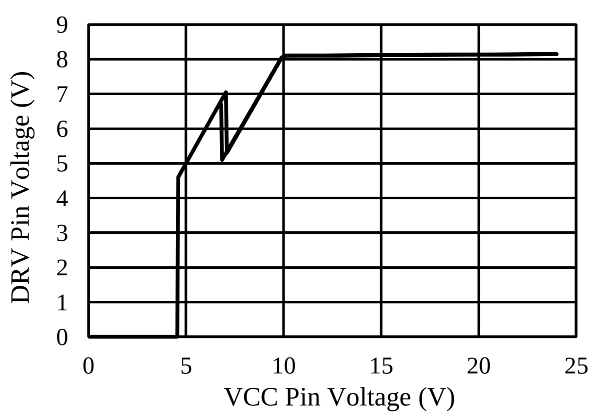


Figure 11-1. VCC Pin Voltage vs. DRV Pin Voltage

11.1.8. OCP

The OCP pin is the detection pin of the drain current of the power MOSFET. The current detection resistor, R_{OCP}, is connected between the source and GND of the power MOSFET, and the voltage is input to the OCP pin.

The drain current value input to the OCP pin is used for the output voltage control (see Section 11.4) and the overcurrent protection.

For the setting of overcurrent detection resistor, see Section 11.8.

11.2. IC Startup

Applying a voltage to the VCC pin starts the internal regulator. The regulator is a highly accurate power supply of 2.5 V ± 2%.

When the VCC pin voltage reaches the Operation Start Voltage, $V_{CC(ON)}$ = 5.1 V, or higher, the power supply in the IC turns on and starts the operation. When the VCC pin voltage decreases to be the Operation Stop Voltage, $V_{CC(OFF)}$ = 4.6 V, or lower, the power supply in the IC turns off and stops the operation.

11.3. Soft Start Function

The IC operates by soft start in the power supply startup. This reduces the voltage and current stress of the power MOSFET and the secondary rectifier diode.

The soft start period is set by the capacitor, C_{SS}, connected to the SS pin. When the VCC pin voltage is $V_{CC(ON)}$ or higher after the power is applied, the IC starts the operation; and the C_{SS} is charged by the SS Pin Source Current, $I_{SRC(SS)} = -15$ µA.

When the power is supplied, the SS pin voltage starts increasing. The OCP threshold voltage also increases proportional to the SS pin voltage until the SS pin voltage reaches V_{HSS} = 2.0 V. Thus the drain current gradually increases in this period. When once the SS pin voltage reaches the V_{HSS}, the OCP threshold voltage is fixed at V_{OCP} = 0.50 V.

The approximate time of soft start operation, t_{SS}, is calculated by the following equation.

$$t_{SS}\ (s) = V_{HSS} \times \frac{C_{SS}}{|I_{SRC(SS)}|}$$

$$= 2.0\ V \times \frac{C_{SS}\ (\mu F)}{|-15\ \mu A|} \quad (1)$$

The C_{SS} value should be set with the delay time of OLP, t_{OLP}, taken into account. If the C_{SS} value is too small, the overload protection is activated in the startup; and the startup failure may be caused.

The recommended C_{SS} value is 0.01 µF to 0.47 µF, and should be determined by confirming the actual operation.

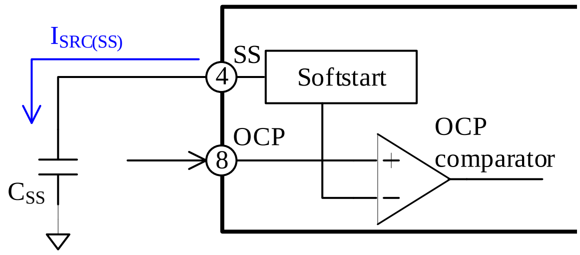


Figure 11-2. SS Pin Peripheral Circuit

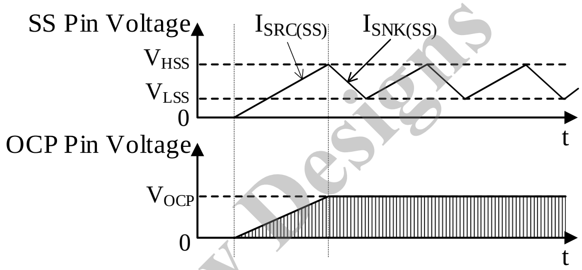


Figure 11-3. Soft Start Operation

11.4. Constant Voltage Control

The output voltage control of switching power supply uses the current-mode control method that provides the high speed response and stable operation. The IC has the error amplifier between the FB pin and the COMP pin, and controls the FB pin voltage to V_{FB} = 2.50 V.

Without an optocoupler, the secondary output voltage is controlled by detecting the voltage coupled by the secondary output and the transformer in the primary side, using the auxiliary winding, D, as shown in Figure 11-4. The relation between the smoothing voltage, V_D, and the secondary output voltage, V_{OUT}, is determined by the ratio of the auxiliary winding turns, N_D, and the secondary winding turns, N_S, as shown in Equation (2).

$$V_{OUT} = \frac{N_S}{N_D} \times V_D \quad (2)$$

V_D is divided by resistors. The divided voltage is input to the FB pin. The IC controls the FB pin voltage to V_{FB} = 2.50 V. Thus, the smoothing voltage, V_D, is calculated by the following equation.

$$V_D = \frac{(R8 + R9)}{R9} \times V_{FB} \quad (3)$$

The secondary output voltage, V_{OUT}, is calculated by the following equation.

$$V_{OUT} = \frac{N_S}{N_D} \times \frac{(R8 + R9)}{R9} \times V_{FB} \quad (4)$$

The actual V_{OUT} and the calculated value in Equation (4) do not match because of the leakage inductance between the secondary-side winding and the auxiliary winding, and the difference of the forward voltage, V_F, between the secondary rectifier diode, D51, and the auxiliary winding diode, D2. Therefore, R8 and R9 must be adjusted by confirming the actual operation.

Where $N_D = N_S$ and $V_{OUT} = V_D$, the accuracy of the secondary output voltage is improved by using the same diode products for D51 and D2.

When there is a big difference of power dissipation between the auxiliary winding and the secondary side, the load regulation is degraded due to the leakage inductance of a transformer. In this case, the dummy resistor, R10, is connected across the auxiliary winding. The value of R10 is adjusted by confirming the actual operation since it differs depending on the power supply specification.

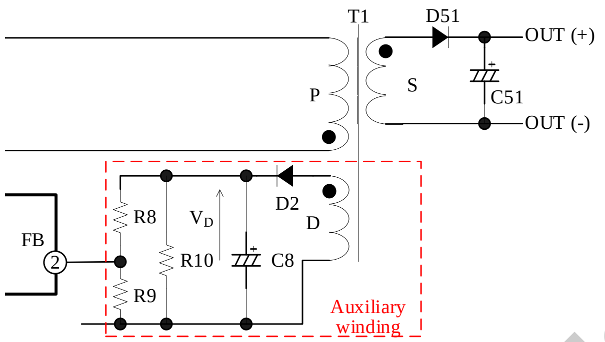


Figure 11-4. Detection by Auxiliary Winding

The voltage control operation in light/heavy load is as follows: (see Figure 11-5)

- **Light Load Conditions**

When the auxiliary winding voltage, V_D, and the FB pin voltage increase according to the output voltage rise, the COMP pin voltage decreases.

The IC generates the target value of the FB comparator by adding the slope compensation signal to the COMP pin voltage. The IC controls the DRV output duty cycle by comparing the peak of the target value and the OCP pin voltage (the drain current of the power MOSFET detected by detection resistor).

When the COMP pin voltage decreases, the target value of the FB comparator drops. As a result, the drain peak current of the power MOSFET decreases to suppress the output voltage rise.

- **Heavy Load Conditions**

In this case, contrary to the operation describe above, the target voltage of FB comparator increases. As a result, the drain peak current also increases to suppress the output voltage drop.

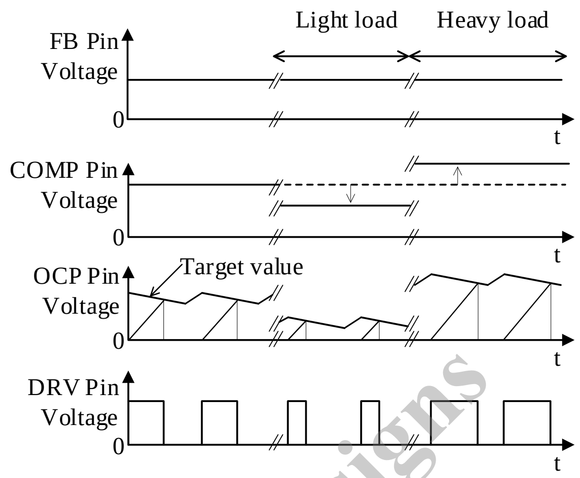


Figure 11-5. Constant Voltage Operation

11.5. Burst Function in Light Load

When the output voltage of the power supply decreases, the on-time of DRV pin shortens due to the COMP pin voltage reduction. As a result, the output voltage is controlled to be constant. However, the on–time of DRV pin cannot be shorter than the Minimum On-time, $t_{ON(MIN)}$. Therefore, the operation of the IC is automatically switched to the burst oscillation operation (intermittent oscillation) in light load.

When the COMP pin voltage decreases to Burst Operation Threshold Voltage, V_{BURST} = 0.18 V, or lower, the DRV pin output is stopped. Then, the output voltage decreases, resulting in the decrease of FB pin voltage. This increases the COMP pin voltage; and the DRV pin oscillates again. As just described, the burst oscillation operation of the DRV pin is repeated in light load. The following factors depend on the application circuit and power supply specification.

- the burst oscillation frequency and on-time in burst oscillation operation
- the stop period of DRV pin

11.6. Oscillation Frequency Setting

The oscillation frequency of the DRV pin output is set by the capacitor, C_{FREQ}, connected to the FREQ pin (see Figure 11-6).

The waveform of the FREQ pin voltage becomes triangular due to the charge/discharge of C_{FREQ}. C_{FREQ} is charged by $I_{SRC(FREQ)}$ = −30 μA as shown in Figure 11-7. When the FREQ pin voltage reaches V_{HF} = 1.0 V, C_{FREQ} is discharged by $I_{SNK(FREQ)}$ = 85 μA. When the FREQ pin voltage decreases to V_{LF} = 1.0 V, C_{FREQ} is charged by $I_{SRC(FREQ)}$ again.

The oscillation frequency of the DRV pin is determined by the frequency of the triangular waveform.

In addition, the maximum duty cycle is controlled by the ratio of charge and discharge. For the setting of oscillation frequency of the DRV pin, see Figure 11-8. Ultimately, the confirmation of actual operation is required.

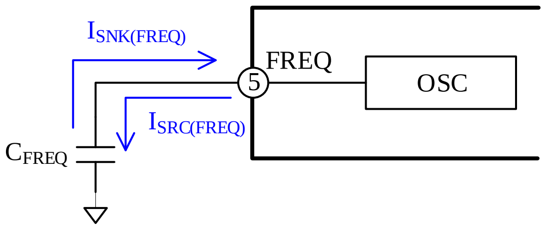


Figure 11-6. FREQ Pin Peripheral Circuit

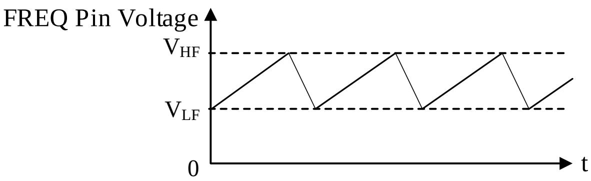


Figure 11-7. FREQ Pin Voltage Waveform

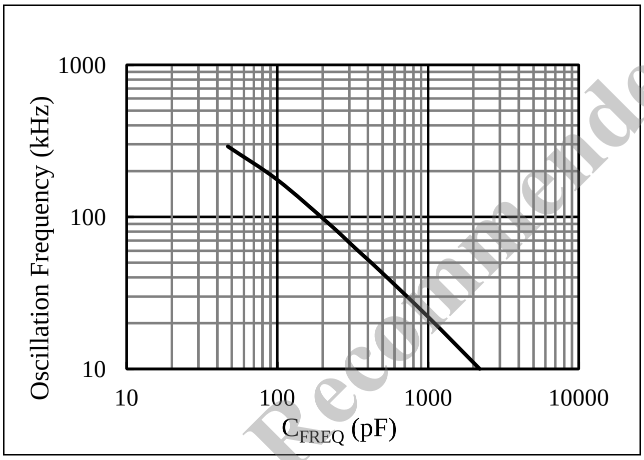


Figure 11-8. Oscillation Frequency vs. C_{FREQ} (Reference)

11.7. Drive Stop Function

The IC has the drive stop function. When a voltage is externally applied to the SS pin, the function is activated, forcibly fixes the DRV pin output to low level, and stops the oscillation. The input voltage to the SS pin must be set higher than 4.5 V and lower than 9 V.

When the SS pin voltage is lower than Drive Stop Threshold Voltage, V_{ST}, after the external applied voltage is stopped, the DRV pin starts oscillating again.

11.8. Overcurrent Protection (OCP)

The IC has the pulse-by-pulse Overcurrent Protection (OCP).

When the OCP pin voltage exceeds the OCP Threshold Voltage, V_{OCP} = 0.50 V, at every switching cycle, the OCP is activated. When the OCP is activated, it turns off the DRV pin output to turn off the power MOSFET, resulting in suppressing the peak of drain current.

A high frequency switching current flows to the detection resistor. If the resistor with high internal inductance is used, the malfunctions may be caused. The resistor with low internal inductance and high surge capability must be selected. In addition, when the IC malfunctions due to surges in switching operation, the RC filter is added to the OCP pin.

- **Design Example of Current Detection Resistor**

The value of the current detection resistor, R_{OCP}, is set according to the following calculation example in discontinuous operation as a reference. Since the R_{OCP} and the calculation example do not match in continuous operation, it is required to ultimately adjust by confirming the actual operation.

The peak drain current, I_{PEAK}, in discontinuous operation is calculated by the following equation.

$$I_{PEAK} = \frac{2 \times P_{OUT}}{\eta \times V_{IN} \times D} \tag{5}$$

Where:
V_{IN} is input voltage,
P_{OUT} is output power,
η is efficiency and
D is duty cycle of the power MOSFET.

The relation between the power, P, and the drain current, I_D, is shown in the following equation.

$$P = \frac{1}{2} \times L \times I_D^{\,2} \tag{6}$$

The drain current is proportional to $\sqrt{P}$. If the OCP is designed to operate at 130% of the rated load (the maximum output power at the minimum input voltage), the peak of drain current at the OCP operation point is about 114% ($\sqrt{130\%}$) of I_{PEAK} at the rated load.

The current detection resistance, R_{OCP}, is calculated by the following equation.

$$R_{OCP} = \frac{V_{OCP} \times \eta \times V_{IN(MIN)} \times D_{(MAX)}}{114\% \times 2 \times P_{OUT(MAX)}} \tag{7}$$

Where:
$D_{(MAX)}$ is the duty cycle at the minimum input voltage, $V_{IN(MIN)}$ and the maximum output power, $P_{OUT(MAX)}$,
η is efficiency, and

V_{OCP} is the OCP Threshold Voltage (0.50 V).

The waveform of the current flowing through the R_{OCP} becomes triangular in discontinuous operation. The RMS current is calculated by the following equation.

$$I_{RMS} = I_{PEAK} \times \sqrt{\frac{D_{(MAX)}}{3}} \quad (8)$$

The power consumption of R_{OCP} is calculated by the following equation.

$$P_{ROCP} = R_{OCP} \times {I_{RMS}}^2 \quad (9)$$

11.9. Overload Protection (OLP)

The IC has the Overload Protection (OLP). When the overload state (where the peak of drain current is limited by OCP, or the DRV pin operates in the maximum duty cycle) continues for a certain time, t_{OLP}, the OLP is activated; and the oscillation of the DRV pin is stopped. This reduces the stress of the power MOSFET and the secondary rectifier diode.

The delay time of the OLP, t_{OLP}, is determined by the capacitance of C_{SS} connected to the SS pin. When C_{SS} is 10 nF, t_{OLP} becomes 42 ms. In another capacitance, the approximate value of t_{OLP} can be calculated by the following equation.

$$t_{OLP}(ms) = 42\ ms \times \frac{C_{SS}\ (nF)}{10\ nF} \quad (10)$$

The soft start time in Section 11.3 should be taken into account in setting the C_{SS} capacitance.

The oscillation stop period of the DRV pin is $7 \times t_{OLP}$. The DRV pin repeats oscillation and stop on an $8 \times t_{OLP}$ cycle until the overload state is dissolved.

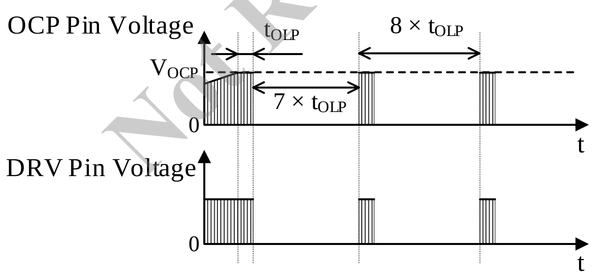


Figure 11-9. Overload Protection Operation

11.10. Thermal Shutdown (TSD)

The IC has the Thermal Shutdown (TSD). When the junction temperature of the IC reaches $T_{JH(TSD)}$ = 165 °C, the DRV pin oscillation is stopped. When the junction temperature of the IC decreases to $T_{JL(TSD)}$ = 150 °C or lower due to the oscillation stop, the DRV pin oscillation is restarted.

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