3 phase BLDC Motor Driver IC

SI-6633M

Application Note

May, 2013 Ver.1.3

MCD division low voltage motor group

This application note is applied to SI-6633M, which is motor driver for 3-phase brushless motor.
Care should be taken since the contents may be changed without any notice.
This application note, which shows in Japanese and English, shall be prior to Japanese.
About the latest information, please refer to our charge section.

(Index)

1. General Description

SI-6633M is motor driver for 3-phase brushless motor with 2A (DC)/4A (peak) as current ratings.
The device has output DMOSFET, pre-drive, PWM current control and protection etc in 1 package.
The device is also applied to 30V of VBB as recommended voltage range.

2. Features

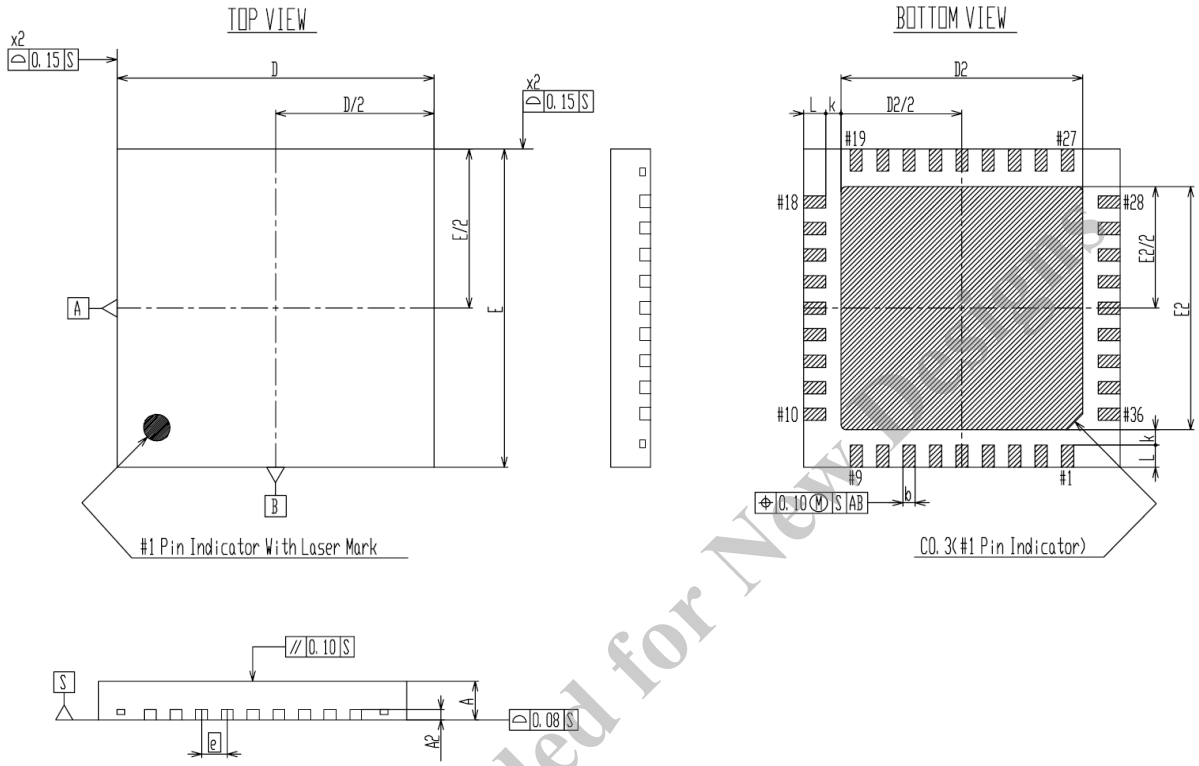
- Motor supply voltage range V_{BB}=10～30V
- Output DMOSFETs are integrated. Output current I_{OUT}=2A (DC)/4A (peak)
- Hall Input
- Current control function
  - Fixed frequency PWM (Internal PWM) with peak current control
  - PWM control by speed control signal with analog voltage (External PWM)
  - PWM control by logic input (Logic PWM)
- Protection
  - Over current protection
  - Over voltage protection
  - Thermal shutdown
  - Under voltage lock out
  - Motor lock detection
    - ※ Alarm output pin (FLAG) is active when any protection is activated.
- Motor speed output by hall input transition (FG)
- Synchronous rectification with low power dissipation
- Select for synchronous rectification (active/passive).
- Stand-by mode

※Although the device may be protected from damaged with protection circuit in the device from design point of view, it can't be guaranteed the device being damaged by the protections in the device.
In the design of set, please take care to avoid abnormal condition with all the countermeasures you can take.

3. Package information, recommended foot print

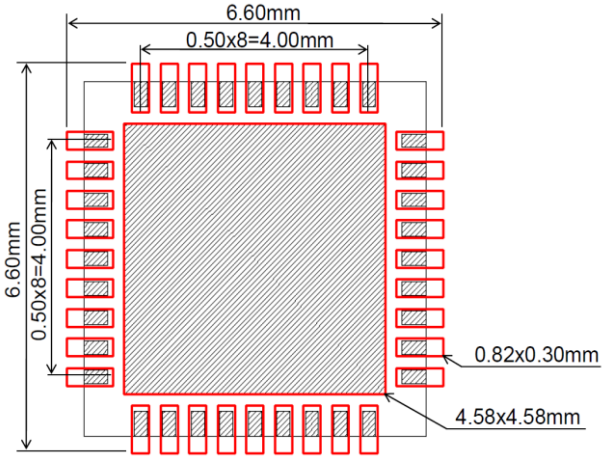
Unit : mm

QFN36 package with exposed pad



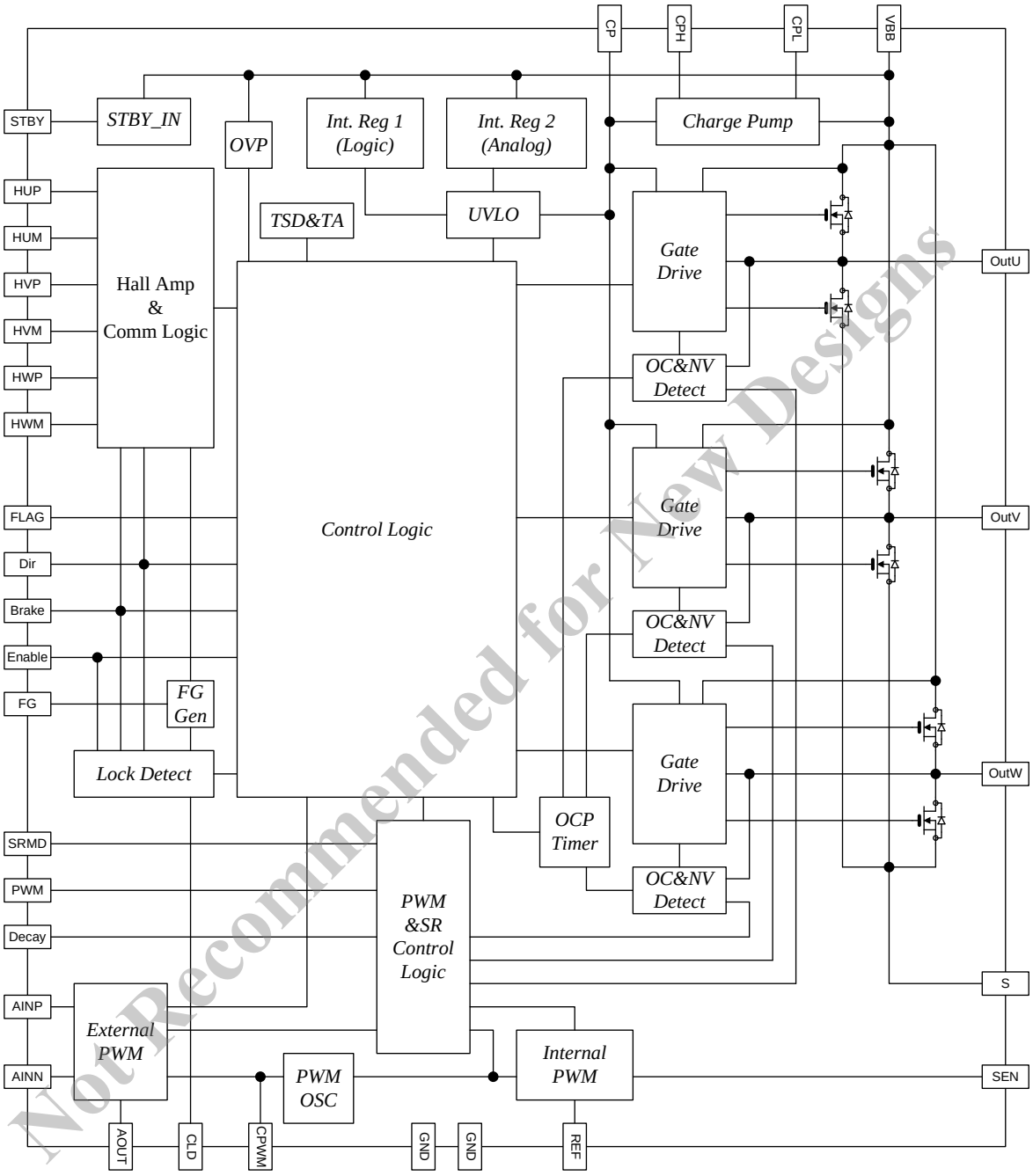
SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.18	0.23	0.28
D	5.90	6.00	6.10
D2	4.43	4.58	4.73
E	5.90	6.00	6.10
E2	4.43	4.58	4.73
e		0.50 BSC.	
k	0.25	—	—
L	0.32	0.42	0.52

Recommended foot print (red line)

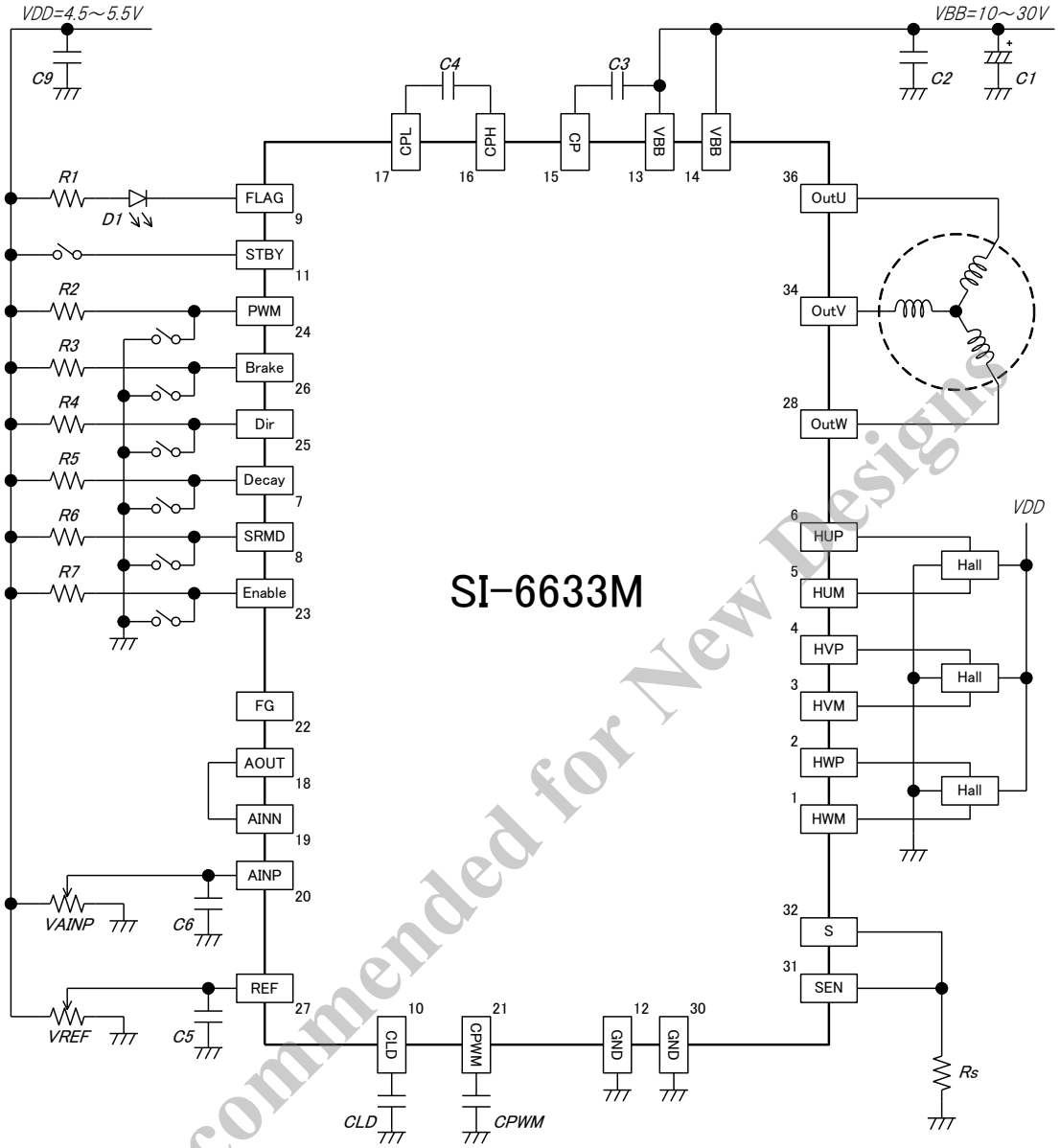


4. Block diagram and application circuit

Block diagram



Application circuit – Hall element input



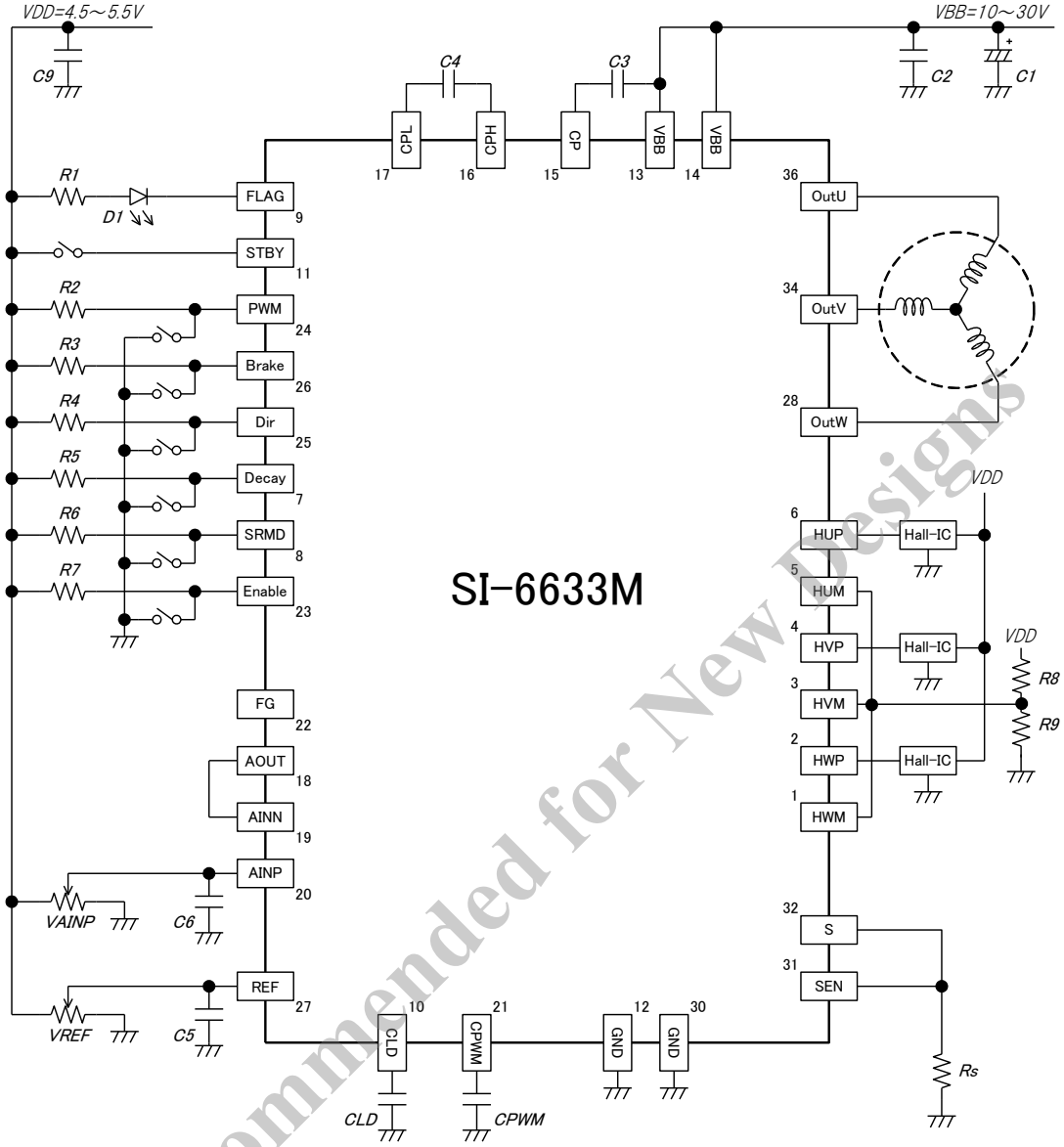
Component value for reference

C1	: 100μF/50V	R1	: 1kΩ	CLD※1	: 0.1μF
C2※1	: 0.1μF/50V	R2	: 10kΩ	CPWM※1	: 1000pF
C3	: 0.1μF/16V	R3	: 10kΩ	Rs※1※2	: 0.1Ω
C4	: 0.1μF/50V	R4	: 10kΩ		
C5	: (option)	R5	: 10kΩ		
C6	: (option)	R6	: 10kΩ		
		R7	: 10kΩ		

※1:These components should be mounted as close to the device as possible.

※2:Care should be taken with power dissipation.

Application circuit – Hall IC input



Component value for reference

C1	: 100µF/50V	R1	: 1kΩ	R8	: 10kΩ
C2※1	: 0.1µF/50V	R2	: 10kΩ	R9	: 10kΩ
C3	: 0.1µF/16V	R3	: 10kΩ	CLD*1	: 0.1µF
C4	: 0.1µF/50V	R4	: 10kΩ	CPWM*1	: 1000pF
C5	: (option)	R5	: 10kΩ	Rs*1*2	: 0.1Ω
C6	: (option)	R6	: 10kΩ		
		R7	: 10kΩ		

※1：These components should be mounted as close to the device as possible.

※2：Care should be taken with power dissipation.

☆Care should be taken to avoid the noise on V_{DD} line.
Switching noise from PCB traces, where high current flows, to the V_{DD} line should be minimized because the noise level more than 0.5V on the V_{DD} line may cause malfunctioning operation.
The tip for avoiding such problem is to separate the logic GND (S-GND) and the power GND (P-GND) on a PCB, and then connect them together at IC GND pin.

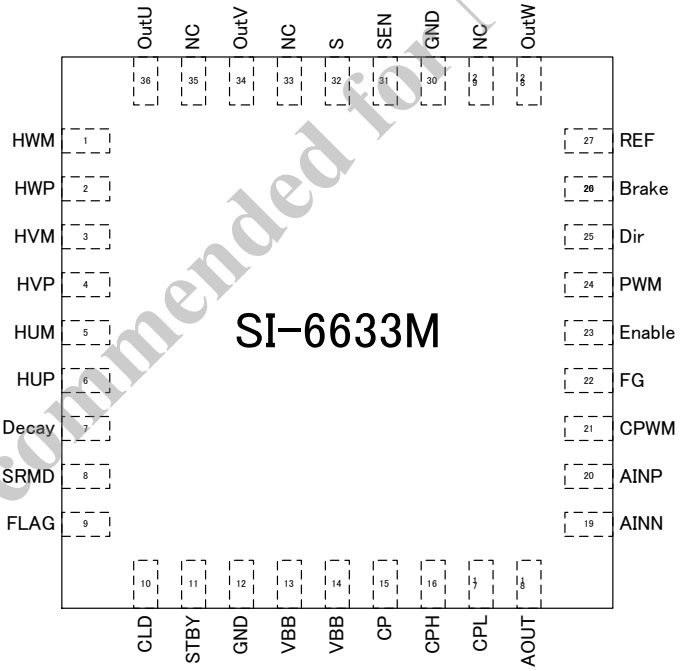
☆Application circuit is also applied to evaluation board for the device.

5. Pin assignment

№	Pin name	Function
1	HWM	Hall input W-
2	HWP	Hall input W+
3	HVM	Hall input V-
4	HVP	Hall input V+
5	HUM	Hall input U-
6	HUP	Hall input U+
7	Decay	Select for decay mode
8	SRMD	Select for synchronous rectification
9	FLAG	Output for protection detected
10	CLD	Setting for lock detection timer
11	STBY	Stand-by input
12	GND	Ground
13	VBB	Motor power supply
14	VBB	Motor power supply
15	CP	Reservoir pin for charge pump
16	CPH	Pumping for charge pump - High
17	CPL	Pumping for charge pump - Low
18	AOUT	Amplifier output and 100% ON input
19	AINN	Minus pin for amplifier input
20	AINP	Plus pin for amplifier input
21	CPWM	Setting pin for PWM frequency
22	FG	Output for FG signal
23	Enable	Reset for lock counter and Enable input

№	Pin name	Function
24	PWM	External PWM control input
25	Dir	Direction input
26	Brake	Brake input
27	REF	Analog input for internal PWM current control
28	OutW	Output for W phase
29	N.C.	No Connection
30	GND	Ground
31	SEN	Current sensing input
32	S	Source pin
33	N.C.	No Connection
34	OutV	Output for V phase
35	N.C.	No Connection
36	OutU	Output for U phase

※Two GND pins should be connected together to ground line on PCB, two VBB pins should be connected together to VBB line.



6. Absolute maximum rating

T_J=+25℃ Unless otherwise noted

Items	Symbol	Condition	Limit	Unit
Power supply voltage	V_{BB}		38	V
Output voltage	V_{OUT}		V_{BB}	V
Output current (※)	$I_{OUT(Ave)}$		±2	A
	$I_{OUT(Peak)}$	tw<500msec/Duty<10%	±4	A
Logic input voltage	$V_{IN(Logic)}$		-0.3~5.5	V
Analog voltage	$V_{IN(Analog)}$		-0.3~6	V
Sense voltage	V_{SENSE}		±0.5	V
Power dissipation	PD	SK evaluation board	2.9	W
Junction temperature	T_J		150	℃
Storage temperature	T_{stg}		-40~150	℃
Ambient temperature	T_A		-20~85	℃

(※) Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified junction temperature (T_j).

Peak current is guaranteed by design.

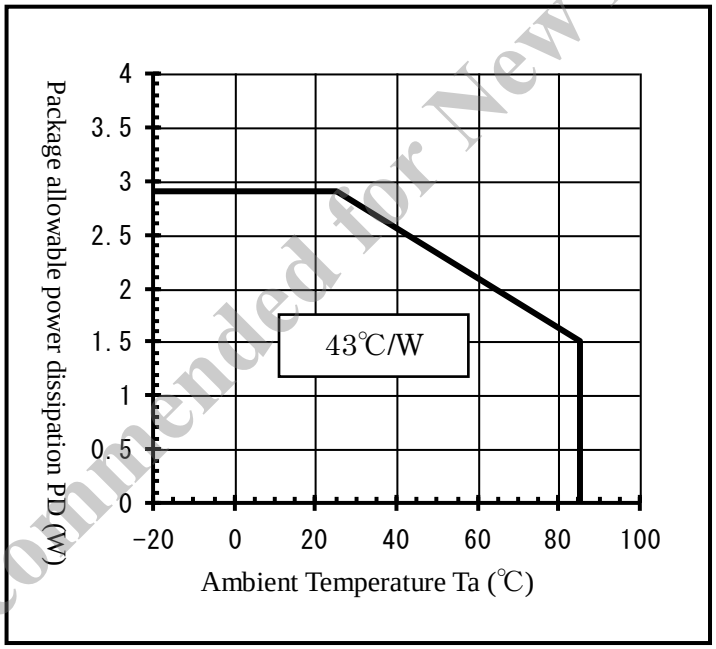
7. Recommended operating range

Item	Symbol	Limit	Unit	Remark
Power supply voltage	V_{BB}	10 - 30	V	Normal operation
Logic input voltage	$V_{IN(Logic)}$	0 - 5.5	V	
Analog input voltage	$V_{IN(Analog)}$	0 - 5.5	V	Except for Ref pin
Ref input voltage	V_{Ref}	0.5 - 5.5	V	Current accuracy is going down under 0.5V.
Sense voltage	V_{SEN}	±0.5	V	
Package temperature	T_C	105	℃	
Ambient temperature	T_A	-20 - 85	℃	

Especially, care should be taken with output current on condition over recommendation range and below absolute max rating. In this case, enough evaluation is needed with thermal design data below and application note to avoid the device being over absolute max rating for other item.

8. Power dissipation

Power dissipation



※SK evaluation board

9. Electrical characteristics

(T_a=25°C, V_{BB}=24V, V_{DD}=5V, Unless Otherwise Noted.)

Item	Symbol	Limit			Unit	Condition	
		Min.	Typ.	Max.			
Power supply voltage range	V_{BB}	10	-	V_{BBOV}	V	Motor operation	
Charge pump voltage	V_{CP}	6	7.5	9	V	Output disable, VCP-VBB voltage	
Charge pump frequency	f_{CP}	90	120	150	kHz		
Power supply current	I_{BB}	5	10	15	mA	Output disable	V_{BB}=38V
	I_{BBSTBY}	-	100	500	μA	V_{STBY}=2.5V	
Output leak current	I_{OLKL}	-200	-100	-50	μA	V_{BB}=38V、V_{OUT}=0V	
	I_{OLKH}	50	100	200	μA	V_{BB}=V_{OUT}=38V	
MOSFET ON resistance	$R_{DS(on)}$	0.1	0.2	0.3	Ω	I_{DS}=2.0A、S pin connected to GND	
Body diode forward voltage	V_{SD}	0.8	1.1	1.4	V	I_{SD}=2.0A	
STBY pin input voltage	V_{STBYL}	0	-	0.8	V		
	V_{STBYH}	2.5	-	V_{DD}	V		
	ΔV_{STBY}	0.1	0.25	0.4	V	Hysteresis	
STBY pin input current	I_{STBYL}	0	±1	±10	μA		
	I_{STBYH}	20	50	100	μA	V_{STBY}=5V	
Logic input voltage	V_{INPL}	0	-	0.8	V		Enable、Brake、Dir、SRMD、Decay、PWM
	V_{INPH}	3.5	-	V_{DD}	V		
	ΔV_{INP}	1	1.5	2	V	Hysteresis	
Logic input current	I_{INPL}	0	±1	±10	μA	V_{IN}=0V	
	I_{INPH}	0	±1	±10	μA	V_{IN}=5.5V	
REF pin input current	I_{REF}	-5	-0.5	1	μA	V_{REF}=0~5.5V	
REF pin input current	V_{REF}	0.5	-	5.5	V		
SEN pin input current	I_{SEN}	0	±2.5	±10	μA	V_{SEN}=0~0.5V	
Current sensing divider ratio	V_{SEN}/V_{REF}	-10	-	10	%	V_{REF}=5.5V	
Current sensing filter time	t_{LPFSEN}	0.6	1.8	3	μs		
CPWM pin threshold voltage	V_{CPWML}	1.1	1.5	1.9	V		
	V_{CPWMH}	3	3.5	4	V		
CPWM pin frequency	f_{CPWM}	15	25	35	kHz	C_{PWM}=1000pF	
CLD pin frequency	f_{CLD}	54	64	74	Hz	C_{LD}=0.1μF	

- Typ data is for reference only.
- Negative current is defined as coming out of the specified pin.

Electrical Characteristic(continued) (T_a=25°C, V_{BB} =24V, V_{DD}=5V, Unless Otherwise Noted.)

Item	Symbol	Limit			Unit	Condition	
		Min.	Typ.	Max.			
Power supply voltage range	V_{BB}	10	-	V_{BBOV}	V	Motor operation	
Charge pump voltage	V_{CP}	6	7.5	9	V	Output disable, VCP-VBB voltage	
Charge pump frequency	f_{CP}	90	120	150	kHz		
AIN pin input current	I_{AIN}	-1	-0.5	1	μA	AINP、AINN pin, V_{AIN}=0~5.5V	
AOUT pin threshold voltage	V_{AOENA}	-	1.2	V_{CPWML}	V	AOUT pin voltage rising	
	$V_{AOENAhys}$	0.05	0.1	0.15	V	Hysteresis	Guaranteed by design
AOUT pin max output voltage	V_{AOUTH}	V_{CPWMH}	4	4.45	V	Output PWM operating	
AOUT pin input voltage range	V_{AOUTEI}	4.5	-	5.5	V	Output 100% ON	
AOUT pin max output current	I_{AOUT}	7.5	-	-	mA	V_{AOUT}=0V	
AOUT pin pull-down resistance	R_{AOUT}	25	32.5	40	kΩ	V_{AOUT}=2.5V	
FLAG pin output voltage	$V_{FLAG(ON)}$	0.1	0.2	0.5	V	I_{FLAG}=2mA	FLAG
FLAG pin leak current	$I_{FLAG(OFF)}$	0	-	20	μA	V_{FLAG}=5.5V	
FG pin output voltage	$V_{FG(ON)}$	0.1	0.2	0.5	V	I_{FG}=2mA	FG
FG pin leak current	$I_{FG(OFF)}$	0	-	20	μA	V_{FG}=5.5V	

- Typ data is for reference only.
- Negative current is defined as coming out of the specified pin.

Electrical Characteristic(continued) (T_a=25°C, V_{BB} =24V, V_{DD}=5V, Unless Otherwise Noted.)

Item	Symbol	Limit			Unit	Condition	
		Min.	Typ.	Max.			
VBB under voltage lock out	V_{BBUVH}	7	7.5	9	V	VBB rising	V_{CP}= V_{BB}+7V
	$V_{BBUVhys}$	0.1	0.3	0.5	V	Hysteresis	
Over voltage threshold	V_{BBOV}	34	35	37.5	V	VBB rising	Motor drive stop
	$V_{BBOVhys}$	1.5	2	2.5	V	Hysteresis	
Over current detect voltage	V_{OCPLS}	1	1.3	1.5	V	OUT-GND voltage, Low side detect	
	V_{OCPHS}	0.7	1.0	1.3	V	VBB-OUT voltage, High side detect	
Over current filter time	t_{LPFOC}	-	0.6	t_{LPFSEN}	µs		
Thermal shutdown	T_{TSD}	150	165	-	°C	Temperature rising	Guaranteed by design
	ΔT_{TSD}	-	50	-	°C	Hysteresis	
Thermal alarm	T_{TA}	-	120	-	°C	Temperature rising	
	ΔT_{TA}	-	10	-	°C	Hysteresis	
Propagation delay	t_{PDON}	-	2.3	-	µs	HALL input to output ON	
	t_{PDOFF}	-	2.1	-	µs	HALL input to output OFF	
	$t_{PDPWMON}$	-	1.1	-	µs	PWM input to output ON	
	$t_{PDPWMOFF}$	-	0.9	-	µs	PWM input to output OFF	
Dead time	t_{DEAD}	100	300	800	ns		
Hall input current	I_{HALL}	-2	-0.5	1	µA	V_{IN}=0.2~4.2V	
Common mode voltage range	V_{CMR}	0.2	-	3.5	V		
AC input voltage range	V_{HALL}	60	-	-	mV		
Hysteresis	V_{HYS}	-	20	V_{HALL}	mV	Guaranteed by design	
Pulse reject filter	t_{pulse}	1	2	3	µs		

- Typ data is for reference only.
- Negative current is defined as coming out of the specified pin.

10. Truth table, timing chart

Excitation control input (Hall and Logic input)

Truth table

Status	Input					Output status DIR=H (L)		
	HallU※1	HallV※1	HallW※1	Enable	Brake	OUTU	OUTV	OUTW
F1	+	−	+	L	H	H (L)	L (H)	Z
F2	+	−	−	L	H	H (L)	Z	L (H)
F3	+	+	−	L	H	Z	H (L)	L (H)
F4	−	+	−	L	H	L (H)	H (L)	Z
F5	−	+	+	L	H	L (H)	Z	H (L)
F6	−	−	+	L	H	Z	L (H)	H (L)
Error	−	−	−	X	H	Z	Z	Z
Error	+	+	+	X	H	Z	Z	Z
Brake	X	X	X	L	L	L	L	L
Disable※2	X	X	X	H	X	Z	Z	Z

※1 HallU、HallV、HallW： '+'=H+>H- 、'-'=H+<H-

※2 There are conditions for the device to be disable

- HallU, HallV and HallW are internal logic signal made from HU+, HU-, HV+, HV-, HW+ and HW-
- Refer to "10.12 Enable and Brake" for disable operation

10.1. Stand-By pin

Truth table

STBY	Status
L	Operation mode
H	Stand-By mode

- In stand-by mode, some internal circuits are shut down with bias current being cut.

10.2. FLAG output

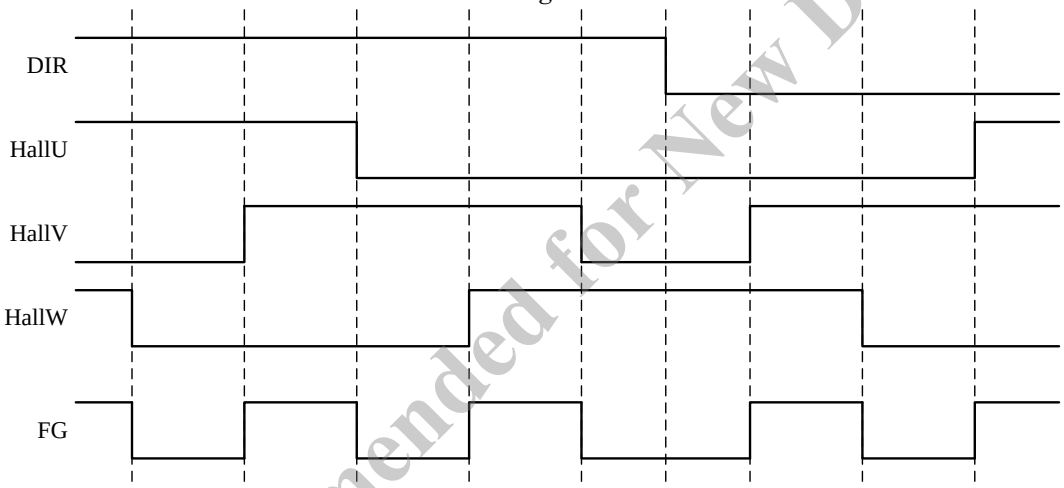
Truth table

Status	Fault
Normal	Output OFF (High impedance)
Fault	L

- Below are the fault conditions.
  - ① Under voltage lock out for VBB (internal regulator)
  - ② Under voltage lock out for charge pump
  - ③ Overvoltage
  - ④ Thermal alarm
  - ⑤ t_{OFFOCP} after over current detection
  - ⑥ Lock detection
- Please take care for FLAG output due to the internal circuit may not be fixed with VBB being low.

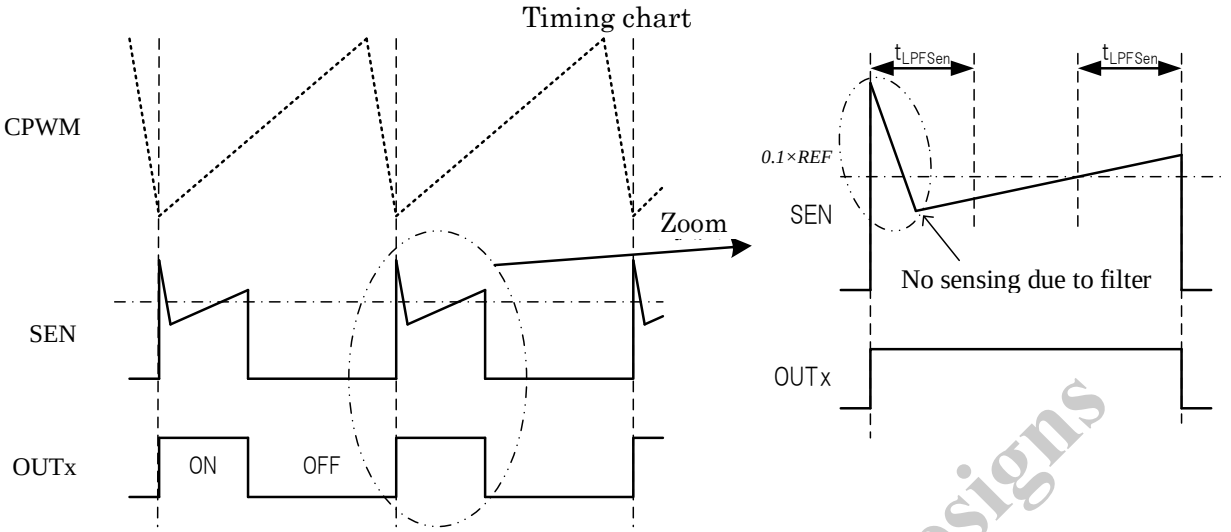
10.3. FG signal

Timing chart



- Refer to "10.1 Hall and Logic input" on HalU, HallV and HallW
- FG is toggled by each phase changed

10.4. Internal PWM control

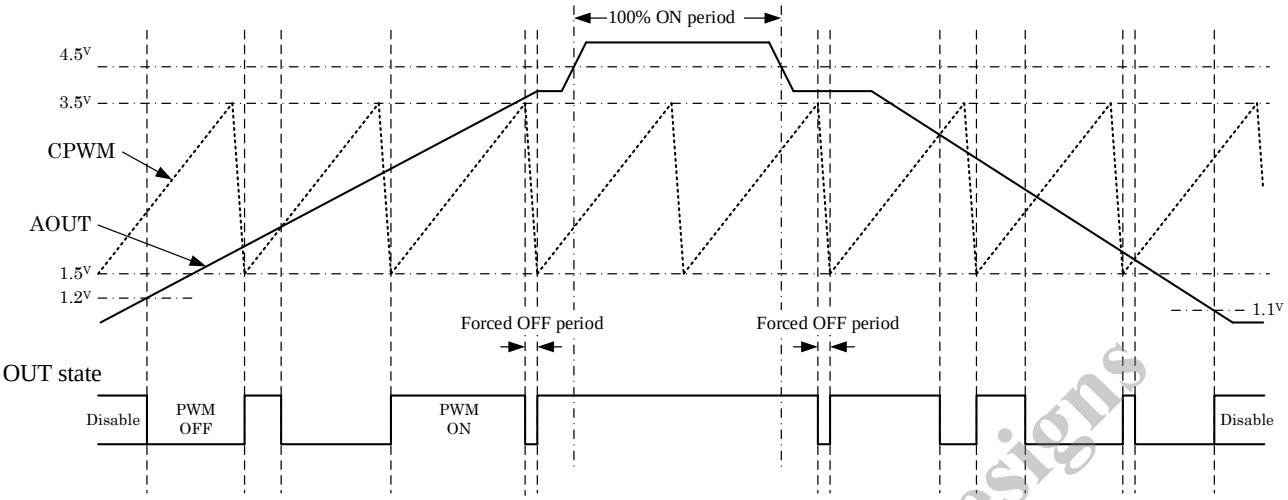


The value is typical in the timing chart

- If not using this function, you should connect SEN pin to GND and put some voltage (from 1V to max in VREF voltage range) to REF pin.
- Internal PWM is active in off time, but the device has blanking time that is almost same as t_{LPFSen}.

10.5. External PWM control

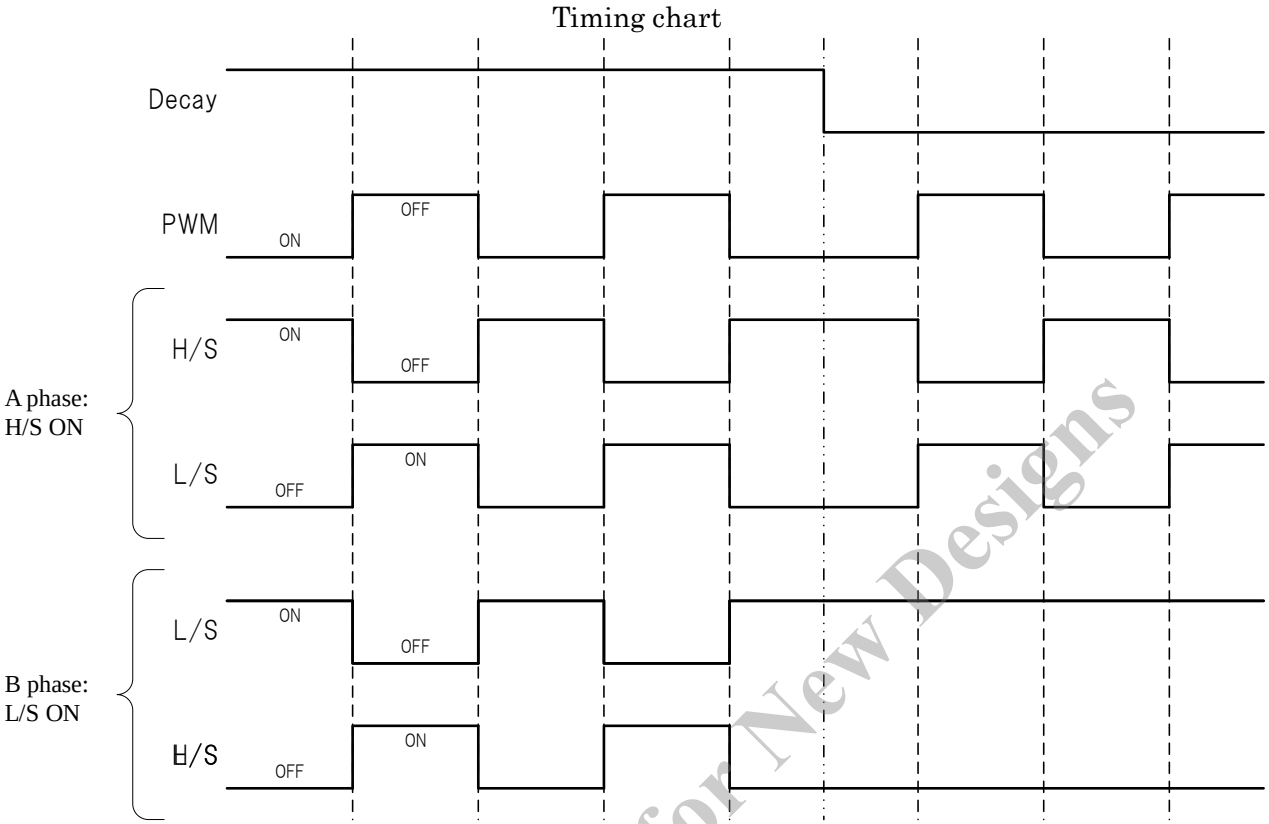
Timing chart



The value is typical in the timing chart

- Outputs are disable below 1.2V (typ, the voltage rising) on AOUT pin.
- The max duty is 95% (typ, design value) due to the forced off time. The forced off time is active even if not using this function.
- To make 100% ON duty, you should put the external voltage over 4.5V on AOUT. However, the voltage range to make 100% ON is from 4.5V to 5.5V.

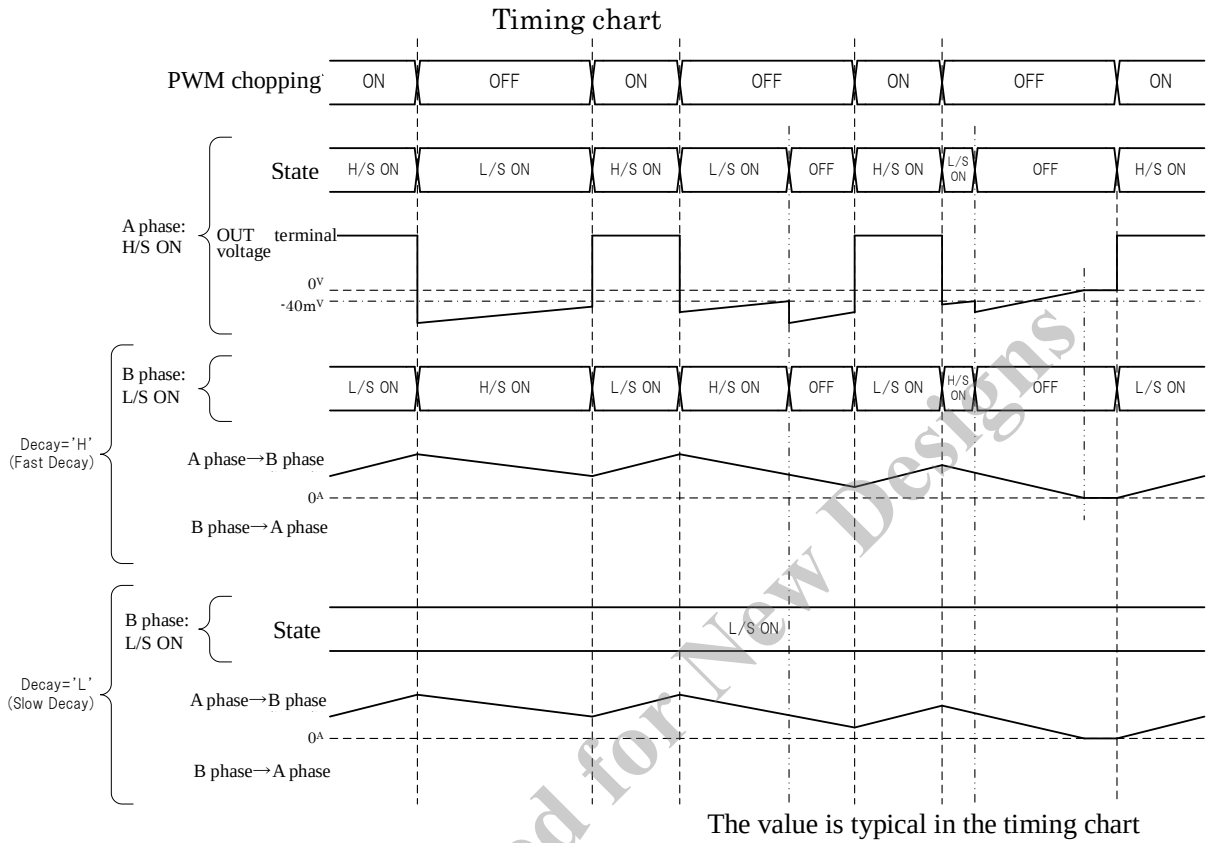
10.6. PWM control (PWM and Decay)



- This diagram only shows the relation between PWM pin and output. However, the forced off time in "10.6 external PWM control" make the outputs be OFF.
- Please tie to "L" when not using this function.

10.7. PWM and Synchronous rectification (Decay pin and SRMD pin)

SRMD='L' (passive mode)

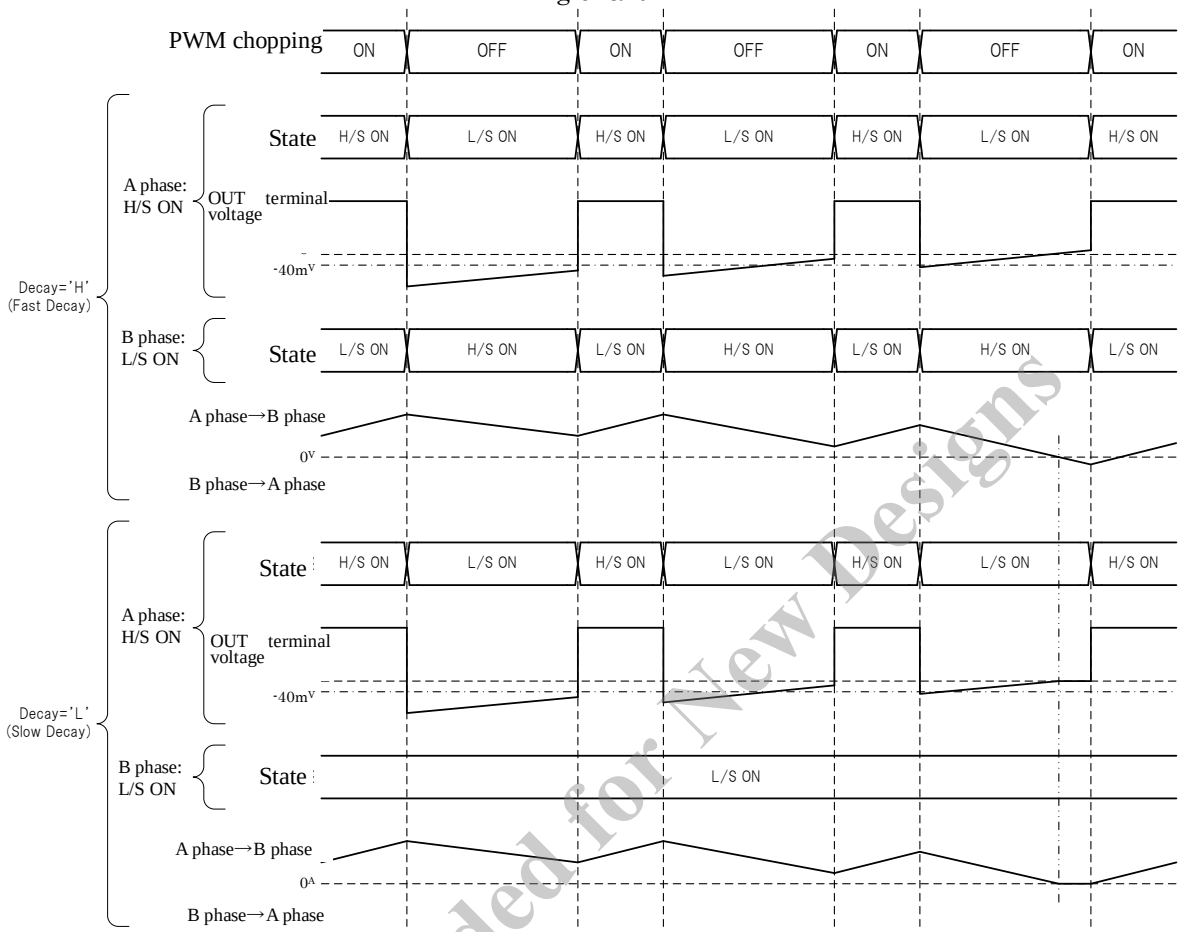


The value is typical in the timing chart

- The device stop the synchronous rectification in PWM off time if the voltage on OUT pin, where low side is ON, is over -40mV (typ, room temp).

SRMD='H' (Active mode)

Timing chart

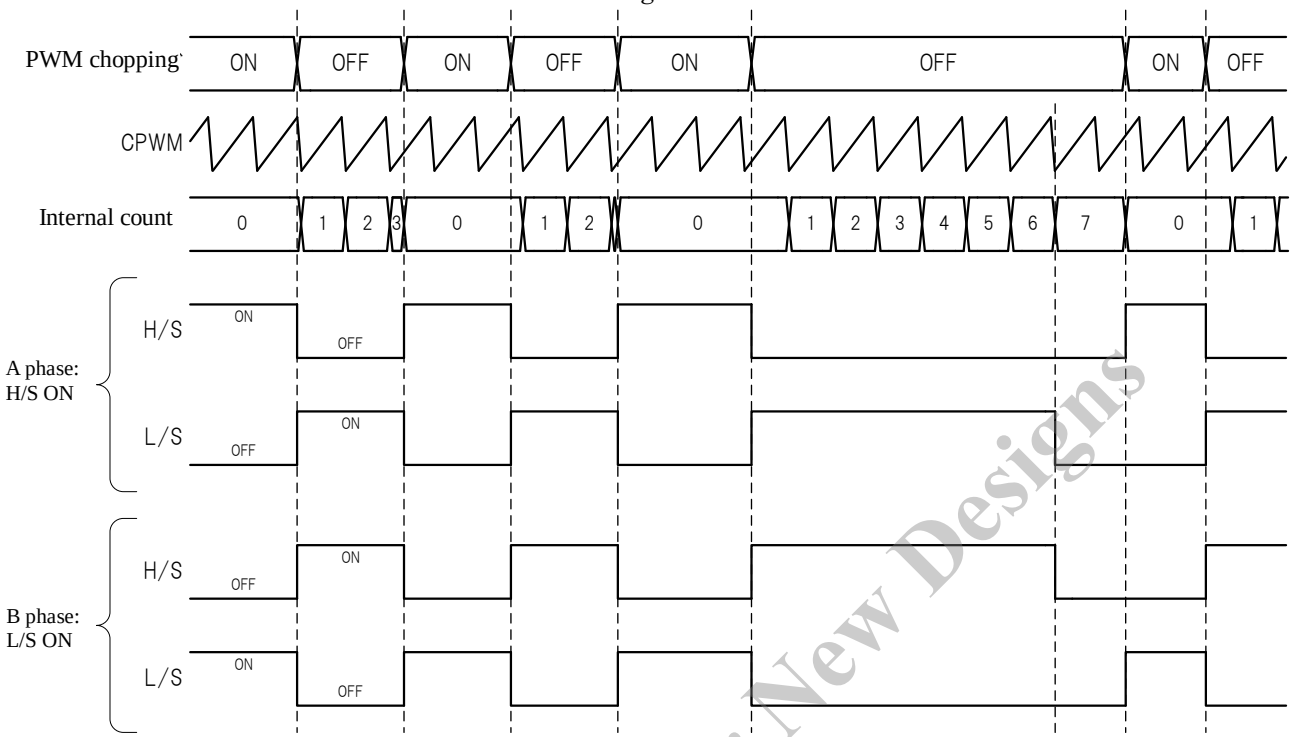


The value is typical in the timing chart

- Synchronous rectification is active in PWM OFF (current recirculation) without monitor on OUT pin.
- In this mode, since the excitation mode is not changed even if current recirculation is finished, the condition of the device is below.
  - Slow Decay: Same as short brake
  - Fast Decay: Reverse current starts to flow.
- In the application where not using internal PWM with fast decay, the device gets OCP protection with long term of synchronous rectification due to the reverse current get large.

10.8. Disable function for synchronous rectification (Fast decay only)

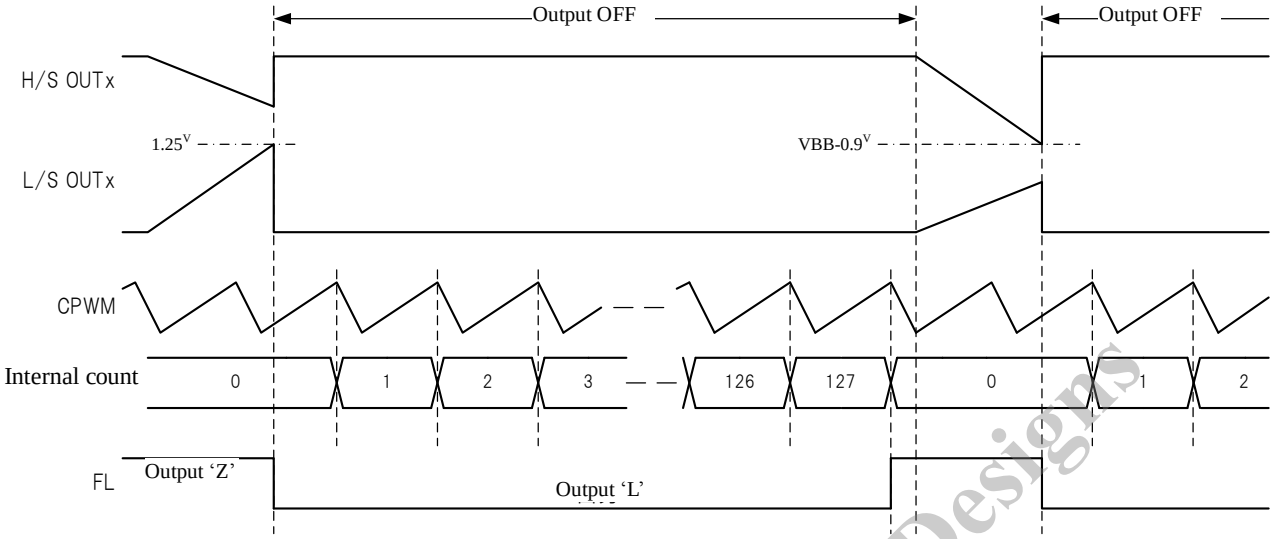
Timing chart



- The device stops synchronous rectification when PWM OFF keeps for 7 cycles of CPWM.
- Synchronous rectification is not activated when in brake mode.

10.9. Over current protection

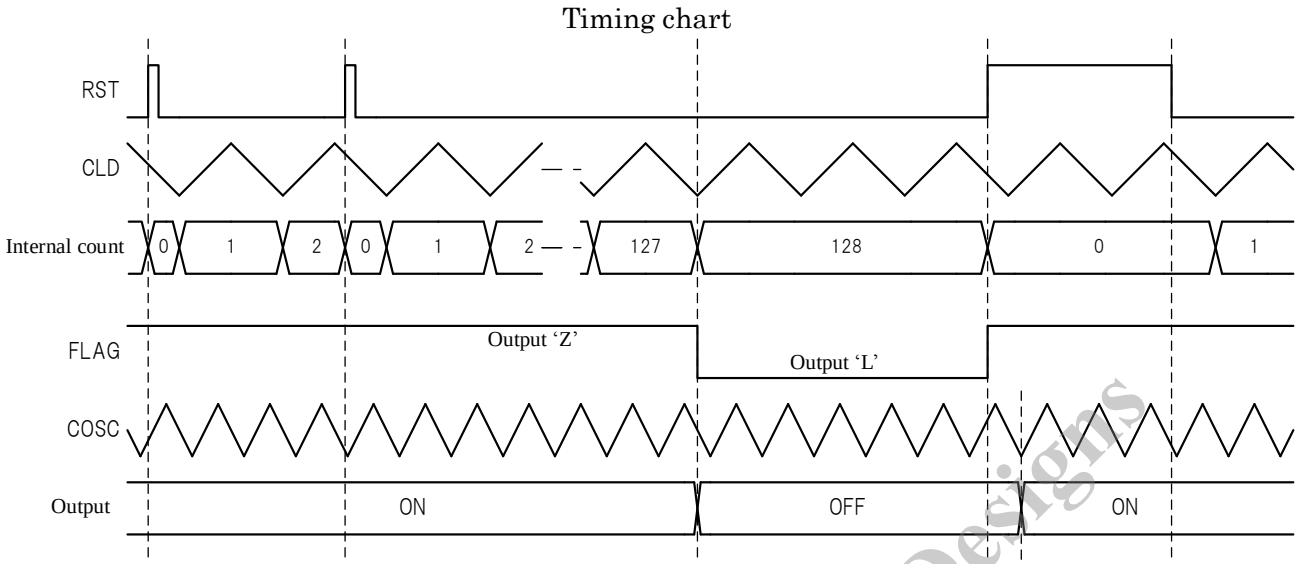
Timing chart



The value is typical in the timing chart

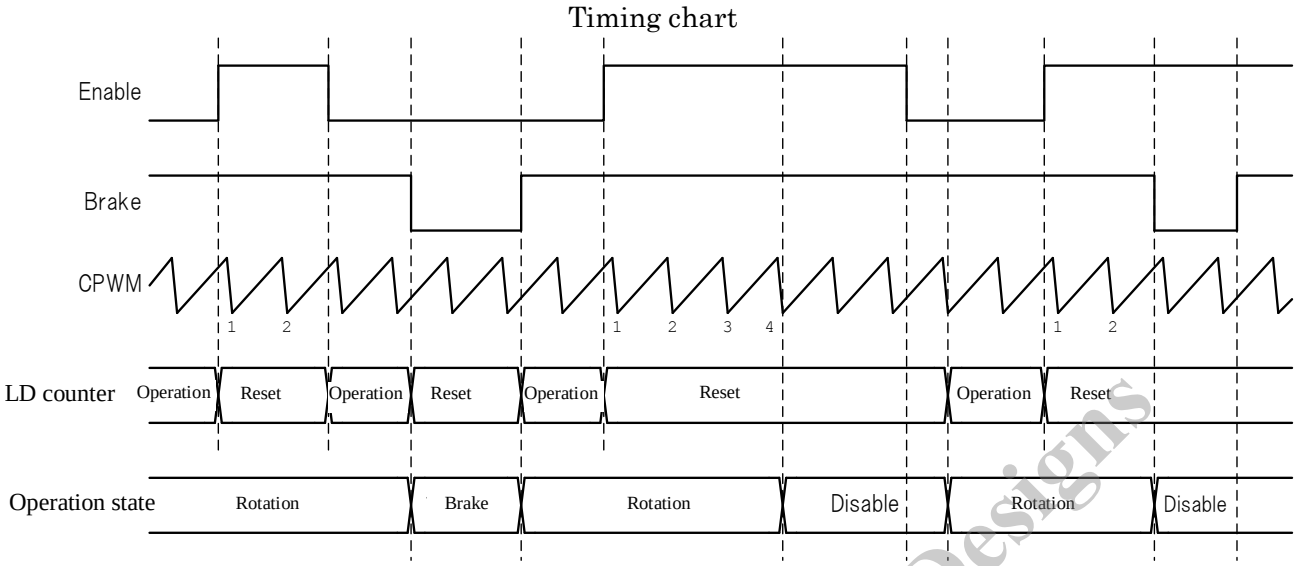
- After OCP function is detected, outputs are disabled for 128 cycles of CPWM. After the disable time (128cycles of CPWM) is finished, the device automatically operates again
- The trigger for off timer count and release of FL output is at the top of CPWM oscillation waveform.
- The trigger for release of off timer count is at the bottom of CPWM oscillation.
- There is time difference between release for FL and actual output on.

10.10. Motor lock



- Lock detection is active in operation only (Enable=L and Brake=H)
- The device recognizes lock condition if RST signal (H) is not for about 128 cycles of CLD.
- RST means internal signal showing release lock condition as in hall input changing. Please refer to timing chart in 10.12 Enable and Brake, or refer to 11.9 Lock detect.

10.11. Enable and Brake



- Enable pin has two functions with priority below.
  - ① Reset for lock counter
    - ➢ Lock counter is reset for Enable being high.
  - ② Enable/Disable operation for output
    - ➢ The device makes output disable at 4th bottom on CPWM oscillation waveform after down-edge of Enable signal.
    - ➢ The device makes output enable at the first on trigger (the bottom of CPWM wave from) after Enable pin changing from "H" to "L".
- Brake signal is neglected for Enable being high.

11. Functional description; individual block

11.1. Stand-By input

This block is to control the device condition between stand-by mode and normal operation.
In stand-by mode, almost all circuits except for this block are disabled to make low power dissipation.
The threshold voltage on STBY pin is the different from that of other logic pins.

11.2. Internal regulator (Int.REG1, Int.REG2)

Reg block is for power supply to operate internal circuits. Reg block has two lines, meaning one is for logic (Int.Reg1) and the other (Int.Reg2) is for analog circuit.

11.3. Charge Pump

This block is gate driver for high-side N-channel MOSFET.
The voltage of CP pin is over that of VBB pin by 7V to 8V.
You should put capacitors at CP-VBB and CPH-CPL, and should also take care below.

- CP-VBB
  The voltage of CP pin is over that of VBB pin by 7V to 8V.
  However, in start-up conditions, the voltage of CP pin may below that of VBB by 1 to 1.5V.

- CPH-CPL
  You should take care of the breakdown voltage for the capacitor due to the voltage on the capacitor is the same as that of VBB.

11.4. Under Voltage Lock Out

This block is for protection to avoid the device damaged. The block makes all outputs shutdown if the device is below voltage where the device can't control internal circuit.
The block monitors the voltages on Int.Reg2 and charge pump.

11.5. Over Voltage Protection

This block monitors VBB voltage and make output shut down with VBB being near to the absolute max rating to keep the device endure from the over voltage condition.
OVP is active with VBB being 35V (typ).
The device can't be operated with OVP.

11.6. Thermal Shut Down

TSD block monitors junction temperature to avoid the overheating of the device.
The block makes all outputs shutdown with junction temperature being over 160C.
The TSD is released with temperature falling by 50C.
TSD function is not for use in normal operation. Care should be taken not to use this function from the thermal design point of view.

11.7. Hall Amplifier and Commutation Logic

This block makes excitation signal based on the position signal of brushless motor.
The device should be connected with hall element as a typical application.

11.8. FG generator

This block makes rotation pulse from FG pin through hall amp and commutation logic.
It also makes reset signal for lock detection.

11.9. Lock Detect

This block is motor lock detection.
If hall input signal is not changed for the time of t_{LD}, which is made by the capacitor on CLD pin and internal divider, the device recognizes "lock condition" and also makes all outputs shut down.

The formula regarding t_{LD} and capacitance on CLD pin is below.

$$t_{LD} \approx 20 \times C_{LD}[\mu F]$$

To reset the internal counter and to resume from all outputs off after lock detection, any of below condition is needed.

- Brake pin tie to L (Brake mode)
- Enable pin tie to H (Disable mode)
- Change the logic signal of Dir pin.
- Power up cycle on VBB.
- Change the hall signal.

Lock counter is reset with every cycle for hall transition.
After motor stopped with lock condition, if the motor is rotated with some external force and hall signal is changed, the device reset lock condition and operate again.

If you intentionally want to avoid lock condition with motor operated, you should change the signal on Dir pin with shorter term than t_{LD} or should put H signal on Enable pin for short time (below 4 cycles of CPWM).

Except for internal Reg UVLO, lock detection function is active even if other protection (charge pump UVLO, TSD, OVP and OCP) is asserted. In this condition, the motor may be stopped with lock condition even if the abnormal mode is released. To make the motor operate again from this condition, you should release lock condition after abnormal mode is released.

11.10. PWM Oscillation

This block sets the PWM operation frequency and basic signal regarding operation timing in the device.
The capacitor is needed on CPWM pin to oscillate.

Oscillation frequency (f_{PWM}) is set to the capacitance on CPWM pin. Below is the formula.

$$f_{PWM}[kHz] \approx 25 / C_{PWM}[nF]$$

Oscillation is the triangle waveform where 95% of a cycle is rising term and 5% of a cycle is falling term.
The falling term is forced off time (The voltage on AOUT is below 4.5V).

11.11. Internal PWM

The block controls peak current of motor winding according to the external analog voltage.
The block also has noise filter for rising edge of chopping ON.

As a operation of internal PWM function, it is chopping ON with trigger signal from PWM OSC (Bottom point of CPWM oscillation waveform) and it is chopping OFF with the motor current hit the peak current setting (I_{Opeak}).

Below is the formula of I_{Opeak}

$$I_{Opeak} \approx 0.1 \times V_{REF} / R_S \quad [A]$$

V_{REF}: analog voltage on REF pin / R_S : sense resistance

You can neglect the function with SEN pin tie to GND and put the analog voltage (the voltage is put between 1V and max voltage range on REF pin) on REF pin.

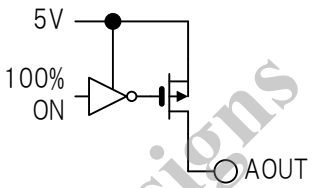
11.12. External PWM

The block control output duty with comparing the voltage between AOUT and CPWM.
There is amplifier constructed by AINP, AINN and AOUT. With the amplifier, feedback control can be made by using speed signal from FG pin.

The device operates below ON condition of the voltage for AOUT pin.

- Below 1.2V
  Outputs are OFF (outputs disable).

- From 1.5V to 3.5V
  There is linear characteristic in this voltage range.



- 3.5V - 4.5V
  From 3.5V to 4.5V
  The max output voltage of amplifier is set in this voltage range.
  Also, output ON duty is set to maximum (95%, ideal).

- Over 4.5V (Below 5.5V, maximum for input voltage on AOUT pin)
  100% duty can be made by putting over 4.5V on AOUT pin.
  However, internal circuit can't make over 4.5V, meaning it is needed to put over 4.5V externally (Refer to above example circuit).
  Please put the external analog voltage within the voltage range on AOUT pin.
  There is no problem with the voltage range (4.5V to maximum voltage on AOUT pin) from the circuit point of view.

Internal amplifier is not balanced with putting external voltage. Please take care it takes some time for the amplifier and output voltage on AOUT to be balanced after stopping put the external voltage.

If not using this function, please connect AINP, AINN and AOUT pins for AOUT voltage to be maximum.
(For example, voltage follower circuit with connecting AINN and AOUT and put 5V on AINP)
But, in this condition, there is forced off time. If you make 100% on condition, please set the voltage on AOUT over 4.5V.

From the circuit point of view, the current may flow from AOUT to VBB.
When you put over 4.5V on AOUT pin, please take care the voltage relation between AOUT and VBB to avoid the current flow from AOUT to VBB.

11.13. Over current and Negative voltage detect

The block monitors the voltage on output and decides the OCP and synchronous rectification (Passive mode only).

11.14. PWM Control Logic

The block makes ON/OFF signal for output by the signals from control blocks and logic input signal as in PWM control, synchronous rectification and decay control.

11.15. Gate Drive

The block is the pre-drive circuit for internal n-channel MOSFET. The block receives the signal from control logic. The block also has dead-time control, which is to avoid shoot thru meaning simultaneous ON condition between high-side and low-side.

11.16. OCP Timer

The block makes output off for t_{OCOFF} after receiving OCP detection signal.
t_{OCOFF} is made from frequency for PWM OSC and internal divider.

12. Others

12.1. About PWM function

The device has three PWM control function below.

① Internal PWM (SEN pin, REF pin)
② External PWM (CPWM pin, AINP pin, AINN pin, AOUT pin)
③ Logic PWM (PWM pin)

Internally, the device makes output ON with all three PWM functions being ON condition (priority with output OFF). Please evaluate and verify if you make combination multiple PWM functions.

12.2. About Thermal shut down

Thermal shut down function is to avoid the device damaged, so the operation temperature of this function is over rating for T_J.

This function can't be used in normal operation. Please verify thermal calculation to avoid this function.

12.3. About over current protection (OCP)

OCP is to avoid the device damaged when in abnormal mode and the over current flowing through output power device, so the operation current for OCP is set over absolute max rating of 4A(peak).

This function can't be used in normal operation. Please verify the operation to avoid the OCP function being active in normal operation.

To achieve this, it is effective to use internal PWM function to control the over-current.

12.4. About the over voltage protection (OVP)

This function is estimated for VBB to go up the voltage by the energy generated from the motor.

This function makes output OFF with OVP detected to protect the device.

However, VBB may continue going up the voltage with OVP active, please make some countermeasure to avoid the device damaged from over-voltage.

12.5. About Flag pin

Please take care for FLAG output due to the internal circuit may not be fixed with VBB being low.

12.6. Logic inputs/output

Be sure to prevent the logic inputs (PWM, Dir, Decay, SRMD, Brake, Enable, STBY) from being "OPEN".

If some of the logic inputs are not used, be sure to connect them to VDD or GND.

※In case some of the logic inputs stay "OPEN", a malfunction may occur due to external noises.

When the logic output (FG, FL) is not used, be sure to keep it "OPEN" or Gnd.

※In case it is connected to VDD, it may cause the device's deterioration or/and breakdown.

12.7. About the protection circuit operation

This product has Two protection circuits (motor coil short-circuit and overheating).
These protection circuits work with detecting the thing that excessive energy joins the driver.
Therefore, it is not possible to protect it when the energy caused by the motor coil short-circuit is outside the tolerance of the driver.

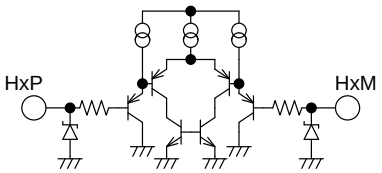
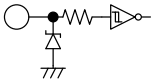
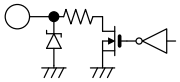
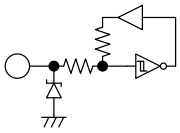
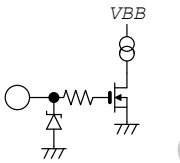
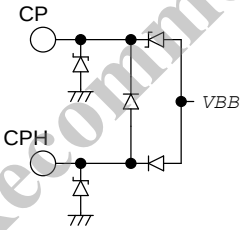
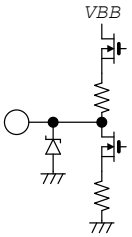
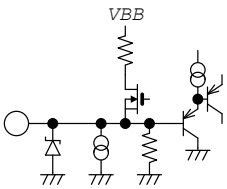
12.8. Notice

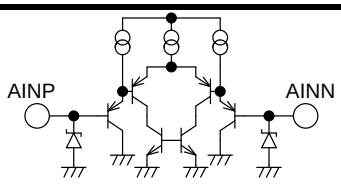
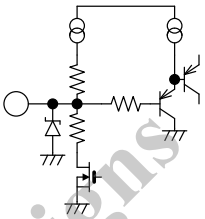
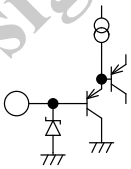
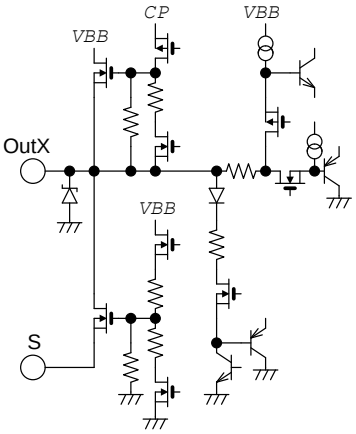
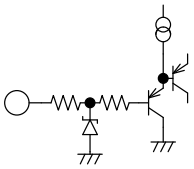
This driver has MOS inputs. Please notice as following contents.

- When static electricity is a problem, care should be taken to properly control the room humidity. This is particularly true in the winter when static electricity is most troublesome.

- Care should be taken with device leads and with assembly sequencing to avoid applying static charges to IC leads. PC board pins should be shorted together to keep them at the same potential to avoid this kind of trouble.

13. Pin diagram

№	Pin name	Pin function
1	HWM	
2	HWP	
3	HVM	
4	HVP	
5	HUM	
6	HUP	
7	Decay	
8	SRMD	
23	Enable	
24	PWM	
25	Dir	
26	Brake	
9	FLAG	
22	FG	
10	CLD	
11	STBY	
15	CP	
16	CPH	
17	CPL	
18	AOUT	

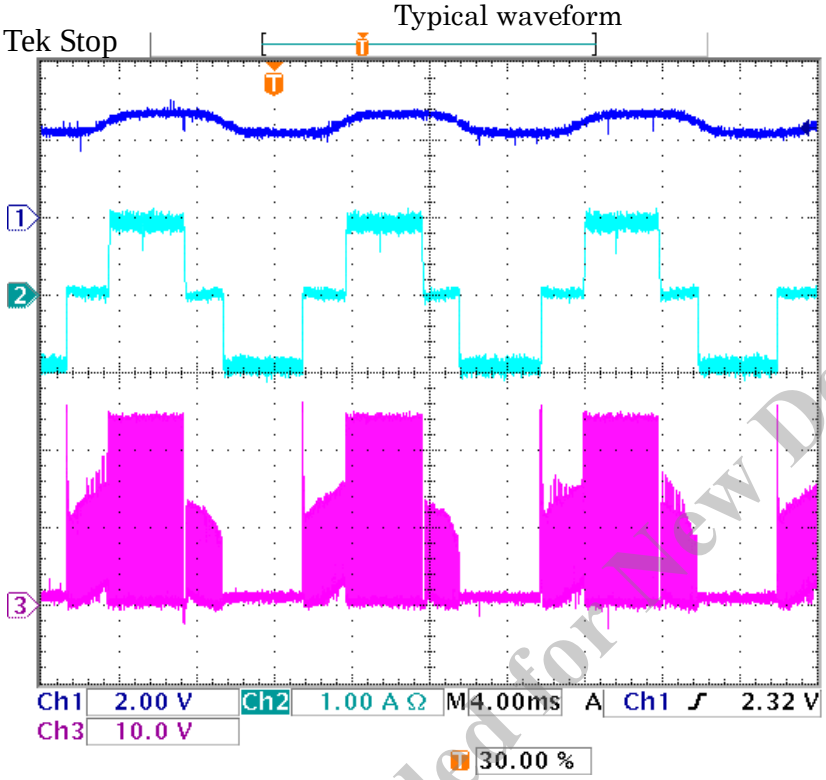
№	Pin name	Pin function
19	AINN	
20	AINP	
21	CPWM	
27	REF	
28	OutW	
34	OutV	
36	OutU	
32	S	
31	SEN	
12	GND	
30	GND	
13	VBB	
14	VBB	
29	N.C.	
33	N.C.	
35	N.C.	

14. Evaluation data

14.1. Operation wave form

Below is the typical waveform.

Typical waveform

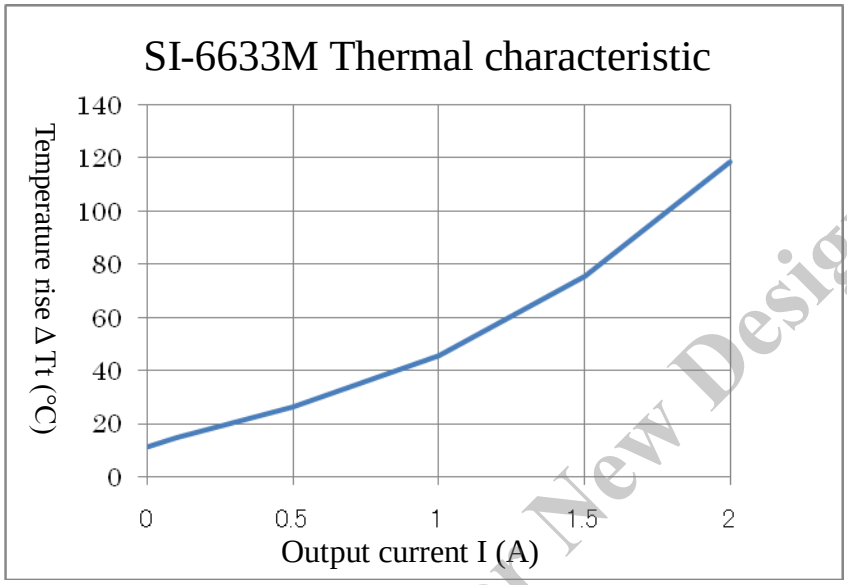


14.2. Thermal characteristic

Below is the thermal characteristic and measurement condition

- SK evaluation board and motor in SK lab use
- VBB=24V
- Decay=L（Slow Decay）

Thermal characteristic for SI-6633M



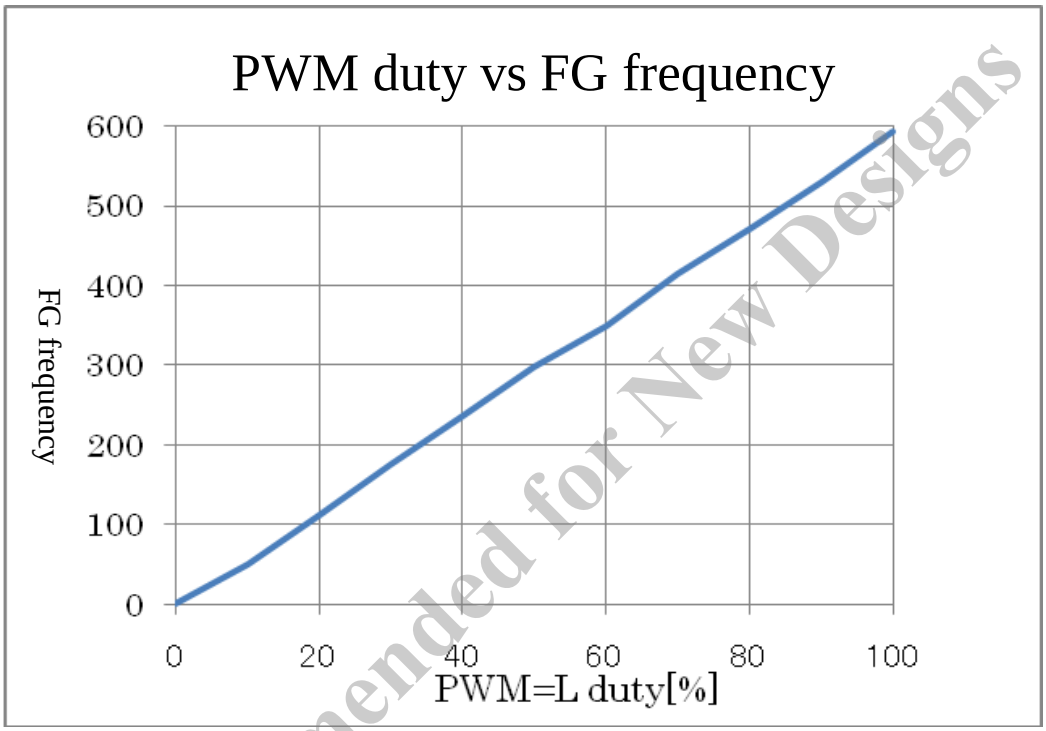
※Delta Tt is the temperature difference between Ta and Ttab (temperature at exposed pad).

14.3. Linearity

Below is the linearity and measurement condition

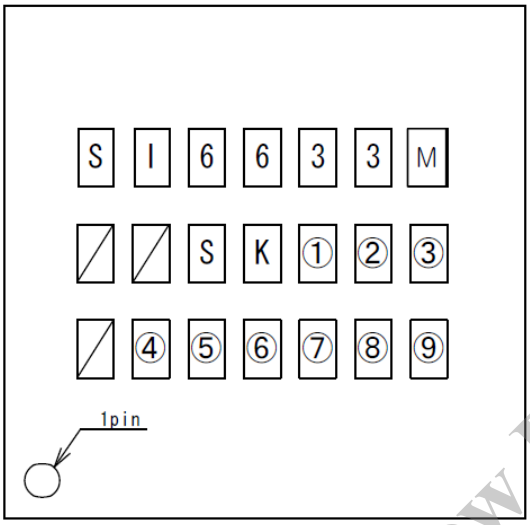
- SK evaluation board and motor in SK lab use
- VBB=24V
- REF=AOUT=5V
- Decay=L（Slow Decay）
- DIR=H
- SENSE=GND

Linearity; PWM Duty vs FG frequency



15. Blanding

SI-6633M Marking Specification



Discrimination	Mark No	Contents
Year	①	Thelast digit of year
Month	②	Month by number or alphabet when assembly is started
		[1-9] in case from January to September
		[10] in case October
		[11] in case November
		[12] in case December
Week	③	[1] in case from first to tenth
		[2] in caes from eleventh to twentieth
		[3] in case from twenty first to thirty first
Control code	④~⑨	

16. Packing

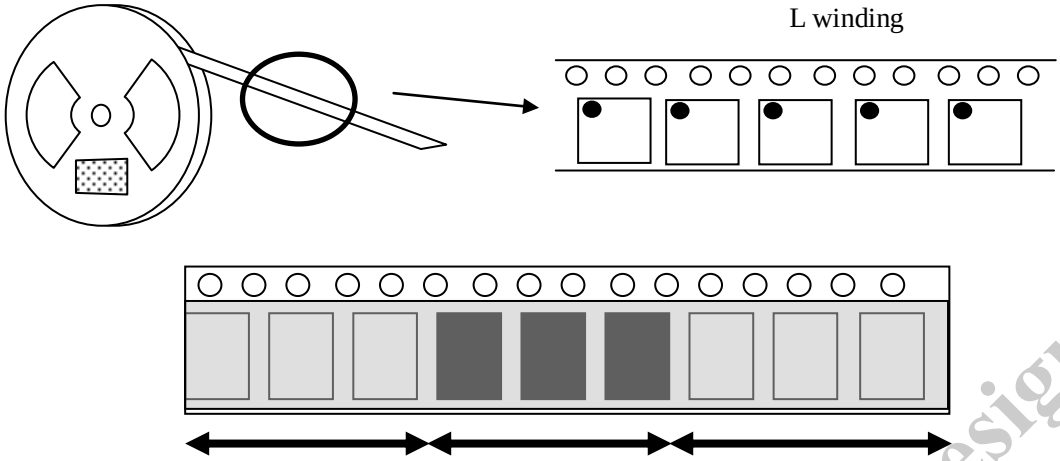
16.1. Container/Material/The number of parts per reel

Container is taping. The number of parts is 2500pcs per reel.
Remainder is packed with combination with next lot.

16.2. The material of taping

Material	
Emboss tape	The width of tape : 16mm
Reel	φ330 [mm]
laminate bag	Size : 0.075×380× 450 [mm]
Inner packing figure	Size : 340×360× 55 [mm]
Outer packing figure	Size : 350×370×230 [mm] 4 reels(max) per 1 outer box

16.3. Emboss tape diagram



Trailer
Over 50pcs of vacant pocket

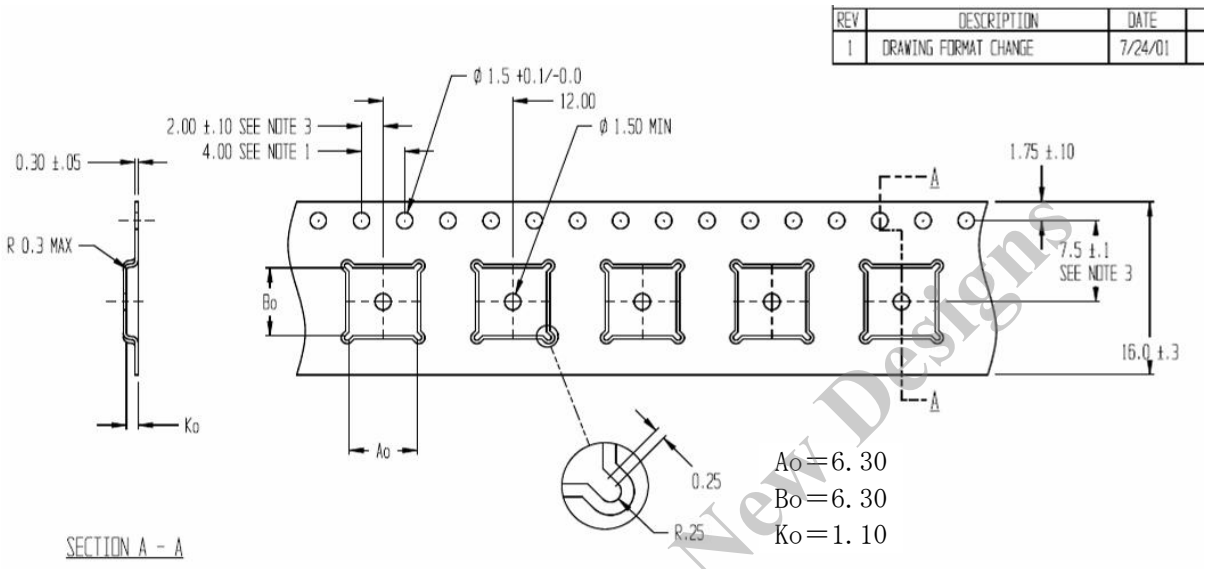
IC mounted

Reader
Over 50pcs of vacant pocket

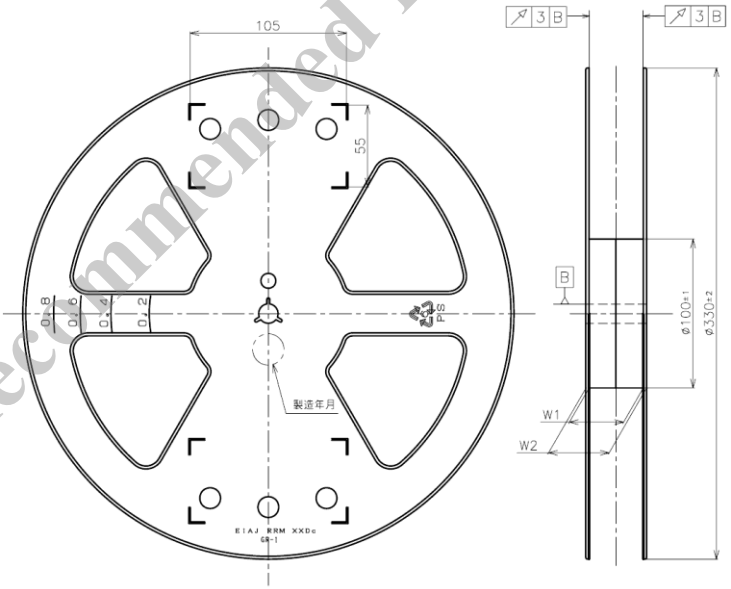
※It is heat-sealed with cover tape in reader and trailer.

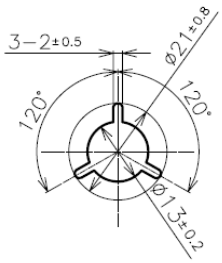
16.4. Dimension, material and diagram

16.4.1. Emboss tape



16.4.2. Reel





Detail drawing of shaft hole

Tape width：16.0mmm

W1 ：17.5±1.0 mm

W2 ；21.5±1. 0mm

Dimension in millimeter

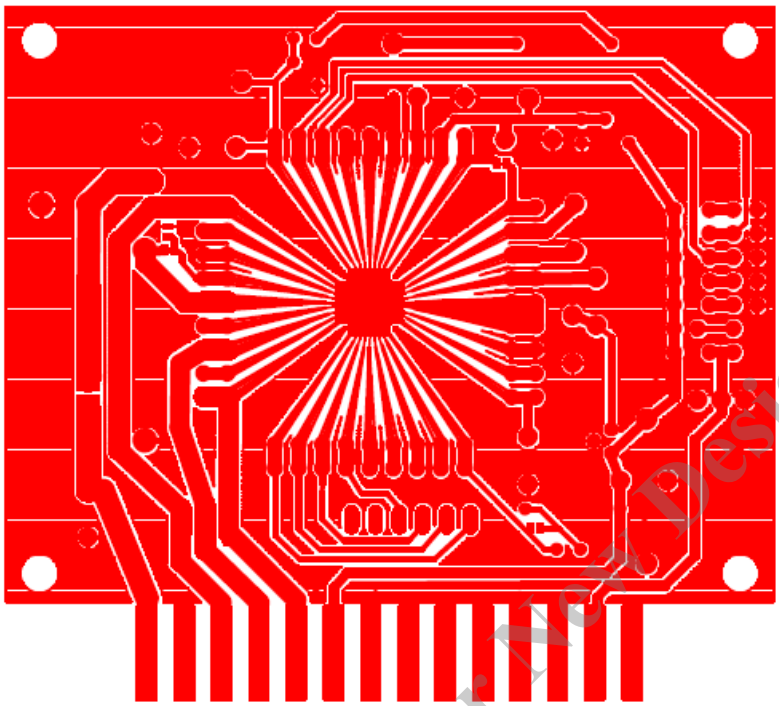
16.5. Storage condition

① Storage environment is below.
Temperature: 5 degrees-30 degrees
Humidity: 90% or below
Storage limitation is within 12month from packing date

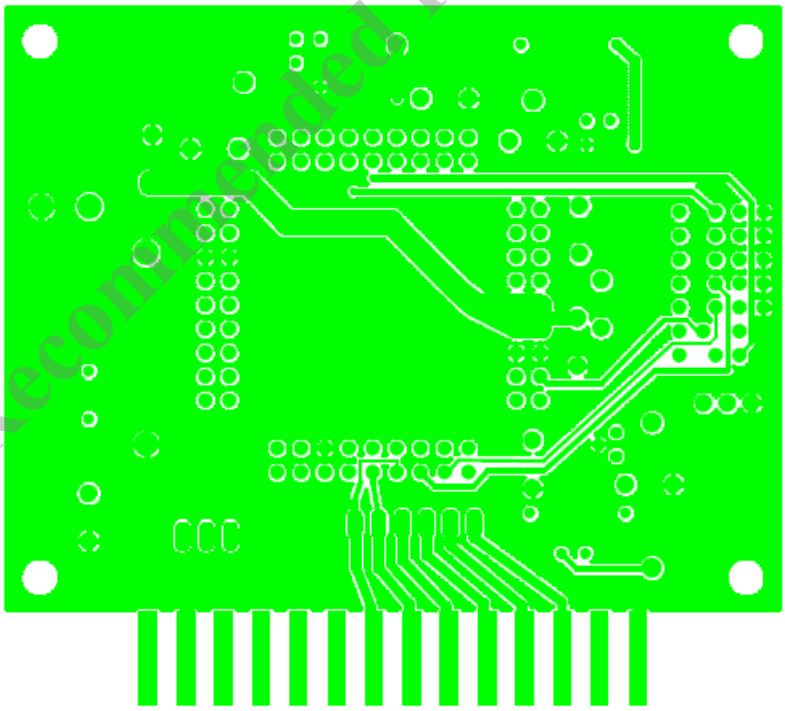
② If the above storage condition (17-5.1) is expired, the device is needed to have baking with 125 degrees for 20 hours. Also, Tape and reel are not guaranteed with the temperature and time condition.
If the device should be baked, it is needed to use container with “heatproof” or temperature to cover baking condition. And the container is needed to have static electricity control.

17. Pattern layout for evaluation board

Component side (top) of evaluation board



Solder side (bottom) of evaluation board



※Due to the conversion to pdf file, some portion is different from actual evaluation board.

18. Caution/Warning

- Application and operation examples described in this document are quoted for the sole purpose of reference for the use of the products herein and Sanken can assume no responsibility for any infringement of industrial property rights, intellectual property rights or any other rights of Sanken or any third party which may result from its use.
- Although Sanken undertakes to enhance the quality and reliability of its products, the occurrence of failure and defect of semiconductor products at a certain rate is inevitable. Users of Sanken products are requested to take, at their own risk, preventative measures including safety design of the equipment or systems against any possible injury, death, fires or damages to the society due to device failure or malfunction.
- Sanken products listed in this document are designed and intended for the use as components in general purpose electronic equipment or apparatus (home appliances, office equipment, telecommunication equipment, measuring equipment, etc.). Please return to us this document with your signature(s) or seal(s) prior to the use of the products herein.
  When considering the use of Sanken products in the applications where higher reliability is required (transportation equipment and its control systems, traffic signal control systems or equipment, fire/crime alarm systems, various safety devices, etc.), please contact your nearest Sanken sales representative to discuss, and then return to us this document with your signature(s) or seal(s) prior to the use of the products herein.
  The use of Sanken products without the written consent of Sanken in the applications where extremely high reliability is required (aerospace equipment, nuclear power control systems, life support systems, etc.) is strictly prohibited.
- In the case that you use our semiconductor devices or design your products by using our semiconductor devices, the reliability largely depends on the degree of derating to be made to the rated values. Derating may be interpreted as a case that an operation range is set by derating the load from each rated value or surge voltage or noise is considered for derating in order to assure or improve the reliability. In general, derating factors include electric stresses such as electric voltage, electric current, electric power etc., environmental stresses such as ambient temperature, humidity etc. and thermal stress caused due to self-heating of semiconductor devices. For these stresses, instantaneous values, maximum values and minimum values must be taken into consideration.
  In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature (Tj) affects the reliability significantly.
- When using the products specified herein by either (i) combining other products or materials therewith or (ii) physically, chemically or otherwise processing or treating the products, please duly consider all possible risks that may result from all such uses in advance and proceed therewith at your own responsibility.
- Anti radioactive ray design is not considered for the products listed herein.
- Sanken assumes no responsibility for any troubles, such as dropping products caused during transportation out of Sanken's distribution network.