Application Note

Full Mold Type Chopper Type Switching Regulator IC

SI-8005Q/SI-8105QL Series

April 2009 Rev.4.0

SANKEN ELECTRIC CO., LTD.

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1. General Description

The SI-8005Q is a buck switching regulator IC with a built-in power MOS. Due to a current control system, it is applicable to such a super low ESR capacitor as a ceramic capacitor. It is provided with various protection functions such as overcurrent protection, low input prohibition, overheat protection etc. In order to protect the IC against in-rush current at start-up, the soft start function is provided. The soft start time can be set by connecting external capacitors. A function to turn on/off external signals is also provided and by sending external signal to the EN terminal, the SI-8105Q can be turned on/off. This device is supplied in the small and thin type HSOP 8-pin package including a heat slag on the backside. The SI-8105QL is mounted in the DIP 8-pin package for flow mounting /power supply board (single side surface board).

● 1-1 Features

- Output current 3.5A

  The output current of each output is maximum 3.5A in the HSOP 8-pin surface mounting package.

- High efficiency

  Maximum efficiency 94% (V_{IN} = 8V / Vo = 5V / I_o = 0.8A)

- Output voltage variable: 0.5 - 24V
- Low ESR capacitor for output

  The ceramic capacitor can be used.

- Operating frequency: 500kHz
- Built-in functions for overcurrent and thermal shutdown

  A current limiting type protection circuit against overcurrent and overheat is built in. (automatic restoration type)

- Soft start function

  By adding an external capacitor, it is possible to delay the rise speed of the output voltage. ON/OFF control of the output is also possible.

- ON/OFF function
- Small package (SI-8005Q)

  HSOP8 pin package with small heat slug

● 1-2 Applications

For on-board local power supplies, power supplies for OA equipment, stabilization of secondary output voltage of regulator and power supply for communication equipment.

● 1-3 Type

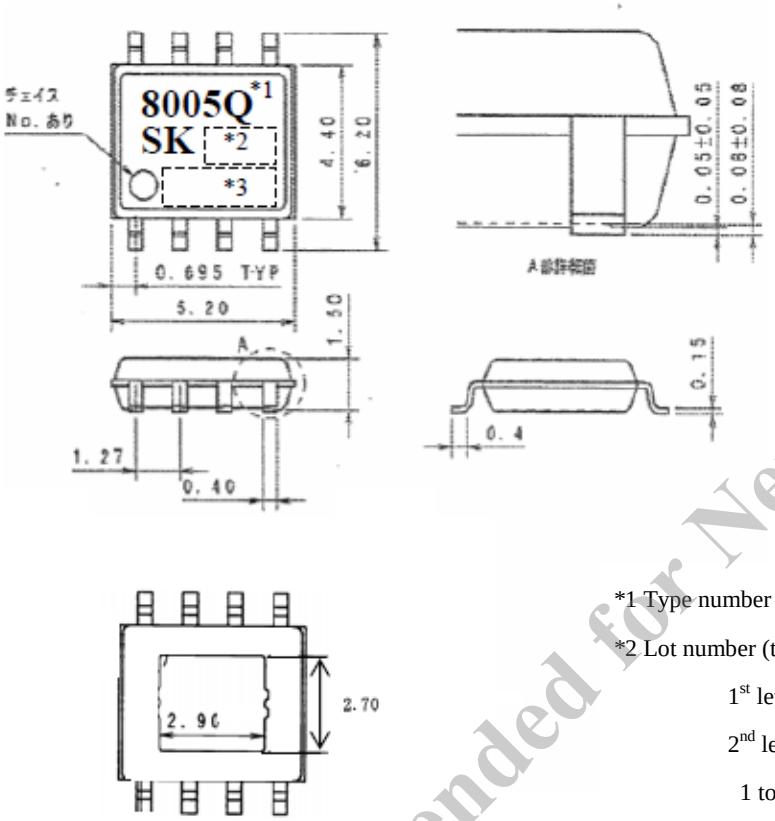
- Type: Semiconductor integrated circuits (monolithic IC)
- Structure: Resin molding type (transfer molding)

2. Specification

● 2-1 Package Information

2-1-1 SI-8005Q

Unit: mm



*1 Type number

*2 Lot number (three digit)

1st letter: The last digit of year

2nd letter: Month

1 to 9 for Jan. to Sep.

O for Oct.

N for Nov.

D for Dec.

3rd and 4th letter: week

*3 Control number (four digit)

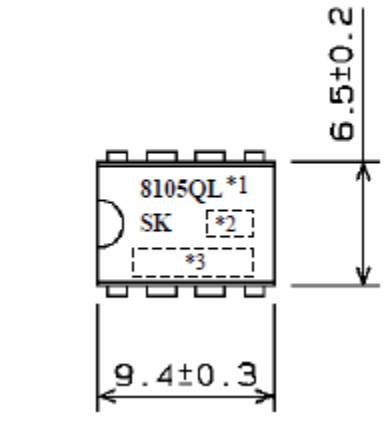
Pin Assignment

1. BS
2. IN
3. SW
4. GND
5. FB
6. COMP
7. EN
8. SS

External Terminal Processing: Sn plating

2-1-2 SI-8105QL

Unit: mm



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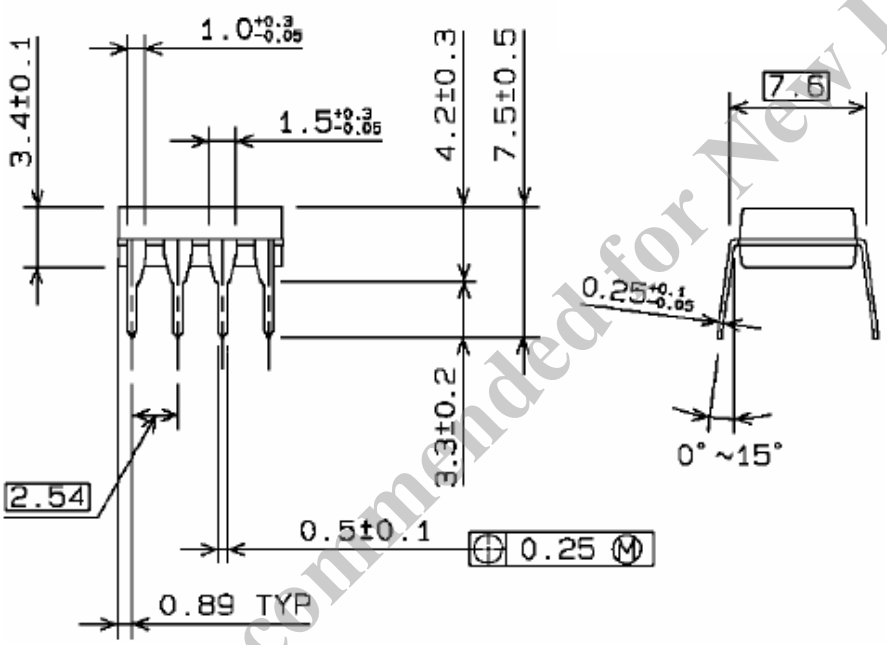


Pin Assignment

1. BS
2. IN
3. SW
4. GND
5. FB
6. COMP
7. EN
8. SS

External Terminal Processing: Sn-Ag plating

● 2-2 Ratings

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Conditions
Input Voltage VIN	VIN	30	V	
Input Voltage VEN	VEN	6	V	
Allowable Power Dissipation *1	Pd	1.35	W	(8005Q) *2
		1.50		(8105QL) *3
Junction Temperature	Tj	150	°C	
Storage Temperature	Tstg	-40～150	°C	
Thermal resistance (Junction and case)	θj-c	40	°C/W	(8005Q) *2
		25		(8105QL) *3
Thermal resistance (Junction and ambient)	θj-a	74	°C/W	(8005Q) *2
		67		(8105QL) *3

*1. Since the thermal shutdown is provided, it may be operated at Tj > 140°C.

*2. Glass epoxy board: 30.0mm × 30.0mm (copper foil area: 25.0mm × 25.0mm)

*3. Glass epoxy board: 70.0mm × 60.0mm (copper foil area: 1310 mm^2)

Table 2 Recommended Conditions

Parameter	Symbol	SI-8005Q/SI-8105QL	Unit
DC Input Voltage	V_{IN}	*2 Vo+3v - 28	V
Output Current	Io	0～3.5	A
Junction Temperature in Operation	Tjop	-30 - +125	°C
Temperature in Operation	Top	-30 - +85	°C

*2 The minimum value of input voltage range is 4.75V or VO + 3V whichever higher.

In the case of VIN = Vo+2 ~ Vo+3, IOUT is equal to 2A MAX.

In the case that the IC is used at VIN = Vo +1 – Vo +2V (especially in the case that VIN voltage is 8V or lower), IC loss will be increased, therefore efficient heat dissipation is required in designing the wiring board.

When sufficient heat dissipation cannot be obtained because of several limitations with respect to the size of wiring boards, mounted component etc, the overheat protection operation will function.

Table 3 Electrical Characteristics (Ta = 25°C, Vo = 5V, R1 = 46kΩ, R2 = 5.1kΩ)

Parameter		Symbol	Ratings			Unit	Test Condition
			MIN	MIN	MIN		
Setting Reference Voltage		VREF	0.485	0.500	0.515	V	V_{IN}=12V, I_O=1.0A
Output Voltage Temperature Coefficient		ΔVREF/ΔT		±0.05		mV/°C	V_{IN}=12V, I_O=1.0A Ta=-25°C to 100°C
Efficiency *8		η		90		%	V_{IN}=12V, Vo=5V, I_O=1A
Operation Frequency (SI-8005Q)		fo	450	500	550	kHz	V_{IN}=16V, Vo=5V, I_O=1A
Operation Frequency (SI-8105QL)		fo	315	350	385	kHz	V_{IN}=16V, Vo=5V, I_O=1A
Line Regulation		VLine		10	60	mV	V_{IN}=8~28V, Vo=5V, I_O=1A
Load Regulation		VLoad		10	60	mV	V_{IN}=12V,Vo=5V, I_O=0.1 - 3.5A
Overcurrent Protection Start Current		IS	3.6		6.0	A	V_{IN}=12V, Vo=5V
Circuit Current in Non-operation 1		IIN		18		mA	V_{IN}= 12V, V_O=5V, I_O=0A, V_{EN}= open
Circuit Current in Non-operation 2		IIN(off)		10	30	uA	V_{IN}= 12V, V_O=5V, I_O=0A, V_{EN}= 0V
SS terminal	Flow-out Current at Low Level Voltage	ISSL		5		μA	V_{SSL}=0V, V_{IN}= 16V
EN terminal	High Level Voltage	VC/EH	2.8			V	V_{IN}=12V
	Low Level Voltage	VC/EL			2.0	V	V_{IN}=12V
	Flow-out Current at Low Level Voltage	IC/EH		1		μA	V_{EN}=0V
Slope Compensation		Kc	0.3			A/μsec	
Error Amplifier Voltage Gain		AEA		1000		V/V	
Error Amplifier Trans-conductance		GEA		800		uA/V	
Current Sense Amplifier Impedance		1/GCS		0.35		V/A	
Maximum ON Duty		DMAX		90		%	
Minimum ON Duty		DMIN		100		nsec	
High-side Switching ON resistance		Ron1		180		mΩ	V_{IN}<10V
		Ron2		130		mΩ	V_{IN}≧10V

● 2-3 Circuit Diagram

2-3-1 Internal Equivalent Circuit

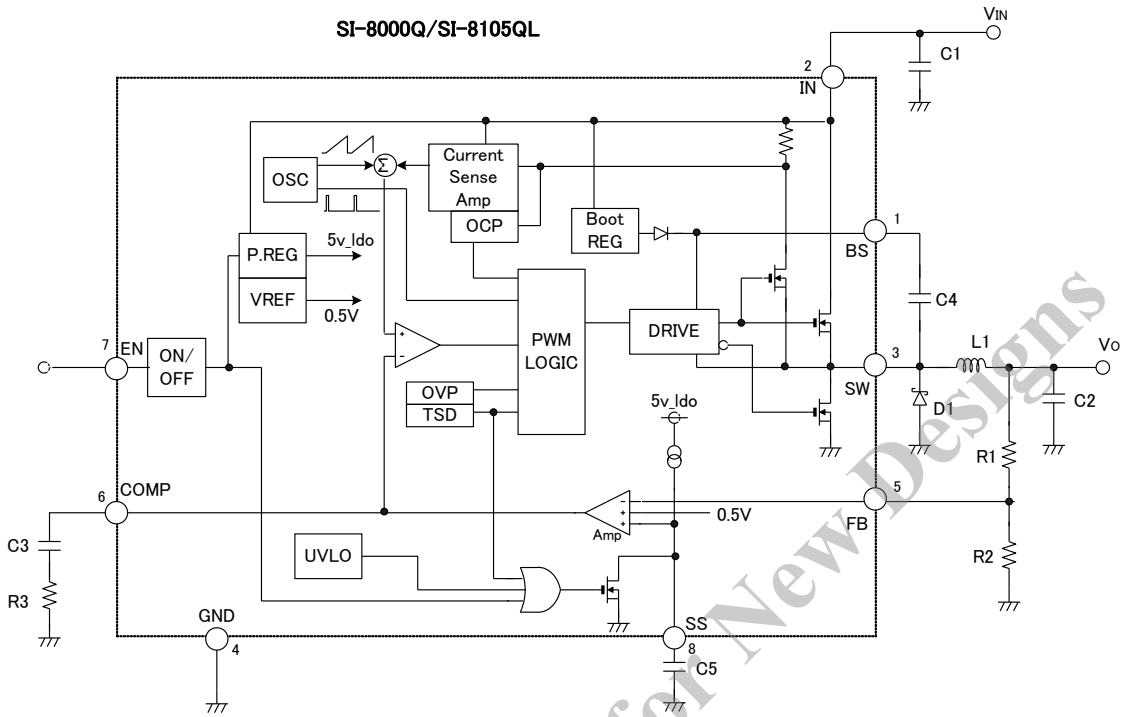


Fig. 1

2-3-2 Typical Connection Diagram

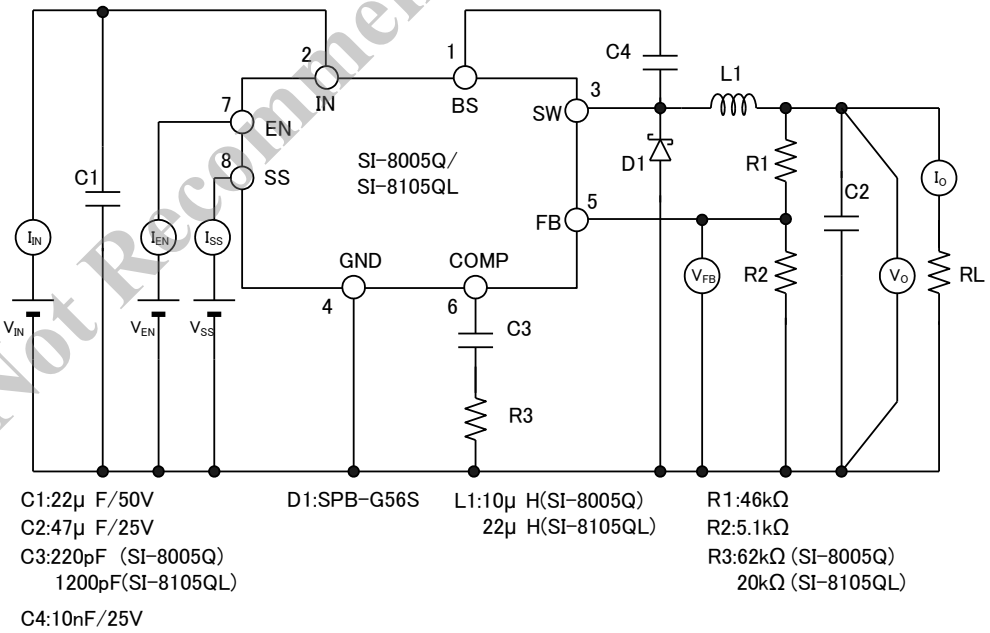


Fig. 2

3. Terminal Description

● 3-1 Terminal List

Table 4

Terminal	SI-8005Q/8105QL	
	Symbol	Description
1	BS	High side boost terminal
2	VIN	Input terminal
3	SW	Switching output terminal
4	GND	Ground terminal
5	FB	Feedback voltage terminal
6	COMP	Phase compensation terminal
7	EN	ON/OFF terminal
8	SS	Soft start terminal

● 3-2 Functional Description of Terminal

- BS (terminal No. 1)

  It is an internal power supply for driving the gate of high side switch Nch - MOS. A capacitor of 10 nF or more is connected between the SW terminal and BS terminal to drive the high side Nch - MOS.

- VIN (terminal No. 2)

  It is an input voltage of IC.

- SW (terminal No. 3)

  It is a switching output terminal which supplies power to the output.

- GND (terminal No. 4)

  It is a ground terminal.

- FB (terminal No. 5)

  It is a terminal for setting the output voltage. The output voltage is set by R1 and R2.

- Comp (terminal No. 6)

  It is a phase compensation terminal for controlling the loop stably.

- EN (terminal No. 7)

  It is a terminal for turning ON/OFF the IC.

- SS (terminal No. 8)

  The soft start of output voltage can be made by connecting a capacitor to this terminal.

4. Operational Description

● 4-1 PWM Output Voltage Control

The SI-8005Q/8105Q consists of 2 systems of feedback loops of current control and voltage control and 3 blocks which compensate slope and, in the voltage control feedback, the output voltage is fed back for PWM control loop and the SI-8005Q is composed of an error amplifier which compares the division of resistance with the reference voltage of 0.5V. The current control feedback is a loop which feeds back the inductor current for PWM control and the inductor current shunted by using a sense MOS is detected by a current sense amplifier. With respect to the slope compensation, in consideration of current control system, in order to avoid the sub harmonic oscillation, slope compensation is made for the current control slope. As shown in Fig.5, in the SI-8005Q, by means of voltage control feedback, current control feedback and calculation of slope compensation, the PWM control by current control system is made.

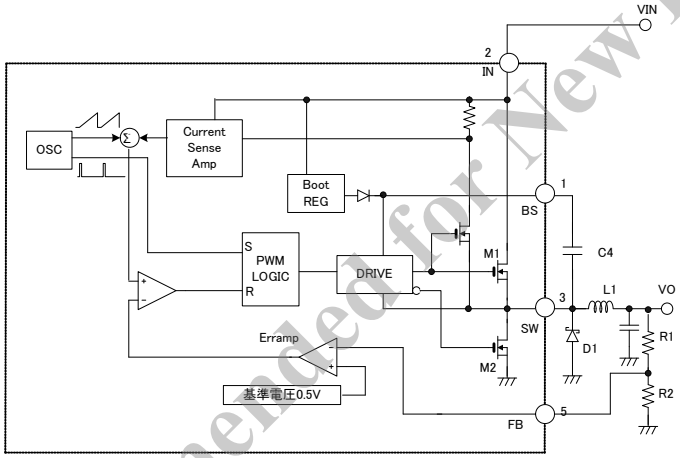


Fig.3 Current Control PWM Chopper Regulator Basic Configuration

Since the SI-8005Q is a current control regulator, the COMP terminal voltage is proportional to the peak value of the inductor current. When the ULVO is released or the EN terminal exceeds the threshold value, the switching operation is made. At first, switching operation is made by MIN ON duty or MAX ON duty and the high side switch (hereinafter called as M1) and the switch for BS capacitor charging (hereinafter called as M2) turn ON and OFF alternately. M1 is a switching MOS which provides power to the output, while M2 charges the capacitor C4 for boost which drives M1.

At M1: ON / M2: OFF, inductor current is increased by applying voltage to the SW switch and inductor, and the output of the current detection amplifier which detects it also rises. The signal to which the output of this current detection amplifier and the Ramp compensation signal are added is compared with the output of the error amplifier by the current comparator (CUR COMP). When the added signal exceeds the output of the error amplifier (COMP terminal voltage), the output of the current comparator becomes “H” to reset the RS flip-flop. Then, M1 turns off and M2 turns on. Thereby, the regenerated current flows through the external SBD (D1).

In the SI-8005Q, the reset signal is generated at each cycle to reset the RS flip-flop. In the case the added signal does not exceed the COMP terminal voltage, the RS flip-flop is reset without fail by the signal of the 10% OFF Duty circuit.

● 4-2 Overcurrent Protection / Thermal Shutdown

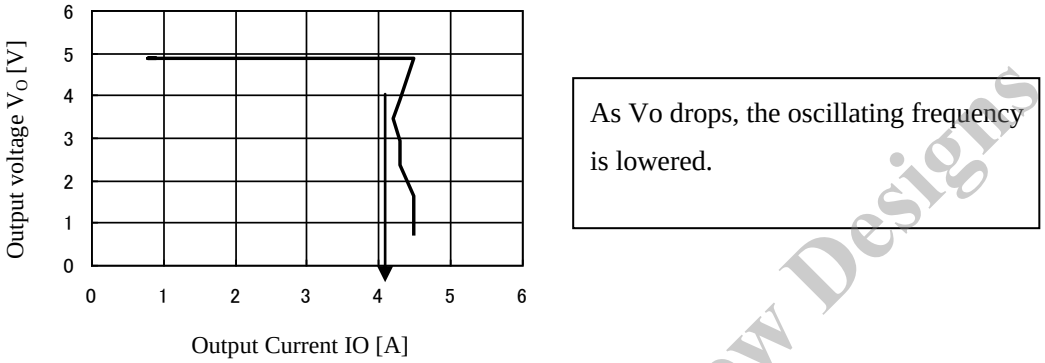


Fig.4 Output Voltage Characteristics in Overcurrent

The SI-8005Q/8105QL integrates a current limiting type overcurrent protection circuit. The overcurrent protection circuit detects the peak current of a switching transistor and when the peak current exceeds the set value, the ON time of the transistor is compulsorily shortened to limit the current by lowering the output voltage.

In addition, when the output voltage is lowered, the increase of current at low output voltage is prevented by dropping the switching frequency to about 50 KHz. When the overcurrent condition is released, the output voltage will be automatically restored.

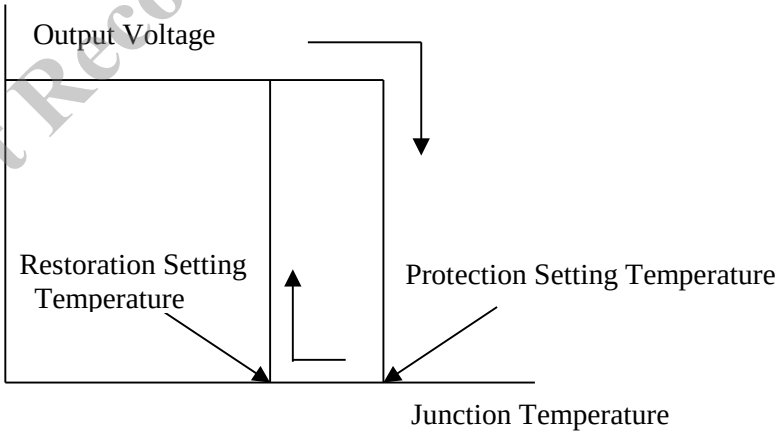


Fig.5 Output Voltage Characteristics in Thermal Shutdown

The thermal shutdown circuit detects the semiconductor junction temperature of the IC and when the junction temperature exceeds the set value (around 140°C), the output transistor is stopped and the output is

turned OFF. When the junction temperature drops from the set value for overheat protection by around 10°C, the output transistor is automatically restored.

* Note for thermal shutdown characteristic

This circuit protects the IC against overheat resulting from the instantaneous short circuit, but it should be noted that this function does not assure the operation including reliability in the state that overheat continues due to long time short circuit.

5. Cautions

● 5-1 External Components

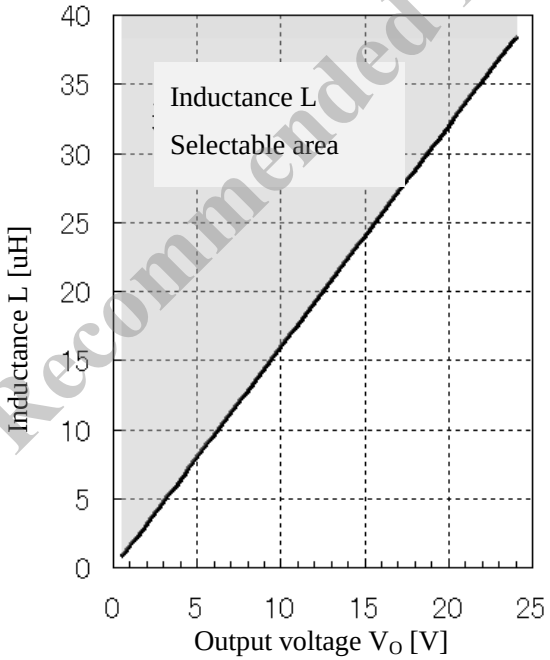
5-1-1 Choke coil L1

The choke coil L1 is one of the most important components in the chopper type switching regulator. In order to maintain the stable operation of the regulator, such dangerous state of operation as saturation state and operation at high temperature due to heat generation must be avoided.

The following points should be taken into consideration for the selection of the choke coil.

a) The choke coil should be fit for the switching regulator. The coil for a noise filter should not be used because of large loss and generated heat.

b) For the peak detection current control, the inductance current may fluctuate at the cycle of integral multiple of switching operation frequency. Such phenomenon is called as sub harmonic oscillation and it may theoritically occur in the peak detection current control mode. Therefore, in order to assure stable operation, the inductance current is compensated inside the IC, and it is required to select a proper inductance value to the output voltage.



Please set the L value, however, as the upper limit of ΔIL > 0.1A

Fig. 6 shows the selection range of the inductance L value to avoid the sub harmonic oscillation.

The pulse current of choke coil ΔIL and the peak current ILp are expressed by the following equation:

$$\Delta IL = \frac{(Vin - Vout) \cdot Vout}{L \cdot Vin \cdot f} \quad \text{---} \quad \text{(A)}$$

$$ILp = \frac{\Delta IL}{2} + Iout \qquad \text{---} \quad (B)$$

From this equation, you will see that as the inductance L of choke coil is decreased, ΔIL and ILP are increased. In the event that the inductance is too small, the fluctuation of choke coil current is larger, resulting in unstable operation of the regulator.

Care should be taken of decrease of inductance of choke coil due to magnetic saturation of overload, load short circuit etc.

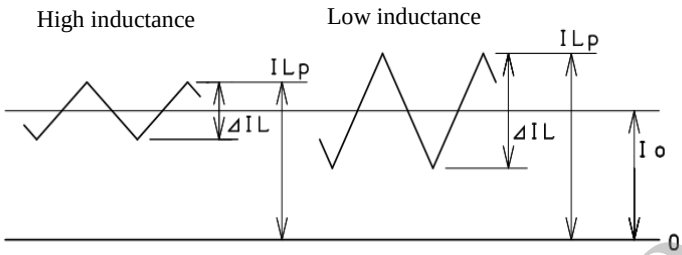


Fig.7 Relation between Ripple current I_{LP} and Output Current I_O

c) The rated current shall be met.

The rated current of the choke coil must be higher than the maximum load current to be used. When the load current exceeds the rated current of the coil, the inductance is sharply decreased to the extent that it causes saturation state at last. Please note that overcurrent may flow since the high frequency impedance becomes low.

d) Noise shall be low.

In the open magnetic circuit core which is of drum shape, since magnetic flux passes outside the coil, the peripheral circuit may be damaged by noise. It is recommended to use the toroidal type, EI type or EE type coil which has a closed magnetic circuit type core as much as possible.

5-1-2 Input Capacitor C1

The input capacitor is operated as a bypass capacitor of the input circuit to supply steep current to the regulator during switching and to compensate the voltage drop of the input side. Therefore, the input capacitor should be connected as close as to the regulator IC.

Even in the case that the rectifying capacitor of the AC rectifier circuit is located in the input circuit, the input capacitor cannot play a role of the rectifying capacitor unless it is connected near the SI-8005Q.

The selection of C1 shall be made in consideration of the following points:

a) The requirement of withstand voltage shall be met.

b) The requirement of the allowable ripple voltage shall be met.

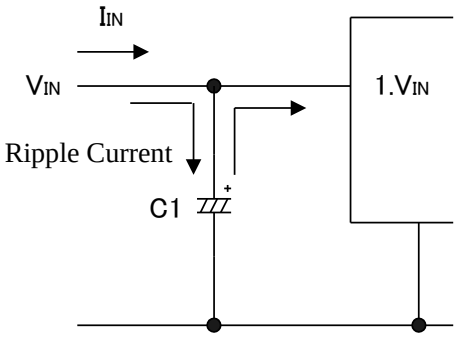


Fig.8 Current Flow of C1

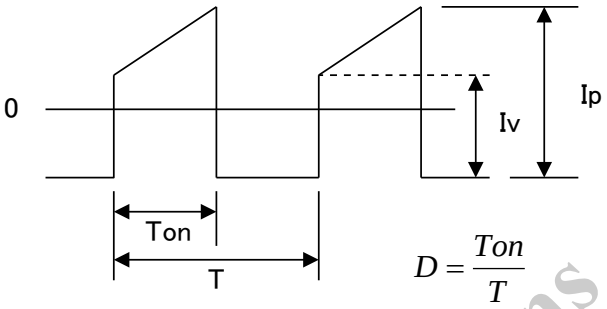


Fig. 9 Current Waveform of C1

The ripple current of the input capacitor is increased in accordance with the increase of the load current.

If the withstanding voltages or allowable ripple voltages are exceeded or used without derating, it is in danger of causing not only the decreasing the capacitor lifetime (burst, capacitance decrease, equivalent impedance increase, etc) but also the abnormal oscillations of regulator.

Therefore, the selection with sufficient margin is needed.

The effective value of ripple current flowing across the input capacitor can be calculated by the following equation (2):

$$Irms \approx 1.2 \times \frac{Vo}{Vin} \times Io \quad --(2)$$

For instance, where V_{IN} = 20V, Io = 3A and Vo= 5V,

$$Irms \approx 1.2 \times \frac{5}{20} \times 3 = 0.9A$$

Therefore, it is necessary to select the capacitor with the allowable ripple current of 0.9A or higher.

5-1-3 Output Capacitor C2

The current control system is a voltage control system to which a loop which detects and feeds back the inductance current is added. By adding inductor current to the feedback loop, stable operation is realized without taking into consideration the influence of secondary delay of the LC filter. Therefore, the capacitance C of the LC filter which is required to compensate the secondary delay can be decreased and furthermore, stable operation can be obtained, even if the low ESR capacitor (ceramic capacitor) is used.

The output capacitor C2 composes a LC low pass filter together with a choke coil L1 and functions as a rectifying capacitor of switching output. The current equivalent to the pulse current ΔIL of the choke coil current is charged and discharged in the output capacitor. Therefore, it is necessary to meet the requirements of withstand voltage and allowable ripple current with sufficient margin like the input capacitor.

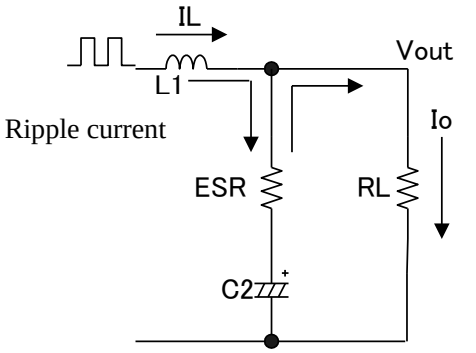


Fig.10 C2 current flow

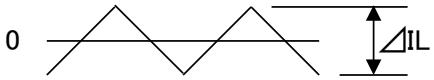


Fig.11 C2 current curve

The ripple current of the output capacitor is equal to the ripple current of the choke coil and does not vary even if the load current increases or decreases.

The ripple current effective value of the output capacitor is calculated by the equation (3).

$$Irms = \frac{\Delta IL}{2\sqrt{3}} \qquad ---(3)$$

When ΔIL = 0.5A,

$$Irms = \frac{0.5}{2\sqrt{3}} \fallingdotseq 0.14A$$

Therefore a capacitor having the allowable ripple current of 0.14A or higher is required.

In addition, the output ripple voltage Vrip of the regulator is determined by a product of the pulse current ΔIL of the choke coil current (= C2 charging/discharging current) and the equivalent series resistance ESR of the output capacitor.

$$Vrip = \Delta IL \cdot C2ESR \qquad ---(4)$$

It is therefore necessary to select a capacitor with low equivalent series resistance ESR in order to lower the output ripple voltage. As for general electrolytic capacitors of same product series, the ESR shall be lower, for the products of higher capacitance with same withstand voltage, or with higher withstand voltage (almost proportional to larger externals) with same capacitance.

When ΔIL = 0.5A, Vrip = 40mV,

$$C2esr = 40 \div 0.5 = 80m\Omega$$

As shown above, a capacitor with the ESR of 80mΩ or lower should be selected. In addition, since the ESR varies with temperature and increases at low temperature, it is required to examine the ESR at the actual operating temperatures. It is recommended to contact capacitor manufacturers for the ESR value since it is peculiar to capacitors.

5-1-4 Flywheel Diode D1

The flywheel diode D1 is to discharge the energy which is stored in the choke coil at switching OFF.

For the flywheel diode, the Schottky barrier diode must be used. If a general rectifying diode or fast recovery diode is used, the IC may be damaged by applying reverse voltage due to the recovery and ON voltage.

In addition, since the output voltage from the SW terminal (pin 3) of the SI-8000Q series is almost equivalent to the input voltage, the flywheel diode with the reverse withstand voltage of the input voltage or higher should be used.

It is recommended not to use the ferrite bead for the flywheel diode.

5-1-5 Phase compensation elements C3, C6, R3

The stability and responsiveness of the loop are controlled through the COMP terminal.

The COMP terminal is an output of the internal trans-conductance amplifier.

The series combination of a capacitor and resistor sets the combination of pole and zero which determines characteristics of the control system. The DC gain of voltage feedback loop can be calculated by the following equation:

$$Adc = Rl \times \mathrm{Gcs} \times \mathrm{A_{EA}} \times \frac{\mathrm{V_{FB}}}{\mathrm{Vout}}$$

Here, VFB is feedback voltage (0.5V). AEA is the voltage gain of error amplifier, G_{CS} trans-inductance of current detection and R1 a load resistance value. There are 2 important poles. One is produced by a phase compensation capacitor (C3) and an output resistor of the error amplifier.

Another one is produced by a output capacitor and a load resistor. These poles appear at the following frequencies:

$$fp1 = \frac{G_{EA}}{2\pi \times C3 \times A_{EA}}$$

$$fp2 = \frac{1}{2\pi \times C2 \times Rl}$$

Here, G_{EA} is the trans-conductance of error amplifier. In this system, one zero is important. This zero is produced by phase compensation capacitor C3 and phase compensation resistance R3. This zero appears in the following frequencies:

$$fz1 = \frac{1}{2\pi \times C3 \times R3}$$

If the output capacitor is large and/or ESR is large, this system may have another important zero. This zero is produced by the ESR and capacitance of the output capacitor. And it exists in the following frequencies:

$$fESR = \frac{1}{2\pi \times C2 \times RESR}$$

In this case, the third pole which is set by the phase compensation capacitor (C6) and phase compensation resistor (R3) is used to compensate the effect of ESR zero on the loop gain.

This pole exists in the following frequencies:

$$p3 = \frac{1}{2\pi \times C6 \times R3}$$

The objective of design of phase compensation is to form the converter transfer function to obtain the desired loop gain. The system crossover frequency where the feedback loop has a single gain is important.

The lower crossover frequency will produce the slower line and load transient. In the meantime, the higher crossover frequency may cause instability of the system. The selection of the most suitable phase

compensation element is described below.

1. A phase compensation resistor (R3) is selected to set the resistor at the desired crossover frequency.
The calculation of R3 is made by the following equation:

$$R3 = \frac{2\pi \times C2 \times fc}{GEA \times GCS} \times \frac{Vout}{VFB} < \frac{2\pi \times C2 \times 0.1 \times fs}{GEA \times GCS} \times \frac{Vout}{V_{FB}}$$

Here, fc is a desired crossover frequency. It should be one tenth or lower of the normal switching frequency (fs).

2. In order to achieve the desired phase margin, a phase compensation capacitor (C3) is selected.
For the application having a representative inductance value, adequate phase margin is provided by setting the zero compensation of one fourth or lower of the crossover frequency.
C3 is calculated by the following equation.

$$C3 > \frac{4}{2\pi \times R3 \times fc}$$

R3 is a phase compensation resistor.

3. It is required to judge whether the second compensation capacitor C6 is necessary or not.
It will be necessary, when the ESR zero of the output capacitor is located at a frequency which is lower than the half of the switching frequency.
Namely, it is necessary, when the following equation is applicable.

$$\frac{1}{2\pi \times C2 \times RESR} < \frac{fs}{2}$$

In this case, the second compensation capacitor C6 is added and the frequency fp3 of ESR zero is set.
C6 is calculated from the following equation.

$$C6 = \frac{C2 \times RESR}{R3}$$

The constants for each output setting voltage in the case that ceramic capacitors or aluminum electrolytic capacitors are used are shown in the following table.
The inductor L should be selected by reference to the choke coil L1 of 4-1-1.

Table 5 Output setting voltage (use ceramic capacitors)

Vout [V]	L [uH]	Cout [uF] (ceramic capacitor)	fc = 50kHz			fc = 20kHz		
			R3 [kΩ]	C3 [pF]	C6 [pF]	R3 [kΩ]	C3 [pF]	C6 [pF]
1.2	2.4~10	22 x 2	14	1000	No	5.7	5600	No
1.8	4.7~10	22 x 2	20	620	No	8.5	3800	No
3.3	6.8~	22 x 2	39	360	No	15	2200	No
5	8.2~	22 x 2	59	220	No	20	1500	No
12	22~	22 x 2	140	100	No	57	620	No

Table 6 Output setting voltage (use aluminum electrolytic capacitors)

Vout [V]	L [uH]	Cout [uF]/ ESR[mΩ] (aluminum electrolytic capacitor)	fc = 50kHz			fc = 20kHz		
			R3 [kΩ]	C3 [pF]	C6 [pF]	R3 [kΩ]	C3 [pF]	C6 [pF]
1.2	2.4~10	220/100	70	180	330	28	1200	860
1.8	4.7~10	220/100	100	180	320	42	820	560
3.3	6.8~	220/100	190	100	150	78	560	330
5	8.2~	220/100	290	100	100	110	330	220
12	22~	220/100	700	100	100	280	120	100

Table 7 Output setting voltage (use ceramic capacitors) (SI-8105QL)

Vout [V]	L [uH]	Cout [uF] (ceramic capacitor)	fc = 35kHz			fc = 14kHz		
			R3 [kΩ]	C3 [pF]	C6 [pF]	R3 [kΩ]	C3 [pF]	C6 [pF]
1.2	2.4~10	22 x 2	10	2200	no	4	10000	No
1.8	4.7~10	22 x 2	15	1800	No	6	8600	No
3.3	6.8~	22 x 2	27	680	No	10	4700	No
5	8.2~	22 x 2	40	470	No	16	3300	No
12	22~	22 x 2	100	220	No	40	1200	No

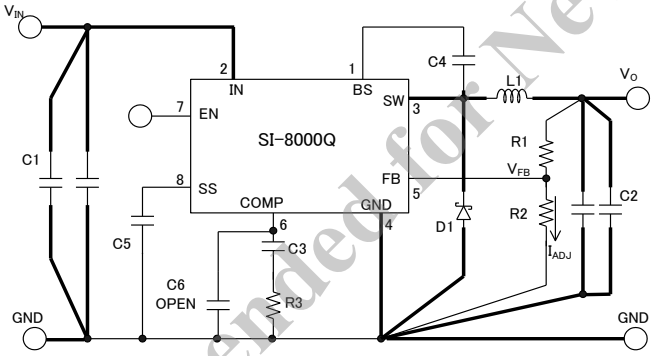
Table 8 Output setting voltage (use aluminum electrolytic capacitors) (SI-8105QL)

Vout [V]	L [uH]	Cout[uF]/ ESR[mΩ] (aluminum electrolytic capacitors)	fc = 35kHz			fc = 14kHz		
			R3 [kΩ]	C3 [pF]	C6 [pF]	R3 [kΩ]	C3 [pF]	C6 [pF]
1.2	2.4~10	220/100	50	390	470	20	3300	1500
1.8	4.7~10	220/100	75	330	330	30	1800	1000
3.3	6.8~	220/100	130	220	220	56	1000	470
5	8.2~	220/100	200	100	150	83	560	330
12	22~	220/100	500	100	100	200	330	180

● 5-2 Pattern Design Notes

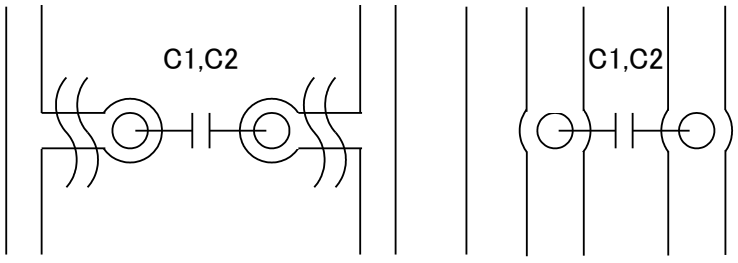
5-2-1 High Current Line

Since high current flows in the bold lines in the connection diagram, the pattern should be as wide and short as possible.



5-2-2 Input/ Output Capacitor

The input capacitor C1 and the output capacitor C2 should be connected to the IC as close as possible. If the rectifying capacitor for AC rectifier circuit is on the input side, it can be used as an input capacitor. However, if it is not close to the IC, the input capacitor should be connected in addition to the rectifying capacitor. Since high current is discharged and charged through the leads of input/output capacitor at high speed, the leads should be as short as possible. A similar care should be taken for the patterning of the capacitor.



Improper Pattern Example Proper Pattern Example

5-2-3 FB Terminal (Output Voltage Set-up)

The FB terminal is a feedback detection terminal for controlling the output voltage. It is recommended to connect it as close as possible to the output capacitor C2. When they are not close, the abnormal oscillation may be caused due to the poor regulation and increase of switching ripple.

The output voltage set-up is achieved by connecting R1 and R2.

I_{FB} should be set to be around 0.1mA.

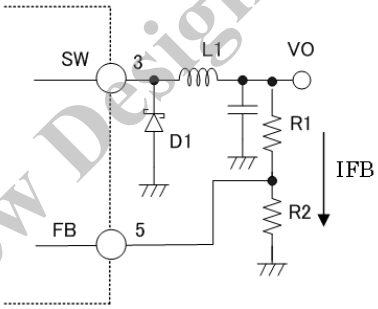
(The I_{FB} lower limit is 0.1mA, and the upper limit is not defined. However, it is necessary to consider that the consumption current shall increase according to the I_{FB} value, resulting in lower efficiency.)

R1, R2 and output voltage are calculated from the following equations:

$$I_{FB} = V_{FB} / R2 \quad *V_{FB} = 0.5V \pm 3\%$$

$$R1 = (Vo - VFB) / I_{FB} \qquad R2 = V_{FB} / I_{FB}$$

$$Vout = R1 \times (V_{FB} / R2) + VFB$$

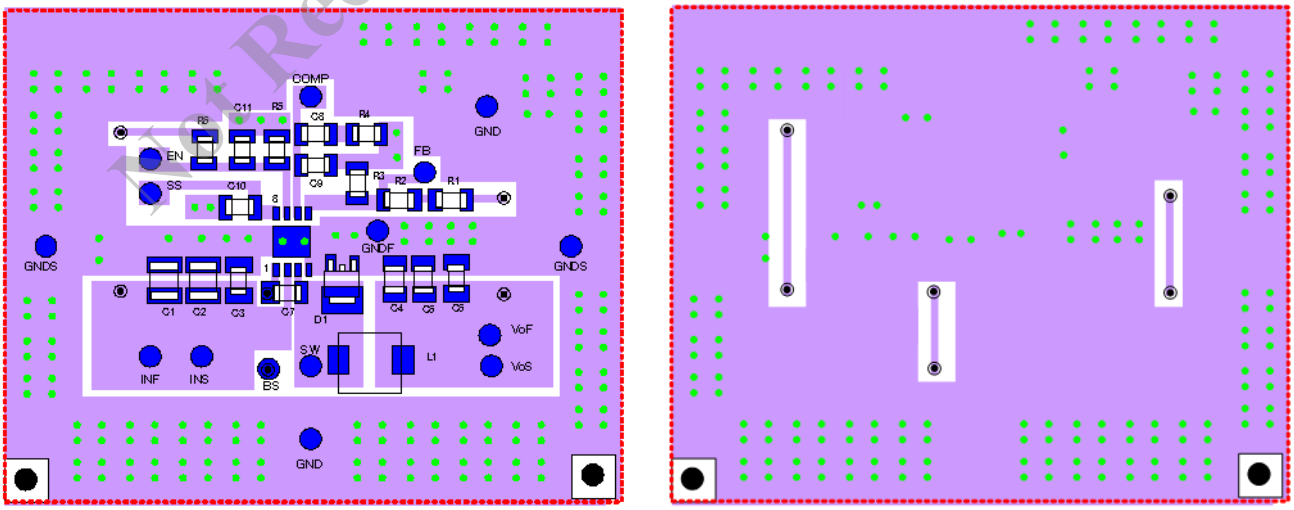


- R2 should be connected for the stable operation when set to Vo = 0.5V.
- It is recommended to set the output voltage to 10% or higher of the input voltage

The wiring of COMP terminal, FB terminal, R1 and R2 that run parallel to the flywheel diode should be avoided, because switching noise may interfere with the detection voltage to cause abnormal oscillation. It is recommended to implement the wiring from the FB terminal to R2 as short as possible.

- Mounting Board Pattern Example

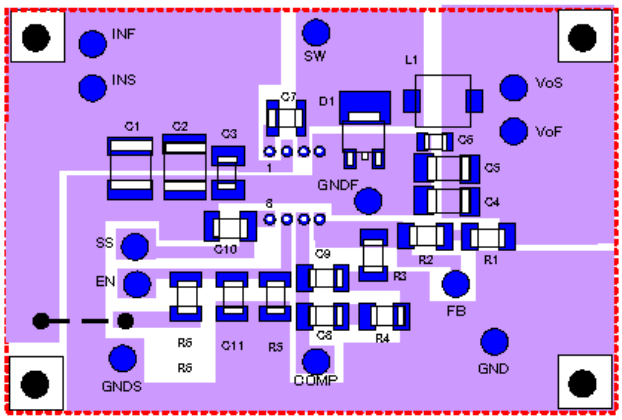
Component Insertion Type (SI-8005Q)



Front side: materials on this side

Back side: GND side

Component Insertion Type (SI-8105QL)



Silk printed side

● 5-3 Power Supply Stability

The phase characteristics of the chopper type regulator are synthesized by the phase characteristics inside the regulator IC and that of output capacitor Cout and the load resistor Rout.

The phase characteristics inside the regulator IC are generally determined by the delay time of the control block and the phase characteristic of the output error amplifier.

Among these two factors, the phase delay due to the delay time of the control block rarely causes problems in actual use. Therefore, the phase characteristics of the error amplifier are important.

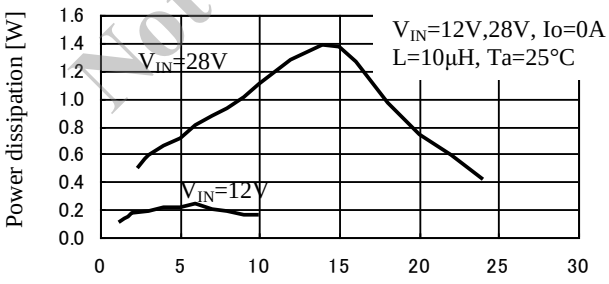
With respect to the compensation of phase characteristics of the output error amplifier, external parts such as resistors and capacitors should be connected outside the IC for phase compensation.

Please refer to phase compensation elements C3, C6 and R3 of 4-1-5.

● 5-4 Power Dissipation of IC with No Load

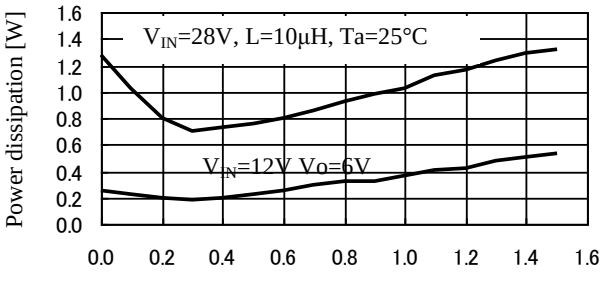
5-4-1 SI-8005Q Power dissipation of IC

(1) Power dissipation with no load



Output Voltage [V]

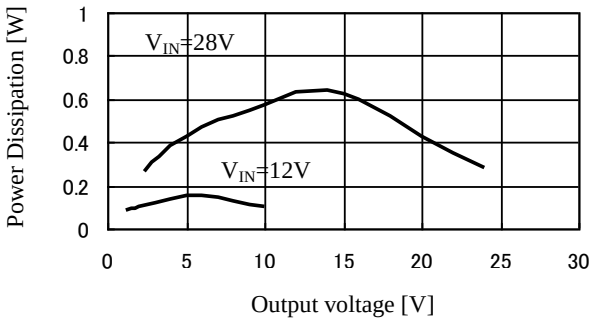
(2) Power dissipation with load



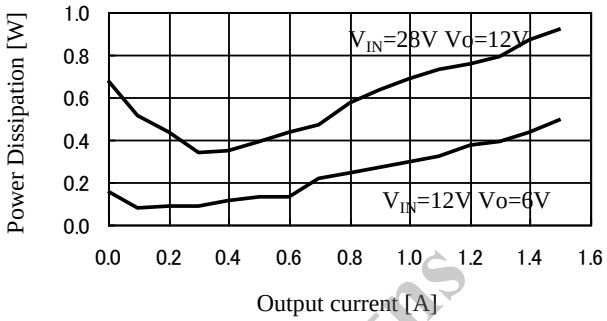
Peak voltage: -3.0V

5-4-2 SI-8105QL Power dissipation of IC

(1) Power dissipation with no load



(2) Power dissipation with load



The SI-8105Q/8105QL have such architecture that the energy of the output capacitor C2 is consumed by the LS SW MOS in the internal equivalent circuit diagram of Fig. 1, therefore loss in the IC will occur. (Refer to (2) Power dissipation with load.)

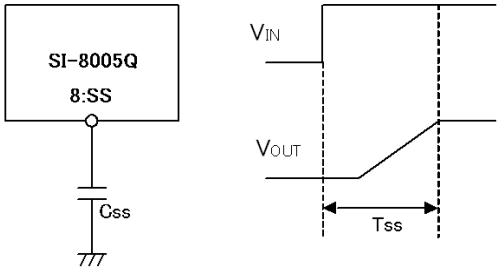
6. Applications

● 6-1 Soft Start

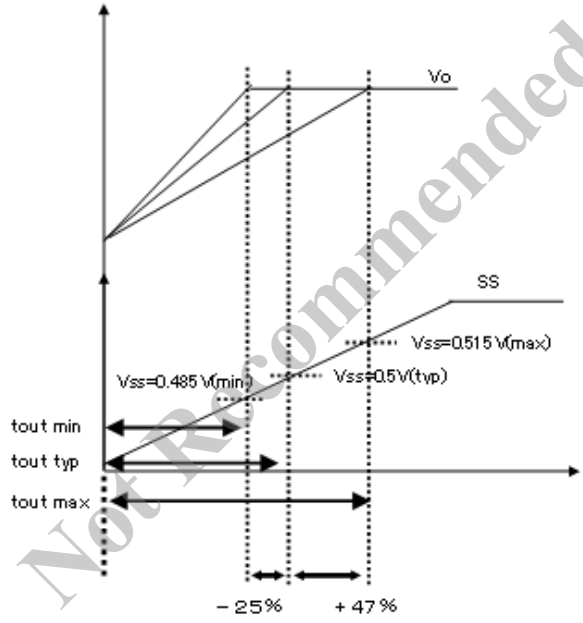
When a capacitor is connected to terminal 8, the soft start is activated when the input voltage is applied. Vout rises in relation with the charging voltage of Css. Therefore, the rough estimation is done by the time constant calculation of Css charging.

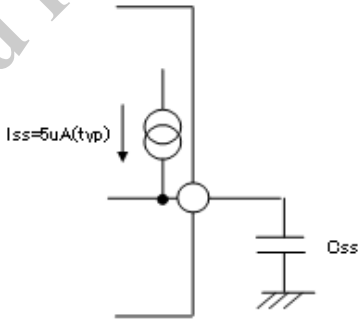
The capacitor Css controls the rise time by controlling the OFF period of PWM control. The rise time tss is calculated approximately by the following equation:

The terminal 8 should be open, when the soft start is not used.



tss = (Css × Vss) / IssL (sec)





The time that output voltage rises to set-up value is equal with the time that Vss rises to 0.5V.

The variation range of each parameter

Vss = 0.5V ±3% (0.485 – 0.515V)

Iss = 5μA ±30% (3.5 – 6.5μA)

Vss and Iss are parameters of soft start time variation.

Variation range can be calculated with following equations.

When Css = 0.47μF,

t_{OUT} min = Css × Vss min / Iss max = 0.47μF × 0.485V / 6.5μA = 37.2msec

t_{OUT} typ = Css × Vss / Iss = 0.47μF × 0.5V / 5μA = 47msec

t_{OUT} max = Css × Vss min / Iss max = 0.47μF × 0.515V / 3.5μA = 69.1msec

Since the SS terminal is pulled up (4.7V TYP) with the internal power supply of IC, the external voltage can not be applied.

If there is no Css or it is extremely low, Vout rises at the time constants charging the output capacitor with the output current restricted by the overcurrent protection Is.

Time constants at output capacitor start-up

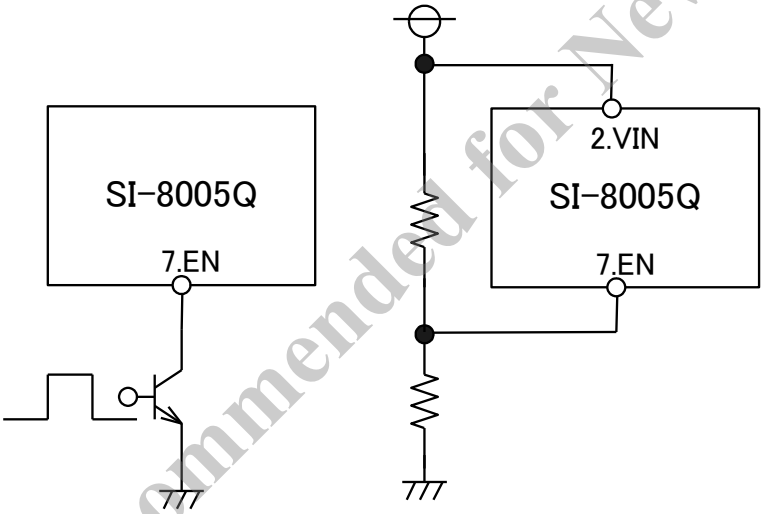
$$t = (Co \times Vo) / Is \text{ (at no load)}$$

*The amount of load current is deducted from the Is value at load.

● 6-2 Output ON/ OFF Control

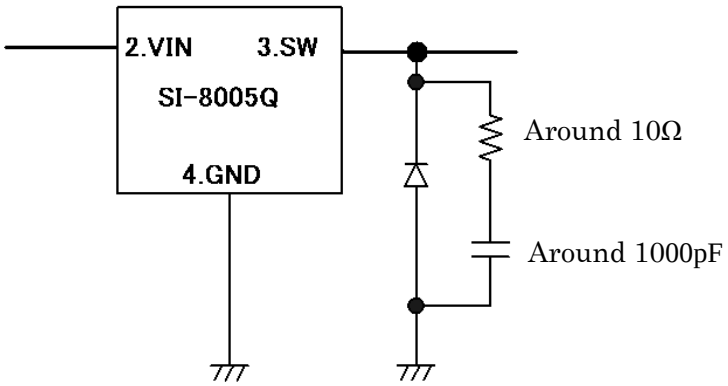
The output ON-Off control is possible using the SS (No.7) terminal. The output is turned OFF when the terminal 7 voltage falls below VENL (2.0V) by such as open collector.

A voltage dividing resistor should be inserted between VIN and GND and divided VIN voltage can be applied to the EN terminal. Over 6V shall not be applied to EN terminal.



● 6-3 Spike Noise Reduction

In order to reduce the spike noise, it is possible to compensate the output waveform of the SI-8005Q and the recovery time of the diode by a capacitor, but it should be noted that the efficiency is also slightly reduced.



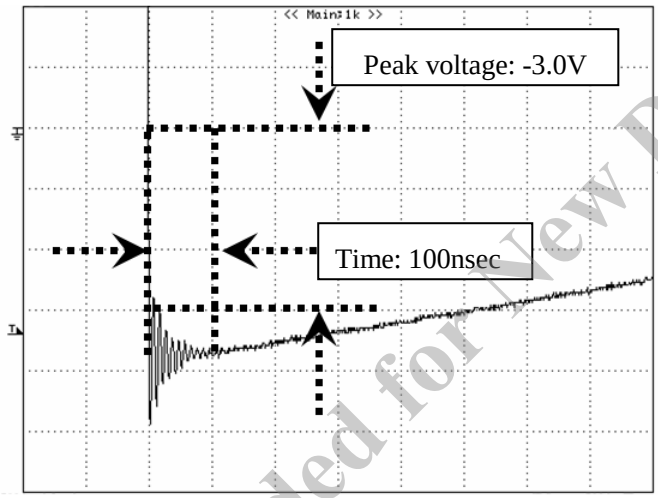
* When the spike noise is observed with an oscilloscope, the lead wire may function as an antenna and the spike noise may be observed extremely higher than usual if the probe GND lead wire is too long. In the observation of spike noise, the probe lead wire should be as short as possible and be connected with the root of the output capacitor.

● 6-4 SW terminal negative potential

The assurance of SW terminal negative electric potential shall be as follows:

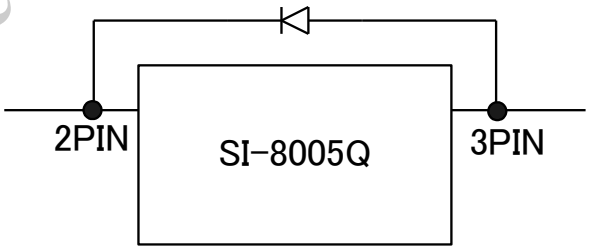
Assured value: within 30V of voltage difference between VIN and VS,

Peak voltage of SW terminal negative potential: -3.0V / hour: shall not exceed 100 nsec.



● 6-5 Reverse Bias Protection

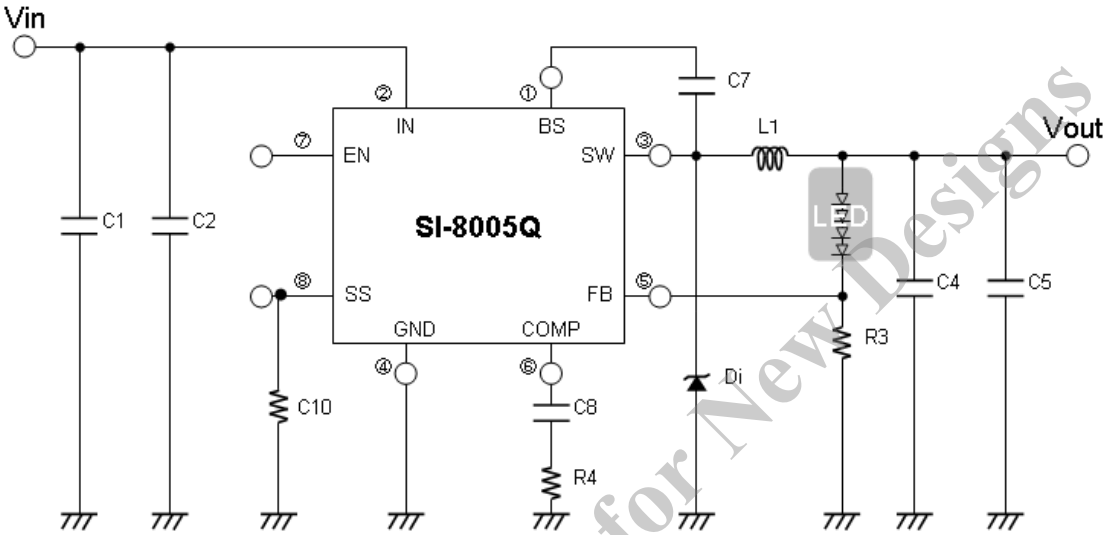
A diode for reverse bias protection will be required between input and output when the output voltage is higher than the input terminal voltage, such as in battery chargers.



● 6-6 LED Series Connection

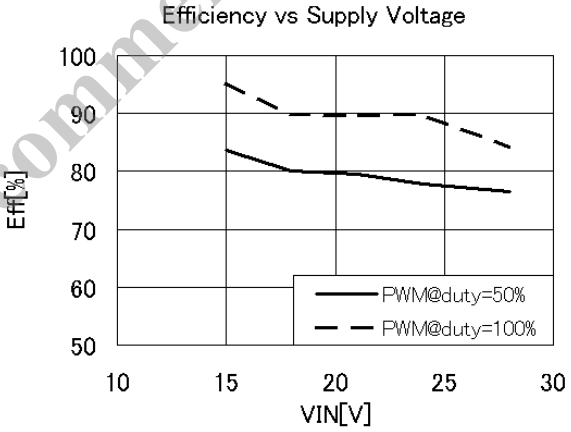
The LED is efficiently operated by its constant current driving system without unevenness of luminance. The current consumption can be reduced due to the EN function at shut down and the light dimming of constant LED current can be made by inputting PWM signal.

- Application circuit diagram



Circled numbers mean Pin no. on IC.

- Characteristics of efficiency



- Bill of materials

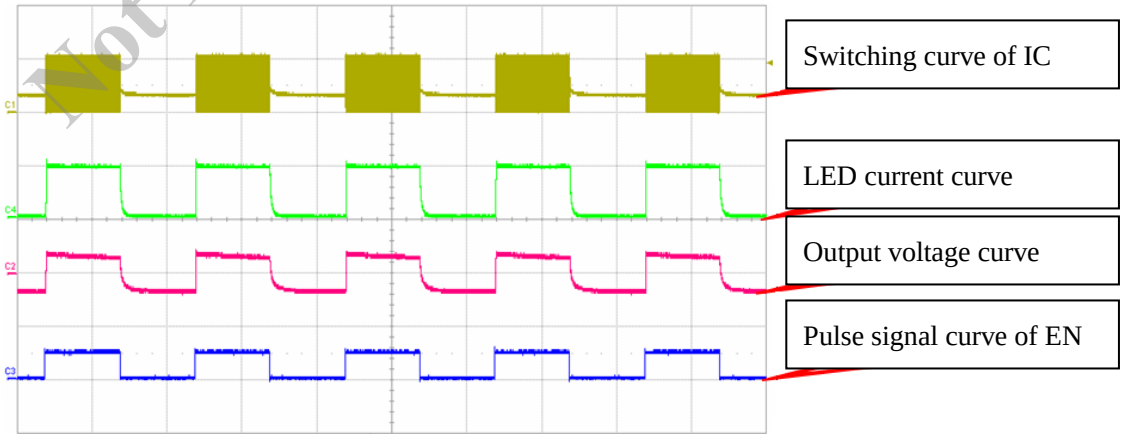
	symbol	Spec.	Description
Capacitor	C1	10μF (BV 50V)	Input capacitor
	C2	10μF (BV 50V)	Input capacitor
	C4	22μF (BV 16V)	Output capacitor
	C5	22μF (BV 16V)	Output capacitor
	C7	10nF (BV 50V)	Booster capacitor
	C8	560pF (BV 50V)	For Phase compensation (3LEDs)
Resistor	R3	0.5Ω (1W)	For Current detection
	R4	46.4kΩ (0.5W)	For Phase compensation (3LEDs)
	C10	1.5MΩ (0.5W)	For Soft start (changed to resistor for quick response)
Diode	Di	60V/5A	Flywheel diode
Coil	L1	10uH	Choke coil

- Constant for phase compensation

LEDs	Cout[uF] (ceramic capacitor)	R4 [kΩ]	C8 [pF]
3	22 × 2	46.4	560
4	22 × 2	69.8	470
6	22 × 2	100	360

- PWM dimming

PWM light dimming can be made by inputting signals into the EN terminal by an oscillator etc.



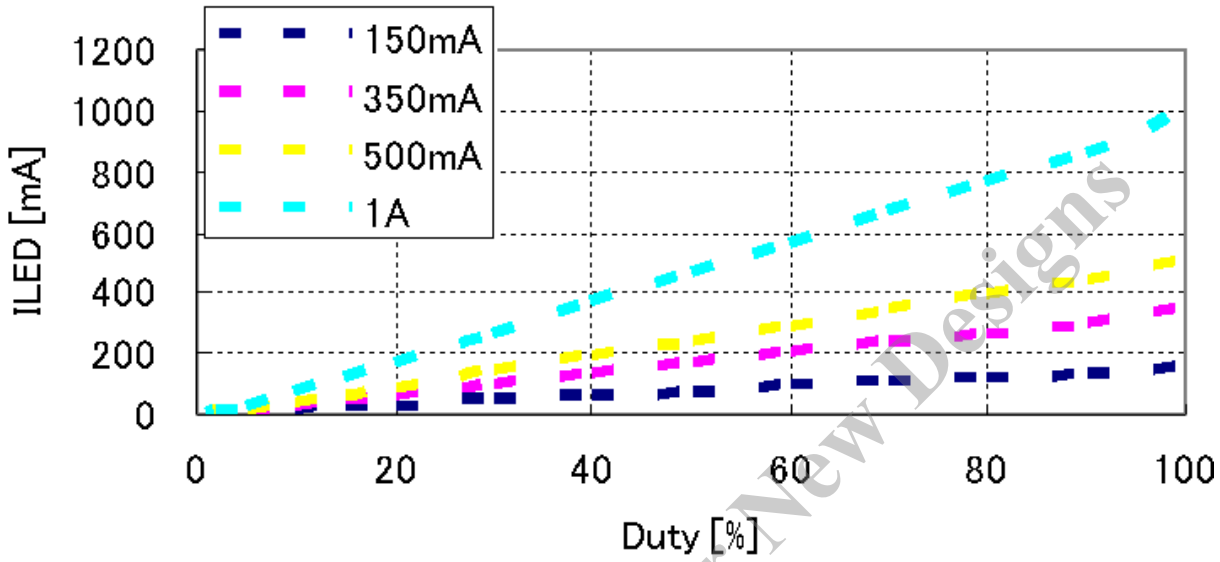
When pulse signals are inputted into the EN terminal, the application voltage of pulse signals should be 3 -

5V and the frequency 100 - 300Hz.

- LED current

The LED current varies subject to duty ratio.

Condition: LED: 4 series (application of 100Hz, 5V from the EN terminal)



When pulse signals are inputted into the EN terminal, the applied voltage and frequency should be 3 - 5V and 100 - 300Hz respectively.

7. Terminology

- Jitter

It is a kind of abnormal switching operations and is a phenomenon that the switching pulse width varies in spite of the constant condition of input and output. The output ripple voltage peak width is increased when a jitter occurs.

- Recommended Conditions

It shows the operation conditions required for maintaining normal circuit functions. It is required to meet the conditions in actual operations.

- Absolute Maximum Ratings

It shows the destruction limits. It is required to take care so that even one item does not exceed the specified value for a moment during instantaneous or normal operation.

- Electrical Characteristics

It is the specified characteristic value in the operation under the conditions shown in each item. If the operating conditions are different, it may be out of the specifications.

- PWM (Pulse Width Modulation)

It is a kind of pulse modulation systems. The modulation is achieved by changing the pulse width in accordance with the variation of modulation signal waveform (the output voltage for chopper type switching regulator).

- ESR (Equivalent Series Resistance)

It is the equivalent series resistance of a capacitor. It acts in a similar manner to the resistor series-connected to the capacitor.

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