SLA6805MH

Description

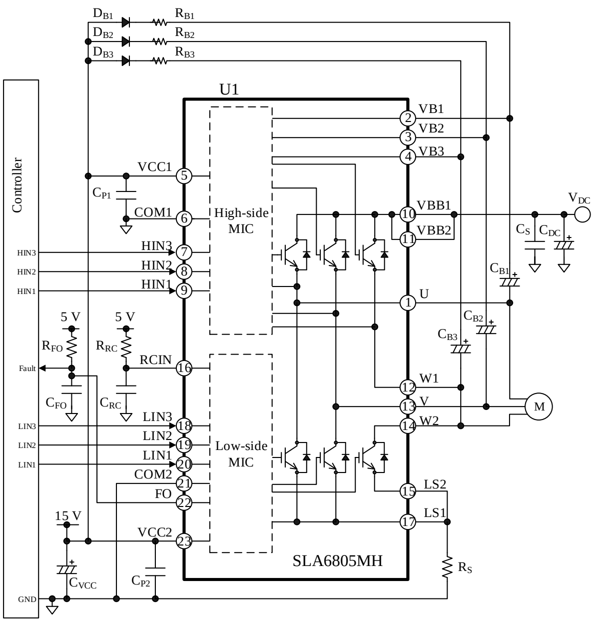
The SLA6805MH is a high voltage 3-phase motor driver in which transistors and pre-drive circuits are highly integrated.

Supplied in a ZIP23 package (heatsink type) with selectable leadforms, the SLA6805MH offers excellent mountability to a wide range of applications. The product can optimally control the inverter systems of low- to medium-capacity motors.

Features

- CMOS-compatible Input (3.3 V or 5 V)
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Fault Signal Output
- Shutdown Function
- Adjustable OCP Hold Time
- Protections Include:
  Undervoltage Lockout for Power Supply
    VBx Pin (UVLO_VB): Auto-restart
    VCC1 Pin (UVLO_VCC1): Auto-restart
    VCC2 Pin (UVLO_VCC2): Auto-restart
  Overcurrent Protection (OCP): Auto-restart

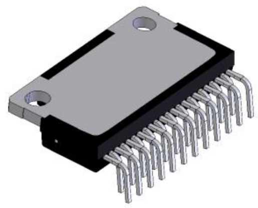
Typical Application



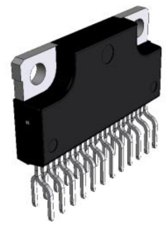
Package

ZIP23 (Heatsink Type)

Leadform 2153



Leadform 2151



Not to scale

Specifications

- Breakdown Voltage: 600 V
- Output Current: 3 A

Applications

For motor drives such as:

- Fan Motor and Pump Motor for Washer and Dryer
- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBBx–LSx	450	V	
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBBx–LSx	500	V	
IGBT Breakdown Voltage	V_{CES}	VBBx–LSx, V_{CC} = 15 V, I_C = 1 mA, V_{IN} = 0 V	600	V	
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	20	V	
	V_{BS}	VB1–U, VB2–V, VB3–W1	20		
Output Current (DC)[1]	I_O	T_C = 25 °C, T_J < 150 °C	3	A	
Output Current (Pulse)	I_{OP}	T_C = 25 °C, T_J < 150 °C, P_W ≤ 100 μs, duty cycle = 1%	6	A	
Input Voltage	V_{IN}	HINx–COM, LINx–COM	−0.5 to 7	V	
RCIN Pin Voltage	V_{RC}	RCIN–COM2	7	V	
Allowable Power Dissipation	P_D	T_C = 25 °C	32.8	W	
Operating Case Temperature[2]	$T_{C(OP)}$		−30 to 100	°C	
Junction Temperature[3]	T_J		150	°C	
Storage Temperature	T_{STG}		−40 to 150	°C	

(1) Should be derated depending on an actual case temperature. See Section 14.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the control MICs, IGBTs, and freewheeling diodes.

2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBBx–LSx	—	300	450	V	
Snubber Capacitor for Main Power Supply	C_S		0.01	—	0.1	μF	
Logic Supply Voltage	V_{CC}	VCCx–COM	13.5	15.0	16.5	V	
	V_{BS}	VB1–U, VB2–V, VB3–W1	13.5	—	16.5	V	
Input Voltage (HINx, LINx, FO)	V_{IN}		0	—	5.5	V	
RCIN Pin Capacitor	C_{RC}		1000	—	4700	pF	
RCIN Pin Pull-up Resistor	R_{RC}		33	—	680	kΩ	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$	$T_J = -25$ to 150 °C	0.5	—	—	μs	
	$t_{IN(MIN)OFF}$	$T_J = -25$ to 150 °C	0.5	—	—	μs	
Dead Time of Input Signal	t_{DEAD}		1.5	—	—	μs	
Bootstrap Capacitor	C_B		1	—	220	μF	
Bootstrap Resistor	R_B		22		220	Ω	
Shunt Resistor	R_S	$I_P \leq 6$ A	92	—	—	mΩ	
PWM Carrier Frequency	f_C		—	—	20	kHz	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Low-side Logic Operation Start Voltage	$V_{CC(ON)}$	VCCx–COM	10.5	11.5	12.5	V	
Low-side Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCCx–COM	10.0	11.0	12.0	V	
Low-side Logic Operation Voltage Hysteresis	$V_{CC(HYS)}$	VCCx–COM	—	0.5	—	V	
High-side Logic Operation Start Voltage	$V_{BS(ON)}$	VB1–U, VB2–V, VB3–W1	9.5	10.5	11.5	V	
High-side Logic Operation Stop Voltage	$V_{BS(OFF)}$	VB1–U, VB2–V, VB3–W1	9.0	10.0	11.0	V	
High-side Logic Operation Voltage Hysteresis	$V_{BS(HYS)}$	VB1–U, VB2–V, VB3–W1	—	0.5	—	V	
Logic Supply Current	I_{CC}	Total sink current of the VCC1 and VCC2 pins.	—	2.0	3.1	mA	
Logic Supply Current	I_{BS}	VBx = 15 V, HINx = 5 V; VBx pin current in 1-phase operation	—	150	—	μA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx, FO)	V_{IH}		—	2.0	2.5	V	Output transistors ON
Low Level Input Threshold Voltage (HINx, LINx, FO)	V_{IL}		1.0	1.5	—	V	Output transistors OFF
Input Threshold Voltage Hysteresis	V_{HYS}		—	0.5	—		
High Level Input Current	I_{IH}	V_{IN} = 5 V	—	50	100	μA	
Low Level Input Current	I_{IL}	V_{IN} = 0 V	—	—	2	μA	
Protection							
FO Pin Low Level Output Voltage	V_{FOL}		0.0	—	1.0	V	
FO Pin High Level Output Voltage	V_{FOH}		4.0	—	5.5	V	
OCP Threshold Voltage	V_{TRIP}		0.45	0.50	0.55	V	
OCP Hold Time	t_{P1}	V_{RC} = 5 V, R_{RC} = 330 kΩ, C_{RC} = 2200 pF	—	440	—	μs	
OCP Hold Time	t_{P2}	V_{RC} = 3.3 V, R_{RC} = 330 kΩ, C_{RC} = 2200 pF	—	870	—	μs	
OCP Blanking Time	t_{BK}		—	2.0	—	μs	

3.2 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance[1]	$R_{(J-C)Q}$[2]	All IGBTs operating	—	—	3.8	°C/W	
	$R_{(J-C)F}$[3]	All freewheeling diodes operating	—	—	5.4	°C/W	
Junction-to-Ambient Thermal Resistance	$R_{(J-A)}$	All IGBTs and freewheeling diodes operating	—	—	27.7	°C/W	

[1] Refers to a case temperature at the measurement point described in Figure 3-1, below.
[2] Refers to steady-state thermal resistance between the junction of the built-in IGBTs and the case. For transient thermal characteristics, see Section 14.1.
[3] Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

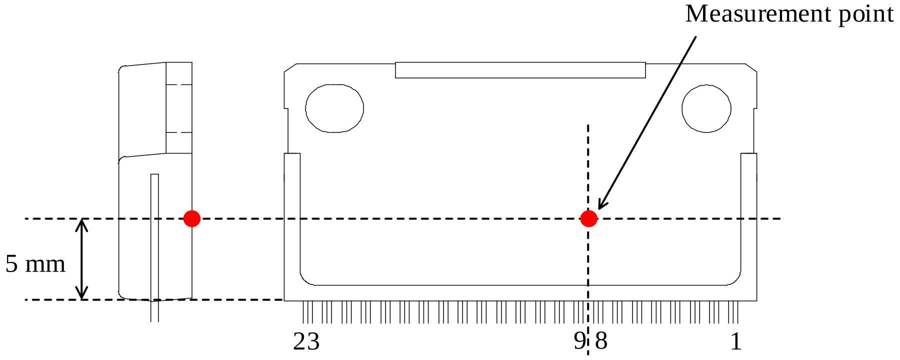


Figure 3-1. Case Temperature Measurement Point

3.3 Transistor Characteristics

Figure 3-2 provides the definitions of switching characteristics described in this and the following sections.

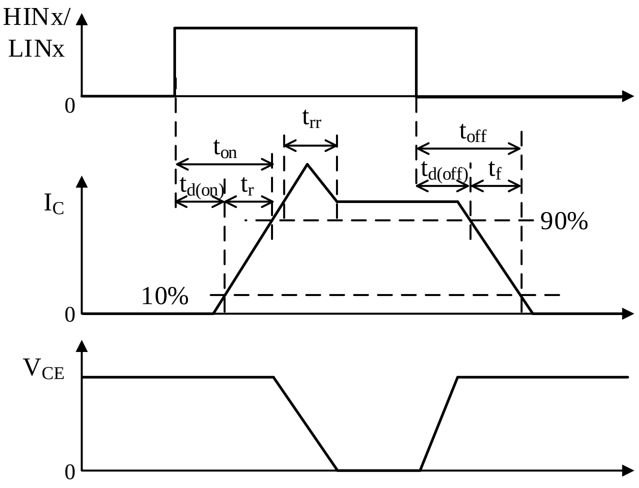


Figure 3-2. Switching Characteristics Definitions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{DS} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 3 A, V_{IN} = 5 V	—	1.7	2.1	V
Diode Forward Voltage	V_F	I_F = 3 A, V_{IN} = 0 V	—	1.65	2.0	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 3 A, V_{IN} = 0 V to 5 V, T_J = 25 °C, inductive load	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	365	—	ns
Rise Time	t_r		—	55	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	365	—	ns
Fall Time	t_f		—	170	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 3 A, V_{IN} = 0 V to 5 V, T_J = 25 °C, inductive load	—	75	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	395	—	ns
Rise Time	t_r		—	60	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	395	—	ns
Fall Time	t_f		—	170	—	ns

4. Mechanical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	58.8	—	78.4	N·cm	

5. Truth Table

Table 5-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx signals in each phase are high at the same time, both the high- and low-side transistors become on (simultaneous on-state). Therefore, HINx and LINx signals, the input signals for the HINx and LINx pins, require dead time setting so that such a simultaneous on-state event can be avoided.

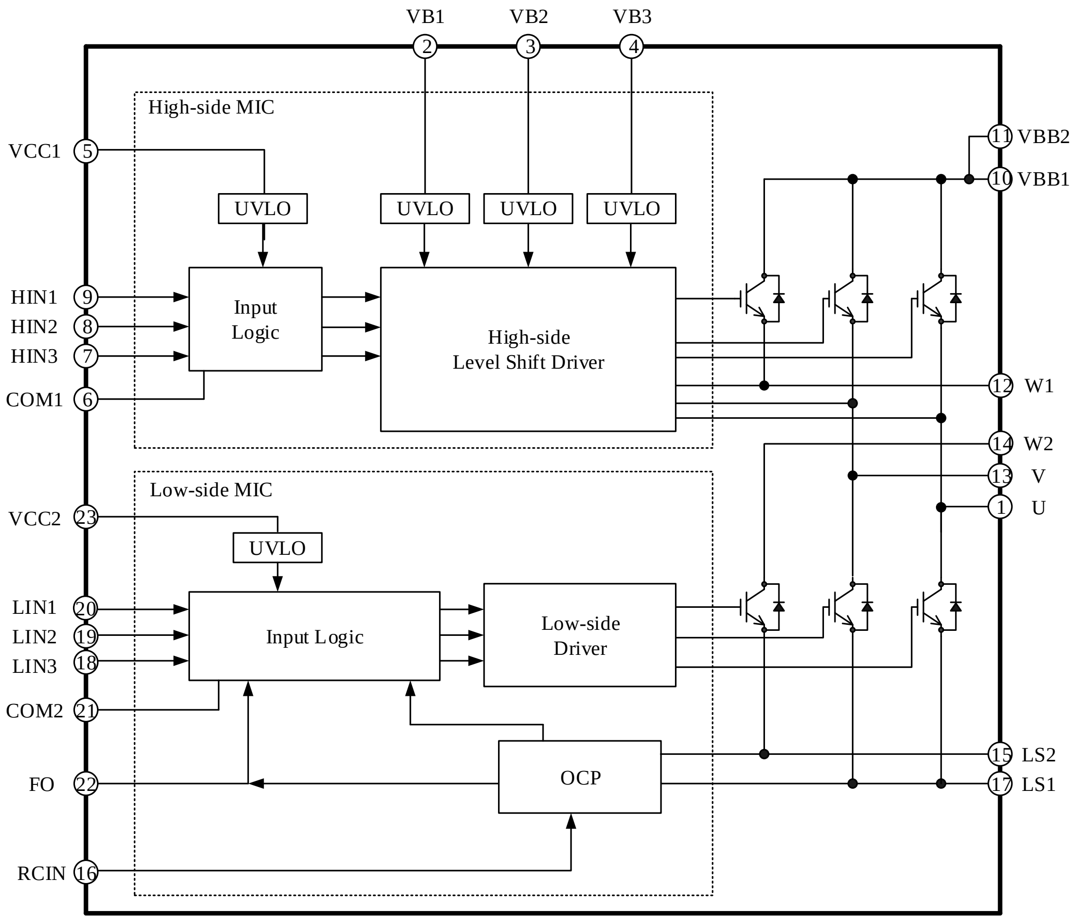
After the IC recovers from a UVLO_VCC2 condition, the low-side transistors resume switching in accordance with the input logic levels of the LINx signals (level-triggered), whereas the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

After the IC recovers from a UVLO_VB or UVLO_VCC1 condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

Table 5-1. Truth Table for Operation Modes

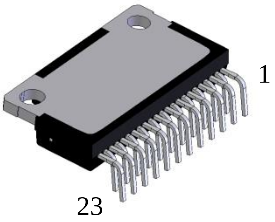
Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON
VBx Pin Undervoltage Lockout (UVLO_VB) VCC1 Pin Undervoltage Lockout (UVLO_VCC1)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
VCC2 Pin Undervoltage Lockout (UVLO_VCC2)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF

6. Block Diagram

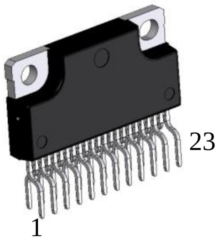


7. Pin Configuration Definitions

- **Leadform 2153**



- **Leadform 2151**



Pin Number	Pin Name	Description
1	U	U-phase output
2	VB1	U-phase high-side floating supply voltage input
3	VB2	V-phase high-side floating supply voltage input
4	VB3	W-phase high-side floating supply voltage input
5	VCC1	High-side logic supply voltage input
6	COM1	High-side logic ground
7	HIN3	Logic input for W-phase high-side gate driver
8	HIN2	Logic input for V-phase high-side gate driver
9	HIN1	Logic input for U-phase high-side gate driver
10	VBB1	Positive DC bus supply voltage (connected to VBB2 externally)
11	VBB2	Positive DC bus supply voltage (connected to VBB1 externally)
12	W1	W-phase output (connected to W2 externally)
13	V	V-phase output
14	W2	W-phase output (connected to W1 externally)
15	LS2	W-phase low-side IGBT emitter (connected to LS1 externally)
16	RCIN	OCP hold time setting
17	LS1	U- and W-phase low-side power IGBT emitter (connected to LS2 externally)
18	LIN3	Logic input for W-phase low-side gate driver
19	LIN2	Logic input for V-phase low-side gate driver
20	LIN1	Logic input for U-phase low-side gate driver
21	COM2	Low-side logic ground
22	FO	Fault signal output
23	VCC2	Low-side logic supply voltage input

8. Typical Application

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

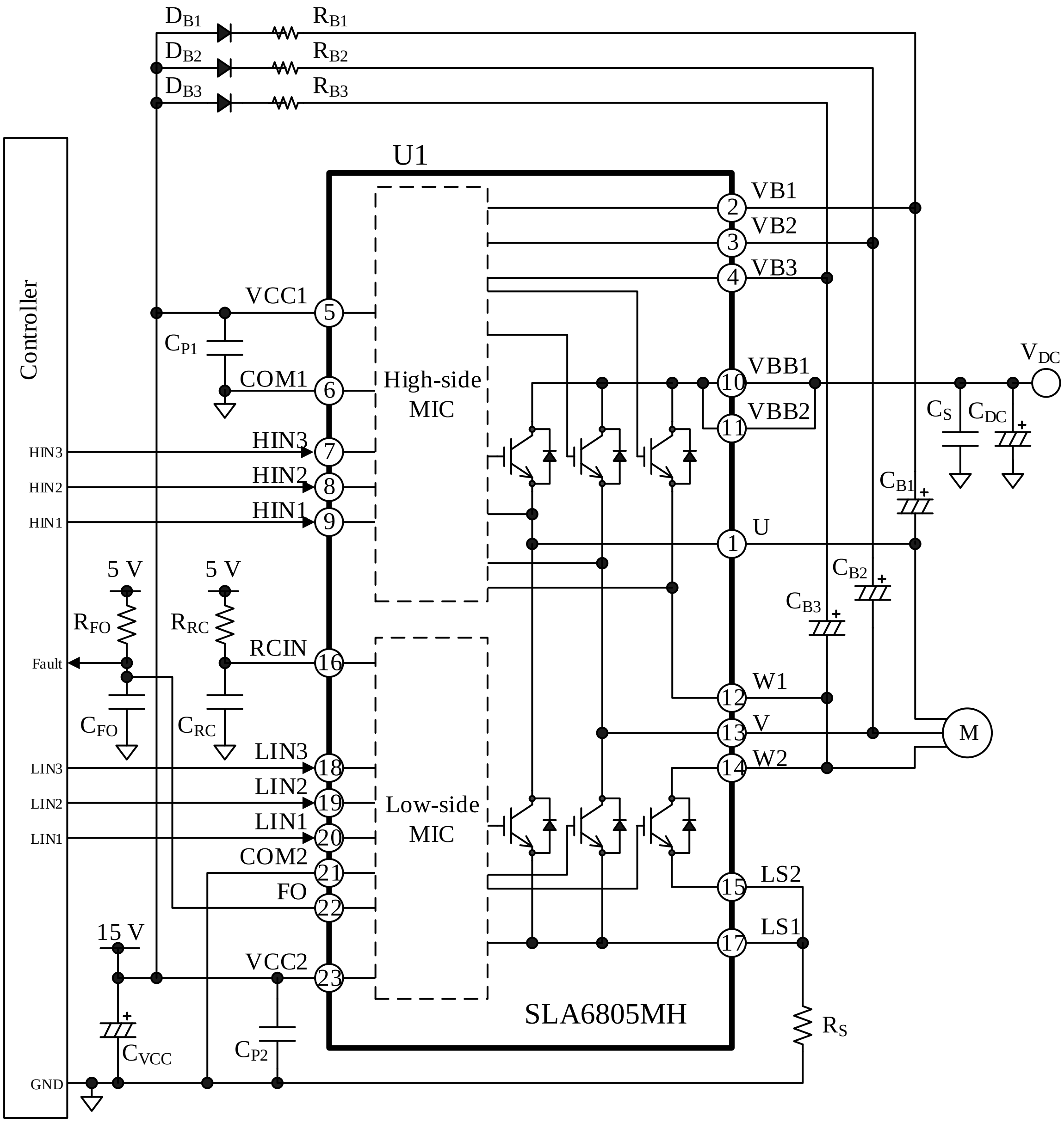
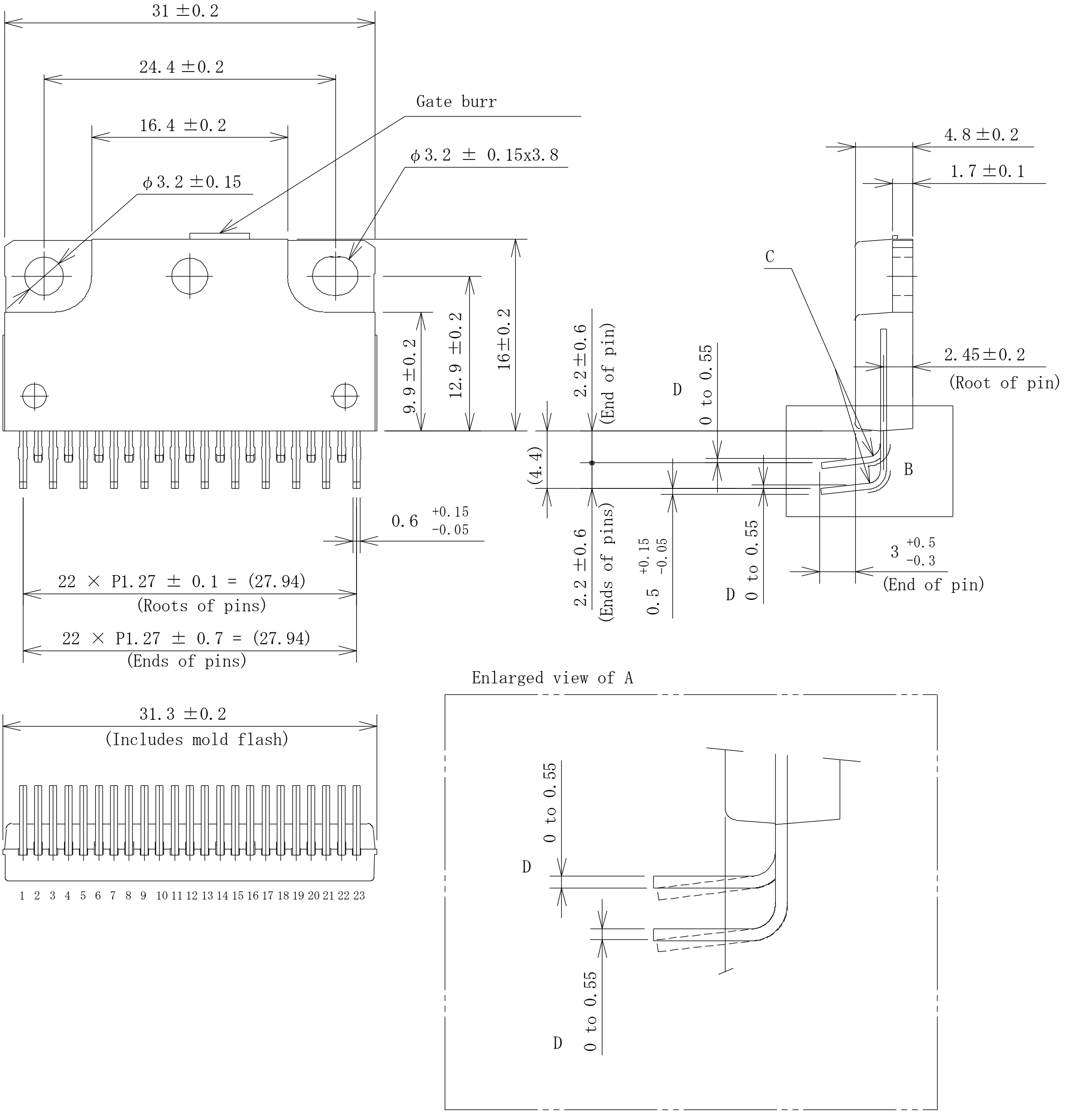


Figure 8-1. Typical Application

9. Physical Dimensions

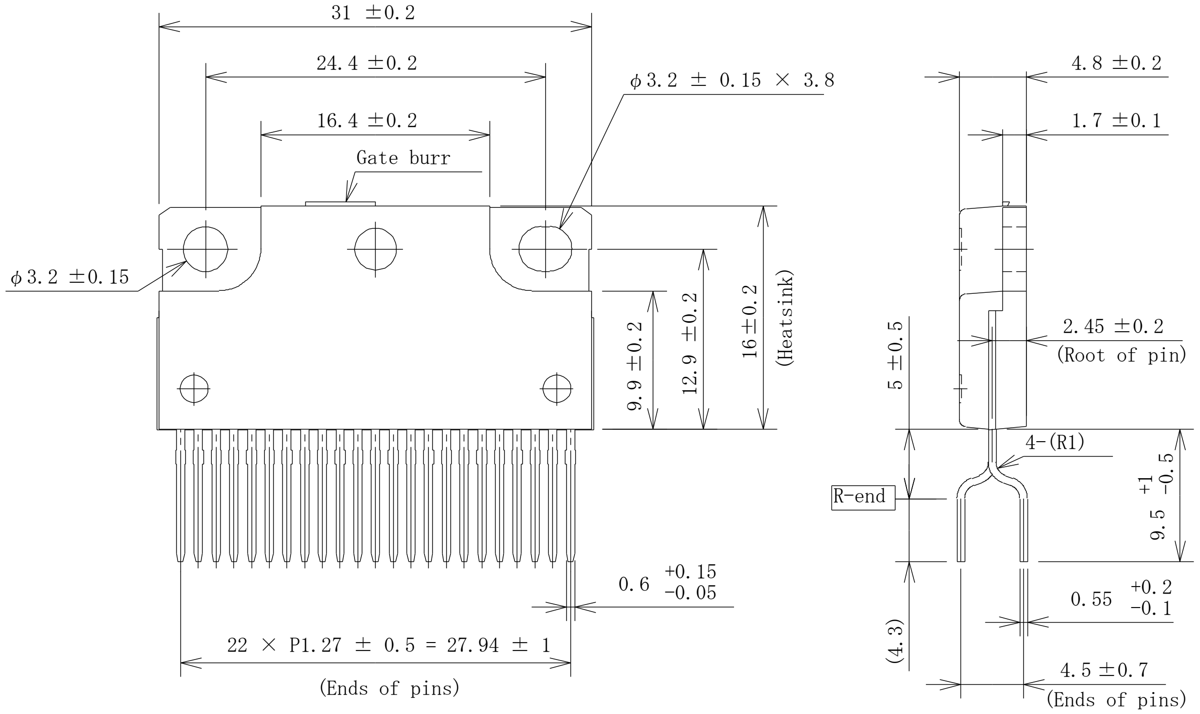
9.1 ZIP23: Heatsink Type (Leadform 2153)

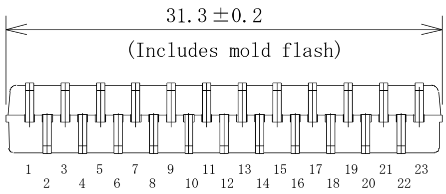


NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Maximum gate burr height is 0.3 mm.
- “B” depicts a pin whose plated surface may be cracked.
- “C” shows pins with a minimum inside radius (R) of 0.65 mm.
- “D” represents a pin illustrated for reference only, not the actual state of a bend.

9.2 ZIP23: Heatsink Type (Leadform 2151)

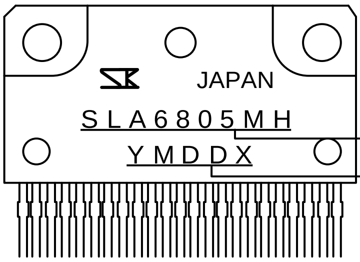




NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Maximum gate burr height is 0.3 mm.

10. Marking Diagram



Part Number

Lot Number:

Y is the last digit of the year of manufacture (0 to 9)

M is the month of the year (1 to 9, O, N, or D)

DD is the day of the month (01 to 31)

X is the control number

11. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. Thus, "the VCCx pin" is used when referring to either or both of the VCC1 and VCC2 pins.
- The COM1 pin is always connected to the COM2 pin.

11.1 Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBBx, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 12.5$ V).

It is required to fully charge bootstrap capacitors, C_{Bx}, at startup (see Section 11.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

11.2 Pin Descriptions

11.2.1 U, V, W1, and W2

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The W1 and W2 pins must be connected to each other on a PCB. The U, V, and W1 pins are the grounds for the VB1, VB2, and VB3 pins. The U, V, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{Bx}. Since high voltages are applied to these output pins (U, V, W1, and W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

11.2.2 VBB1 and VBB2

These are the input pins for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin. The VBB1 and VBB2 pins must be connected to each other on a PCB. Voltages between the VBBx and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBBx pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBBx pin.

11.2.3 LS1 and LS2

The LS1 pin is connected to the low-side IGBT emitters of the U- and V-phases; the LS2 pin is connected to the low-side IGBT emitter of the W phase. The LS1 and LS2 pins must be connected to each other on a PCB. For current detection, these pins should be connected to an external shunt resistor, R_S. When connecting the shunt resistor, place it as near as possible to the IC with a minimum length of traces to the LSx and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

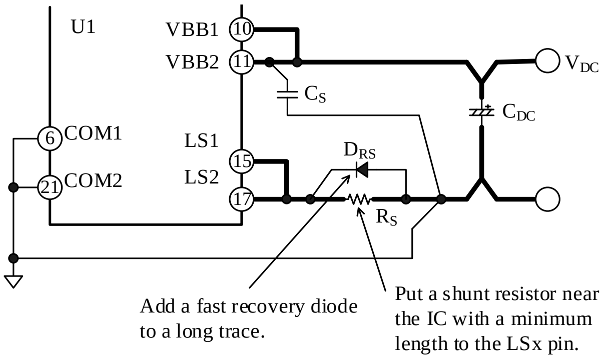


Figure 11-1. Connections to LSx Pin

11.2.4 VB1, VB2, and VB3

These are the inputs of the high-side floating power supplies for the individual phases.

Figure 11-2 illustrates bootstrap circuits used as power sources of the high-side IGBT drive circuits. Each bootstrap circuit is placed between the VCC1 and VBx pins and is composed of the following parts: a diode, D_{Bx}, a resistor, R_{Bx}, and a capacitor, C_{PBx}. Note that each phase requires this bootstrap circuit to be implemented. For proper startup, turn on the low-side transistors first, then fully charge the bootstrap capacitors, C_{Bx}.

D_{Bx} and R_{Bx} should be regulated within the individual recommended operational ranges (see Section 2). For the capacitance of the bootstrap capacitors, C_{Bx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{Bx}.

$$C_{Bx}(\mu F) > 800 \times t_{L(OFF)} \tag{1}$$

$$1\ \mu F \le C_{Bx} \le 220\ \mu F \tag{2}$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{Bx}), measured in seconds.

Even while the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section11.5.1.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

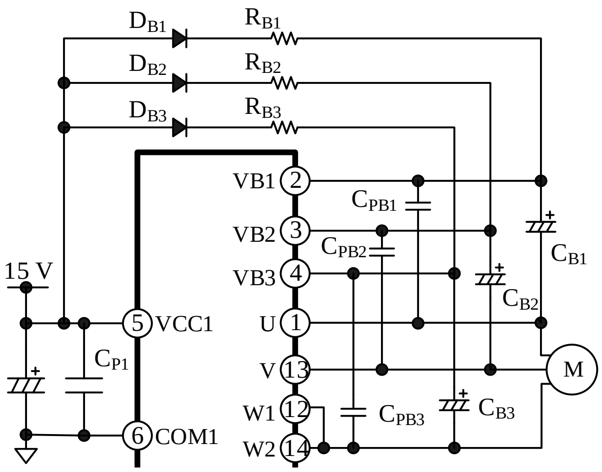


Figure 11-2. Bootstrap Circuit

Figure 11-3 shows an internal level-shifting circuit. A high-side output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a “Set” signal is generated. When the HINx input signal transits from high to low (falling edge), a “Reset” signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 11-4 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and output pins (U, V, or W1; hereafter “VBx–HSx”) occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of an HOx signal stays logic high (or “H”) because the SR flip-flop does not respond. With the HOx state being held high (i.e., the high-side transistor is in an on-state), the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition, which may result in critical damage to the IC. To protect the VBx pin against such a noise effect, add a bootstrap capacitor, C_{Bx}, in each phase. C_{Bx} must be placed near the IC, and be connected between the VBx and HSx pins with a minimal length of traces. To use an electrolytic capacitor, add a 0.01 µF to 0.1 µF bypass capacitor, C_{PBx}, in parallel near these pins used for the same phase.

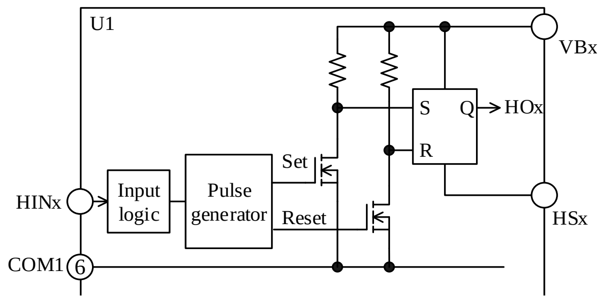


Figure 11-3. Internal Level-shifting Circuit

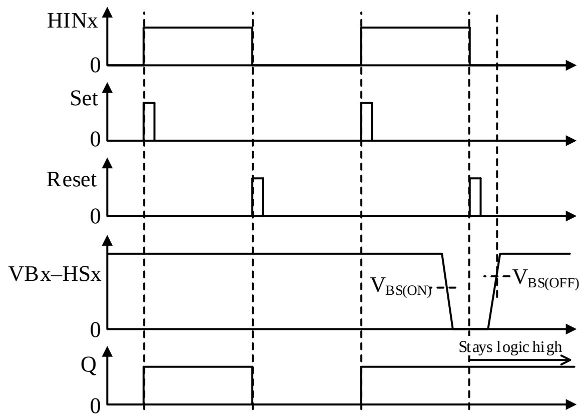


Figure 11-4. Waveforms at VBx–HSx Voltage Drop

11.2.5 VCC1 and VCC2

These are the logic supply pins for the built-in control MICs. The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{Px}, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins. Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

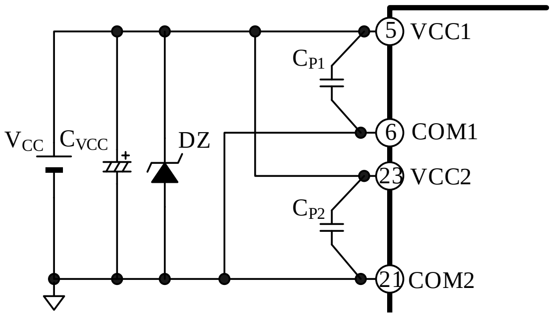


Figure 11-5. VCCx Pin Peripheral Circuit

11.2.6 COM1 and COM2

These are the logic ground pins for the built-in control MICs. The COM1 and COM2 pins should be connected externally on a PCB because they are not internally connected. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 11-6).

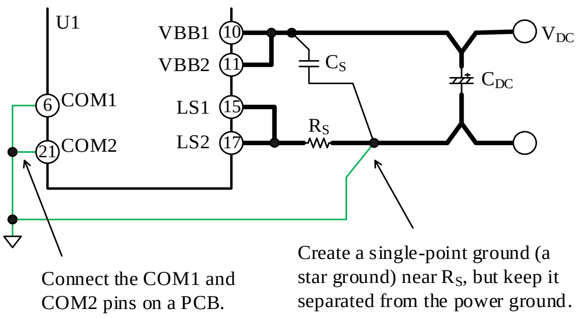


Figure 11-6. Connections to Logic Ground

11.2.7 HIN1, HIN2, and HIN3; LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller. Figure 11-7 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 20 kΩ pull-down resistor, and its input logic is active high.

Input signals applied across the HINx–COMx and the LINx–COMx pins in each phase should be set within the ranges provided in Table 11-1, below. <u>Note that dead time setting must be done for HINx and LINx signals</u> because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 1.

Table 11-1. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 μs	≥0.5 μs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥1.5 μs	

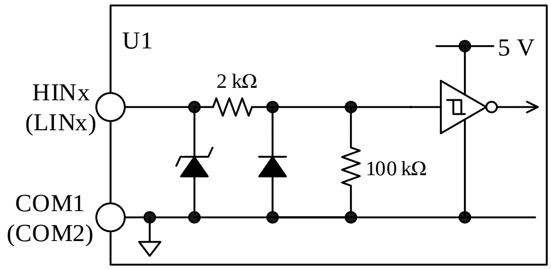


Figure 11-7. Internal Circuit Diagram of HINx or LINx Pin

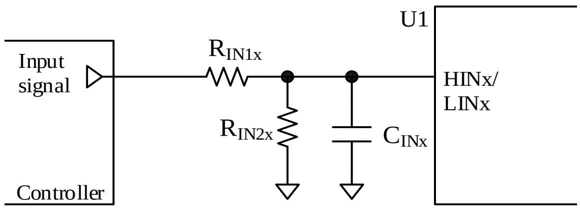


Figure 11-8. Filter Circuit for HINx or LINx Pin

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, the outputs from the microcontroller output line should not be high impedance. Also, if the traces from the microcontroller to the HINx or LINx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 11-8).

Here are filter circuit constants for reference:

- R_{IN1x}: 33 Ω to 100 Ω
- R_{IN2x}: 1 kΩ to 10 kΩ
- C_{INx}: 100 pF to 1000 pF

Care should be taken in adding R_{IN1x} and R_{IN2x} to the traces. When they are connected to each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

11.2.8 RCIN

Figure 11-9 illustrates an internal circuit diagram of the RCIN pin and its peripheral circuit.

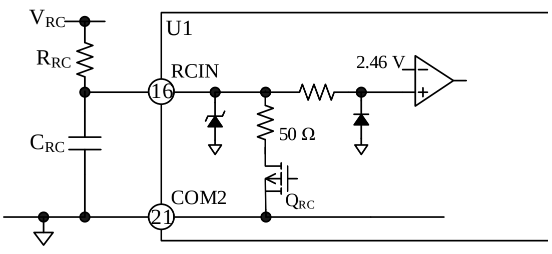


Figure 11-9. Internal Circuit Diagram of RCIN Pin and Its Peripheral Circuit

The RCIN pin should be connected to a pull-up resistor, R_{RC}, and a capacitor, C_{RC}, which determine a time from OCP activation until OCP release (i.e., the OCP Hold Time, t_P). Because of its open-drain nature, the RCIN pin should be tied by the pull-up resistor, R_{RC}, to the external power supply, which should range from 3.0 V to 5.5 V. R_{RC} should have a resistance of 33 kΩ to 680 kΩ; C_{RC} should have a capacitance of 1000 pF to 0.0047 μF. If R_{RC} is left open, the IC cannot release the OCP operation. Conversely, if R_{RC} is shorted, the IC cannot activate the OCP circuit. If C_{RC} is left open, t_P becomes shorter and the IC releases the OCP operation in a shorter time correspondingly. Therefore, care should be taken when you set these components.

Figure 11-10 is a timing chart showing the RCIN pin waveform during the OCP operation. The enabled OCP circuit turns off the low-side transistors and puts the FO pin into a high state. (Section 11.5.2 provides more details on the OCP.) At the same time, the internal power MOSFET of the RCIN pin, Q_{RC}, turns on, then the RCIN pin becomes logic low. Q_{RC} turns off about 5 μs after the QRC turn-on. Subsequently, the RCIN pin voltage increases with the time constant which is determined by R_{RC} and C_{RC}. When the RCIN pin voltage reaches 2.46 V, the IC releases the OCP operation.

The OCP Hold Time, t_P, depends on the external power supply voltage, V_{RC}. The approximate value of t_P is calculated by the following equations:

- **When External Power Supply Voltage, V_{RC} = 3.3 V:**

$$t_P = 1.35 \times R_{RC} \times C_{RC}\,. \tag{3}$$

- **When External Power Supply Voltage, V_{RC} = 5 V:**

$$t_{RC} = 0.65 \times R_{RC} \times C_{RC}\,. \tag{4}$$

Here is an example: when V_{RC} = 5 V, R_{RC} = 330 kΩ, and C_{RC} = 0.0047 μF, we find that t_{RC} = 1 ms.

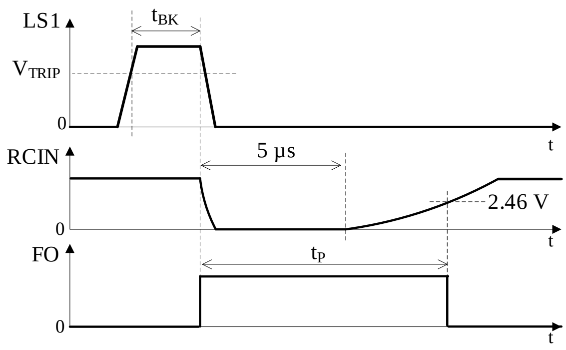


Figure 11-10. RCIN Pin Waveform during OCP Operation

11.2.9 FO

This pin operates as the fault signal output and the shutdown signal input. Section 11.3 provides detailed functional descriptions on the fault signal output; Section 11.4 describes the shutdown function.

Figure 11-11 illustrates an internal circuit diagram of the FO pin and its peripheral circuit. Because of its open-collector nature, the FO pin should be tied by a pull-up resistor, R_{FO}, to the external power supply, which should range from 3.0 V to 5.5 V. Therefore, it is recommended to use a 3.3 kΩ to 10 kΩ pull-up resistor. To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FO and COMx pins. C_{FO} should have a capacitance of 0.001 μF to 0.01 μF.

For avoiding repeated OCP activations, the microcontroller must shut off any input signals to the IC within on OCP hold time, t_P, after the FO pin becomes logic high. (For more details, see Section 11.5.2)

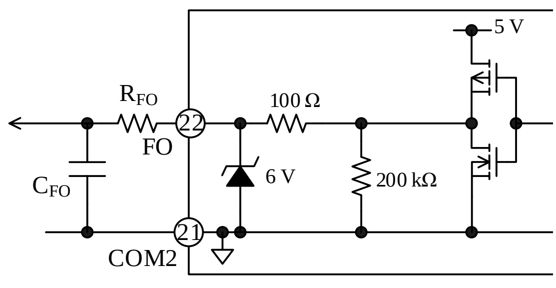


Figure 11-11. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

11.3 Fault Signal Output

The FO pin is logic low in normal operation and is logic high in fault signal output operation.

The FO pin becomes logic high while one or more of the following protections are operating: the VCC2 pin undervoltage lockout for power supply (UVLO_VCC2) and the overcurrent protection (OCP). While the FO pin is in the high state, all the low-side transistors turn off. The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HINx and LINx pins to logic low within the predetermined OCP hold time, t_P. t_P is determined by the value of the pull-up resistor and capacitor which are externally connected to the RCIN pin (see Section 11.5.2).

11.4 Shutdown Signal Input

The FO pin also acts as the input pin of shutdown signals. When the FO pin becomes logic high, all the low-side transistors turn off.

The voltages and pulse widths of the shutdown signals to be applied are listed in Table 11-2.

Table 11-2. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	—	≥6 µs

11.5 Protection Functions

This section describes the various protection circuits provided in the SLA6805MH. The protection circuits are as follows: the undervoltage lockout for power supplies (UVLO) of the VBx, VCC1, and VCC2 pins; the overcurrent protection (OCP).

In the following functional descriptions, "HOx" denotes a gate input signal on the high-side transistor, whereas "LOx" denotes a gate input signal on the low-side transistor. "VBx–HSx" refers to the voltages between the VBx pin and output pins (U, V, and W1).

11.5.1 Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case.

To prevent this event, the IC has the undervoltage lockout (UVLO) circuits for each of the VBx, VCC1, and VCC2 pins.

11.5.1.1. VBx Pin (UVLO_VB)

Figure 11-12 shows operational waveforms of the VBx pin undervoltage lockout for power supply (i.e., UVLO_VB).

When the voltage between the VBx and output pins (VBx–HSx) decreases to the High-side Logic Operation Stop Voltage ($V_{BS(OFF)}$ = 10.0 V) or less, the UVLO_VB circuit in the corresponding phase gets activated and sets an HOx signal to logic low. When the voltage between the VBx and HSx pins increases to the High-side Logic Operation Start Voltage ($V_{BS(ON)}$ = 10.5 V) or more, the IC releases the UVLO_VB operation. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VB release. Any fault signals are not output from the FO pin during the UVLO_VB operation. The VBx pin has an internal filter circuit to prevent noise-induced malfunctions.

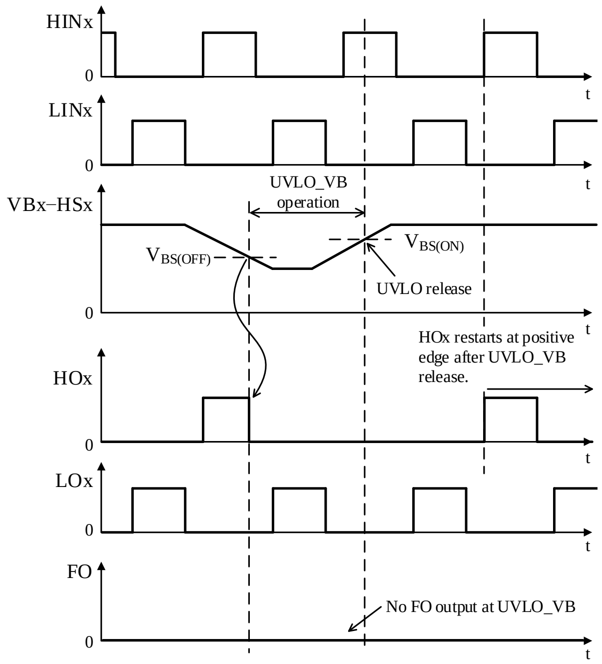


Figure 11-12. UVLO_VB Operational Waveforms

11.5.1.2. VCC1 Pin (UVLO_VCC1)

Figure 11-13 shows operational waveforms of the VCC1 pin undervoltage lockout for power supply (i.e., UVLO_VCC1).

When the VCC1 pin voltage decreases to the Low-side Logic Operation Stop Voltage ($V_{CC(OFF)}$ = 11.0 V) or less, the UVLO_VCC1 circuit gets activated and sets an HOx signal to logic low. When the VCC1 pin voltage increases to the Low-side Logic Operation Start Voltage ($V_{CC(ON)}$ = 11.5 V) or more, the IC releases the UVLO_VCC1 operation. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VCC1 release. The VCC1 pin has an internal filter circuit to prevent noise-induced malfunctions.

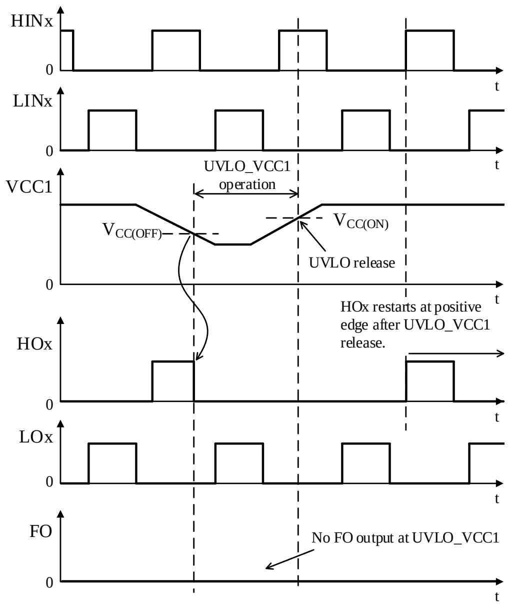


Figure 11-13. UVLO_VCC1 Operational Waveforms

11.5.1.3. VCC2 Pin (UVLO_VCC2)

Figure 11-14 shows operational waveforms of the VCC2 pin undervoltage lockout for power supply (i.e., UVLO_VCC2).

When the VCC2 pin voltage decreases to the Low-side Logic Operation Stop Voltage ($V_{CC(OFF)}$ = 11.0 V) or less, the UVLO_VCC2 circuit gets activated and sets an LOx signal to logic low. When the VCC2 pin voltage increases to the Low-side Logic Operation Start Voltage ($V_{CC(ON)}$ = 11.5 V) or more, the IC releases the UVLO_VCC2 operation. The IC then resumes transmitting an LOx signal according to an input command on the LINx pin. During the UVLO_VCC2 operation, the FO pin becomes logic high and sends fault signals.

The VCC2 pin has an internal filter circuit to prevent noise-induced malfunctions.

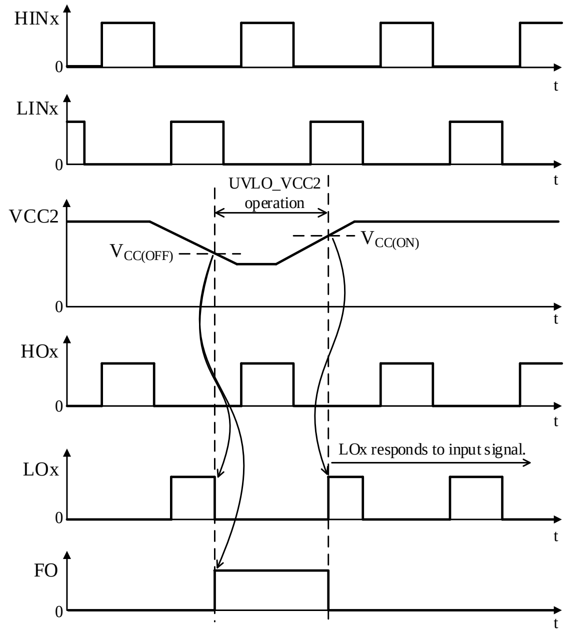


Figure 11-14. UVLO_VCC2 Operational Waveforms

11.5.2 Overcurrent Protection (OCP)

The overcurrent protection (OCP) is a protection against large inrush currents (i.e., high di/dt).

Figure 11-15 is an internal circuit diagram describing the LS1 pin and its peripheral circuit. The LS1 pin should be connected to an external shunt resistor, R_S, on a PCB. The LS1 pin voltage increases proportionally to a rise in the current flowing through the external shunt resistor, R_S. The built-in dedicated circuit monitors changes in the LS1 pin voltage to detect overcurrents.

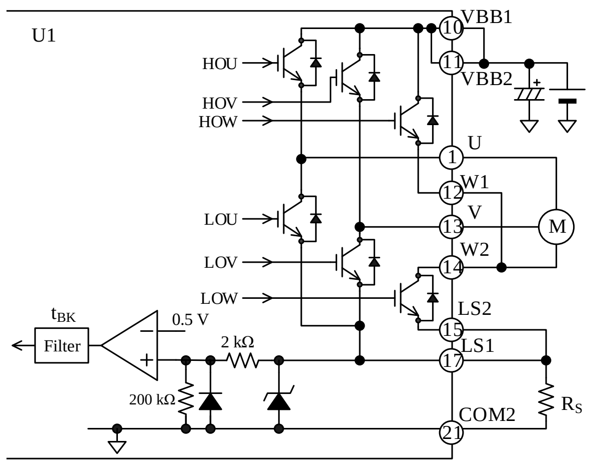


Figure 11-15. Internal Circuit Diagram of LS1 Pin and Its Peripheral Circuit

Figure 11-16 is a timing chart that represents operational waveforms during OCP operation. When the LS1 pin voltage increases to the OCP Threshold Voltage (V_{TRIP} = 0.50 V) or more, and remains in this condition for a period of the OCP Blanking Time (t_{BK} = 2.0 μs) or longer, the OCP circuit is activated. When the OCP is activated, the IC puts an LOx signal to a low sate and the FO pin to a high state.

The current flowing through R_S decreases while the LOx signal is in the low state. Even if the LS1 pin voltage falls below V_{TRIP}, the IC holds the FO pin in the high state for a fixed OCP hold time (t_P). Then, the output transistors operate according to input signals. t_P is determined by the RCIN pin. For details on the RCIN pin setting, see Section 11.2.8.

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, the external microcontroller, where a fault signal from the FO pin is input via its interrupt pin (INT), must be programmed to put the HINx and LINx pins to logic low within a predetermined OCP hold time, t_P.

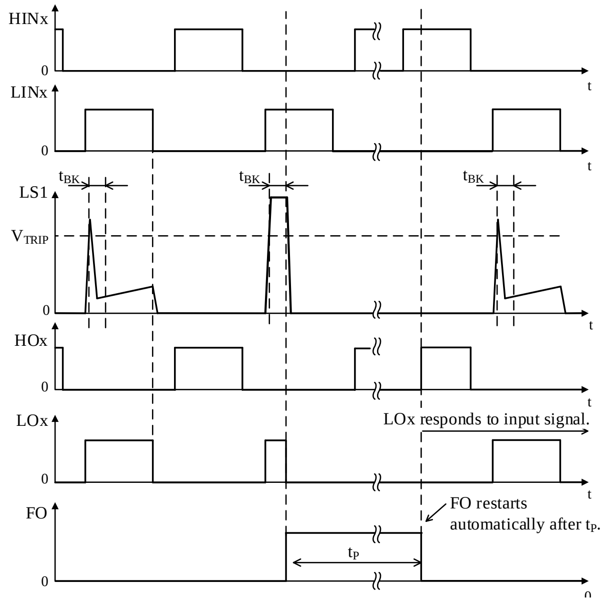


Figure 11-16. OCP Operational Waveforms

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

Note that overcurrents are undetectable when one or more of the U, V, and W1/W2 pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

12. Design Notes

12.1 PCB Pattern Layout

Figure 12-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

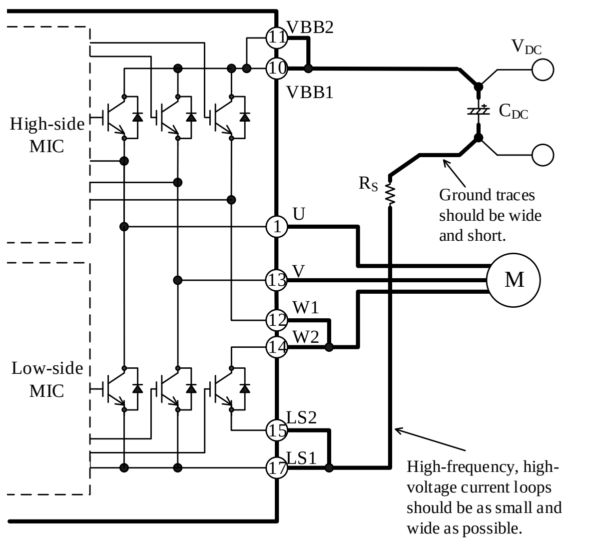


Figure 12-1. High-frequency, High-voltage Current Paths

12.2 Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- It is recommended to use a metric screw of M2.5. To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to about 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 4.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible.

12.3 Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that the gate and source of each transistor should have the same potential. Moreover, care should be taken during the measurement because each transistor is connected as follows:

- All the high-side drains are internally connected to the VBBx pin.
- In the U-phase, the high-side source and the low-side drain are internally connected to the U pin. (In the W-phase, the high- and low-side transistors are unconnected inside the IC.)

The gates of the high-side transistors are pulled down to the corresponding output (U, V, and W1) pins; similarly, the gates of the low-side transistors are pulled down to the COM2 pin.

When measuring the breakdown voltage or leakage current of the transistors, note that all of the output (U, V, and W1), LSx, and COMx pins must be appropriately connected. Otherwise, the output transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 12-2 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 12-3 shows the low-side transistor (Q_{1L}) in the U-phase. And all the pins that are not represented in these figures are open.

When measuring the high-side transistors, leave all the pins not be measured open. When measuring the low-side transistors, connect the LSx pin to be measured to the COM2 pin, then leave other unused pins open.

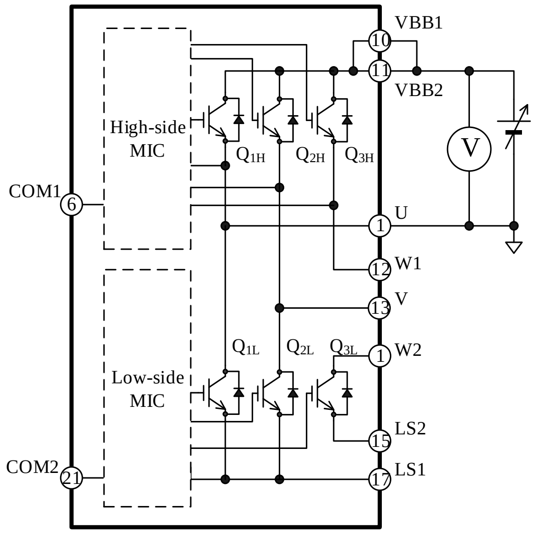


Figure 12-2. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

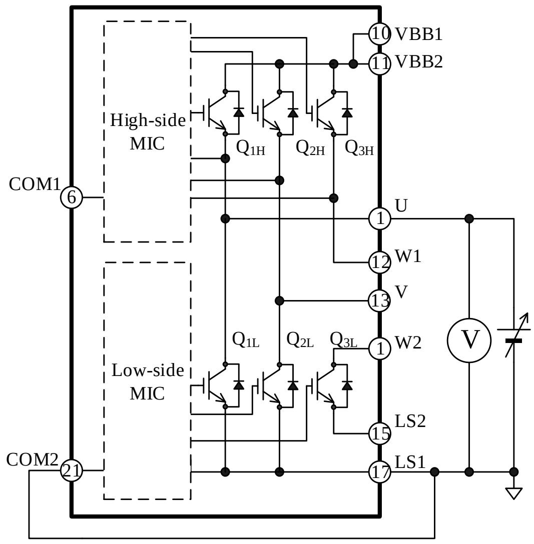


Figure 12-3. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

13. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in an output transistor, and to estimate a junction temperature (in all-element operation). Note that the descriptions listed here are applicable to the SLA6805MH, which is controlled by a 3-phase sine-wave PWM driving strategy.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0107: SLA6805MH Calculation Tool
  https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbtall_caltool2_en.html

Total power loss in an output transistor can be obtained by taking the sum of IGBT steady-state loss, P_{ON}, IGBT switching loss, P_{SW}, and freewheeling diode steady-state loss, P_F. The following subsections contain the mathematical procedures to calculate these losses (P_{ON}, P_{SW}, and P_F) and the junction temperature of all IGBTs and freewheeling diodes operating.

13.1 IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-1, linear approximations at a range the I_C is actually used are obtained by: $V_{CE(SAT)} = \alpha \times I_C + \beta$. The values gained by the above calculation are then applied as parameters in Equation (5), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} + \frac{4}{3\pi}M \times \cos\theta\right) I_M{}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} + \frac{\pi}{8}M \times \cos\theta\right) I_M\,. \qquad (5)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT (V),
I_C is the collector current of the IGBT (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
$\cos\theta$ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve, and
β is the intercept of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve.

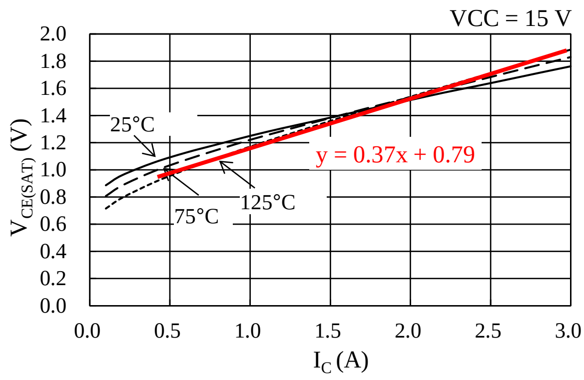


Figure 13-1. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C Curve

13.2 IGBT Switching Loss, P_{SW}

Switching loss in an IGBT, P_{SW}, can be calculated by Equation (6), letting IM be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}\,. \qquad (6)$$

Where:

f_C is the PWM carrier frequency (Hz),
V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and
α_E is the slope on the switching loss curve (see Section 14.3.2).

13.3 Estimating Junction Temperature of IGBT

The junction temperature of all IGBTs operating, T_J, can be estimated with Equation (7):

$$T_J = R_{(J-C)Q} \times \{(P_{ON} + P_{SW}) \times 6\} + T_C\,. \qquad (7)$$

Where:

$R_{(J-C)Q}$ is the junction-to-case thermal resistance (°C/W) of all the IGBTs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

13.3.1 Freewheeling Diode Steady-state Loss, P_F

Steady-state loss in a freewheeling diode can be computed by using the V_F vs. I_F curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-2, a linear approximation at a range the I_F is actually used is obtained by: $V_F = \alpha \times I_F + \beta$.

The values gained by the above calculation are then applied as parameters in Equation (8), below. Hence, the equation to obtain the freewheeling diode steady-state loss, P_F, is:

$$P_F = \frac{1}{2\pi}\int_0^{\pi} V_F(\varphi) \times I_F(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right){I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right)I_M \,. \quad (8)$$

Where:

V_F is the forward voltage of the freewheeling diode (V),
I_F is the forward current of the freewheeling diode (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the V_F vs. I_F curve, and
β is the intercept of the linear approximation in the V_F vs. I_F curve.

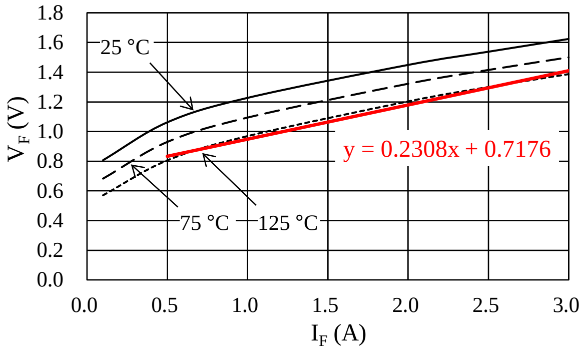


Figure 13-2. Linear Approximate Equation of V_F vs. I_F

13.3.2 Estimating Junction Temperature of Freewheeling Diode

The junction temperature of all freewheeling diodes operating, T_J, can be estimated with Equation (9):

$$T_J = R_{(J-C)F} \times (P_F \times 6) + T_C \,. \quad (9)$$

Where:

$R_{(J-C)F}$ is the junction-to-case thermal resistance (°C/W) of all the freewheeling diodes operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

14. Performance Curves

14.1 Transient Thermal Resistance Curve

The following graph represents transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

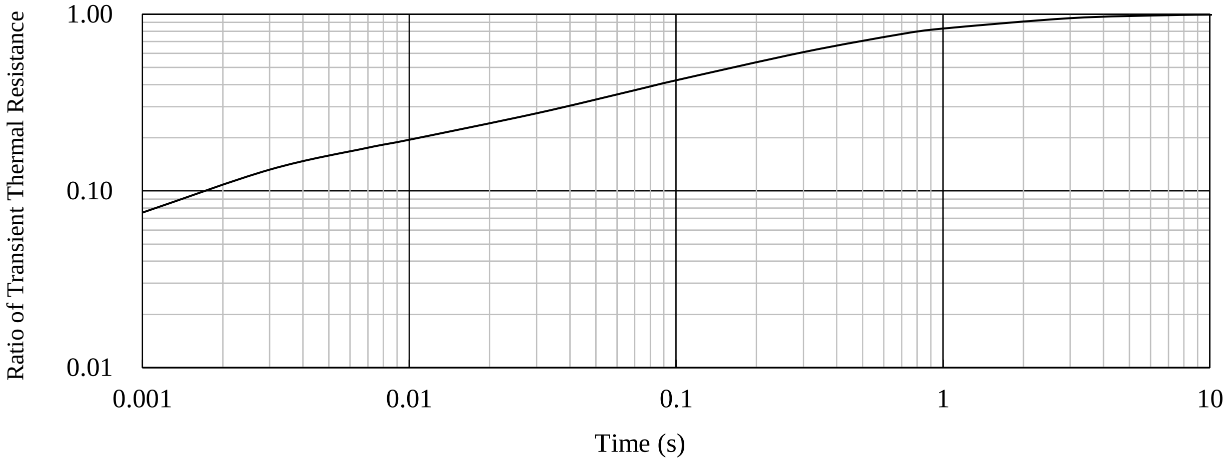


Figure 14-1. Transient Thermal Resistance: SLA6805MH

14.2 Performance Curves of Control Parts

Figure 14-2 to Figure 14-24 provide performance curves of the control parts integrated in the SLA6805MH, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 14-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 14-2	Logic Supply Current, I_{CC} vs. T_C (HINx = 0 V, LINx = 0 V)
Figure 14-3	Logic Supply Current, I_{CC} vs. VCCx Pin Voltage, V_{CC}
Figure 14-4	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C
Figure 14-5	Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C
Figure 14-6	VBx Pin Voltage, V_B vs. Logic Supply Current, I_{BS} (HINx = 0 V)
Figure 14-7	High-side Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 14-8	High-side Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 14-9	Low-side Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 14-10	Low-side Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 14-11	UVLO_VB Filtering Time vs. T_C
Figure 14-12	UVLO_VCC1 Filtering Time vs. T_C
Figure 14-13	UVLO_VCC2 Filtering Time vs. T_C
Figure 14-14	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 14-15	Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C
Figure 14-16	HINx Pin Input Current, $I_{IN(H)}$ vs. T_C
Figure 14-17	LINx Pin Input Current, $I_{IN(L)}$ vs. T_C
Figure 14-18	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 14-19	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 14-20	FO Pin Low Level Output Voltage, V_{FOL} vs. T_C
Figure 14-21	FO Pin High Level Output Voltage, V_{FOH} vs. T_C
Figure 14-22	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 14-23	OCP Hold Time, t_P vs. T_C
Figure 14-24	OCP Blanking Time, t_{BK} + Propagation Delay, t_D vs. T_C

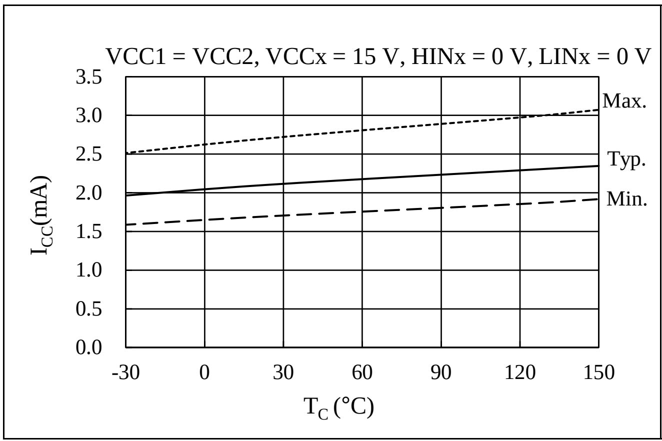


Figure 14-2. Logic Supply Current, I_{CC} vs. T_C (HINx = 0 V, LINx = 0 V)

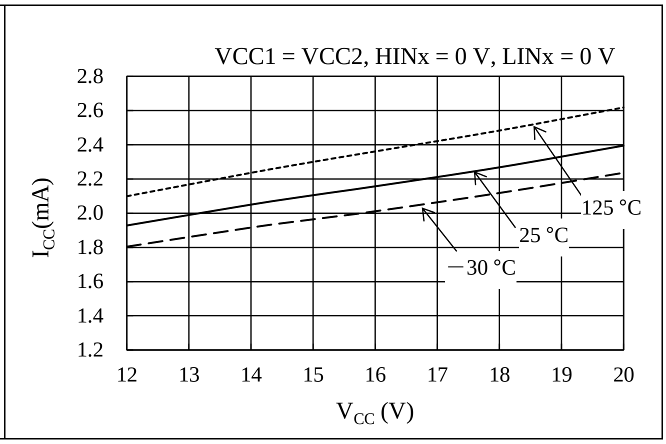


Figure 14-3. Logic Supply Current, I_{CC} vs. VCCx Pin Voltage, V_{CC}

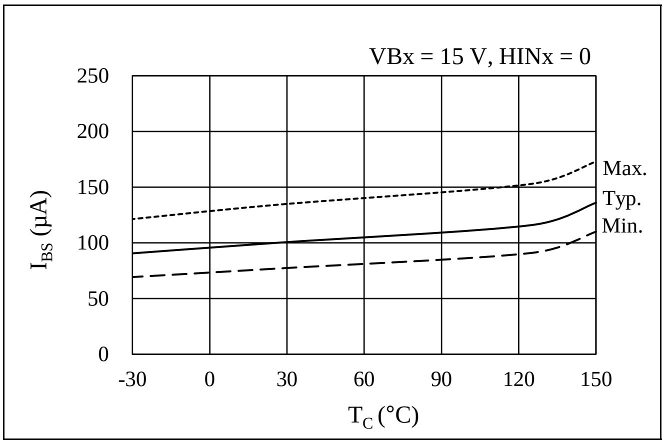


Figure 14-4. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C

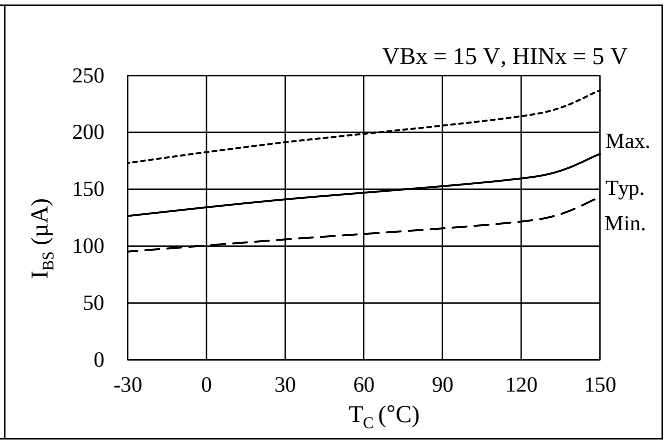


Figure 14-5. Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C

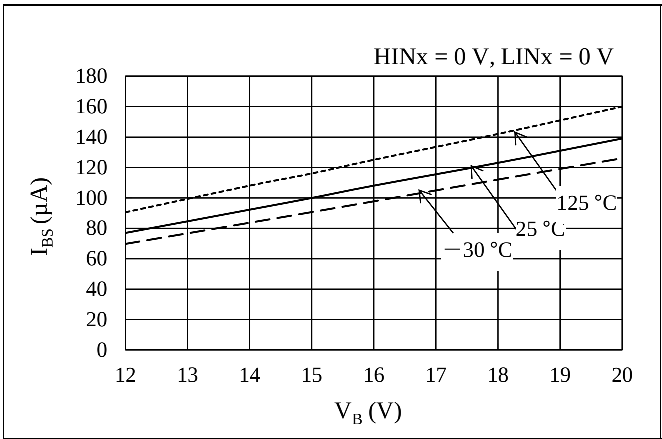


Figure 14-6. VBx Pin Voltage, V_B vs. Logic Supply Current, I_{BS} (HINx = 0 V)

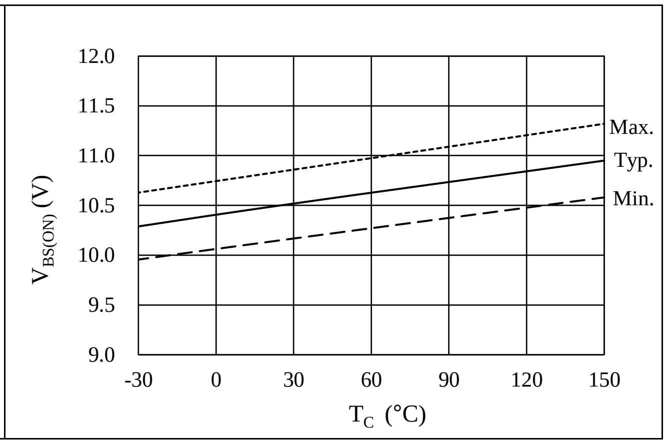


Figure 14-7. High-side Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

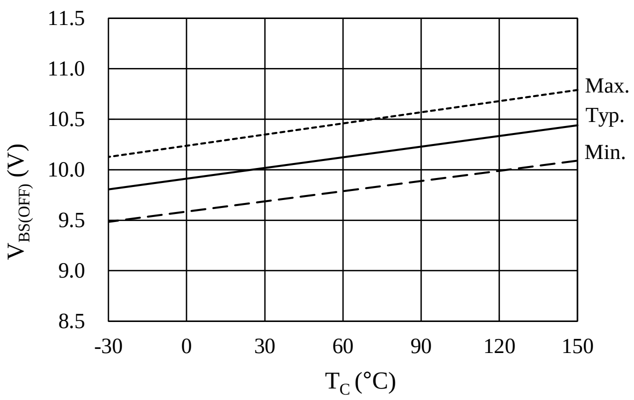


Figure 14-8. High-side Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

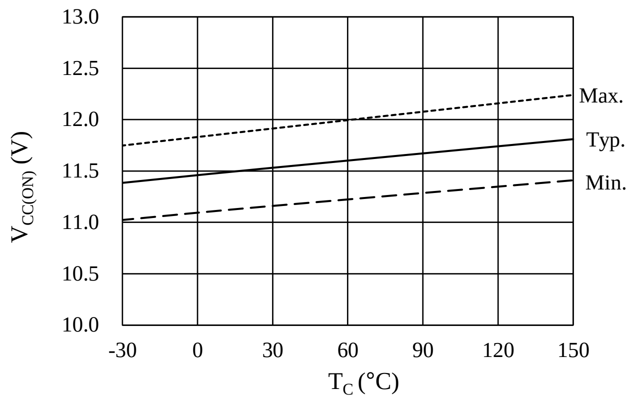


Figure 14-9. Low-side Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

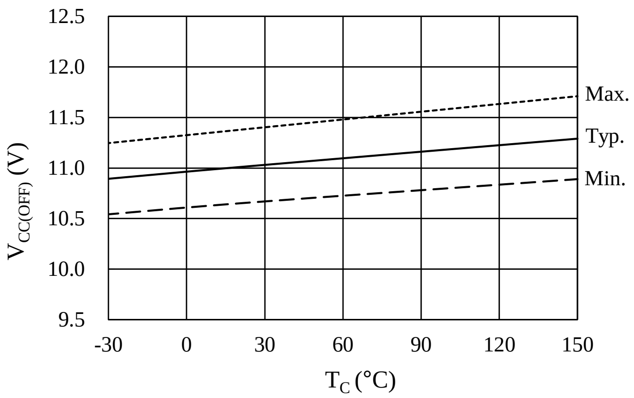


Figure 14-10. Low-side Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

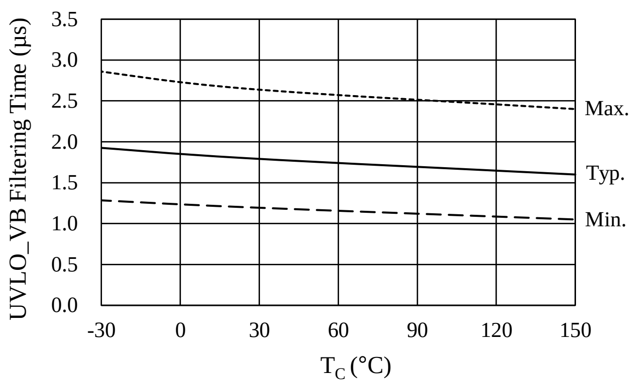


Figure 14-11. UVLO_VB Filtering Time vs. T_C

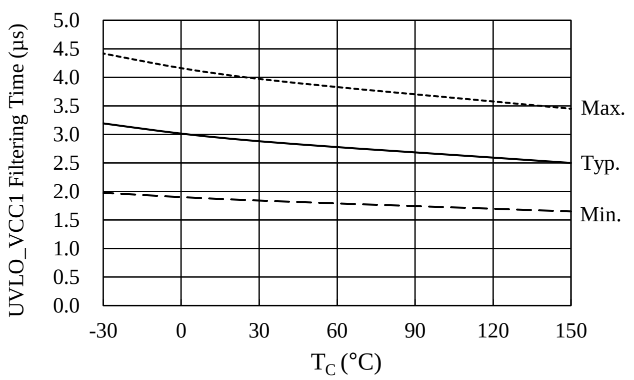


Figure 14-12. UVLO_VCC1 Filtering Time vs. T_C

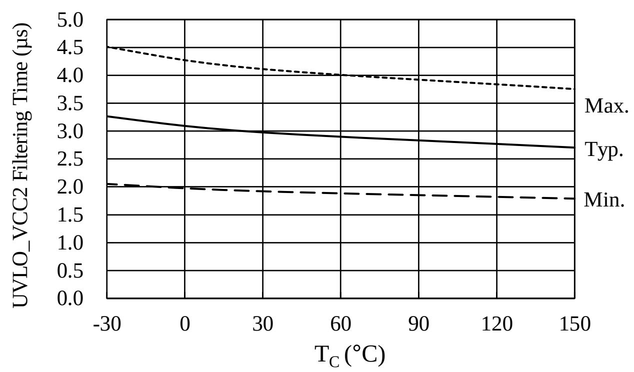


Figure 14-13. UVLO_VCC2 Filtering Time vs. T_C

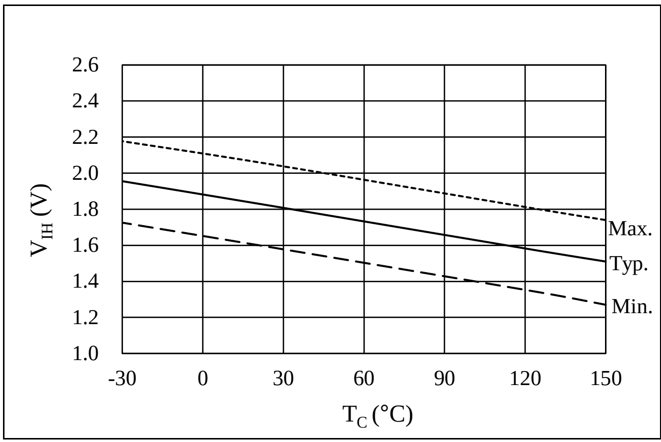


Figure 14-14. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

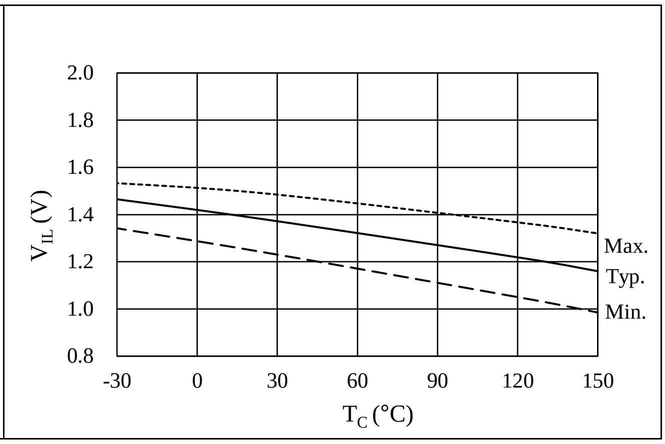


Figure 14-15. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

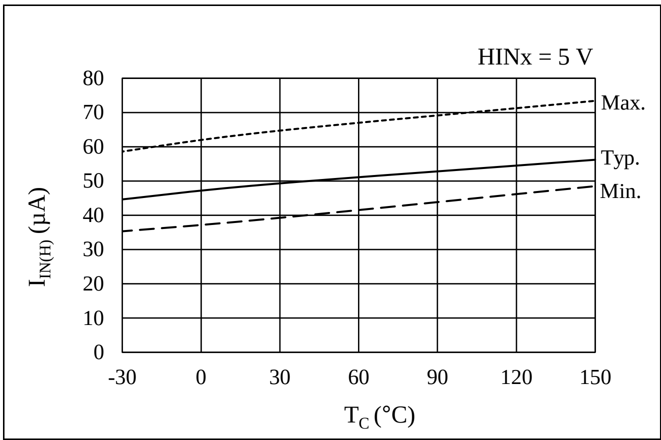


Figure 14-16. HINx Pin Input Current, $I_{IN(H)}$ vs. T_C

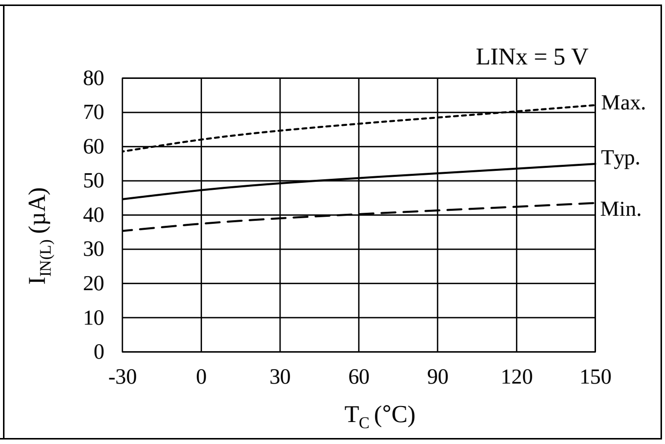


Figure 14-17. LINx Pin Input Current, $I_{IN(L)}$ vs. T_C

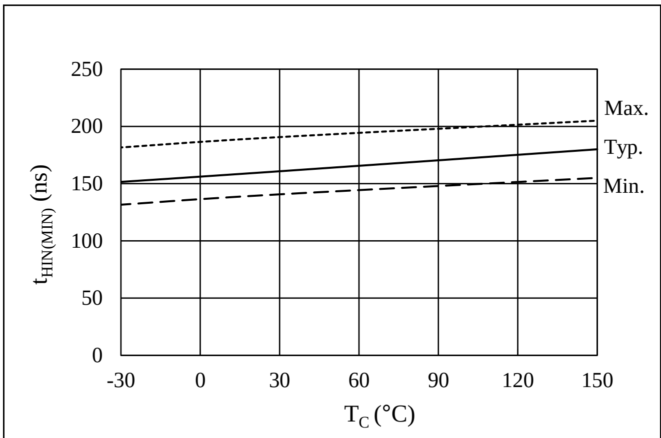


Figure 14-18. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

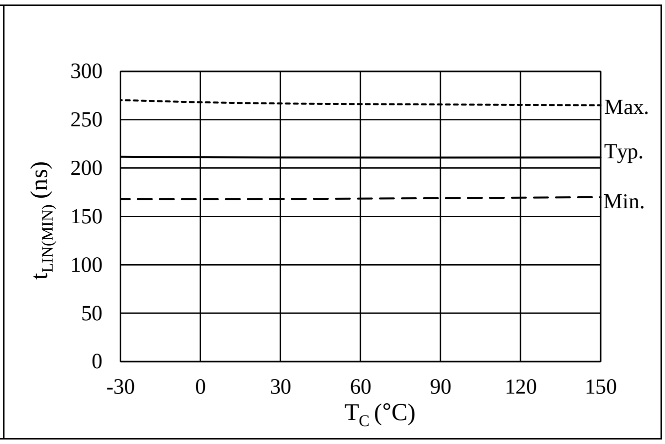


Figure 14-19. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

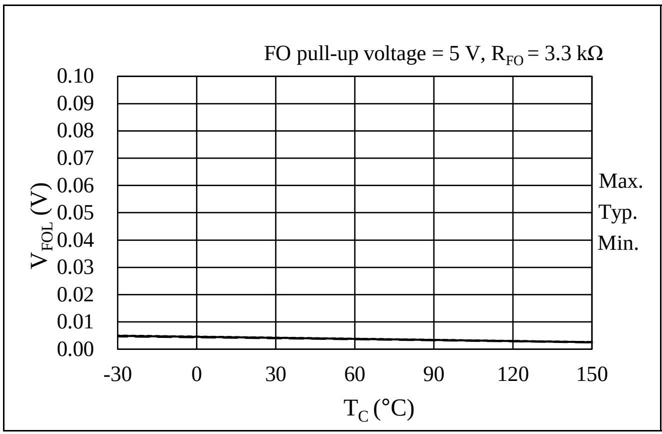


Figure 14-20. FO Pin Low Level Output Voltage, V_{FOL} vs. T_C

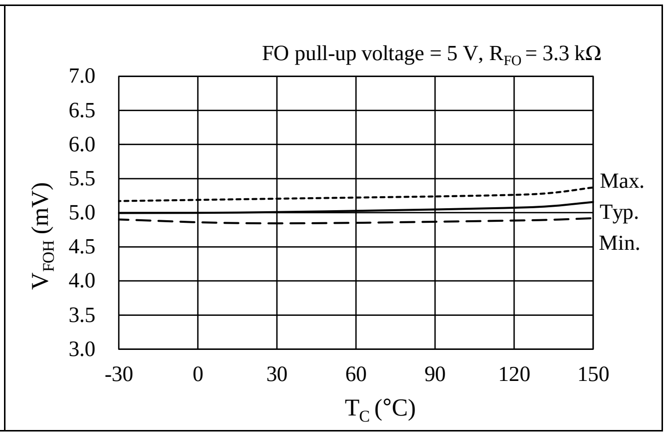


Figure 14-21. FO Pin High Level Output Voltage, V_{FOH} vs. T_C

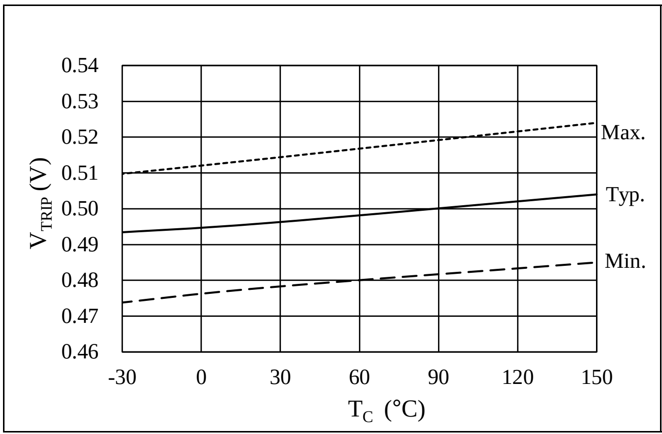


Figure 14-22. OCP Threshold Voltage, V_{TRIP} vs. T_C

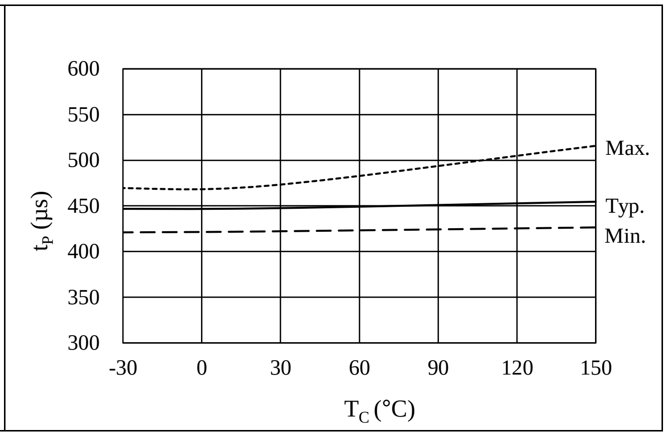


Figure 14-23. OCP Hold Time, t_P vs. T_C

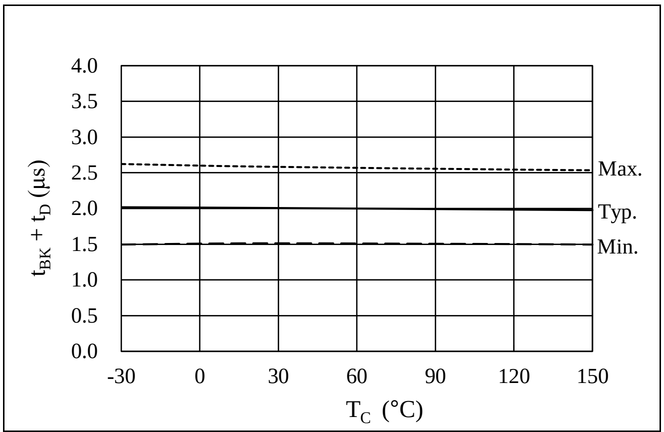


Figure 14-24. OCP Blanking Time, t_{BK} + Propagation Delay, t_D vs. T_C

14.3 Performance Curves of Output Parts

14.3.1 Output Transistor Performance Curves

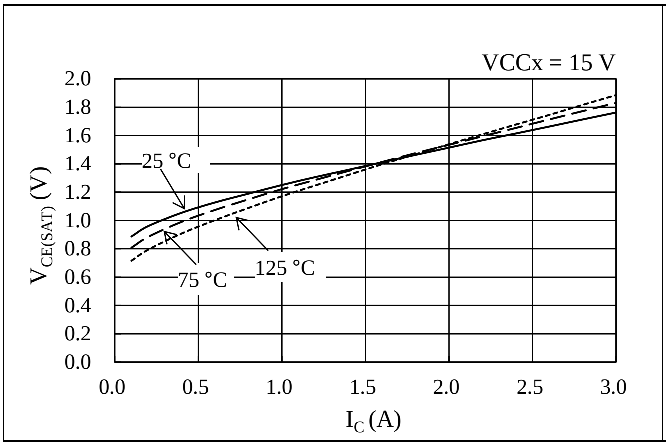


Figure 14-25. IGBT $V_{CE(SAT)}$ vs. I_C

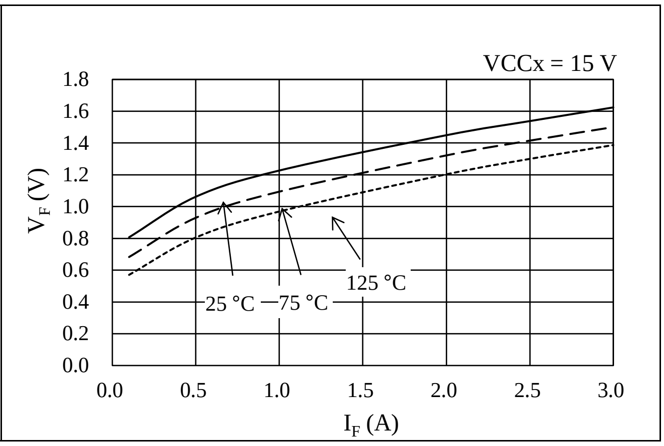


Figure 14-26. Freewheeling Diode V_F vs. I_F

14.3.2 Switching Loss Curves

Conditions: VBBx pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

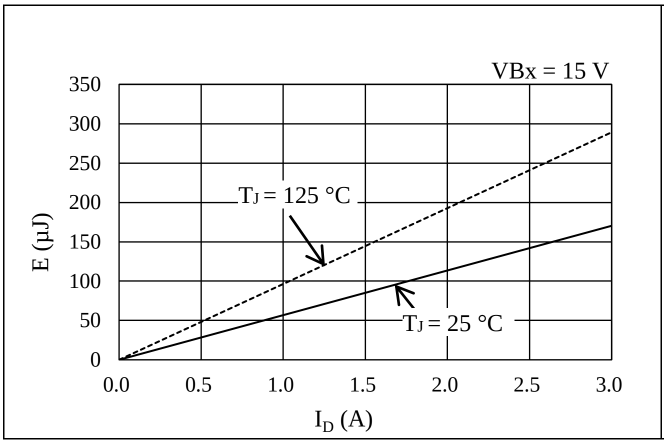


Figure 14-27. High-side Switching Loss

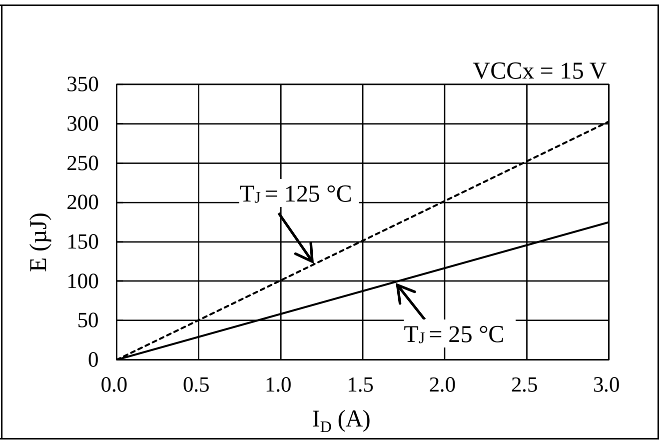


Figure 14-28. Low-side Switching Loss

14.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $V_{CE(SAT)}$ and typical switching losses.

Operating conditions: VBBx pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

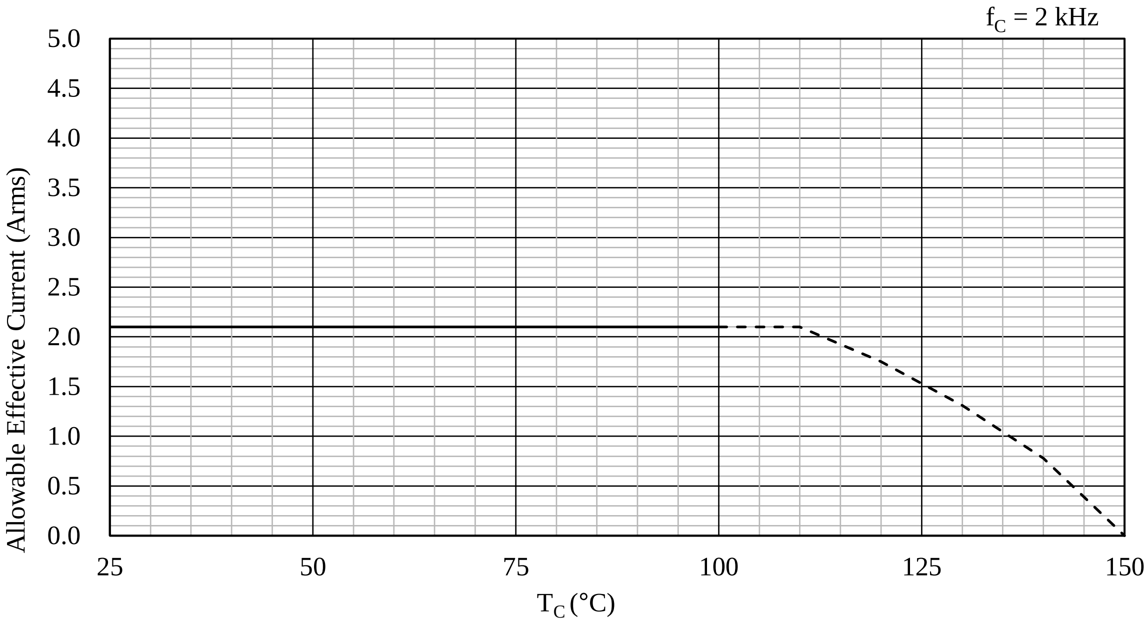


Figure 14-29. Allowable Effective Current (f_C = 2 kHz)

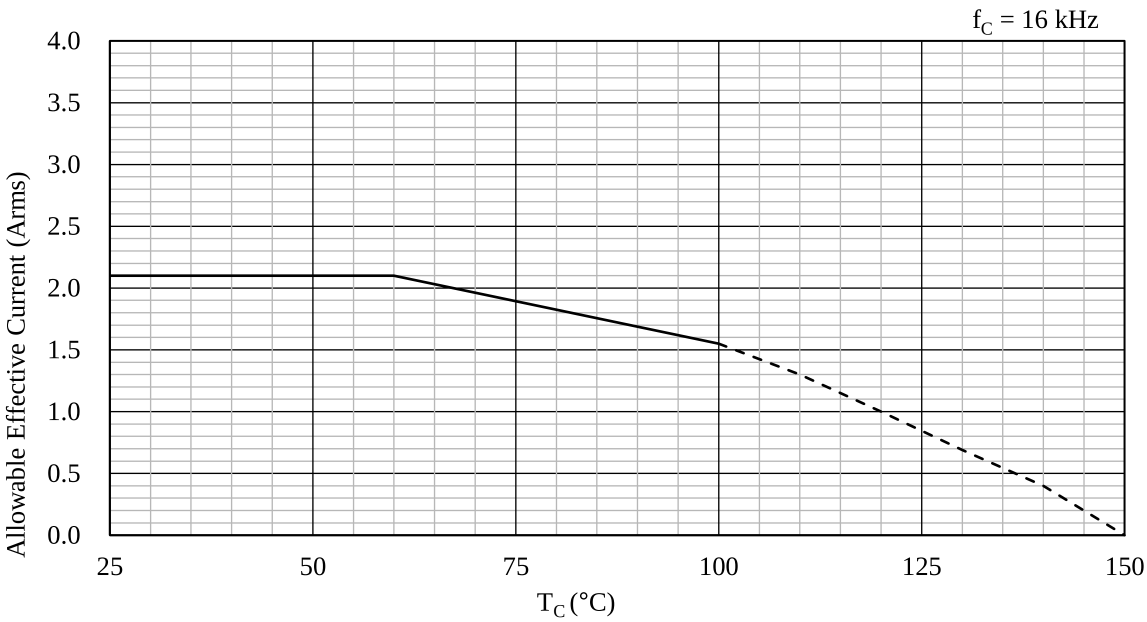


Figure 14-30. Allowable Effective Current (f_C = 16 kHz)

14.5 Short Circuit SOA (Safe Operating Area)

Conditions: $V_{DC} \leq 400$ V, 13.5 V $\leq V_{CC} \leq$ 16.5 V, T_J = 125 °C, 1 pulse.

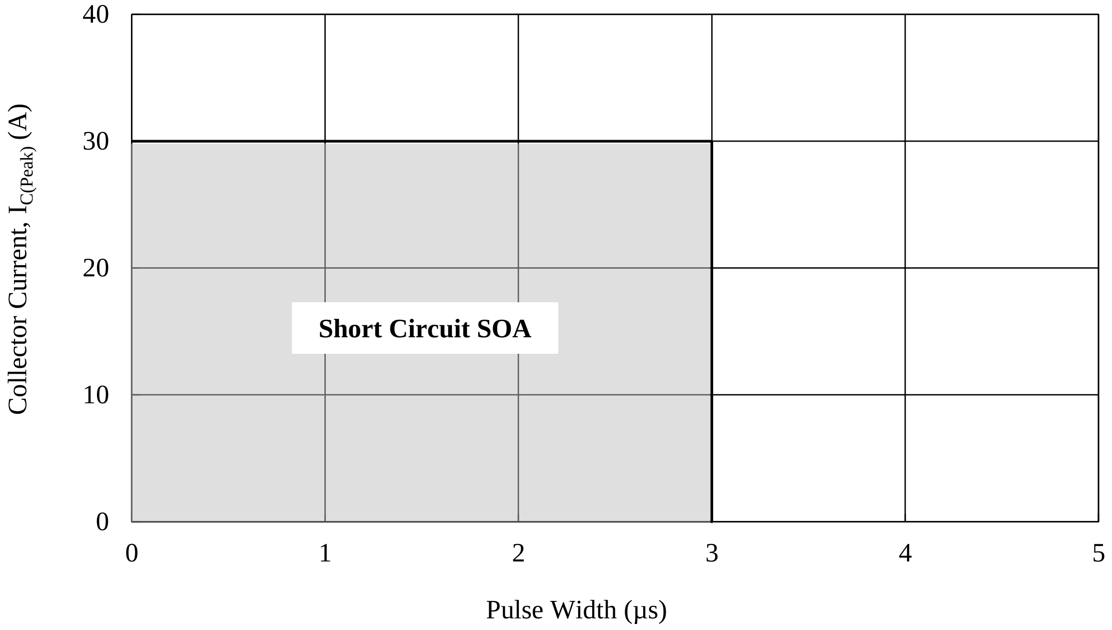


Figure 14-31. Short Circuit SOA

15. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using the IC.

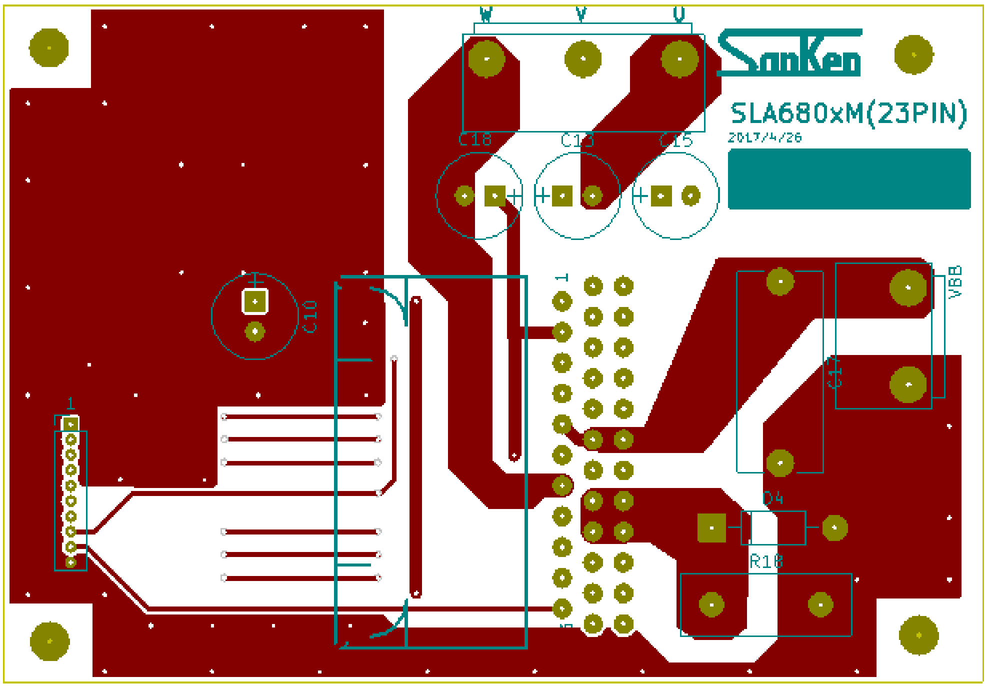


Figure 15-1. Top View

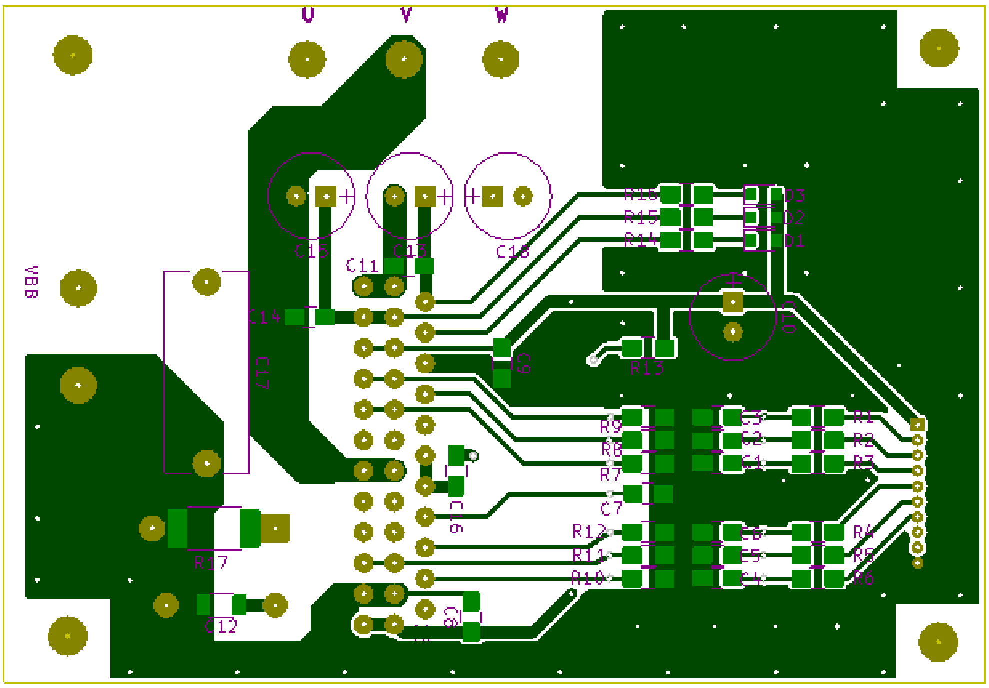


Figure 15-2. Bottom View

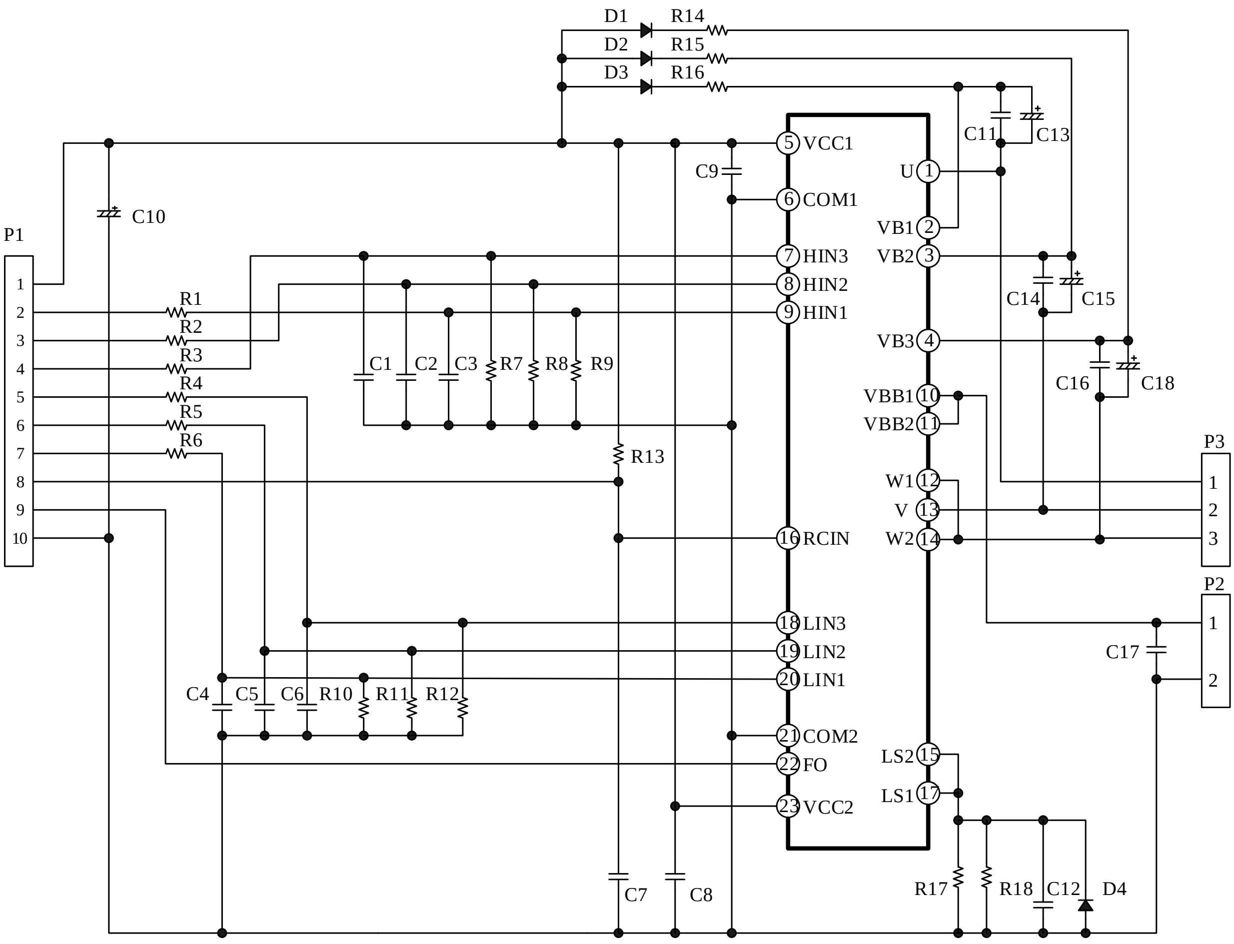


Figure 15-3. Circuit Diagram of PCB Pattern Layout Example

16. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SLA6805MH
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	70 W

- **Circuit Diagram**

See Figure 15-3.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Ceramic	100 pF, 50 V	R1	General	100 Ω, 1/8 W
C2	Ceramic	100 pF, 50 V	R2	General	100 Ω, 1/8 W
C3	Ceramic	100 pF, 50 V	R3	General	100 Ω, 1/8 W
C4	Ceramic	100 pF, 50 V	R4	General	100 Ω, 1/8 W
C5	Ceramic	100 pF, 50 V	R5	General	100 Ω, 1/8 W
C6	Ceramic	100 pF, 50 V	R6	General	100 Ω, 1/8 W
C7	Ceramic	1000 pF, 50 V	R7[(1)]	General	4.7 kΩ, 1/8 W
C8	Ceramic	100 pF, 50 V	R8[(1)]	General	4.7 kΩ, 1/8 W
C9	Ceramic	100 pF, 50 V	R9[(1)]	General	4.7 kΩ, 1/8 W
C10	Electrolytic	0.01 μF, 50 V	R10[(1)]	General	4.7 kΩ, 1/8 W
C11[(1)]	Ceramic	0.01 μF, 50 V	R11[(1)]	General	4.7 kΩ, 1/8 W
C12[(1)]	Ceramic	Open	R12[(1)]	General	4.7 kΩ, 1/8 W
C13	Electrolytic	47 μF, 50 V	R13	General	330 kΩ, 1/8 W
C14[(1)]	Ceramic	0.01 μF, 50 V	R14	General	22 Ω, 1/8 W
C15	Electrolytic	47 μF, 50 V	R15	General	22 Ω, 1/8 W
C16[(1)]	Ceramic	0.01 μF, 50 V	R16	General	22 Ω, 1/8 W
C17	Film	0.1 μF, 400 V	R17[(1)]	Metal plate	0.2 Ω, 2 W
C18	Electrolytic	47 μF, 50 V	R18[(1)]	Metal plate	0.2 Ω, 2 W
D1	Fast recovery	600 V, 2 A	IPM1	IC	SLA6805MH
D2	Fast recovery	600 V, 2 A	P1	Pin header	
D3	Fast recovery	600 V, 2 A	P2	Connector	
D4	General	50 V, 1 A	P3	Connector	

[(1)] Refers to a part that requires adjustment based on operation performance in an actual application.

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