Brushless Motor Driver IC for Automotive

SPF6001

Data Sheet

Description

The SPF6001 is a brushless motor driver IC developed for configuring circuits to match the number of phases of the brushless motor by using multiple units of the IC. The IC is suitable for the applications which the maximum applied voltage to the motor is 150 V or less.

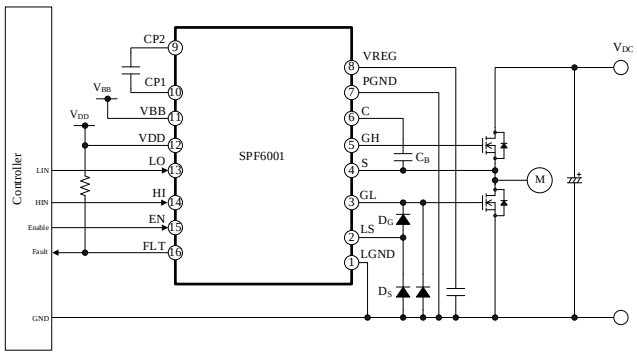
The IC is driven by a bootstrap circuit, and the charge to this boost power supply (boot capacitor) is supplied from the internal auxiliary power supply. This auxiliary power supply is boosted by the internal charge pump circuit and supplies a stable voltage that does not depend on the automotive inherent battery variation to the gate drive circuit.

The IC uses the compact SMD package, HSOP16 with high thermal dissipation and provides high-density mounting. Since the IC has the various protection functions, it can drive brushless motor with few external components.

Features

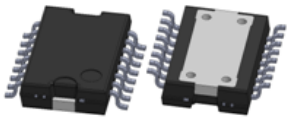
- AEC-Q100 Qualified
- Built-in Bootstrap Diode
- Built-in Auxiliary Power Supply (VREG)
- Bare Lead Frame: Pb-free (RoHS compliant)
- Enable Function
  (All phases shutdown with EN = logic low)
- Fault Signal Output at Protect Circuit Activated
- Protections
- Simultaneous On-state Prevention
- VBB Pin Overvoltage Protection (VBB_OVP): Auto-restart
- Undervoltage Lockout
  VBB Pin (VBB_UVLO): Auto-restart
  VDD Pin (VDD_UVLO): Auto-restart
  VREG Pin (VREG_UVLO): Auto-restart
  High-side Driver (S_UVLO): Auto-restart
- Thermal Shutdown (TSD)

Typical Application



Package

HSOP16



Not to scale

Specifications

- Maximum Main Supply Voltage: V_{DC} = 150 V
- Maximum Logic Supply Voltage: VBB = 35 V
- Typical On-resistance of Internal Drive Circuit
  Sink: 4 Ω
  Source: 5 Ω

Applications

For driving DC brushless motor such as:

- Electronic Power Steering (EPS)
- Integrated Starter Generator (ISG) Hybrid System
- Radiator Pump
- Fan for Air Conditioner

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, and reference ground is the LGND pin.

Parameter	Symbol	Conditions	Ratings	Unit
Direct Current Input Voltage	V_{BB}		−0.6 to 35	V
VREG Pin Voltage	V_{REG}		−0.6 to 18	V
VDD Pin Voltage	V_{DD}		−0.3 to 6	V
HI, LO and EN Pin Voltage	V_{IN}		−0.3 to 6	V
LS Pin Voltage	V_{LS}		−4 to 4	V
GL Pin Voltage	V_{GL}		−4 to 18	V
S Pin Voltage	V_S		−4 to 132	V
GH Pin Voltage	V_{GH}		−4 to 150	V
C Pin Voltage	V_C		−0.3 to 150	V
FLT Pin Voltage	V_{FLT}		−0.3 to 6	V
CP1 Pin Voltage	V_{CP1}		−0.3 to 18	V
CP2 Pin Voltage	V_{CP2}		−0.3 to 18	V
Power Dissipation	P_{D1}	Infinite Heatsink	18.6	W
	P_{D2}	Glass-epoxy Board*	2.97	W
Junction Temperature	T_J		−40 to 150	°C
Operating Ambient Temperature	T_{OP}		−40 to 105	°C
Storage Temperature	T_{STG}		−40 to 150	°C
Junction-to-Case Thermal Resistance	θ_{J-C}		6.7	°C/W
Junction-to-Ambient Thermal Resistance	θ_{J-A}		42	°C/W

* Board size is 50 mm × 74 mm, thickness of glass-epoxy is 1.6 mm, and thickness of copper laminate is 18 µm.

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VBB Pin Input Supply Voltage	V_{BB}		7	14	18	V
VDD Pin Input Supply Voltage	V_{DD}		4.5	5.0	5.5	V

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = −30 °C to 125 °C, V_{BB} = 14 V, V_{DD} = EN = 5 V, C_{REG} = 10 µF, f_{PWM} = 22.5 kHz, and $C_P = C_B$ = 0.1 µF.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VBB Input Current 1	I_{BB1}	VDD = EN = 0 V HI = LO = 0 V	—	3	—	mA
VBB Input Current 2	I_{BB2}	HI = LO = 0 V	—	4	—	mA
VDD Input Current	I_{DD}	HI = LO = 0 V	—	1.0	5.0	mA
C Pin, GH Pin, S Pin Current	I_{CL}	C = GH = S = 90 V	—	—	100	µA
VREG Output Voltage 1	V_{REG1}	7 V < VBB < 8 V	10	12	18	V
VREG Output Voltage 2	V_{REG2}	8 V ≤ VBB	12	15	18	V
Enable Voltage	V_{ENH}	HI = 5 V, LS = S = LGND	2.0	—	—	V
Enable Release Voltage	V_{ENL}		—	—	0.8	V
Enable Voltage Hysteresis	ΔV_{EN}		—	0.15	—	V
HI Pin Logic High Input Voltage	V_{HIH}	LO = 5 V, LS = S = LGND	2.0	—	—	V
HI Pin Logic Low Input Voltage	V_{HIL}		—	—	0.8	V
HI Pin Input Voltage Hysteresis	ΔV_{HI}		—	0.15	—	V
LO Pin Logic High Input Voltage	V_{LOH}	HI = 5 V, LS = S = LGND	2.0	—	—	V
LO Pin Logic Low Input Voltage	V_{LOL}		—	—	0.8	V
LO Pin Input Voltage Hysteresis	ΔV_{LO}		—	0.15	—	V
EN Pin Input Current (H)	I_{ENH}	EN = 5 V	—	100	500	µA
EN Pin Input Current (L)	I_{ENL}	EN = 0 V	−100	—	—	µA
HI Pin Input Current (H)	I_{HIH}	HI = 5 V	—	100	500	µA
HI Pin Input Current (L)	I_{HIL}	HI = 0 V	−100	—	—	µA
LO Pin Input Current (H)	I_{LOH}	LO = 5 V	—	100	500	µA
LO Pin Input Current (L)	I_{LOL}	LO = 0 V	−100	—	—	µA
FLT Pin Output Saturation Voltage	V_{FLT}	$I_{FLT(L)}$ = 1 mA	—	—	0.4	V
Bootstrap Diode Forward Voltage	$V_{TH(BD)}$	I_F = 1 mA	0.4	1.2	1.7	V
GH Pin Source On-resistance	$R_{DS(SC\_GH)}$	HI = 5 V, LO = 0 V, LS = S = LGND, C > 10 V, VREG > 10 V	6	9	15	Ω
GH Pin Sink On-resistance	$R_{DS(SI\_GH)}$		4	6	10	Ω
GL Pin Source On-resistance	$R_{DS(SC\_GL)}$	HI = 0 V, LO = 5 V, LS = S = LGND, C > 10 V, VREG > 10 V	6	9	1	Ω
GL Pin Sink On-resistance	$R_{DS(SI\_GL)}$		4	6	10	Ω
High-side Output Delay Time	$t_{on(H)}$	Ciss = 3300 pF, see Figure 3-1	150	250	420	ns
	$t_{off(H)}$		150	200	410	ns
Low-side Output Delay Time	$t_{on(L)}$	Ciss = 3300 pF, see Figure 3-1	150	250	420	ns
	$t_{off(L)}$		150	200	410	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
GH Pin Output Rise Time	$t_{r(GH)}$	20%V_{GH} to 80%V_{GH}, Ciss = 3300 pF, see Figure 3-1	10	50	100	Ns
GH Pin Output Fall Time	$t_{f(GH)}$		10	50	100	ns
GL Pin Output Rise Time	$t_{r(GL)}$	20%V_{GL} to 80%V_{GL}, Ciss = 3300 pF, see Figure 3-1	10	50	100	ns
GL Pin Output Fall Time	$t_{f(GL)}$		10	50	100	ns
VDD Pin Undervoltage Lockout Release Voltage	$V_{UVDD(H)}$		3.5	4.0	4.5	V
VDD Pin Undervoltage Lockout Operating Voltage	$V_{UVDD(L)}$		3.3	3.8	4.3	V
VDD Pin Undervoltage Lockout Hysteresis	ΔV_{UVDD}		—	0.2	—	V
VBB Pin Overvoltage Protection Operating Voltage	$V_{OVBB(H)}$		24	28	32	V
VBB Pin Overvoltage Protection Release Voltage	$V_{OVBB(L)}$		22	25	31	V
VBB Pin Overvoltage Protection Hysteresis	ΔV_{OVBB}		—	3	—	V
VBB Pin Undervoltage Lockout Release Voltage	$V_{UVBB(H)}$		6.0	6.5	7.0	V
VBB Pin Undervoltage Lockout Operating Voltage	$V_{UVBB(L)}$		5.5	6.1	6.6	V
VBB Pin Undervoltage Lockout Hysteresis	ΔV_{UVBB}		—	0.4	—	V
VREG Pin Undervoltage Lockout Release Voltage	$V_{UVREG(H)}$		6.5	7.5	8.5	V
VREG Pin Undervoltage Lockout Operating Voltage	$V_{UVREG(L)}$		6.0	7.1	8.2	V
VREG Pin Undervoltage Lockout Hysteresis	ΔV_{UVREG}		—	0.4	—	V
High-side Driver Undervoltage Lockout Operating Voltage	$V_{UVS(L)}$		8.4	9.4	10.8	V
High-side Driver Circuit Current	I_{CS1}	V_{SC} = 10 V	0	—	240	µA
	I_{CS2}	V_{SC} = 14 V	0	—	480	µA
Thermal Shutdown Starting Temperature*	T_{TSD}		151	—	—	°C

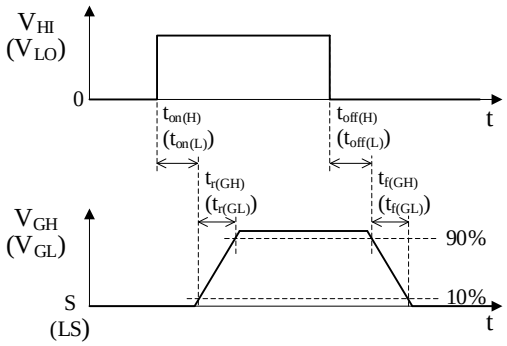


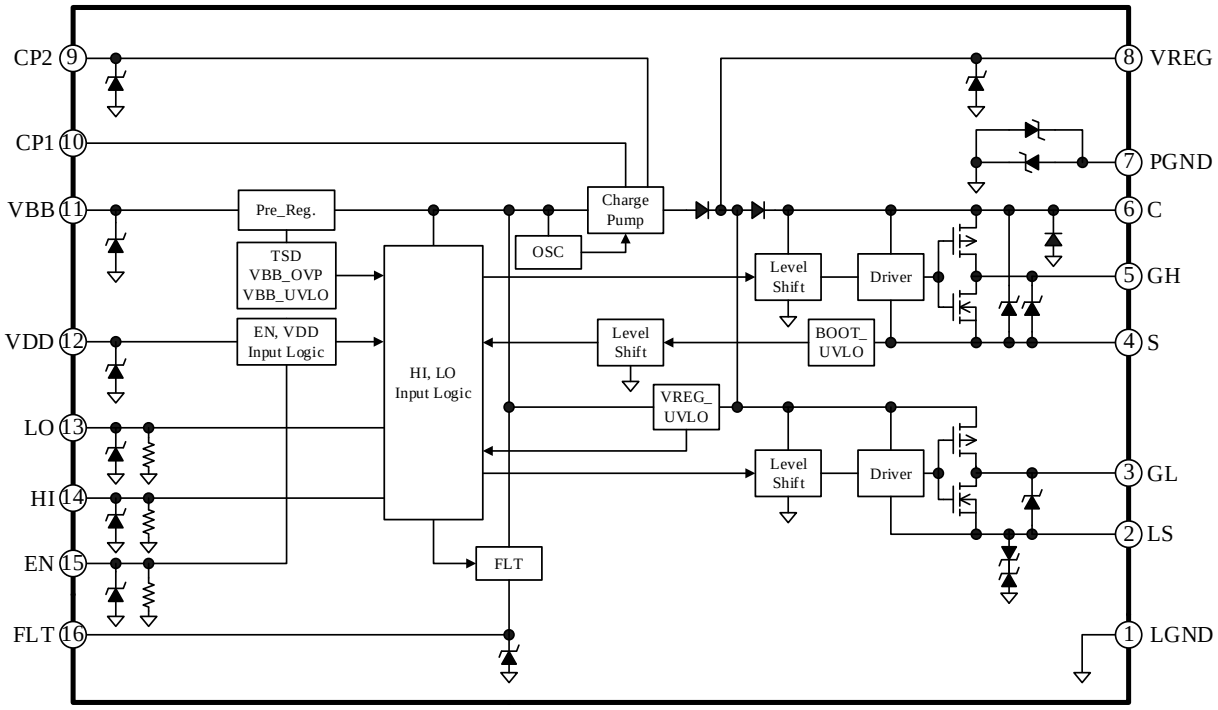
Figure 3-1. Definition of Switching Time

* It is guaranteed by design. The typical design value of thermal shutdown starting temperature is 165 °C.

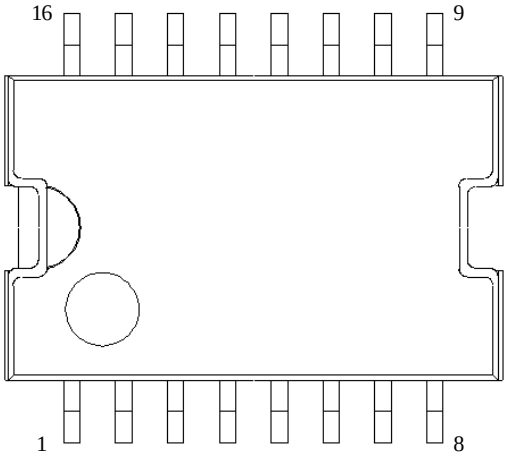
4. Mechanical Characteristics

Parameter	Min.	Typ.	Max.	Unit
Package Weight	—	0.87	—	g

5. Block Diagram



6. Pin Configuration Definitions



Pin Number	Pin Name	Function
1	LGND	Control ground
2	LS	Low-side source connection
3	GL	Low-side gate drive signal output
4	S	High-side source connection
5	GH	High-side gate drive signal output
6	C	Boot capacitor connection
7	PGND	Power ground
8	VREG	Capacitor connect pin for high-and low-side gate drive
9	CP2	Capacitor connect pin 2 for charge pump circuit
10	CP1	Capacitor connect pin 1 for charge pump circuit
11	VBB	Main supply input
12	VDD	Logic supply input for input signal
13	LO	Low side logic input
14	HI	High side logic input
15	EN	Enable signal input
16	FLT	Fault signal output (Open drain)

7. Typical Application

In the case of the application so that the LS pin voltage exceeds the absolute maximum rating of ±4 V, a diode, D_S, must be added between the LS pin and the LGND pin.

If the GL pin voltage becomes lower by about 0.6 V to 1.8 V than the LS pin voltage, the IC may be damaged. To avoid the situation, a diode, D_G, must be added between the GL pin and the LS pin.

D_S and D_G must be placed near the IC, and connected with a minimal length of traces.

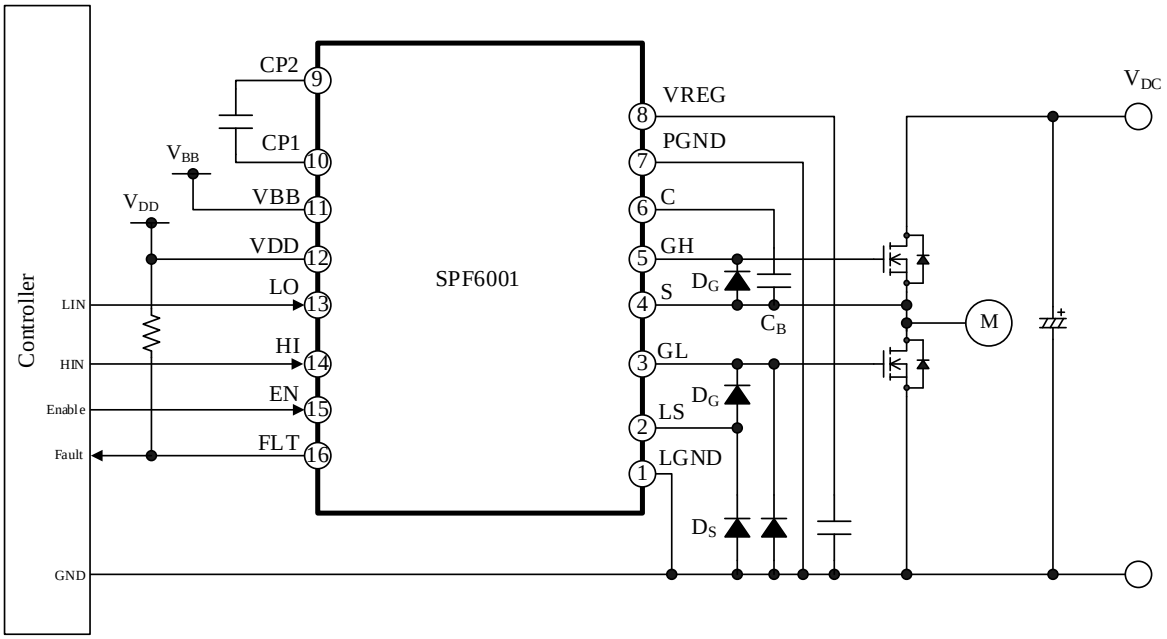


Figure 7-1. Typical Application

8. Truth Table

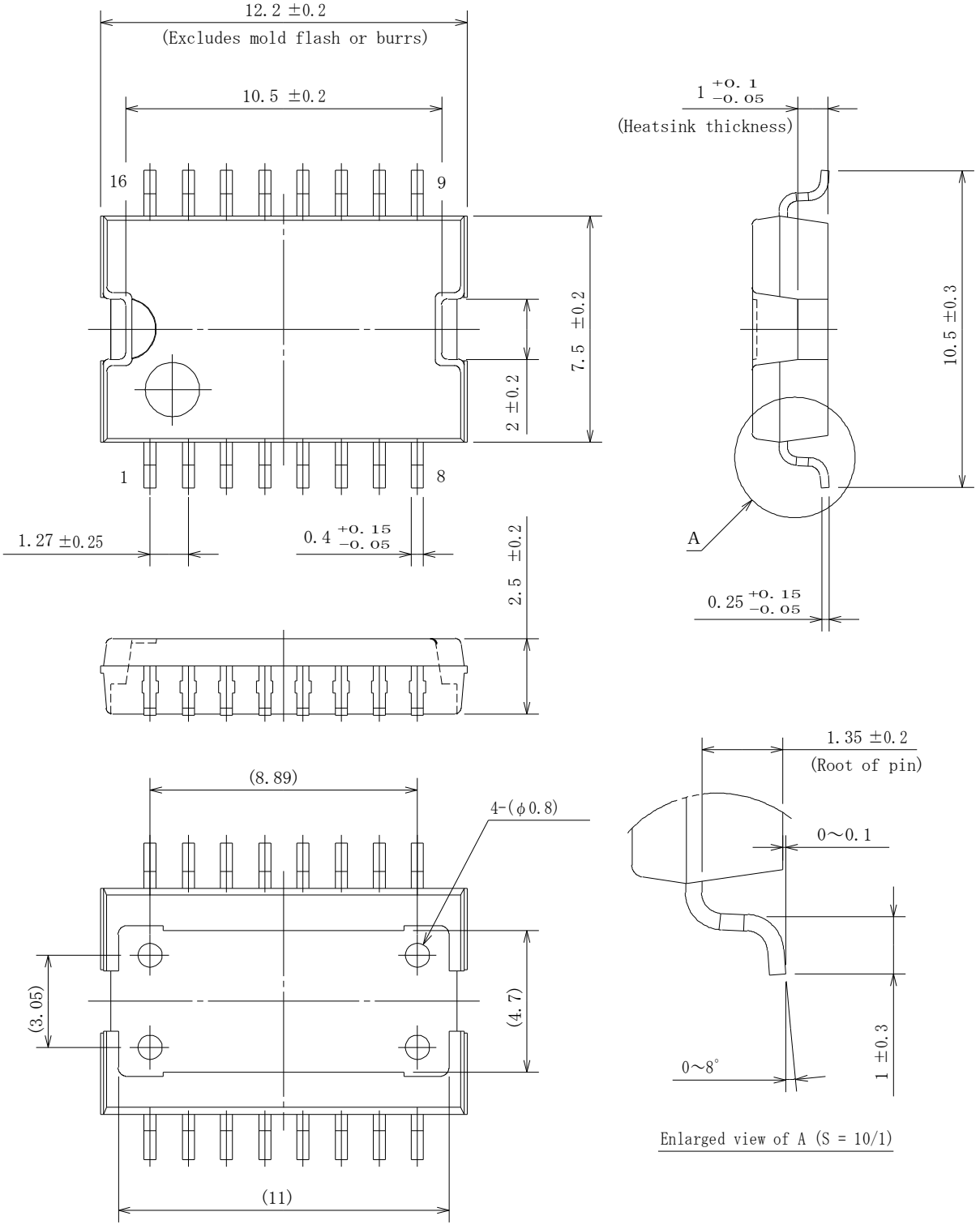
Table 8-1. Truth Table for Operation Modes

Mode	Input Pin		Output Pin			Remarks
	HI	LO	GH	GL	FLT*	
Normal Operation	L	L	L	L	H	
	H	L	H	L	H	
	L	H	L	H	H	
	H	H	L	L	H	Simultaneous On-state Prevention
VBB Pin Undervoltage Lockout (VBB_UVLO)	L	L	L	L	L	
	H	L	L	L	L	
	L	H	L	L	L	
	H	H	L	L	L	
VDD Pin Undervoltage Lockout (VDD_UVLO)	L	L	L	L	L	
	H	L	L	L	L	
	L	H	L	L	L	
	H	H	L	L	L	
Enable Signal Input (EN pin is low level)	L	L	L	L	H	
	H	L	L	L	H	
	L	H	L	L	H	
	H	H	L	L	H	
VREG Pin Undervoltage Lockout (VREG_UVLO)	L	L	L	L	L	
	H	L	H	L	L	
	L	H	L	H	L	
	H	H	L	L	L	Simultaneous On-state Prevention
High-side Driver Undervoltage Lockout (S_UVLO)	L	L	L	L	L	
	H	L	H	L	L	
	L	H	L	H	L	
	H	H	L	L	L	
Thermal Shutdown (TSD)	L	L	L	L	L	
	H	L	L	L	L	
	L	H	L	L	L	
	H	H	L	L	L	

*The FLT pin is pulled up to the VDD pin.

9. Physical Dimensions

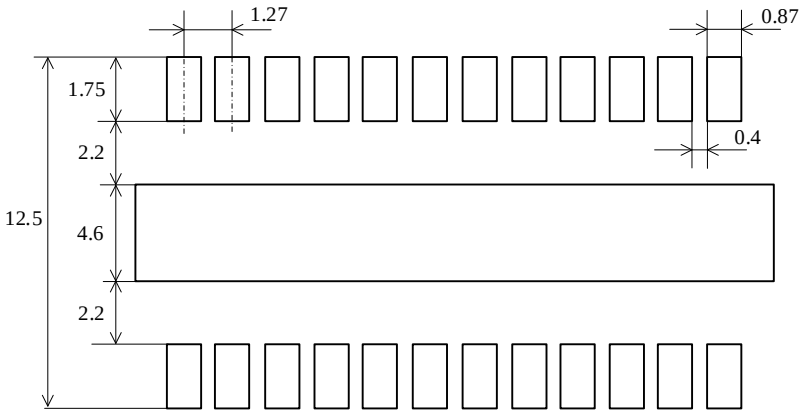
● **HSOP16 Package**



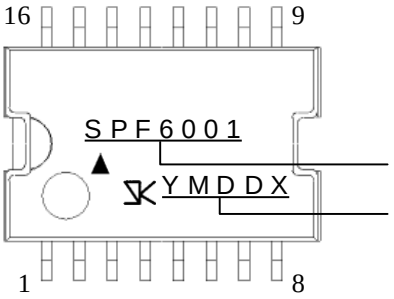
NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)

● **HSOP16 Land Pattern Example**



10. Marking Diagram



Part Number

Lot Number

Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

11. Operational Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

11.1. Pin Descriptions

11.1.1. VBB

This is the main supply input pin of the IC. Recommended applied voltage to the VBB pin is 7 V to 18 V.

When the same power supply is connected to the VBB pin and the external output transistors, power supply loop trace should be designed as wide and short as possible. A Bypass capacitor for noise reduction should be connected to the VBB pin as needed. The bypass capacitor should be placed near the VBB pin, and connected to the VBB pin with a minimal length of traces.

11.1.2. VDD

This is the supply input for input logic circuit. Recommended applied voltage to the VDD pin is 4.5 V to 5.5 V.

11.1.3. VREG

The power supply of high- and low-side gate drive circuit is generated by the internal charge pump circuit. Thus, the gate can be driven stably even if the VBB pin voltage is low (7 V or more).

Capacitor (10 μF or more is recommended) for holding supply voltage of gate drive circuit should be connected to the VREG pin. External power supply connection is unnecessary.

11.1.4. CP1 and CP2

Connect a capacitor for internal charge pump circuit between the CP1 pin and the CP2 pin. The recommended capacitance is 0.1 μF.

11.1.5. C

Connect a high-side boot capacitor, C_B, between the C pin and the S pin. The recommended capacitance of C_B is 0.1 μF or more. Since the capacitance depends on the drive frequency and control duty, the setting is required according to the application. For proper startup, turn on the low-side output transistors first, and then charge C_B up to its maximum capacity.

11.1.6. HI and LO

These are the signal input pins. The HI pin acts as high-side controller whereas the LO pin acts as low-side controller. Since the HI and LO pins incorporate a pull-down resistor, the initial state is low (see the block diagram in Section 4).

The width of the input signals to the HI and LO pins is required 500 ns or more.

Note that dead time setting for the input signals of the HI and LO pins must be done because the IC does not have a dead time generator. Dead time must be set so that the simultaneous on-state does not occur according to the output transistors to be used.

11.1.7. EN

When the high signal is input to the EN pin, all output signals of the GH and GL pins become logic low. Since the EN pin incorporates a pull-down resistor, the initial state is low (see the block diagram in Section 4).

11.1.8. FLT

This is the output pin of fault signal. Pull up the FLT pin because the FLT pin is open drain. When the FLT pin is pulled up to the power supply of 5 V, the recommended pull-up resistor is about 20 kΩ. The FLT pin logic level is high in normal operation, and becomes low when one or more the following protections are activated.

- VBB pin Overvoltage Protection (VBB_OVP)
- VBB pin Undervoltage Lockout (VBB_UVLO)
- VDD pin Undervoltage Lockout (VDD_UVLO)
- VREG pin Undervoltage Lockout (VREG_UVLO)
- High-side driver Undervoltage Lockout (S_UVLO)
- Thermal Shutdown (TSD)

11.1.9. GH and GL

These are the gate drive outputs, and are connected to the gate of external output transistors. The GH pin acts as high-side controller whereas the GL pin acts as low-side controller. A pull-down resistor of 100 kΩ (typ.) and protection Zener diodes (the Zener diode) of 18 V (typ.) are internally connected between the GH pin and the S pin, and between the GL pin and the LS pin respectively (see Figure 11-1 and Figure 11-2).

When the current from motor flows to the forward direction of this Zener diode, this may be damaged. In

the application that the current flows to the forward direction of the Zener diode, an external diode, D_G, must be added between the GH pin and the S pin, and between the GL pin and the LS pin respectively (see Figure 7-1).

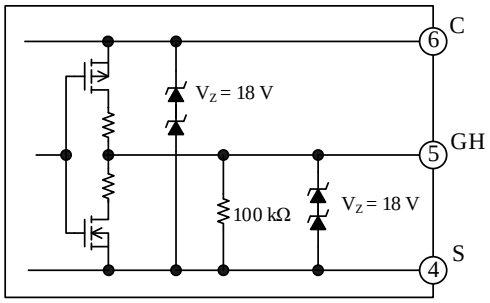


Figure 11-1. Internal Circuit of High-side Output

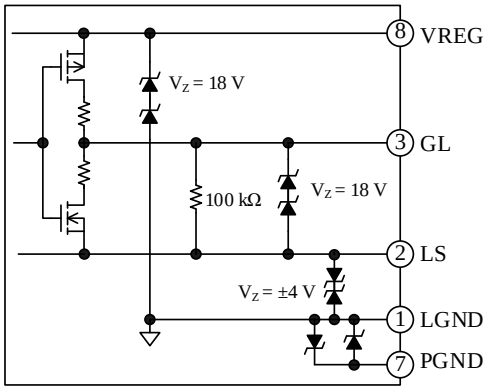


Figure 11-2. Internal Circuit of Low-side Output

11.1.10. S and LS

Connect the S pin to the source pin of high-side output transistors and the drain pin of low-side output transistors, and the LS pin to the source pin of low-side output transistors.

An ESD protection bidirectional Zener diode of ±4 V is internally connected between the LS pin and the LGND pin (see Figure 11-2). In the application that the voltage of ±4 V or more is applied between the S pin and the LGND pin, the external diode, D_S, must be connected between the LS pin and the LGND pin (see Figure 7-1).

11.1.11. LGND and PGND

The LGND pin is control ground of the IC. The PGND pin is power ground. A Zener diode is internally connected bidirectionally between the LGND pin and the PGND pin in parallel (see Figure 11-2).

11.2. Basic Operation

At startup, the voltage is applied to the VBB and VDD pins which are the power supply of the IC. Then, the high signal is input to the EN pin. After that, input the signal to the HI and LO pins; and on/off controls of the output transistors start.

When the high signal is input to the HI pin, high-side gate output (the GH pin) becomes logic high. When the high signal is input to the LO pin, low-side gate output (the GL pin) becomes logic high (see Table 8-1).

The EN pin has an internally low-pass filter of 2.5 µs for the noise malfunction prevention. The HI and LO pins do not have internal low-pass filter.

11.3. Simultaneous On-state Prevention

When the high signal is input to the HI and LO pins at once, the Simultaneous On-state Prevention is activated, and the outputs of the GH and GL pins become logic low. This prevents the breakdown of the output transistors.

11.4. Protections

The IC has the following protection functions.

When the following protections are activated, the outputs of the GH and GL pins become logic low, and stop the output transistors. In addition, the fault signal is output (the FLT pin logic level becomes low).

When the protection is released after the fault conditions are removed, the FLT output becomes logic high. Then, the GH and GL pins restart output the signals according to the input commands on the HI and LO pins from the next falling edge.

However, during VREG_UVLO is activated, the IC outputs the fault signal with maintaining the outputs of the GH and GL pins according to input signal.

- VBB Pin Overvoltage Protection (VBB_OVP)
- VBB Pin Undervoltage Lockout (VBB_UVLO)
- VDD Pin Undervoltage Lockout (VDD_UVLO)
- VREG Pin Undervoltage Lockout (VREG_UVLO)
- High-side Driver Undervoltage Lockout (S_UVLO)
- Thermal Shutdown (TSD)

11.4.1. VBB Pin Overvoltage Protection (VBB_OVP)

When the VBB pin voltage increases to the VBB pin overvoltage protection operating voltage $V_{OVBB(H)}$ = 28 V or more, VBB_OVP is activated. When the VBB pin voltage decreases to the release voltage $V_{OVBB(L)}$ = 25 V or less, the IC returns to the normal operation.

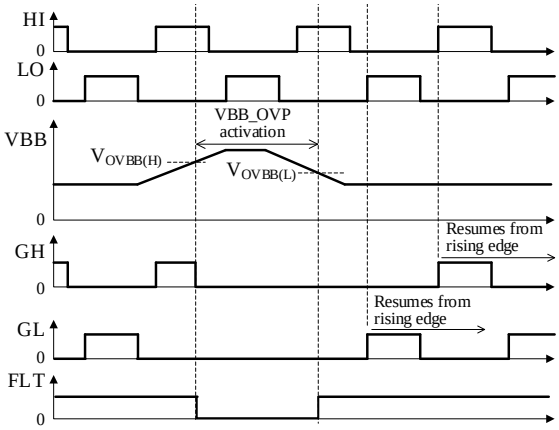


Figure 11-3. Operational Waveform of VBB_OVP

11.4.2. VBB Pin Undervoltage Lockout (VBB_UVLO)

The VBB pin voltage decrease to the VBB pin undervoltage lockout operating voltage $V_{UVBB(L)}$ = 6.1 V or less, VBB_UVLO is activated. When the VBB pin voltage increases to the release voltage $V_{UVBB(H)}$ = 6.5 V or more, the IC returns to the normal operation. During the VBB_UVLO activation, the internal charge pump circuit (OSC circuit operation is maintained) and the VREG pin boost operation are stopped.

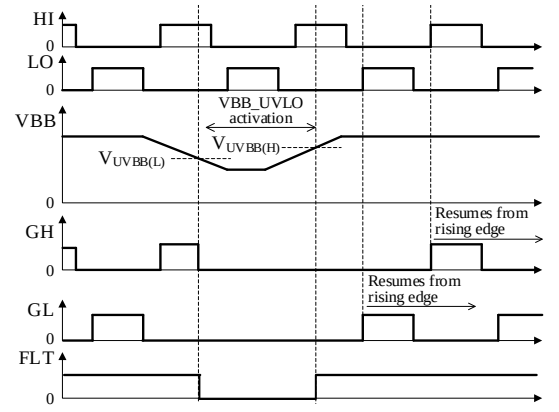


Figure 11-4. Operational Waveform of VBB_UVLO

11.4.3. VDD Pin Undervoltage Lockout (VDD_UVLO)

When the VDD pin voltage decreases to the VDD pin undervoltage lockout operating voltage $V_{UVDD(L)}$ = 3.8 V or less, the VDD_UVLO is activated.

When the VDD pin voltage increases to the release voltage $V_{UVDD(H)}$ = 4.0 V or more, the IC returns to the normal operation.

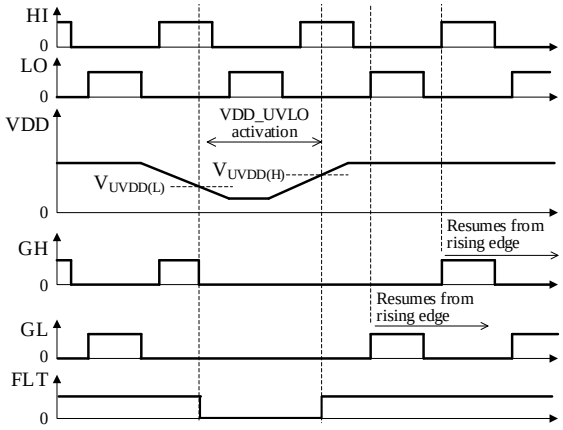


Figure 11-5. Operational Waveform of VDD_UVLO

11.4.4. VREG Pin Undervoltage Lockout (VREG_UVLO)

When the VREG pin voltage decreases to VREG pin undervoltage lockout operating voltage $V_{UVREG(L)}$ = 7.1 V or less due to the leak current of the capacitor connecting to the VREG pin, the VREG_UVLO is activated.

When the VREG pin voltage increases to the release voltage $V_{UVREG(H)}$ = 7.5 V or more, the IC returns to the normal operation.

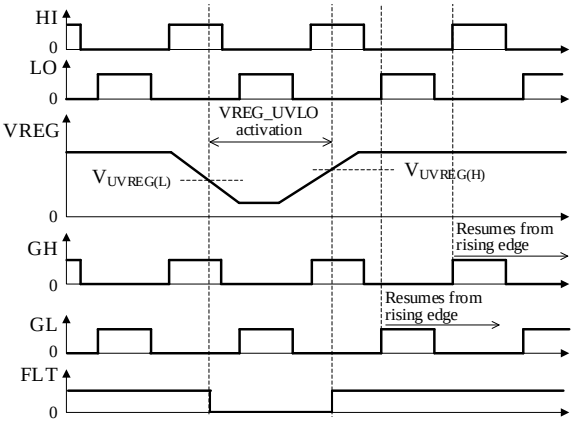


Figure 11-6. Operational Waveform of VREG_UVLO

11.4.5. High-side Driver Undervoltage Lockout (S_UVLO)

The SPF6001 incorporates the high-side driver undervoltage lockout (S_UVLO) between the S and C pins. The voltage between S and C pins decrease to the high-side driver undervoltage lockout operating voltage $V_{UVS(L)}$ = 9.4 V or less, S_UVLO is activated.

When the voltage between S and C pins increases to 9.5 V or more, the IC returns to its normal operation.

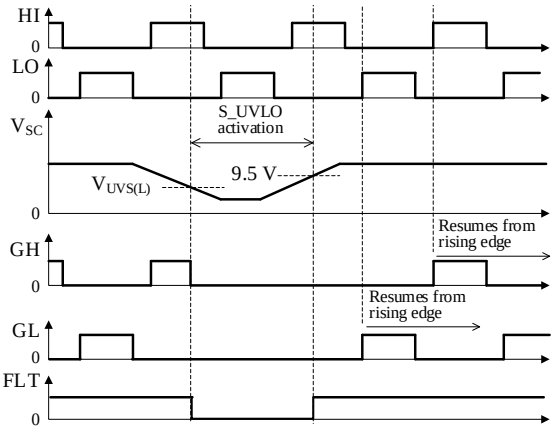


Figure 11-7. Operational Waveform of S_UVLO

11.4.6. Thermal Shutdown (TSD)

When the junction temperature of the IC increases to T_{TSD} = 151 °C (min.) or more, the TSD is activated. The design value of TSD operating temperature is 165 °C (typ.). TSD has the temperature hysteresis. When the temperature decreases by about 10 °C from the junction temperature of TSD operation, TSD is released, and the IC returns to the normal operation.

TSD protects the IC against instantaneous heat generation, and does not guarantee the operation including reliability for a state that the heat generation continues for a long time.

11.5. Enable Function

The IC has an enable function.

When the low signal (0.8 V or less) is input to the EN pin, the input signals of the GH and GL pins become logic low. When the high signal (2.0 V or more) is input to the EN pin, the GH and GL pins restart output the signals according to the input commands on the HI and LO pins from the next rising edge. During the EN pin logic is low, the FLT pin logic level is maintained high.

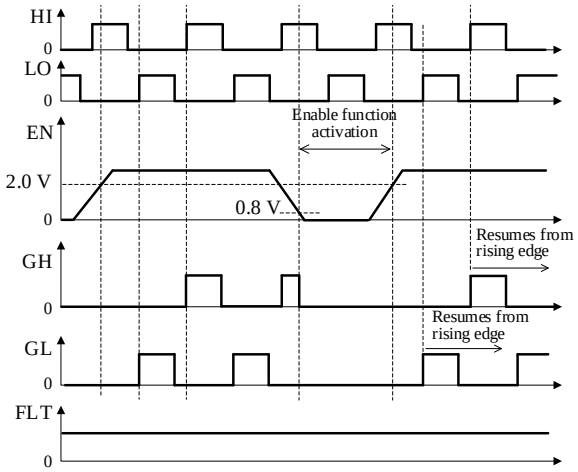


Figure 11-8 Operational Waveform of Enable Function

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