SSC2001S Power Factor Correction Continuous Conduction Mode Controller

General Description

The SSC2001S is a continuous conduction mode (CCM) control IC for power factor correction (PFC). The IC allows the realization of high-power output, high-efficiency, and power management systems which require few external components by the average current control system.

Features and Benefits

- Continuous conduction mode (CCM) system: low peak current and suitability for high power applications
- Average current control system: no multiplier and few external components allows simple circuit configuration because no input voltage detection required
- PWM and frequency modulation functions: PWM operation frequency fixed at 65 kHz (typ) with superimposed variable frequency according to duty cycle
- Maximum duty cycle 94% (typ)
- Error amplifier reference voltage 3.5 V (typ)
- Built-in high speed load response (HSR) function
- Brown-in/brown-out protection function: protects the power supply at low input voltages
- Protection functions:
  - Output overvoltage protection (OVP): turns off gate output on pulse-by-pulse basis, with auto restart
  - Overcurrent protection (OCP): two types, both with auto restart:
    - $V_{IS(OCPL)}$: limits power by reducing duty cycle of next cycle after detection
    - $V_{IS(OCPH)}$: turns off gate output on pulse-by-pulse basis
  - Open loop detection (OLD) on output: stops oscillation, and the operation switches to standby mode; auto restart after removal of cause of open loop

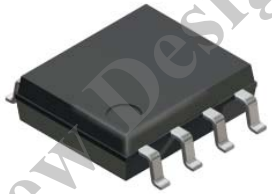

Figure 1. SSC2001S packages are industry-standard SOP8 surface mount.

Applications

Power factor correction of middle to high power for electronic devices such as:

- AC/DC power supplies
- Digital appliances for large size LCD/PDP television and so forth
- Office automation (OA) equipment for computer, server, montior, and so forth
- Communication facilities

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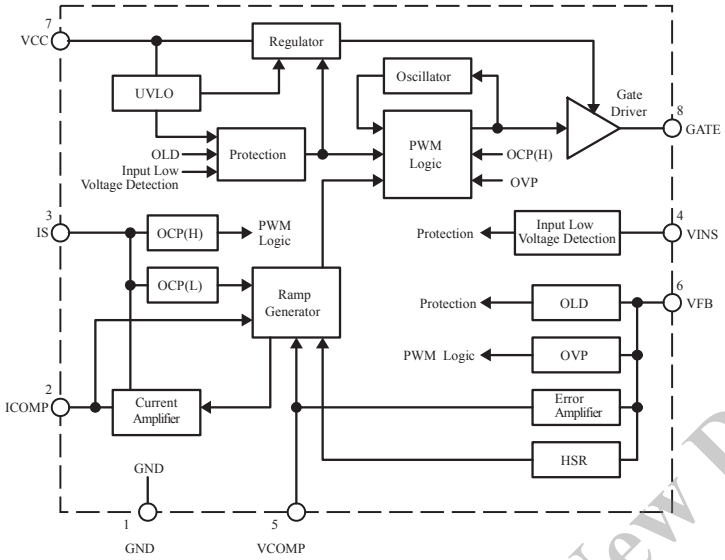
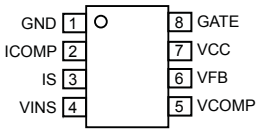
Functional Block Diagram



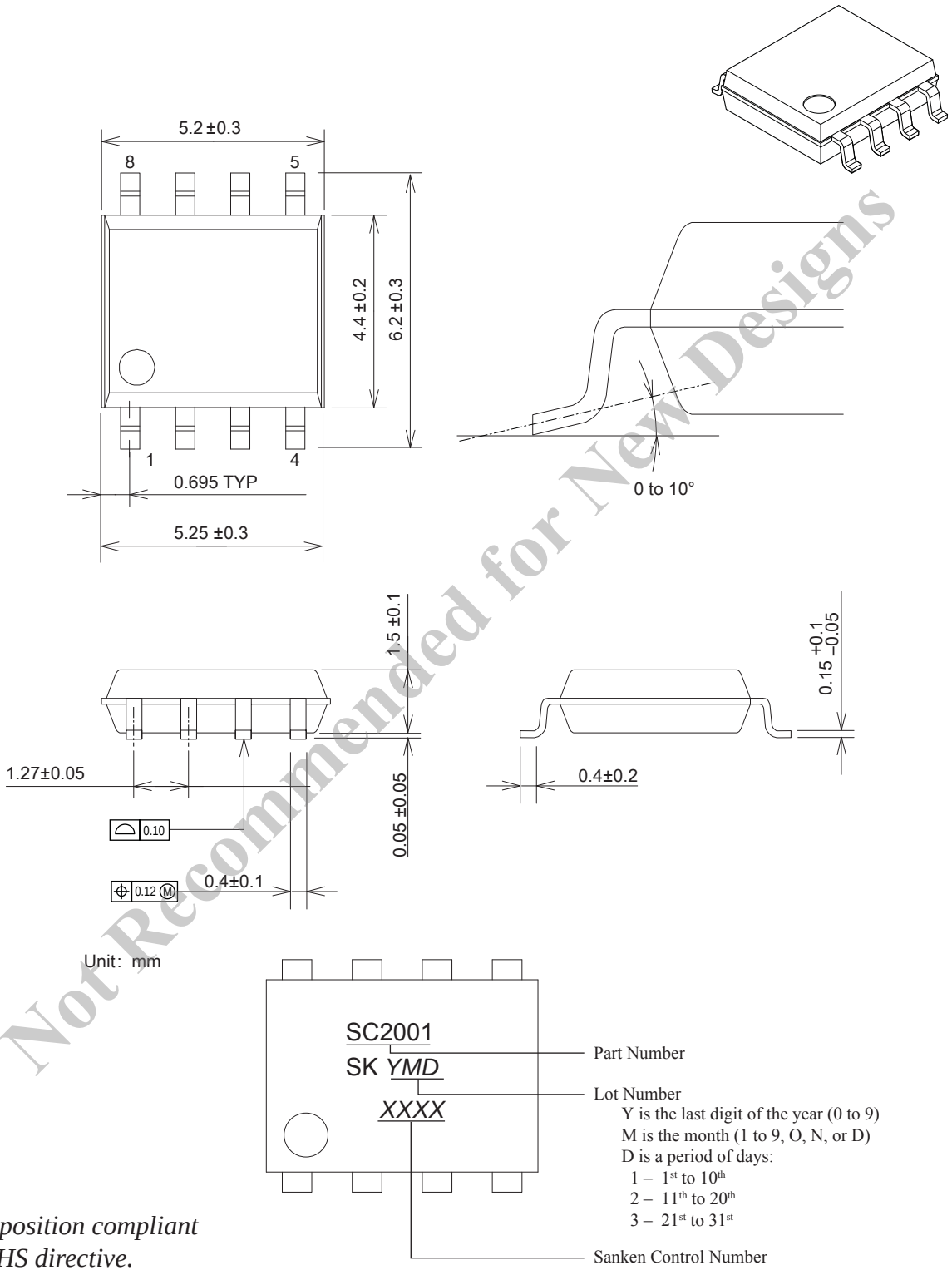
Pin-out Diagram



Pin List Table

Name	Number	Function
1	GND	Ground
2	ICOMP	Current amplifier output
3	IS	Overcurrent detection signal input
4	VINS	Input low voltage detection signal input (Brown-in/brown-out protection function)
5	VCOMP	Error amplifier output/phase compensation
6	VFB	Output constant voltage control signal/output overvoltage signal/output open loop detection signal input
7	VCC	Control circuit power supply input
8	GATE	Gate drive output

Package Diagram
SOP8 package



Part Number

Lot Number
Y is the last digit of the year (0 to 9)
M is the month (1 to 9, O, N, or D)
D is a period of days:
1 – 1st to 10th
2 – 11th to 20th
3 – 21st to 31st

Sanken Control Number

Pb-free.
Device composition compliant with the RoHS directive.

Electrical Characteristics

- Refer to the datasheet for details.
- The polarity value for current specifies a sink as "+ ," and a source as "–," referencing the IC.

Absolute Maximum Ratings Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Pins	Rating	Unit
VCC Pin Voltage	V_{CC}	7 – 1	–0.3 to 30	V
VINS Pin Voltage	V_{INS}	4 – 1	–0.3 to 5.5	V
ICOMP Pin Voltage	V_{ICOMP}	2 – 1	–0.3 to 5.5	V
IS Pin Voltage	V_{IS}	3 – 1	–5.5 to 0.3	V
IS Pin Current	I_{IS}	3 – 1	–1 to 1	mA
VFB Pin Voltage	V_{FB}	6 – 1	–0.3 to 5.5	V
VFB Pin Current	I_{FB}	6 – 1	–1 to 1	mA
VCOMP Pin Voltage	V_{VCOMP}	5 – 1	–0.3 to 5.5	V
GATE Pin Voltage	V_{GATE}	8 – 1	–0.3 to 30	V
Frame Temperature during Operation	T_{FOP}	–	–40 to 110	°C
Storage Temperature	T_{stg}	–	–40 to 125	°C
Junction Temperature	T_J	–	–40 to 150	°C

Electrical Characteristics of Control Part Unless specifically noted, T_A is 25°C, V_{CC} = 15 V

Characteristic	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Unit
Power Supply Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		7 – 1	10.5	11.3	12.1	V
Operation Stop Voltage	$V_{CC(OFF)}$		7 – 1	9.5	10.3	11.1	V
Operation Voltage Hysteresis	$V_{CC(HYS)}$		7 – 1	0.7	0.9	1.1	V
Circuit Current in Non-Operation	$I_{CC(OFF)}$	V_{CC} = 10 V	7 – 1	30	100	200	µA
Circuit Current in Operation	$I_{CC(ON)}$		7 – 1	6.0	9.0	12.0	mA
Circuit Current in Standby	$I_{CC(STANDBY)}$	V_{FB} = 0.5 V	7 – 1	2.0	4.0	6.0	mA
Oscillation Operation							
Operation Frequency	f_{OSC}	V_{IS} = 0 V, V_{VCOMP} = 4 V	8 – 1	57	65	70	kHz
Maximum Duty Cycle	D_{MAX}	V_{IS} = 0 V, V_{VCOMP} = 4 V	8 – 1	90	94	99.3	%
Minimum Duty Cycle	D_{MIN}	V_{IS} = 0.5 V, V_{VCOMP} = 0 V	8 – 1	–	–	0	%
Minimum Off-Time*	t_{OFFMIN}		8 – 1	150	250	350	ns
Protection Operation							
VFB Pin Open Loop Detection Threshold Voltage	$V_{FB(OLD)}$		6 – 1	0.51	0.55	0.59	V
VFB Pin Overvoltage Protection Threshold Voltage	$V_{FB(OVP)}$		6 – 1	3.57	3.745	3.85	V
IS Pin Overcurrent Protection High Threshold Voltage	$V_{IS(OCPH)}$		3 – 1	−0.81	−0.75	−0.69	V
IS Pin Overcurrent Protection Low Threshold Voltage	$V_{IS(OCPL)}$		3 – 1	−0.54	−0.5	−0.46	V
VINS Pin Input Undervoltage Protection Low Threshold Voltage	$V_{INS(L)}$	V_{VINS} = 0 V	4 – 1	0.51	0.55	0.59	V
VINS Pin Input Undervoltage Protection High Threshold Voltage	$V_{INS(H)}$		4 – 1	0.94	1.0	1.08	V
VINS Pin Input Undervoltage Protection Bias Current	$I_{VINS(BIAS)}$		4 – 1	−1.0	−	0	µA
Current Loop							
Current Amplifier Transconductance Gain	gm_{CA}		–	1.1	1.4	1.7	mS
Current Amplifier Output Source Current*	$I_{CA(SO)}$		–	–	−50	–	µA
Current Amplifier Output Sink Current*	$I_{CA(SK)}$		–	–	50	–	µA
ICOMP Pin Output Open Loop Detection Threshold Voltage	$V_{ICOMP(OLD)}$	V_{FB} = 0.5 V	2 – 1	3.6	4.0	4.3	V
Voltage Loop							
Error Amplifier Reference Voltage	$V_{FB(REF)}$	I_{VCOMP} = 0 µA	6 – 1	3.4	3.5	3.6	V
Error Amplifier Transconductance Gain	gm_{EA}		–	45	60	75	µS
Error Amplifier Maximum Source Current	$I_{VCOMP(SO)}$		5 – 1	−38	−30	−21	µA
Error Amplifier Maximum Sink Current	$I_{VCOMP(SK)}$		5 – 1	21	30	38	µA

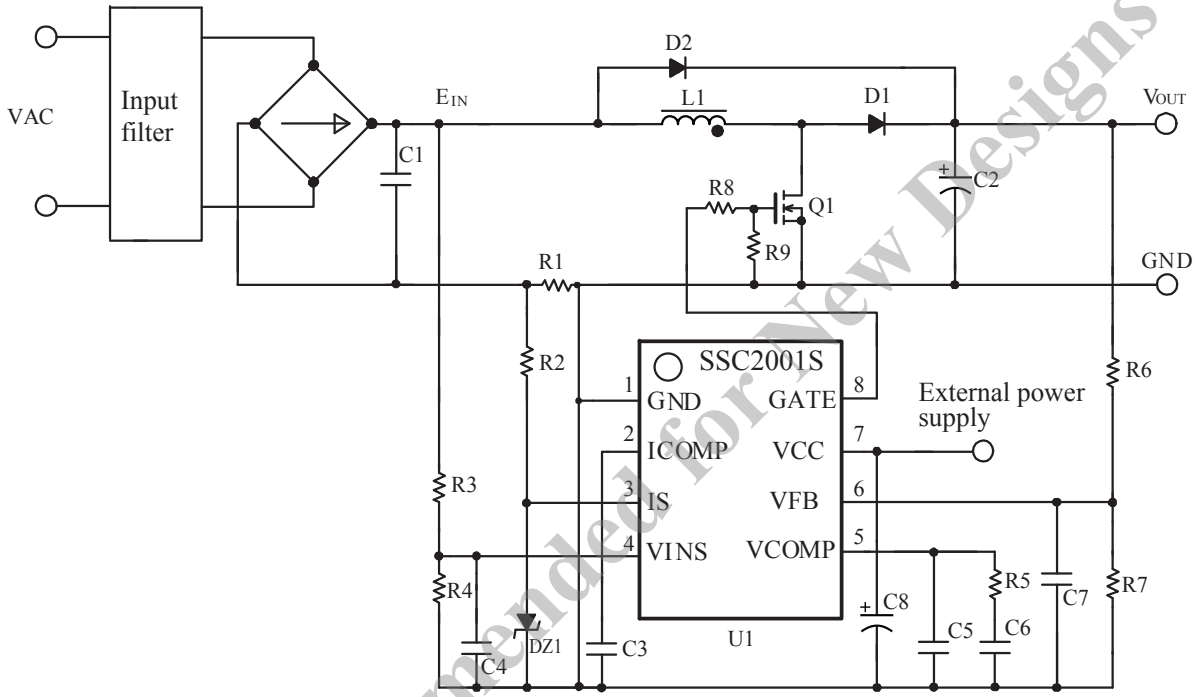
Continued on the next page…

Electrical Characteristics of Control Part (continued) Unless specifically noted, T_A is 25°C, V_{CC} = 15 V

Characteristic	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Unit
Voltage Loop (continued)							
VFB Pin High Speed Load Response Operation Enable Voltage*	$V_{FB(HSR)ENABLE}$		6 – 1	–	3.4	–	V
VFB Pin High Speed Load Response Operation Start Voltage	$V_{FB(HSR)ACTIVE}$		6 – 1	3.24	3.325	3.41	V
VCOMP Pin High Speed Load Response Source Current	$I_{VCOMP(SOHSR)}$		5 – 1	−127	−100	−72	µA
VFB Pin Input Bias Current	$I_{FB(BIAS)}$		6 – 1	–	–	1	µA
VCOMP Pin Output Open Loop Detection Threshold Voltage	$V_{VCOMP(OLD)}$	V_{FB} = 0.5 V	5 – 1	0.60	1.03	1.40	V
Drive Circuit							
GATE Pin Voltage (Low)	$V_{GATE(L)}$	I_{GATE} = −20 mA	8 – 1	–	–	0.4	V
GATE Pin Voltage (High)	$V_{GATE(H)}$	V_{CC} = 11 V	8 – 1	–	10.5	–	V
GATE Pin Rise Time	t_r		8 – 1	–	100	–	ns
GATE Pin Fall Time	t_f		8 – 1	–	50	–	ns
GATE Pin Peak Source Current*	$I_{GATE(SO)}$		8 – 1	–	−0.5	–	A
GATE Pin Peak Sink Current*	$I_{GATE(SK)}$		8 – 1	–	1.0	–	A
Thermal Resistance from Junction to Frame	$R_{\theta J-F}$	The frame temperature, T_F, is specified by using the temperature at the base of pin 1.	–	–	65	85	°C /W

*Determined by design, not tested in production.

Typical Application Circuit



Functional Description

With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

Startup Operation

Figure 1 shows the VCC pin peripheral circuit. The VCC pin is the control circuit power supply input to supply voltage from the external power supply.

As shown in figure 2, when VCC pin voltage rises to the operation start voltage, $V_{CC\,(ON)}$, of 11.3 V (typ), the control circuit starts operation.

When V_{CC} drops to the operation stop voltage, $V_{CC(OFF)}$, of 10.3 V (typ), the control circuit stops operation by the UVLO (undervoltage lockout) circuit, and reverts to the state before startup.

The control voltage range of the VCC pin is wide: from $V_{CC(OFF)}$ of 11.1 V (max) to the maximum rating of 30 V (max). This permits a very wide value range for the external power supply voltage.

When the distance between the IC and the electrolytic capacitor C8 is long, a film capacitor C_f (approximately 0.1 μF) should be added between the VCC pin and the GND pin.

After the input voltage at startup of the power supply meets the following conditions, and the VCC pin voltage reaches $V_{CC\,(ON)}$, the soft start function starts operation (as described in the Soft Start Function section):

- VINS pin voltage > Input Undervoltage Protection High Threshold Voltage, $V_{INS(H)}$ = 1.0 V (typ) (refer the Brown-In/Brown-Out Function section)
- VFB pin voltage > Output open loop detection voltage $V_{FB(OLD)}$ = 0.55 V (typ); $V_{FB(OLD)}$ = 0.55 V (typ) is equivalent to 16% of the error amplifier reference voltage $V_{FB(REF)}$ = 3.5 V (typ) (refer to the Output Open Loop Detection (OLD) section)

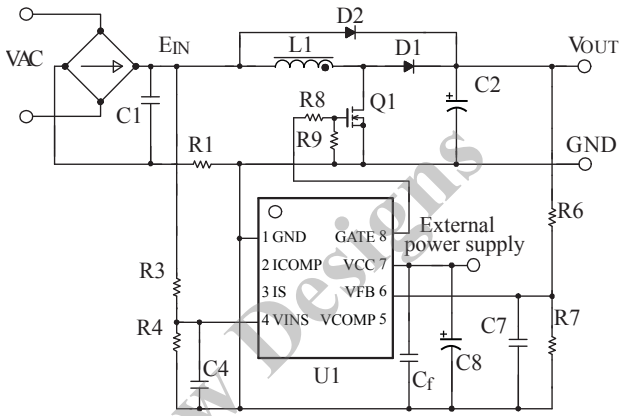


Figure 1. VCC pin peripheral circuit

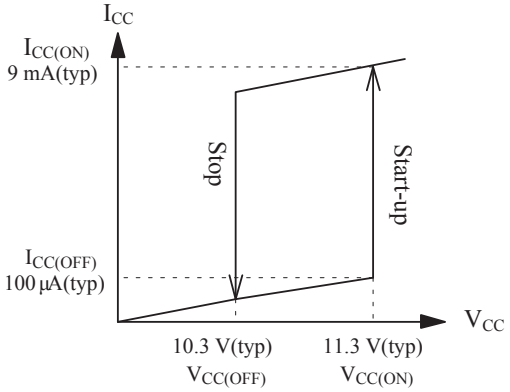


Figure 2. V_{CC} versus I_{CC}

Soft Start Function

When the input voltage meets the power supply startup conditions (refer to the Startup Operation section) and the VCC pin voltage reaches the $V_{CC(ON)}$ voltage, the power supply enters soft start operation.

During soft start, the VCOMP pin is charged by the error amplifier maximum source current $I_{VCOMP(SO)}$ = –30 µA (typ) until the VFB pin voltage becomes approximately 3 V, which is approximately 85% of output voltage setting, and then power is gradually increased to reduce the stress on component parts.

Continuous Conduction Mode (CCM) Operation

When the inductor current of the PFC circuit is in a continuous state, continuous conduction mode (CCM) operation is occurring. In CCM, the peak inductor current becomes low compared to the peak during discontinuous conduction mode (DCM), at the same output power (refer to figures 3 and 4). This allows a reduction in the rated current of the boosting power MOSFET and a decrease of loss to $R_{DS(ON)}$. This characteristic is suitable for high output power.

The continuity of inductor current depends on the value of inductance. During light loads, the operation is in DCM, but the requirement of the class D of IEC1000-3-2 for harmonic currents can be met.

By means of CCM in the operation of the IC series, the usual requirement for a multiplier to transform the input current into a sinusoidal waveform, as well as the related components for the detection of the input voltage, are no more required. This results in a reduction of external parts and simple circuit configurations.

For the off duty cycle, D_{OFF}, of the booster system, the input voltage, V_{IN}, and the output voltage, V_{OUT}, have the relationship of $D_{OFF} = V_{IN} / V_{OUT}$ and so the off-time is proportional to V_{IN}.

The IC generates a sinusoidal waveform for input current and constant output voltage, by means of duty cycle control, which combines current control and voltage control.

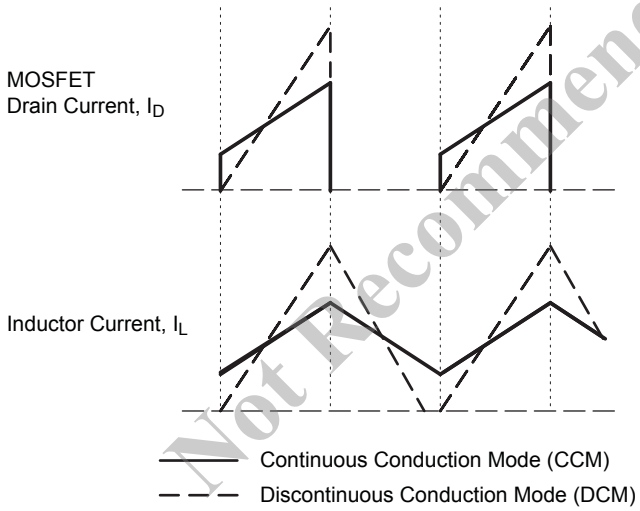


Figure 3. Current waveforms in continuous and discontinuous conduction modes

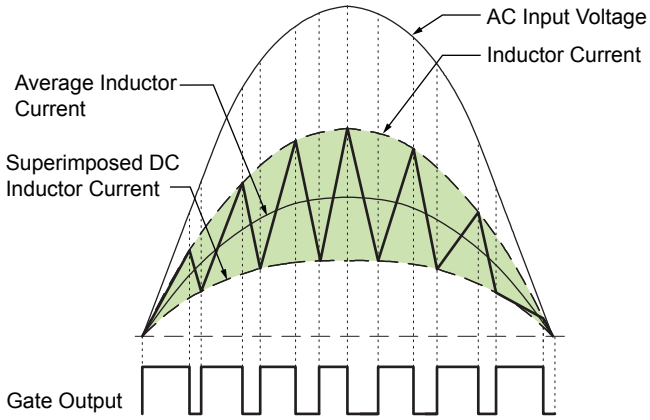


Figure 4. Inductor current in continuous conduction mode

Current Control (PFC Control)

Figure 5 shows a typical peripheral circuit for the IC. The inductor current, I_L, is detected at the detection resistor, R1, and input into the IS pin to be averaged at capacitor C3 (on the ICOMP pin) via the current amplifier in the IC so that the ICOMP pin voltage is produced in proportion to the inductor average current.

As shown in figure 6, the input current is controlled to be sinusoidal by comparing the ICOMP pin voltage with the waveform of a ramp generator in the IC. In standby mode or at the operation of a protection circuit, the ICOMP pin voltage is clamped at 4 V (typ) in the IC.

The C3 value has a filtering effect on the switching frequency and the ripple voltage of the inductor current. I_L. The time constant should be set so as to be subjected to the AC mains frequency.

The reference value of C3 is from 1 to 22 nF, and it should be adjusted so that the AC input current becomes sinusoidal, while varying loads in actual operation in the application.

Voltage Control (Output Constant Voltage Control)

The VFB pin voltage, which is the value of the output voltage, V_{OUT}, divided by R6 and R7 in figure 5, is compared to the reference voltage, $V_{FB(REF)}$ = 3.5 V (typ) by the error amplifier in the IC. This result is output to the VCOMP pin. The VCOMP pin voltage, which is added compensation values by C5, C6, and R5, adjusts the slope of the ramp waveform shown in figure 6, so that V_{OUT} is controlled constant.

When V_{OUT} decreases due to increased load, the VCOMP pin voltage is increased, making the slope of the ramp waveform steeper, and the output power is increased by raising the duty cycle.

In order to boost the input voltage at the AC mains frequency, voltage control is generally activated in response to 20 Hz or lower against AC mains frequency.

The reference value of R6 is several hundred kilohms to several megohms. Because of high voltage applied and high resistance value, it is recommended to select a resistor designed against electromigration or use a combination of resistors for that.

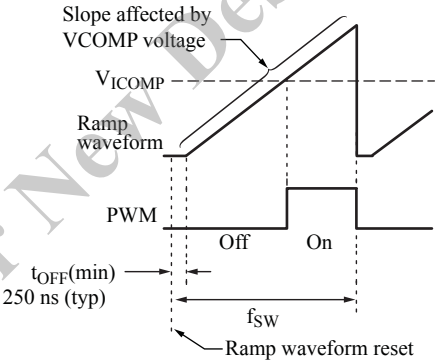


Figure 6. Internal ramp function waveform

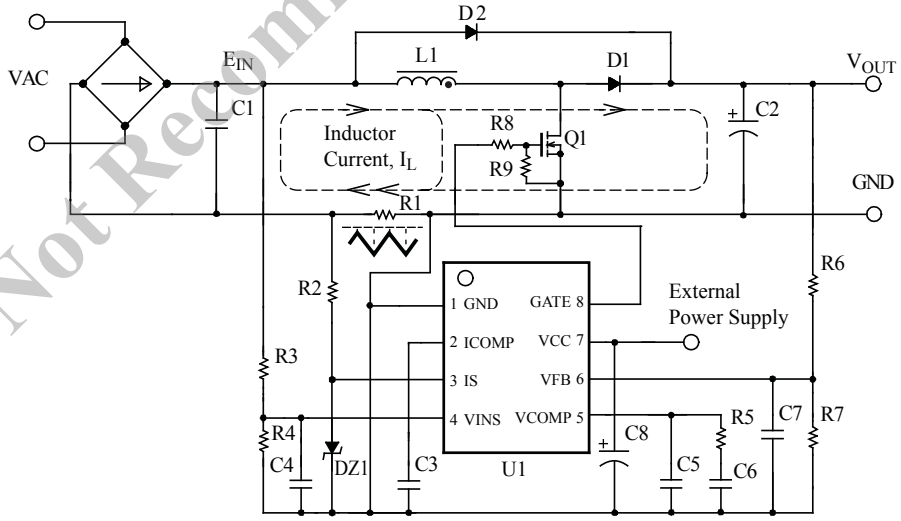


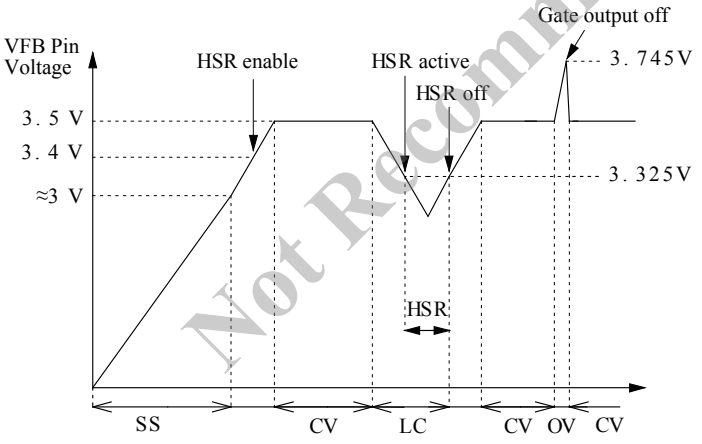
Figure 5. IC peripheral circuits

The reference value of C7 is from 0.047 to 0.1 µF for high frequency noise reduction. The reference value of C5 is from 0.047 to 0.47 µF, that of C6 is 0.47 to 10 µF, and that of R5 is 10 to 47 kΩ. The values should be adjusted under actual operation in the application in order to decrease ripple on the output voltage, V_{OUT}, waveform.

High Speed Load Response (HSR)

Because the AC mains input voltage and frequency are used for the PFC of the boost system, voltage control is activated in response to low mains frequency, and as a result the dynamic load response is slow and a decrease of output voltage, V_{OUT}, is likely to occur. In order to suppress the variation in V_{OUT} at the time of dynamic load conditions, the high speed load response function (HSR) is built in to the IC.

As shown in figure 7, the high speed load response function (HSR) is enabled when the VFB pin voltage exceeds the high speed load response operation enabling voltage, $V_{FB(HSR)ENABLE}$ = 3.4 V (typ). Later, when V_{OUT} decreases due to dynamic load response below the high speed load response operation start voltage, $V_{FB(HSR)ACTIVE}$ = 3.325 V (typ), the HSR becomes active and the VCOMP pin is charged by the high speed load response source current $I_{VCOMP(SOHSR)}$ = –100 µA (typ) until the VFB pin voltage increases to $V_{FB(HSR)ACTIVE}$. This increases the output power and suppresses the decrease of V_{OUT}. $V_{FB(HSR)ACTIVE}$ = 3.325 V (typ) is 95% of the error amplifier reference voltage $V_{FB(REF)}$ = 3.5 V (typ) set by the output voltage, V_{OUT}.



CV – Steady operation period
HSR – High speed load response operation period
LC – Dynamic load variation period
OV – Overvoltage operation period
SS – Soft start period

Figure 7. VFB pin voltage

Frequency Modulation

The built-in frequency modulation function references an internally generated fixed operation frequency, f_{OSC} = 65 kHz (typ). It superimposes a variable frequency which modulates at a rate based on the output duty cycle.

The modulation frequency is low when the duty cycle is large (input voltage is low), and the modulation frequency is high when the duty cycle is small (input voltage is high). The second harmonic frequency after modulation keeps less than 150 kHz.

Gate Drive

The peak source current /peak sink current of the GATE pin are set at –0.5 A (typ) / 1.0 A (typ), and the low voltage /high voltage are set at 0.4 V (max) / 10.5 V (typ) for directly driving the power MOSFET.

Peripheral component values of the GATE pin in figure 8 are affected by the printed circuit board trace layout and the power MOSFET capacitance, which should be adjusted under actual operation of the application.

R8 is adjusted to decrease ringing of GATE pin voltage and EMI noise. The reference value of R8 is several ohms to several dozen ohms.

R9 is used to prevent malfunctions due to steep dv / dt at turn-off of the power MOSFET, and the resistor is connected near the MOSFET, between the gate and source. The reference value of R9 is from 10 to 100 kΩ.

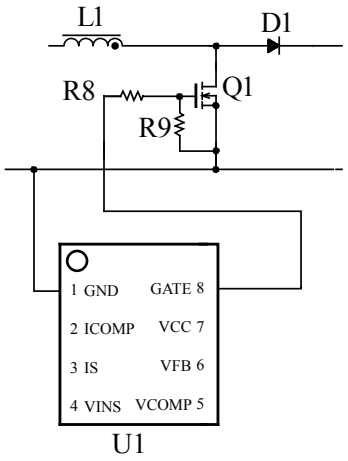


Figure 8. GATE pin peripheral circuit

Protection Functions

Brown-In / Brown-Out

The brown-in/brown-out function prevents switching operation while input voltage is low. This protects against exceeding input current ratings and overheating the IC and the power supply.

As shown in figure 1, the VINS pin voltage is the value of the input voltage V_{IN} divided by R3 and R4. When the VINS pin voltage is at the input undervoltage protection high threshold voltage, $V_{INS(H)}$ =1.0V (typ), or more, the control circuit is allowed to operate. When the VINS pin voltage is at the input undervoltage protection low threshold voltage, $V_{INS(L)}$ = 0.55 V (typ), or less, the control circuit stops switching oscillation, and the IC enters standby mode.

R3 is usually several megohms. Because of high voltage applied and high resistance value, it is recommended to select a resistor designed against electromigration or a combination of resistors for that. C4 is used to decrease the ripple on the detected voltage and to set the delay time, and the reference value is from 0.047 to 1 µF.

If using remote on/off control of the PFC function, to remotely implement the off state, the voltage at the VINS pin should be $V_{INS(L)}$ or less. It should be noted that during the previous remote-off control, power consumption occurs by $I_{CC(STANDBY)}$ = 4 mA (typ). In order to minimize power consumption during remote-off, the following methods are recommended: to turn off the external power supply on the VCC pin, or turn off an external switch inserted on power source line to the VCC pin.

Overcurrent Protection (OCP)

As shown in figure 9, the inductor current, I_L, is detected at the detection resistor R1 and input into the current amplifier in the IC via the IS pin. The overcurrent protection operation (OCP) has the following two states:

1. IS pin overcurrent protection (low), $V_{IS(OCPL)}$

This is the first level of OCP. When the IS pin voltage is at the overcurrent protection low threshold voltage, $V_{IS(OCPL)}$ = –0.5 V (typ), or less, the duty cycle is reduced at the next cycle to restrict the input power.

The value of detection resistor R1 is adjusted in a manner that the IS pin does not go below $V_{IS(OCPL)}$ at the lower limit of input voltage and peak load. The value of R2 is 220 Ω resistance, to maintain the IS pin current within ±1 mA during surges such as in-rush current. DZ1 is 4.7 V Zener diode connected for protection against any overvoltage applied.

2. IS pin overcurrent protection (high), $V_{IS(OCPH)}$

This is the second level of OCP. When the IS pin voltage is at the overcurrent protection high threshold voltage, $V_{IS(OCPH)}$ = –0.75 V (typ), or less, the gate output is turned off using pulse-by-pulse basis. When the cause of the overcurrent is removed, the IC returns to normal operation automatically.

In order to prevent malfunction due to noise, a leading edge blanking period of 300 ns is built in.

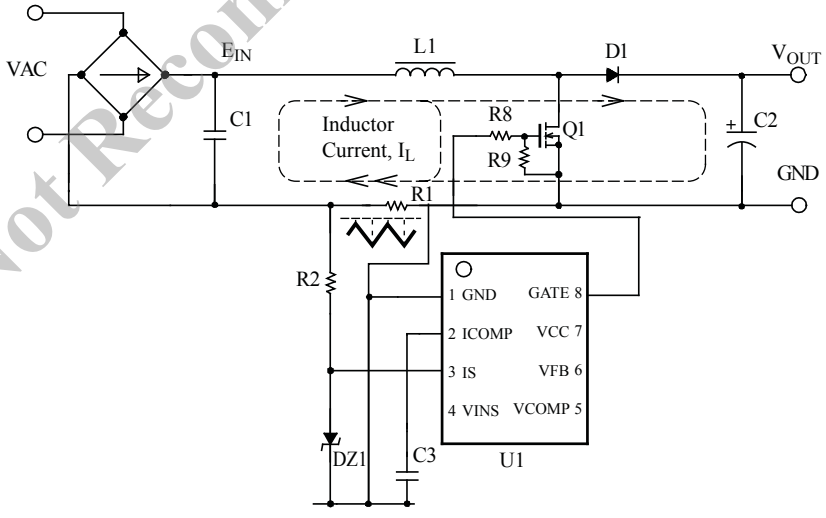


Figure 9. IS pin peripheral circuit

Output Overvoltage Protection (OVP)

When the VFB pin voltage exceeds the output overvoltage protection threshold voltage, $V_{FB(OVP)}$ = 3.745 V (typ), the gate output is turned off using pulse-by-pulse basis. When the cause of the overvoltage is removed, the IC returns to normal operation automatically. $V_{FB(OVP)}$ = 3.745 V (typ) is equivalent to 107% of the error amplifier reference voltage $V_{FB(REF)}$ = 3.5 V (typ) for output voltage V_{OUT} setting.

Output Open Loop Detection (OLD)

As a protection against open loop of the output voltage, when the VFB pin voltage is at the output open loop detection threshold voltage, $V_{FB(OLD)}$ = 0.55V (typ), or less, the control circuit stops switching oscillation, and the IC enters standby mode. $V_{FB(OLD)}$ = 0.55 V (typ) is equivalent to 16% of the error amplifier reference voltage, $V_{FB(REF)}$ = 3.5 V (typ) for output voltage V_{OUT} setting. When the cause of the open loop is removed, the IC returns to normal operation automatically.

When this protection function is activated, the VCOMP pin is clamped to 1.03 V (typ) in the IC.

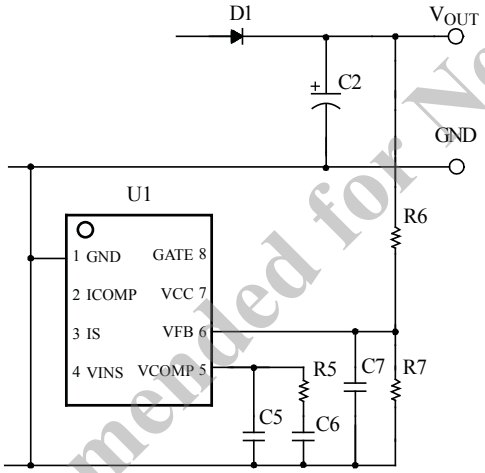


Figure 10. VFB pin peripheral circuit

Design Notes

Inductor Design Parameters

The following abbreviations are used in this description:

P_{IN} – PFC input power (W)

P_O – PFC output power (W)

η – Efficiency of PFC section (reference value: 0.92)

V_{INRMS} – Input voltage rms (root mean square) value (V)

V_{OUT} – Output voltage (V)

I_{INRMS} – Input current rms value (A)

I_{OUT} – Output current (A), P_O / V_{OUT}

D_{ON} – Duty cycle, $(V_{OUT} - \sqrt{2}\, V_{INRMS}) / V_{OUT}$

D_{OFF} – Off-portion of duty cycle, $\sqrt{2}\, V_{INRMS} / V_{OUT}$

f_{SW} – Switching frequency, 65 kHz (typ)

f_{AC} – AC mains frequency (Hz)

r – Ratio of ripple current to maximum peak input current, $I_{LRIPPLE}/I_{INPEAK}(max)$

1. Output voltage V_{OUT} setting for boost converter

Given the relationship of input voltage < output voltage, set the voltage of V_{OUT} higher than the peak value of the AC input voltage by approximately 10 V, according to the following equation:

$$V_{OUT} > \sqrt{2}\, V_{INRMS}(max) + 10 \ (V) \quad (1)$$

2. Inductor current setting

As shown in figure 12, the inductor ripple current is superimposed on the input current, I_{IN}.

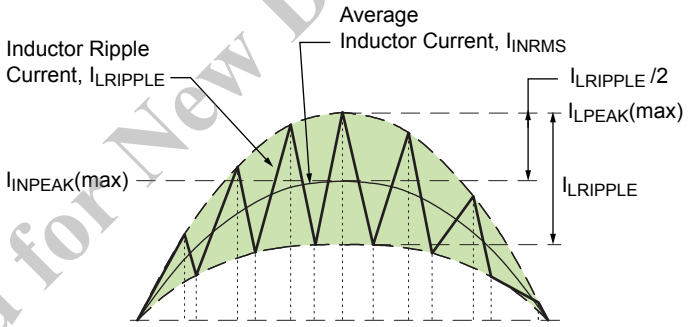


Figure 12. Inductor current

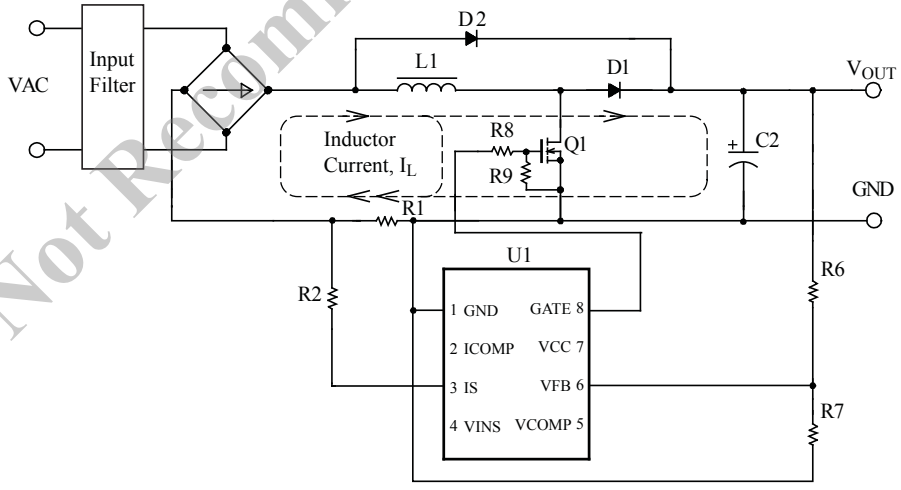


Figure 11. Boost converter circuit

The inductor maximum peak current $I_{LPEAK}(max)$ is obtained by the following steps.

The maximum input current rms value $I_{INRMS}(max)$ is:

$$I_{INRMS}(max) = \frac{P_{OUT}(max)}{\eta \times V_{INRMS}(min)} \quad (A) \qquad (2)$$

The maximum input current peak value $I_{INPEAK}(max)$ is:

$$I_{INPEAK}(max) = \sqrt{2}\ I_{INRMS}(max) \quad (A) \qquad (3)$$

The inductor maximum current peak value $I_{LPEAK}(max)$ is:

$$I_{LPEAK}(max) = I_{INPEAK}(max)\left(1+\frac{r}{2}\right) \quad (A) \qquad (4)$$

In consideration of inductor size and the extent of superimposed ripple current, the ripple ratio, r, is generally 15% to 40%.

3. Inductance value

The inductance can be calculated as:

$$L_1 \geq \frac{V_{INRMS}^2(min) \times (V_{OUT} - \sqrt{2}V_{INRMS}(min))}{r \times f_{SW} \times P_{IN} \times V_{OUT}} \quad (H) \qquad (5)$$

4. Overcurrent detection resistor R1

R1 is obtained from the IS pin overcurrent protection low threshold value $V_{IS(OCPL)}$ and the inductor maximum peak current $I_{LPEAK}(max)$ for the first level of overcurrent protection, as shown in the following equation:

$$R_1 \leq \frac{|V_{IS(OCPL)}|}{I_{LPEAK}(max)} \quad (\Omega) \qquad (6)$$

5. Current limiting value $I_{LOCP}(MAX)$ at overcurrent operation

$I_{LOCP}(max)$ is obtained from IS pin overcurrent protection high threshold value $V_{IS(OCPH)}$ and R1 for the second level of overcurrent protection:

$$I_{LOCP}(max) = \frac{|V_{IS(OCPH)}|}{R_1} \quad (A) \qquad (7)$$

When the IS pin overcurrent protection high threshold is activated, the gate output is turned off using pulse-by-pulse basis. The inductor must be designed to accommodate the power supply operation at overcurrent levels.

6. Output capacitor C2 capacitance

The capacitance, C_O, of C2 is selected using either of the following two methods, whichever yields the larger value:

6a. Ripple voltage

When the ripple voltage of C2 is expressed as peak-to-peak $V_{OUTRIPPLE}$, for example, 10 V_{pp}, the following equation is obtained:

$$C_O \geq \frac{I_{OUT}}{2\pi f_{AC} \times V_{OUTRIPPLE}} \quad (F) \qquad (8)$$

In addition, the voltage of C2 will be:

$$V_{OUT} \pm V_{OUTRIPPLE}/2 \qquad (9)$$

When this voltage exceeds the output overvoltage protection detection voltage ($V_{OUT} \times 1.07$), or falls below the peak value of the input voltage, boost operation is stopped and the input waveform may eventually be distorted. If the distortion is significant, it is necessary to make C_O larger or alter the output voltage setting value (boost voltage value).

6b. Output holding time

When the minimum input voltage of C2 at the output holding time, t_{HOLD}, is expressed as $V_{OUT}(min)$, the following equation is obtained:

$$C_O \geq \frac{2 \times P_{OUT} \times t_{HOLD}}{(V_{OUT}^2 - V_{OUT}^2(min)) \times \eta} \quad (F) \qquad (10)$$

Peripheral Components

Take care to use the proper rating and proper type of components. For circuit symbols please refer to figure 13.

• The electrolytic capacitor C2 should have some margin for ripple current/voltage and temperature rise. High ripple and low impedance type parts for switch-mode power supplies should be used.

• The inductor L1 should have some margin for temperature rise due to core loss and copper loss.

• Because high frequency switching current flows across the current detection resistor R1, the use of a resistor with large internal inductance may cause malfunctions. A resistor with small inductance and high surge tolerance should be used.

• The resistors such as R3 and R6, which have applied high voltage and have high resistance values, should be selected from resistors designed against electromigration or use a combination of resistors for that.

• D2 is a bypass diode which protects D1 against overcurrents, such as in-rush current. Therefore a diode with high surge tolerance is recommended.

• For D1, an ultra high speed diode with short reverse recovery time, t_{rr}, is recommended to decrease noise and loss.

• With respect to the product lineup of rectifier and bypass diodes, please contact our sales division.

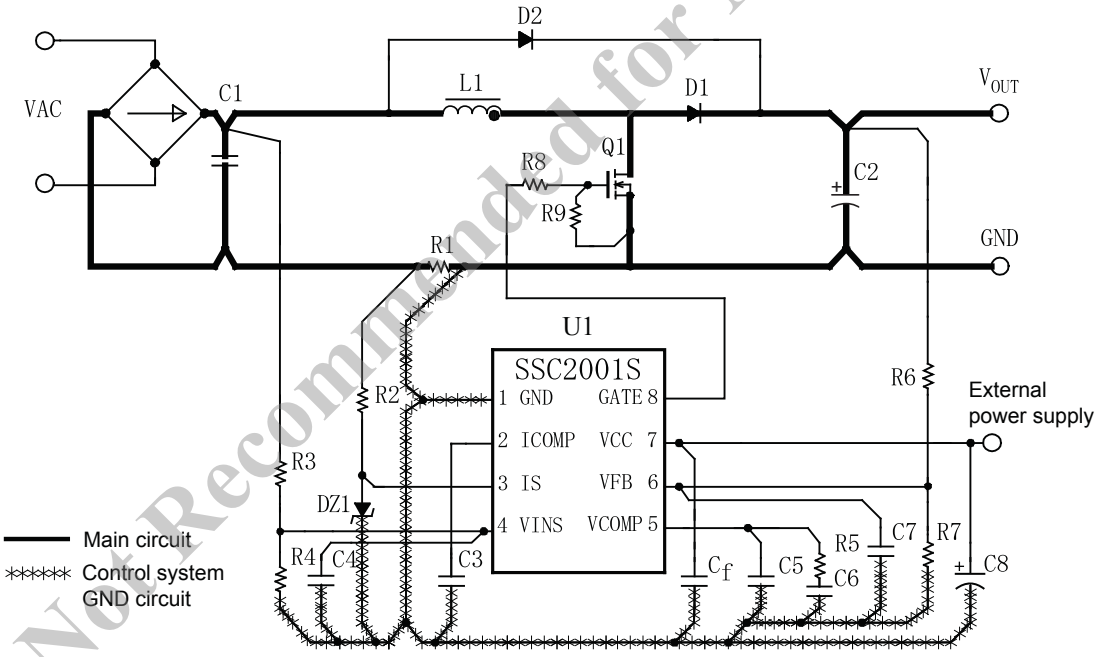


Figure 13. Example of connection of peripheral components

PCB Trace Layout and Component Placement

PCB circuit trace design and component layout significantly affect operation, EMI noise, and power dissipation. Therefore, pay extra attention to these designs. In general, where high frequency current traces form a loop, as shown in figure 14, wide, short traces, and small circuit loops are important to reduce line impedance. In addition, earth ground traces affect radiated EMI noise, and the same measures should be taken into account.

Switch-mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines.

Furthermore, because the incorporated power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it when preparing a thermal design.

Figure 13 shows a circuit layout design example.

• The control circuit traces should not be placed in parallel with the main circuit traces in order not to pick up crosstalk noise.

• In order to minimize the common impedance of the control ground circuit and main circuit ground, the GND pin (pin 1) trace should be connected at the pin of R1 by a dedicated trace, using the shortest trace possible. The R2 trace also should be connected at the pin of R1 in a similar way.

• Peripheral circuit components should be connected to the IC by using the shortest traces possible.

• If the VCC pin and electrolytic capacitor C8 are distant from each other, placing a capacitor (approximately 0.1 to 1.0 μF film capacitor) close to the VCC pin and the GND pin is recommended.

• R9 must be connected to the gate pin and source pin of Q1.

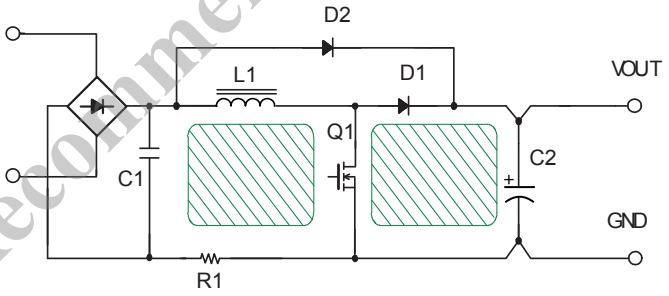


Figure 14. High frequency current loops (hatched areas)

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