Critical Conduction Mode PFC Control IC

SSC2005S

General Description

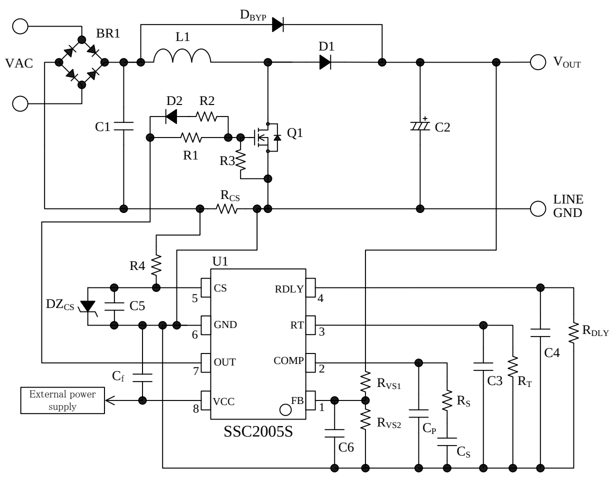
SSC2005S is a Critical Conduction Mode (CRM) control IC for power factor correction (PFC).

Since no input voltage sensing and no auxiliary winding for inductor current detection are required, the IC allows the realization of low standby power and the low number of external components. The product achieves high cost-performance and high efficiency PFC converter system.

Features and Benefits

- Inductor Current Detection
  (No auxiliary winding required)
- Low Standby Power
  (No input voltage sensing required)
- Minimum Off-time Limitation Function to restrict the Rise of Operation Frequency
- High Accuracy Overcurrent detection: −0.60 V ± 5 %
- Protection Functions
  Overcurrent Protection (OCP) -------pulse-by-pulse
  Overvoltage Protection (OVP) ------------ auto restart
  FB Pin Undervoltage Protection (FB_UVP)
  --- auto restart
  Thermal Shutdown Protection with hysteresis (TSD)
  --- auto restart

Typical Application Circuit



Package

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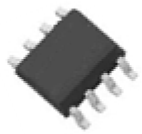
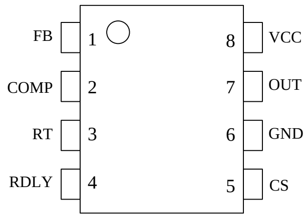




Not to scale

Electrical Characteristics

- VCC pin Absolute Maximum Ratings, V_{CC} = 28 V
- OUT pin source current, $I_{OUT(SRC)}$ = −500 mA
- OUT pin sink current, $I_{OUT(SNK)}$ = 1000 mA

Applications

PFC Circuit up to 200 W of Output Power such as:

- AC/DC Power Supply
- Digital appliances for large size LCD/PDP television and so forth
- OA equipment for Computer, Server, Monitor, and so forth
- Communication facilities

CONTENTS

1. Absolute Maximum Ratings

- For additional details, refer to the datasheet.
- The polarity value for current specifies a sink as "+", and a source as "−", referencing the IC.
- Unless specifically noted Ta = 25 °C

Parameter	Symbol	Conditions	Pins	Rating	Unit	Notes
VCC Pin Voltage	V_{CC}		8 – 6	28	V	
OUT Pin Source Current	$I_{OUT(SRC)}$		7 – 6	−500	mA	
OUT Pin Sink Current	$I_{OUT(SNK)}$		7 – 6	1000	mA	
FB Pin Voltage	V_{FB}		1 – 6	−0.3 to 5	V	
COMP Pin Current	I_{COMP}		2 – 6	−200 to 200	μA	
RT Pin Current	I_{RT}		3 – 6	−500 to 0	μA	
RDLY Pin Current	I_{RDLY}		4 – 6	−500 to 0	μA	
CS Pin Voltage	V_{CS}		5 – 6	−5 to 0.3	V	
Allowable Power Dissipation	P_D		−	0.5	W	
Operating Ambient Temperature	T_{OP}		−	−40 to 110	°C	
Storage Temperature	T_{stg}		−	−40 to 150	°C	
Junction Temperature	T_j		−	150	°C	

2. Recommended Operating Conditions

Recommended operating conditions means the operation conditions maintained normal function shown in electrical characteristics.

Parameter	Symbol	Pins	Min.	Max.	Unit	Notes
VCC Pin Voltage in Operation	$V_{CC(OP)}$	8 – 6	14	26	V	
RT Pin Resistance	R_{RT}	3 – 6	15	47	kΩ	
RDLY Pin Resistance	R_{RDLY}	4 – 6	15	47	kΩ	
Output Voltage – Input Voltage	$V_{OUT} - V_{IN}$	−	20	−	V	

3. Electrical Characteristics

- For additional details, refer to the datasheet.
- The polarity value for current specifies a sink as "+", and a source as "–", referencing the IC.
- Unless specifically noted, Ta = 25 °C, V_{CC} = 14 V, V_{CS} = 0.1 V

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Power Supply Operation							
Operation Start Voltage	$V_{CC(ON)}$		8 – 6	10.5	12.0	13.5	V
Operation Stop Voltage	$V_{CC(OFF)}$		8 – 6	8.2	9.5	11.0	V
Operation Voltage Hysteresis	$V_{CC(HYS)}$		8 – 6	1.4	2.5	3.1	V
Circuit Current in Operation	$I_{CC(ON)}$		8 – 6	2.0	3.1	4.4	mA
Circuit Current in Non-Operation	$I_{CC(OFF)}$	V_{CC} = 9.5 V	8 – 6	40	80	160	µA
Oscillation Operation							
Maximum On-Time	$t_{ON(MAX)}$	V_{FB} = 1.5 V R_{DLY} = 22 kΩ	7 – 6	15	23	33	µs
Minimum Off-Time	$t_{OFF(MIN)}$	R_{DLY} = 22 kΩ	7 – 6	1.8	2.5	3.2	µs
RDLY Pin Voltage	V_{RDLY}		4 – 6	1.3	1.5	1.7	V
RT Pin Voltage	V_{RT}		3 – 6	1.3	1.5	1.7	V
Feedback Control Voltage	V_{FB}		1 – 6	2.46	2.50	2.54	V
Feedback Line Regulation	$V_{FB(LR)}$		1 – 6	−8	1	12	mV
FB Pin Bias Current	I_{FB}		1 – 6	−3.2	−2.0	−1.0	µA
Error Amplifier Transconductance Gain	gm		1 – 6 2 – 6	60	103	150	µS
COMP Pin Sink Current	$I_{COMP(SNK)}$		2 – 6	18	40	72	µA
COMP Pin Source Current	$I_{COMP(SRC)}$		2 – 6	−72	−40	−18	µA
Zero Duty COMP Voltage	$V_{COMP(ZD)}$		2 – 6	0.50	0.65	0.90	V
Restart Time	t_{RS}		−	30	50	80	µs
Drive Output							
Output Voltage (High)	V_{OH}	I_{OUT} = –100 mA	7 – 6	10.0	12.0	13.5	V
Output Voltage (low)	V_{OL}	I_{OUT} = 200 mA	7 – 6	0.40	0.75	1.25	V
Output Rise Time (2)	t_r	C_{OUT} = 1000 pF	7 – 6	−	60	120	ns
Output Fall Time (2)	t_f	C_{OUT} = 1000 pF	7 – 6	−	20	70	ns
Zero Current Detection and Overcurrent Protection Function							
Zero Current Detection Threshold Voltage	$V_{CS(ZCD)}$		5 – 6	−16	−10	−4	mV
Zero Current Detection Delay Time (1)	$t_{DLY(ZCD)}$	R_{DLY} = 22 kΩ	5 – 6	1.00	1.35	1.70	µs
Overcurrent Protection Threshold Voltage	$V_{CS(OCP)}$		5 – 6	−0.63	−0.60	−0.57	V
Overcurrent Protection Delay Time (1)	$t_{DLY(OCP)}$		5 – 6	100	250	400	ns
CS Pin Source Current	I_{CS}		5 – 6	−110	−75	−40	µA

(1) Design assurance item
(2) Shown in Figure 3-1

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
FB Pin Protection Function							
Overvoltage Protection Threshold Voltage	V_{OVP}		1 – 6	1.075 $\times V_{FB}$	1.090 $\times V_{FB}$	1.105 $\times V_{FB}$	V
Overvoltage Protection Hysteresis	$V_{OVP(HYS)}$		1 – 6	55	90	125	mV
Undervoltage Protection Threshold Voltage	V_{UVP}		1 – 6	200	300	400	mV
Undervoltage Protection Hysteresis	$V_{UVP(HYS)}$		1 – 6	80	120	160	mV
Thermal Shutdown Protection							
Thermal Shutdown Threshold (1)	$T_{j(TSD)}$		–	135	150	–	°C
Thermal Shutdown Hysteresis (1)	$T_{j(TSDHYS)}$		–	–	10	–	°C
Thermal Resistance							
Junction to Ambient Resistance (1)	$\theta_{j\text{-}A}$		–	–	–	180	°C/W

(1) Design assurance item

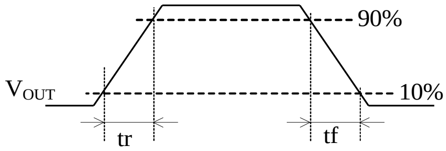
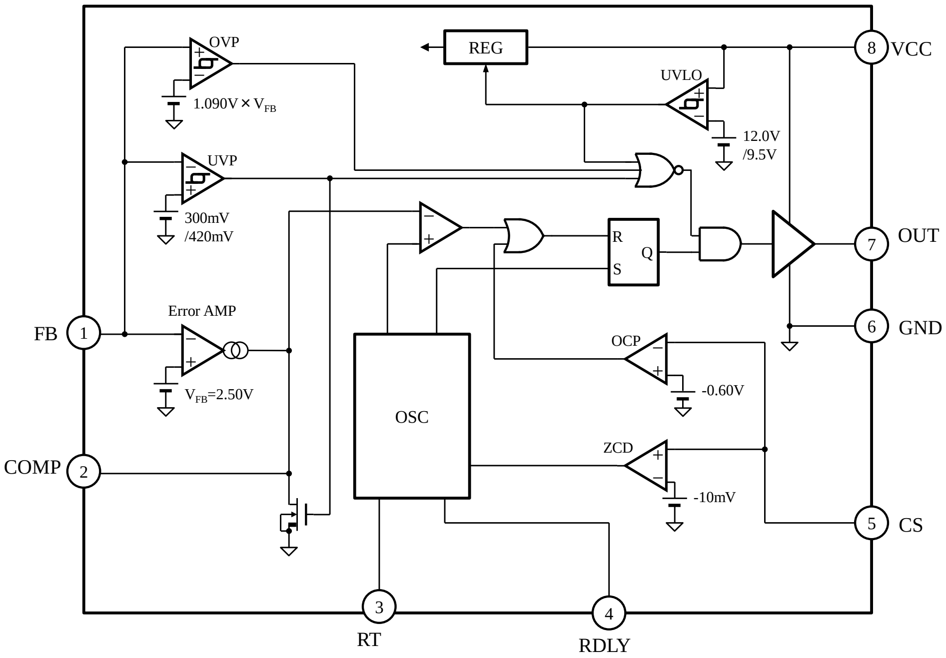
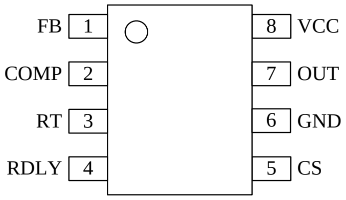


Figure 3-1 Switching time

4. Functional Block Diagram

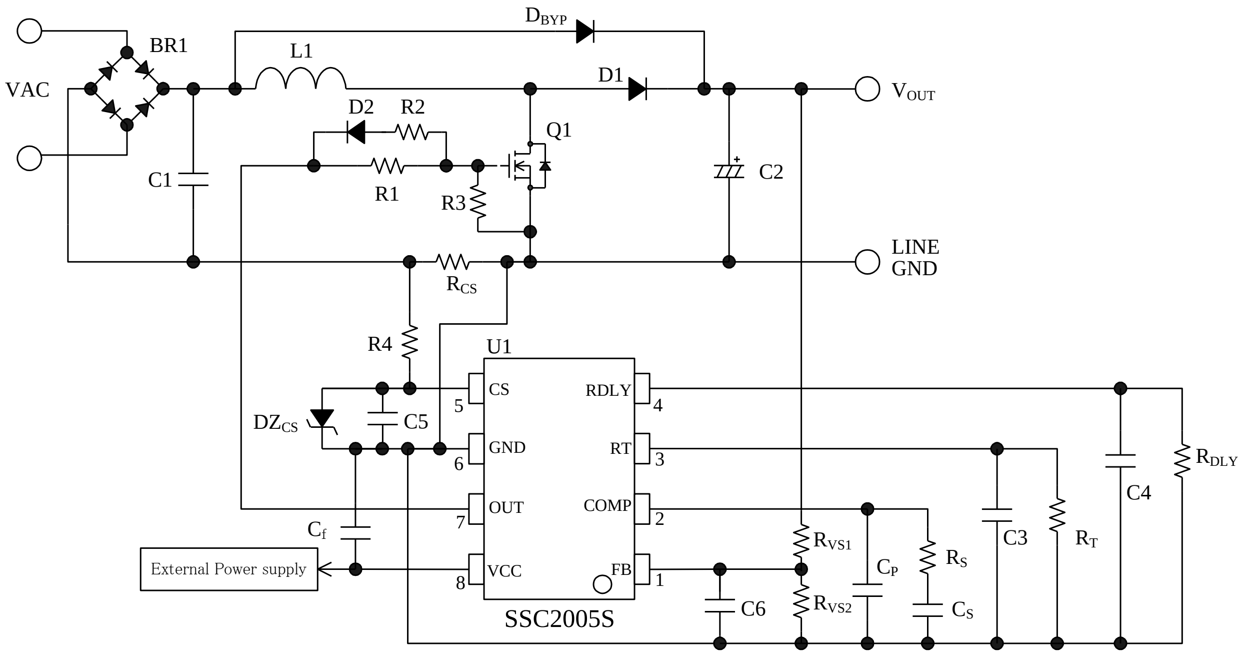


5. Pin Configuration Definitions



Number	Name	Function
1	FB	Feedback signal input, overvoltage protection signal input and FB pin undervoltage protection signal input
2	COMP	Phase compensation
3	RT	Maximum on-time adjustment
4	RDLY	Turn-on delay time adjustment
5	CS	Overcurrent protection signal input and zero current detection signal input
6	GND	Ground
7	OUT	Gate drive output
8	VCC	Power supply input for control circuit

6. Typical Application Circuit



7. Package Outline

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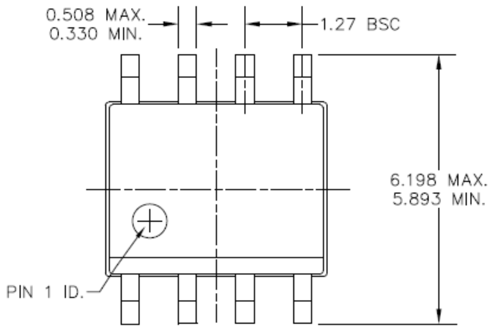
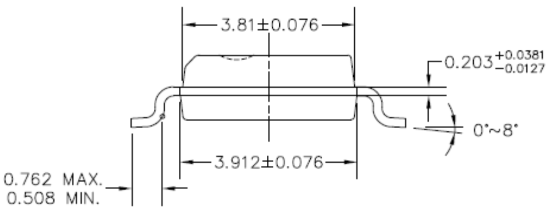
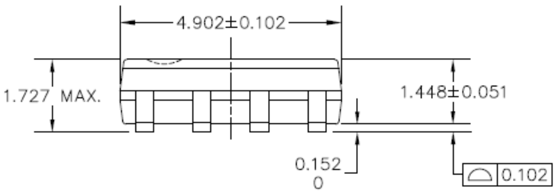
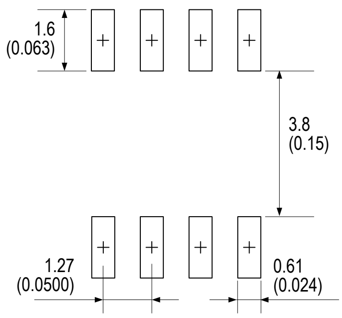




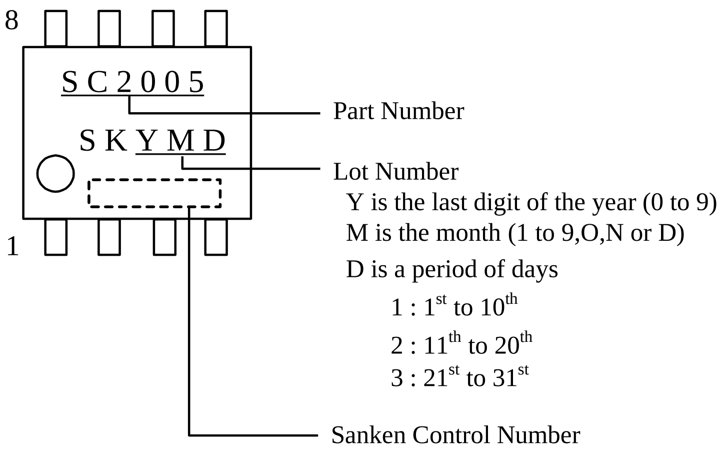




Land Pattern Example (not to scale)

NOTES:
1) All liner dimensions are in millimeters
2) Pb-free. Device composition compliant with the RoHS directive.

8. Marking Diagram



9. Operational Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

9.1 Critical Conduction Mode: CRM

Figure 9-1 and Figure 9-2 show the PFC circuit and CRM operation waveform. The IC performs the on/off operation of switching device Q1 in critical mode (the inductor current is zero) as shown in Figure 9-1.Thus the low drain current variation di/dt of power MOSFET is accomplished. Also, adjusting the turn-on timing at the bottom point of V_{DS} free oscillation waveform (quasi-resonant operation), low noise, low switching loss and high efficiency PFC circuit is realized.

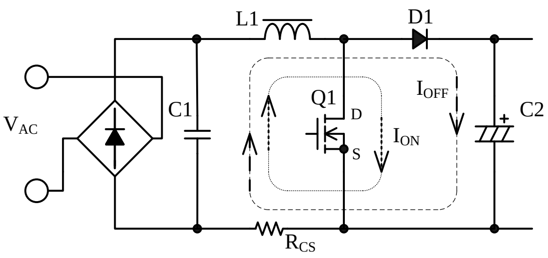


Figure 9-1 PFC circuit

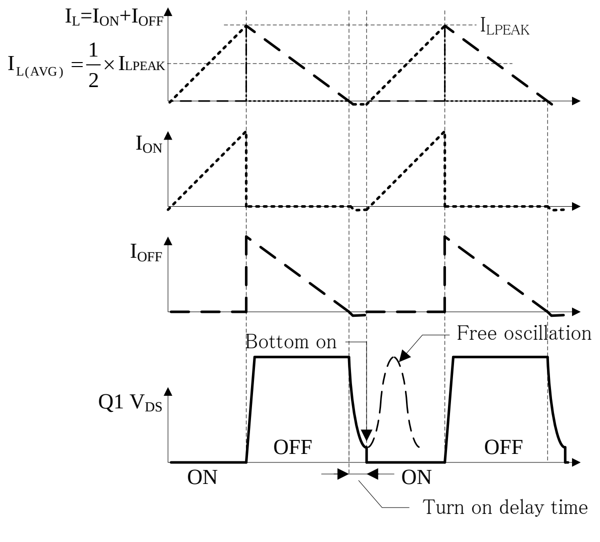


Figure 9-2 CRM operation and bottom on operation

Figure 9-3 shows the internal CRM control circuit.

The power MOSFET Q1 starts switching operation by self-oscillation.

The control of on-time is as follows: the detection voltage R_{VS2} is compared with the reference voltage V_{FB} = 2.50 V by using error amplifier (Error AMP) connected to FB pin. The output of the Error AMP is averaged and phase compensated. This signal V_{COMP} is compared with the ramp signal V_{OSC} to achieve on-time control. The ON time becomes almost constant in commercial cycle by setting V_{COMP} respond to below 20 Hz (Figure 9-4). This is achieved by tuning the capacitor connected to COMP pin.

The off-time and the bottom on timing of V_{DS} are set by both zero current detection of drain current and the delay time configured by RDLY pin resistance. Thus simple PFC circuit with inductor having no auxiliary winding is realized.

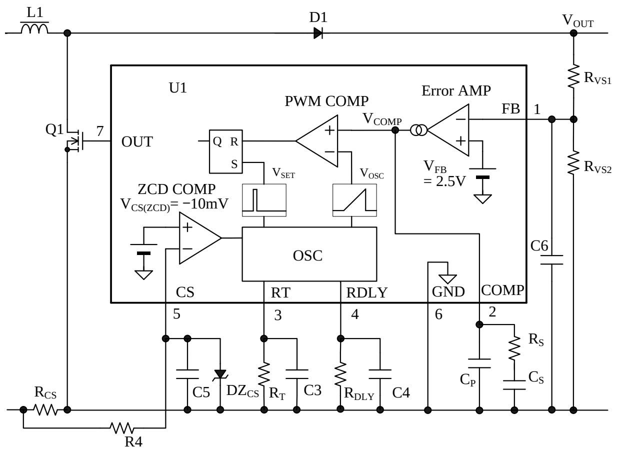


Figure 9-3 CRM control circuit

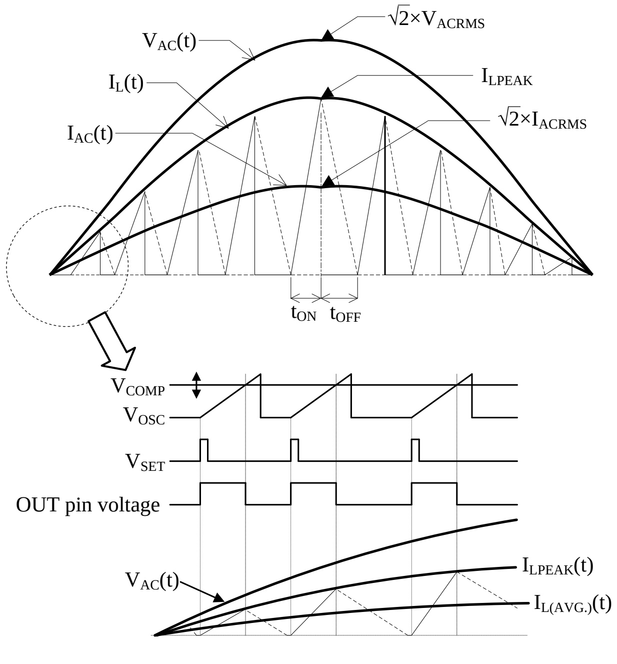


Figure 9-4 CRM operation waveforms

The off duty D_{OFF} of boost converter in CRM mode have the relation of $D_{OFF}(t) = V_{AC}(t)/V_{OUT}$ and is proportional to input voltage, where $V_{AC}(t)$ is the input voltage of AC line as a function of time.

As a result of aforementioned control shown in Figure 9-4, the peak current I_{LPEAK} of the inductance current I_L becomes sinusoidal. Since the averaged input current become similar to AC input voltage waveform by Low Pass Filter at input stage, high power factor is achieved.

9.2 Startup Operation

Figure 9-5 shows the VCC pin peripheral circuit.

VCC pin is a control circuit power supply input. The voltage is supplied by using external power supply. As shown in Figure 9-6, when VCC pin voltage rises to the Operation Start Voltage $V_{CC(ON)}$ = 12.0 V, the control circuit starts operation.

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.5 V, the control circuit stops operation by Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

Since the COMP pin voltage rises from zero during startup period, the V_{COMP} signal shown in Figure 9-3gradually rises from low voltage. The on-width gradually increased to restrict the rise of output power by the Softstart Function. Thus the stress of the peripheral component is reduced.

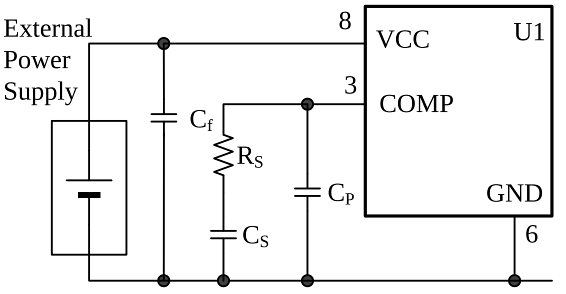


Figure 9-5 VCC pin peripheral circuit

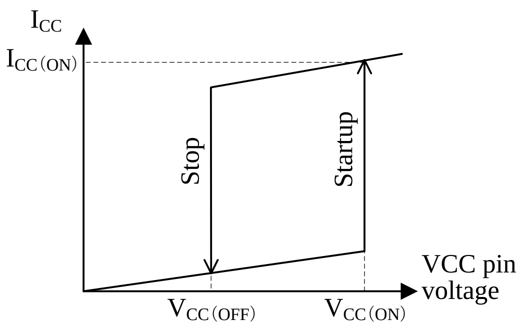


Figure 9-6 Relationship between VCC pin voltage and I_{CC}

9.3 Restart Circuit

Since the IC is self-oscillation type, when the duration of off-state of OUT pin voltage exceeds the Restart Time t_{RS} = 50 μs or more, OUT pin outputs on-signal as a trigger of switching operation and switching operation starts. At startup and intermittent oscillation period at light load, the restart circuit is activated and the switching operation is stabilized.

Since t_{RS} = 50 μs corresponds to the operational frequency of 20 kHz, the minimum frequency should be set to higher than 20 kHz at the inductance value design. In normal operation, the zero current detection circuit determines off-time.

9.4 Maximum On-time setting

In order to reduce audible noise of transformer at transient state, the IC has the Maximun on-time, $t_{ON(MAX)}$. This $t_{ON(MAX)}$ is adjusted by the resistance R_T which is connected to RT pin.

Figure 9-7 shows the relation between R_T value and $t_{ON(MAX}$ in IC design. The $t_{ON(MAX)}$ is made into a larger value than $t_{ON(SET)MAX}$ that is result of Equation (9) in Section 10.1 Inductor.

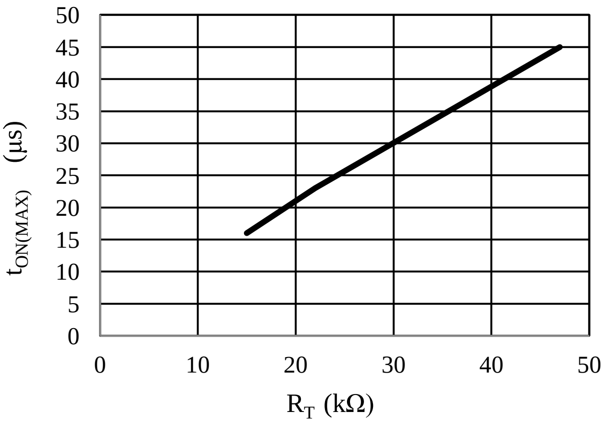


Figure 9-7 Relationship between R_T value and .$t_{ON(MAX)}$ value (IC design)

9.5 Zero Current Detection

Figure 9-8 shows the peripheral circuit of RDLY pin and CS pin. Figure 9-9 shows the waveform of each pin.

The off-time and the bottom on timing of V_{DS} are set by both zero current detection of inductor current, I_L and the delay time. Thus simple PFC circuit with inductor having no auxiliary winding is realized.

The zero current detection signal of I_L is detected by R_{CS} and it is inputted to CS pin as shown in Figure 9-8. While the power MOSFET is in OFF state, the CS pin voltage decrease to the absolute value of Zero Current Detection Threshold Voltage, $V_{CS(ZCD)} = -10$ mV, or less, the OUT pin outputs ON signal after turn-on delay time, t_{DLY}.

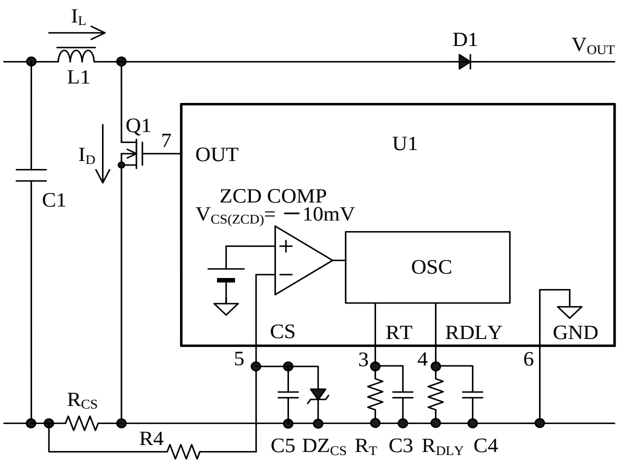


Figure 9-8 The peripheral circuit of RDLY pin and CS pin

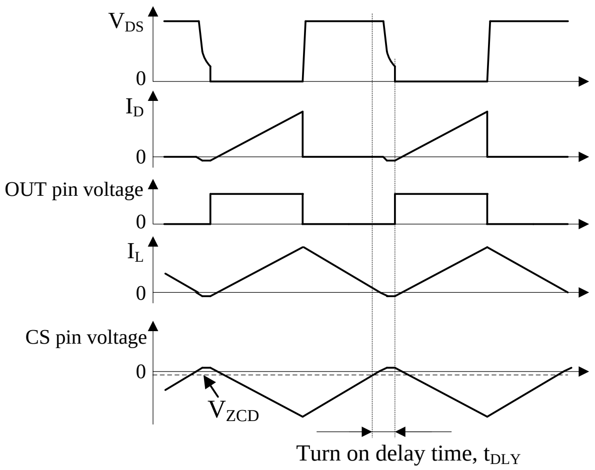


Figure 9-9 Zero current detection waveform

The value of t_{DLY} is determined by the value of the resistor, R_{DLY}, connected to RDLY pin.

Figure 9-10 shows relationship between R_{DLY} value and .t_{DLY} value (IC design). As shown in Figure 9-11, the value of R_{DLY} adjusts the turn-on timing to the bottom point of V_{DS} free oscillation waveform on actual operation in the application.

Adjusting the output timing of the on signal to the bottom point of V_{DS} free oscillation waveform (quasi-resonant operation), low noise, low switching loss and high efficiency PFC circuit is realized.

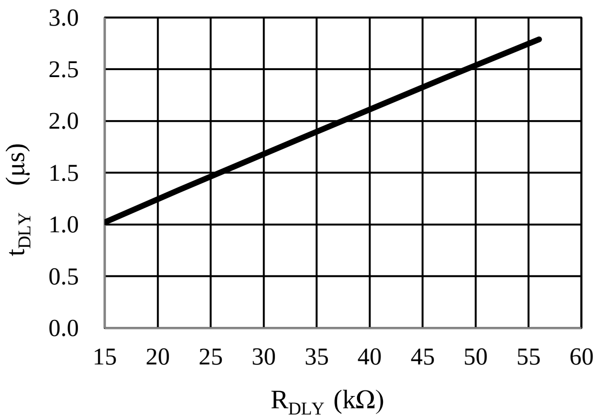


Figure 9-10 Relationship between R_{DLY} value and .t_{DLY} value (IC design)

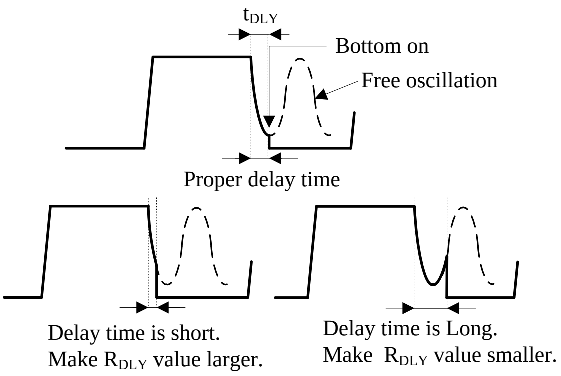


Figure 9-11 Turn-on timing of V_{DS}

9.6 Minimum Off-time Limit Function

In order to prevent the rise of operation frequency at light load, the IC have the Minimum Off-Time $t_{OFF(MIN)} = 2.5$ µs.

If this Minimum Off-Time is shorter than the freewheeling time of inductor, the IC operates in discontinuous condition mode (DCM).

9.7 Overvoltage Protection (OVP) Function

Figure 9-12 shows the waveforms of Overvoltage Protection operation. When the FB pin voltage increase to Overvoltage Protection Threshold Voltage, V_{OVP}, OUT pin voltage become Low immediately and the switching operation stops. As a result, the rise of output voltage is prevented. V_{OVP} is 1.090 times the Feedback Control Voltage, V_{FB} = 2.50 V. When the cause of the overvoltage is removed and FB pin voltage decreases to $V_{OVP} - V_{OVP(HYS)}$, the switching operation restarts.

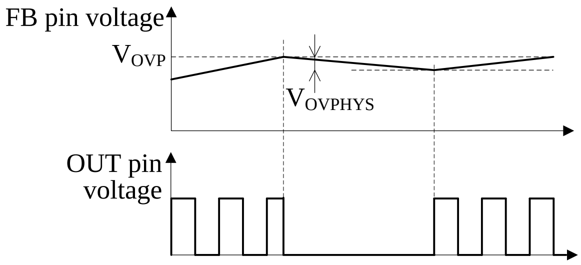


Figure 9-12 Overvoltage protection waveform

9.8 FB pin Under Voltage Protection (FB_UVP) Function

FB pin Under Voltage Protection (FB_UVP) is activated when the FB pin voltage is decreased by the malfunctions in feedback loop such as the open of R_{VS1} or the short of R_{VS2}.

Figure 9-13 shows the FB pin peripheral circuit and internal circuit. When the FB pin voltage is decreased to V_{UVP} = 300 mV or less, the OUT pin output is turned-off immediately and switching operation stops. This prevents the rise of output voltage. When the cause of malfunction is removed and the FB pin voltage rises to $V_{UVP} + V_{UVP(HYS)}$, the switching operation restarts.

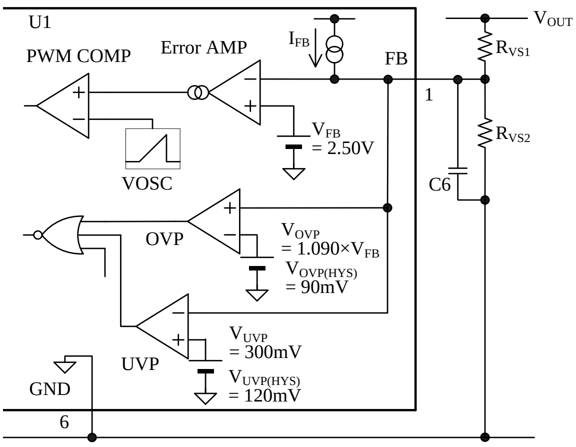


Figure 9-13 The FB pin peripheral circuit and internal circuit.

In case the FB pin is open the FB pin voltage is increase and Overvoltage Protection (OVP) Function is activated as described in Section 0.

When the cause of malfunction is removed and the IC becomes nomal control, the switching operation rstarts.

9.9 Overcurrent Protection (OCP) Function

Figure 9-14 shows the CS pin peripheral circuit and internal circuit. The inductor current, I_L is detected by the detection resistor, R_{CS}. The detection voltage, V_{RCS}, is fed into CS pin. The OCP COMP compares the detection voltage, V_{RCS} with Overcurrent Protection Threshold Voltage, $V_{CS(OCP)} = -0.6$ V. When V_{RCS} increases to absolute value of $V_{CS(OCP)}$ or more, the OUT pin output is turned-off by pulse-by-pulse.

As shown in Figure 9-14, the CS pin is connected to capacitor-resistor filter (R4 and C5) and zener diode, DZ_{CS}, for CS pin overvoltage protection.

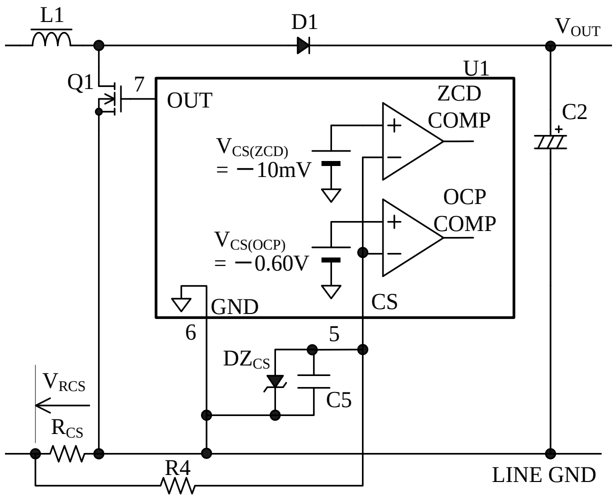


Figure 9-14 The CS pin peripheral circuit and internal circuit.

10. Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

Figure 10-1 shows the IC peripheral circuit.

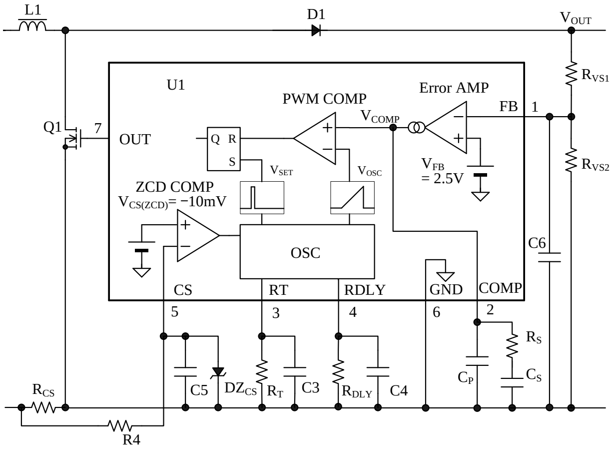


Figure 10-1 The IC peripheral circuit.

- **FB Pin Peripheral Circuit (Output VoltageDetection)**

The output voltage V_{OUT} is set using R_{VS1} and R_{VS2}. It is expressed by the following formula:

$$V_{OUT} = \left(\frac{V_{FB}}{R_{VS2}} + I_{FB} \right) \times R_{VS1} + V_{FB} \qquad (1)$$

Where,

V_{FB} : Feedback reference voltage = 2.50 V

I_{FB} : Bias current = –2 μA

R_{VS1}、R_{VS2} : Combined resistance to set V_{OUT}

Since R_{VS1} have applied high voltage and have high resistance value, R_{VS1} should be selected from resistors designed against electromigration or use a combination of resistors for that.

The value of capacitor C6 between FB pin and GND pin is set approximately 100 pF to 3300 pF, in order to reduce the switching noise.

- **COMP Pin Peripheral Circuit, R_S, C_S, C_P**

Figure 10-1 shows the IC peripheral circuit.

The FB pin voltage is induced into internal Error AMP. The output voltage of the Error AMP is averaged by the COMP pin. The on-time control is achieved by comparing the signal V_{COMP} and the ramp signal V_{OSC}.

C_S and R_S adjust the response speed of changing on-time according to output power.

The typical value of C_S and R_S are 1 μF and 10 kΩ, respectively. When C_S value is too large, the response becomes slow at dynamic variation of output and the output voltage decreases.

Since C_S and R_S affect on the soft-start period at startup, adjustment is necessary in actual operation.

The ripple of output detection signal is averaged by C_P. When the C_P value is too small, the IC operation may become unstable due to the output ripple. The value of capacitor C_P is approximately 0.47 μF.

- **RT Pin Peripheral Circuit, R_T, C3**

R_T shown in Figure 10-1 is for the adjustment of maximum on-time, $t_{ON(MAX)}$.The $t_{ON(MAX)}$ is made into a larger than $t_{ON(SET)MAX}$ value which is the result of Equation (9) in page 13 "Inductor"(see Figure 9-7).

The value of capacitor C3 in parallel with R_T is approximately 0.01 μF, in order to reduce the switching noise.

- **RDLY Pin Peripheral Circuit, R_{DLY}, C4**

R_{DLY} shown in Figure 10-1 is for the adjustment of the turn-on delay time, $t_{DLY,}$ of the Power MOSFET. As shown in Section 0 Zero Current Detection, adjust the value of R_{DLY} and turn-on timing to the bottom point of V_{DS} free oscillation waveform on actual operation in the application. The value of capacitor C4 is approximately 0.01 μF, in order to reduce the switching noise.

- **CS Pin Peripheral Circuit,**

R_{CS} shown in Figure 10-1 is current sensing resistor. R_{CS} is calculated using the following Equation (2), where Overcurrent Protection Threshold Voltage $V_{CS(OCP)}$ is −0.6 V and I_{LP} is calculated using Equation (12).

$$R_{CS} \leq \frac{\left| V_{CS(OCP)} \right|}{I_{LP}} \qquad (2)$$

Both CR filter (R4 and C5) and DZ_{CS}(zenar diode) are connected to CS pin.

CR filter (R4 and C5) prevents IC from responding to the drain current surge at MOSFET turn-on and avoids the unstable operation of the IC.

R4 value of approximately 47 Ω is recommended, since the CS Pin Source Current affects the accuracy of OCP detection (see Section 0).

C5 value is reccommended to be calculated by using following formula in which cut-off frequency of CR filter (C5 and R4) is approximately 1 MHz.

$$C5 = \frac{1}{2 \times \pi \times 1\mathrm{MHz} \times R4} \qquad (3)$$

In case R4 value is 47 Ω, C5 value is approximately 3300 pF.

The absolute voltage of CS pin is −5 V. The CS pin voltage may exceed the absolute value when the

startup current to charge output capacitor, C2, flows R_{CS}. Thus DZ_{CS} is used for the overvoltage protection of the CS pin.
DZ_{CS} value of approximately 3.9 V is recommended. The value should be higher than $V_{CS(OCP)}$ and be lower than CS pin absolute maximum rating of −5 V.

- **OUT Pin Peripheral Circuit (Gate Drive Circuit)**

Figure 10-2 shows the OUT pin peripheral circuit.
The OUT pin is the gate drive output which can drive the external power MOSFET directly.

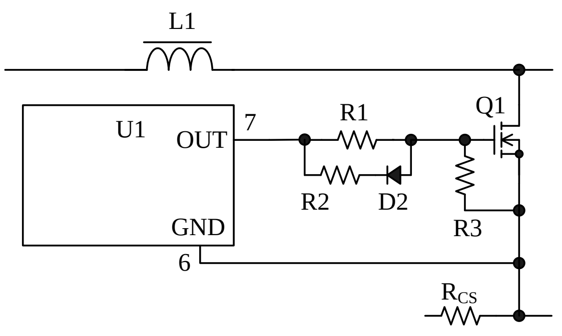


Figure 10-2 the OUT pin peripheral circuit.

The maximum output voltage of OUT pin is the VCC pin voltage. The maximum current is −500 mA for source and 1 A for sink, respectively.
R1 is for source current limiting. Both R2 and D2 are for sink current limiting. The values of these components are adjusted to decrease the ringing of Gate pin voltage and the EMI noise. The reference value is several ohms to several dozen ohms.
R3 is used to prevent malfunctions due to steep dv/dt at turn-off of the power MOSFET, and the resistor is connected near the MOSFET, between the gate and source. The reference value of R3 is from 10 kΩ to 100 kΩ.
R1, R2, D2 and R3 are affected by the printed circuit board trace layout and the power MOSFET capacitance. Thus the optimal values should be adjusted under actual operation of the application.

- **VCC Pin Peripheral Circuit**

Figure 10-3 shows the VCC pin peripheral circuit.

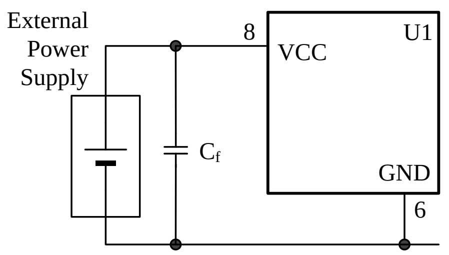


Figure 10-3 VCC pin peripheral circuit

VCC pin is power supply input. VCC pin is supplied from an external power.
When VCC pin and the external power supply are distant from each other, placing a film capacitor C_f between the VCC pin and the GND pin is recommended.
The value of capacitor C_f is set approximately 0.47 μF, in order to reduce the switching noise.

- **Power MOSFET Q1**

Choose a power MOSFET having proper margin of V_{DSS} against output voltage V_{OUT}. The size of heat sink is chosen taking into account some loss by switching and ON resistance of MOSFET. The RMS value of drain current, I_{DRMS} is expressed as follows:

$$I_{DRMS} = \frac{2\times\sqrt{2}\times P_{OUT}}{\eta\times V_{ACRMS(MIN)}} \times \sqrt{\frac{1}{6} - \frac{4\times\sqrt{2}\times V_{ACRMS(MIN)}}{9\times\pi\times V_{OUT}}} \tag{4}$$

The loss $P_{RDS(ON)}$ by on-resistance $R_{DS(ON)}$ of power MOSFET is calculated as follows:

$$P_{RDS(ON)} = \left(I_{DRSM}\right)^2 \times R_{DS(ON)125^\circ C} \tag{5}$$

where,
$V_{ACRMS(MIN)}$: Minimum AC input voltage rms value (V)
P_{OUT} : Output power (W)
η : Efficiency of PFC
$R_{DS(ON)125°C}$: ON resistance of MOSFET at T_{ch} = 125 °C

- **Boost Diode, D_{FW}**

Choose a boost diode having proper margin of a peak reverse voltage V_{RSM} against output voltage V_{OUT}.
A fast recovery diode is recommended to reduce the switching noise and loss. Please ask our staff about our lineup. The size of heat sink is chosen taking into account some loss by V_F and recovery current of boost diode.
The loss of V_F, P_{DFW} is expressed as follows:

$$P_{DFW} = V_F \times I_{OUT} \tag{6}$$

Where,
V_F : Forward voltage of boost diode (V)
I_{OUT} : Out put current (A)

- **Bypass Diode, D_{BYP}**

Bypass diode protects the boost diode from a large current such as an inrush current. A high surge current tolerance diode is recommended. Please ask our staff about our lineup.

- **Output Capacitor, C2**

Apply proper design margin to accommodate the ripple current, the ripple voltage and the temperature

rise. Use of high ripple current and low impedance types, designed for switch-mode power supplies, is recommended, depending on their purposes.
In order to obtain C2 value Co, caalculate both Equation (7) and (8) described in following and select a larger value.

1) Given the C2 ripple voltage $V_{OUTRIPPLE}$ (V_{PP}) (10 V_{PP} for example), C_O is expressed as follows:

$$C_O > \frac{I_{OUT}}{2\times\pi\times f_{LINE}\times V_{OUT(RI)}} \tag{7}$$

where,
f_{LINE} :Line frequency (Hz)
I_{OUT} :Output current (A)

The C2 voltage is expressed as follows:

$$V_{C2} = V_{OUT} \pm \frac{V_{OUT(RI)}}{2}$$

When the output ripple is high, the V_{C2} voltage may reach to Overvoltage Protection voltage, V_{OVP} in near the maximum value of V_{C2}, or input current waveform may be distorted due to the stop of the boost operation in near the minmum value of V_{C2}. It is necessary to select large C_O value or change the setting of output voltage (boost voltage).

2) Given the output hold time as t_{HOLD} (s), C_O is expressed as follows:

$$C_O > \frac{2\times P_{OUT}\times t_{HOLD}}{\left((V_{OUT})^2-(V_{OUT(MIN)})^2\right)\times\eta} \tag{8}$$

where,
t_{HOLD} :Output hold time (s)
$V_{OUT(MIN)}$:Minmum output voltage of C2 during output hold (V)
η :Efficiency

In case t_{HOLD} = 20 ms, P_O = 200 W, η = 90 % and the output voltage = 330 V to 390 V, C_O value is derived as 205 μF. Thus, C_O value of approximately 220 μF is connected.

- **Inductor**

Apply proper design margin to temperature rise by core loss and copper loss.
Inductance L_P of PFC in CRM mode are calculated as follows:

1) Operational Frequency, $f_{SW(SET)}$ and Maximum On-time, $t_{ON(SET)MAX}$

At first, determine $f_{SW(SET)}$ that is minimum operational frequency at the peak of the AC line waveform. The frequency becomes higher with lowering the input voltage. The frequency at the peak of the AC line waveform, $f_{SW(SET)}$ should be set above frequency of 25 kHz.
The $t_{ON(SET)MAX}$ at $f_{SW(SET)}$ is calculated by Equation (9). The $t_{ON(MAX)}$ described in “9.4 Maximmum on-time setting” should be set above $t_{ON(SET)MAX}$.

$$t_{ON(SET)MAX} = \frac{V_{OUT}-\sqrt{2}\times V_{ACRMS(MIN)}}{f_{SW(SET)}\times V_{OUT}} \tag{9}$$

Where,
V_{OUT} : Output voltage (V)
$V_{ACRMS(MIN)}$: Maximum AC input voltage rms value (V)

2) Output Voltage, V_{OUT}

The output voltage V_{OUT} of boost-converter is higher than input voltage.
Set the voltage of V_{OUT} higher than the peak value of the AC input voltage by approximately 20 V, according to following equation:

$$V_{OUT} \geq \sqrt{2}\times V_{ACRMS(MAX)} + 20(V) \tag{10}$$

Where,
$V_{ACRMS(MAX)}$:Maximum AC input voltage rms value (V)

3) Inductance, L_P

Substituting both minimum and maximum of AC input voltage to V_{ACRMS}, choose a smaller one as L_P value.
L_P is calculated as follows:

$$L_P = \frac{\eta\times(V_{ACRMS})^2\times\left(V_{OUT}-\sqrt{2}\times V_{ACRMS}\right)}{2\times P_{OUT}\times f_{SW(SET)}\times V_{OUT}} \tag{11}$$

Where,
V_{ACRMS} : AC input voltage rms value (V)
P_{OUT} : Output power (W)
η : Efficiency of PFC(In general, the range of η is 0.90 to 0.97, depending on on-resistance of power MOSFET $R_{DS(ON)}$ and forward voltage drop of rectifier diode V_F.)

4) Inductor peak current, I_{LP}

I_{LP} is peak current of the peak at the minimum AC input voltage.
I_{LP} calculated as follows:

$$I_{LP} = \frac{2\times\sqrt{2}\times P_{OUT}}{\eta\times V_{ACRMS(MIN)}} \tag{12}$$

10.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 10-4 shows the circuit design example. Figure 10-5 shows the PCB pattern layout example around IC.

(1) Main Circuit Trace
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

(2) Control Ground Trace Layout
Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 10-4 as close to the R_{CS} pin as possible.

(3) R_{CS} Trace Layout
R_{CS} should be placed as close as possible to the Source pin and the CS pin.
The peripheral components of CS pin should be connected by dedicated pattern from root of R_{CS}.
The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 10-4) which is close to the base of R_{CS}.

(4) Peripheral Component of IC
The components for control connected to the IC should be placed as close as possible to the IC, and should be connected as short as possible to the each pin.

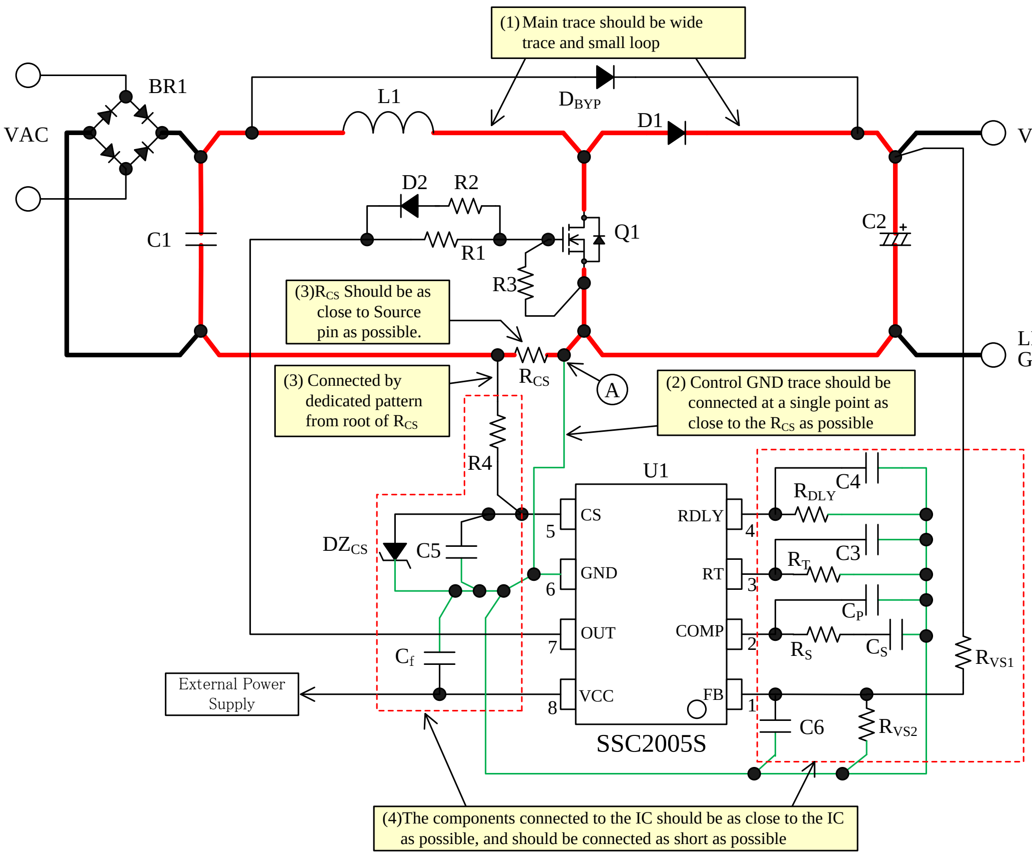


Figure 10-4 Example of connection of peripheral component

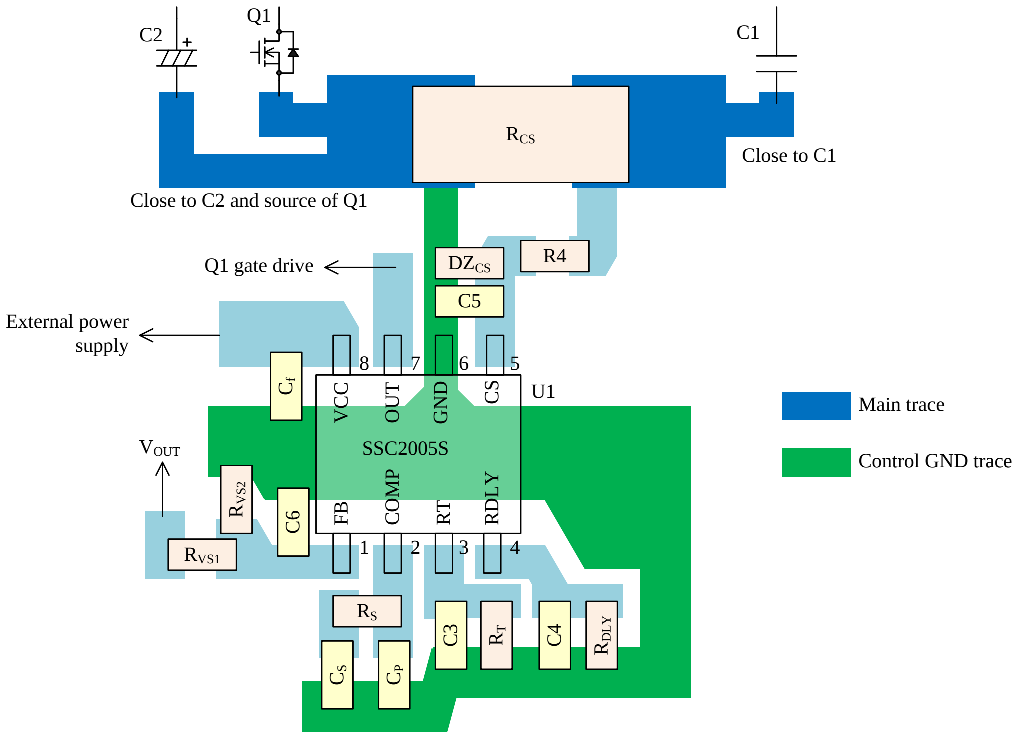


Figure 10-5 Example of connection of peripheral component

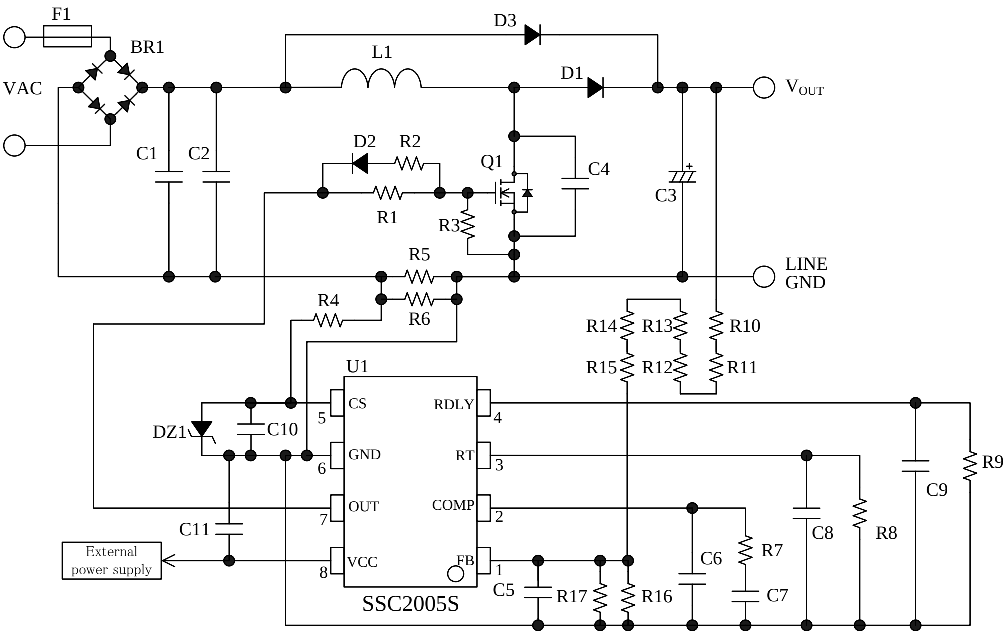
11. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

- Circuit schematic

IC	SSC2005S
Input voltage	AC 85 to AC 265 V
Input power	200 W
Output voltage	398 V
Operation frequency (at maximum AC input)	60 kHz (AC 265 V)

- Circuit schematic



- Bill of materials

Symbol	Part type	Ratings[1]	Recommended Sanken Parts	Symbol	Part type	Ratings[1]	Recommended Sanken Parts
BR1	General	600 V		R5	General	0.15 Ω, 2W	
F1	Fuse	AC 250 V		R6	General	0.15 Ω, 2W	
L1	Inductor	160 µH		R7	General	10 kΩ	
C1	Ceramic	450 V, 0.68 µF		R8	General	22 kΩ	
C2	Ceramic	450 V, 0.68 µF		R9 [2]	General	22 kΩ	
C3 [2]	Ceramic	450 V, 180 µF		R10 [3]	General	470 kΩ	
C4 [2]	Ceramic	1kV, 100pF		R11 [3]	General, 1%	560 kΩ	
C5	Ceramic	1000 pF		R12 [3]	General, 1%	560 kΩ	
C6	Ceramic	0.47 µF		R13 [3]	General, 1%	560 kΩ	
C7	Ceramic	1 µF		R14 [3]	General, 1%	680 kΩ	
C8	Ceramic	0.01 µF		R15 [3]	General, 1%	680 kΩ	
C9	Ceramic	0.01 µF		R16	General, 1%	680 kΩ	
C10	Ceramic	3300 pF		R17	General	33 kΩ	
C11	Ceramic	0.47 µF		D1	Fast recovery	600V, 10 A	FMNS-1106S
R1 [2]	General	100 Ω		D2	Schottky	60 V, 0.7 A	AK06
R2 [2]	General	10 Ω		D3	General	600V, 1.2A	RM10A
R3 [2]	General	100 kΩ		U1	IC	SSC2005S	
R4	General	47 Ω					

[1] Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
[2] It is necessary to be adjusted based on actual operation in the application.
[3] Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

OPERATING PRECAUTIONS

In the case that you use Sanken products or design your products by using Sanken products, the reliability largely depends on the degree of derating to be made to the rated values. Derating may be interpreted as a case that an operation range is set by derating the load from each rated value or surge voltage or noise is considered for derating in order to assure or improve the reliability. In general, derating factors include electric stresses such as electric voltage, electric current, electric power etc., environmental stresses such as ambient temperature, humidity etc. and thermal stress caused due to self-heating of semiconductor products. For these stresses, instantaneous values, maximum values and minimum values must be taken into consideration. In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5 to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of the products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between the product pins, and wrong connections. Ensure all test parameters are within the ratings specified by Sanken for the products.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:
  - 260 ± 5 °C 10 ± 1 s (Flow, 2 times)
  - 380 ± 10 °C 3.5 ± 0.5 s (Soldering iron, 1 time)

Electrostatic Discharge

- When handling the products, the operator must be grounded. Grounded wrist straps worn should have at least 1MΩ of resistance from the operator to ground to prevent shock hazard, and it should be placed near the operator.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in order to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in Sanken shipping containers or conductive containers, or be wrapped in aluminum foil.

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