LLC Current-resonant Off-line Switching Controller

SSC3S937

Data Sheet

Description

The SSC3S937 is a controller with SMZ* method for LLC current resonant switching power supplies, incorporating a floating drive circuit for a high-side power MOSFET. The IC includes useful functions such as standby function, automatic dead time adjustment, and capacitive mode detection. The IC achieves high efficiency, low noise and high cost-effective power supply systems with few external components.

*SMZ: Soft-switched Multi-resonant Zero Current switch, achieved soft switching operation during all switching periods.

Package

SOP18

Not to scale

Features

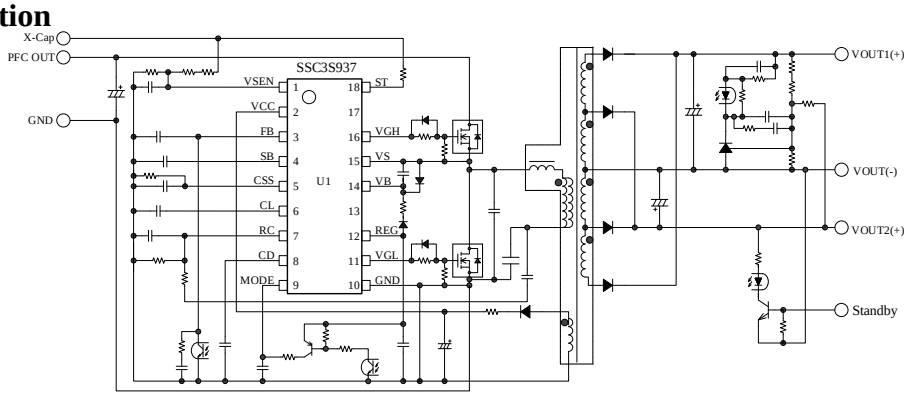
- Pb-free (RoHS Compliant)
- Standby Mode Change Function by External Signal
  - Output Power at Light Load:
    P_O = 150 mW (P_{IN} = 0.27 W)
  - Burst Operation in Standby Mode
  - Soft-on/Soft-off Function: Reduces Audible Noise
- Soft-start Function
- Capacitive Mode Detection Function
- Reset Detection Function
- Automatic Dead Time Adjustment Function
- Built-in Startup Circuit
- X-capacitor Discharge Function (AC Input Mode)
- Input Capacitor Discharge Function (DC Input Mode)
- Protections
  - Input Voltage Protection
    Input Overvoltage Protection (HVP): Auto-restart
    Input Undervoltage Protection (UVP): Auto-restart
  - High-side Driver UVLO: Auto-restart
  - Overcurrent Protection (OCP): Auto-restart, Peak Drain Current Detection, Two Types Protection
  - Overload Protection (OLP): Auto-restart
  - VCC Pin Overvoltage Protection (VCC_OVP): Auto-restart
  - REG Pin Overvoltage Protection (REG_OVP): Auto-restart
  - Thermal Shutdown (TSD): Auto-restart

Applications

Switching power supplies for electronic devices such as:

- Digital Appliances (e.g., Television)
- Office Automation (OA) Equipment (e.g., Server, MultiFunction Printer)
- Industrial Apparatus
- Communication Facilities

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25°C.

Parameter	Symbol	Pins	Rating	Unit
VSEN Pin Sink Current	I_{SEN}	1 − 10	1.0	mA
Control Part Input Voltage	V_{CC}	2 − 10	−0.3 to 35	V
FB Pin Voltage	V_{FB}	3 − 10	−0.3 to 6	V
SB Pin Voltage	V_{SB}	4 − 10	−0.3 to 6	V
CSS Pin Voltage	V_{CSS}	5 − 10	−0.3 to 6	V
CL Pin Voltage	V_{CL}	6 − 10	−0.3 to 6	V
RC Pin Voltage	V_{RC}	7 − 10	−6 to 6	V
CD Pin Voltage	V_{CD}	8 − 10	−0.3 to 6	V
MODE Pin Sink Current	I_{MODE}	9 − 10	100	μA
VGL pin Voltage	V_{GL}	11 − 10	−0.3 to V_{REG} + 0.3	V
REG pin Source Current	I_{REG}	12 − 10	−10.0	mA
Voltage Between VB Pin and VS Pin	V_B−V_S	14 − 15	−0.3 to 20.0	V
VS Pin Voltage	V_S	15 − 10	−1 to 600	V
VGH Pin Voltage	V_{GH}	16 − 10	V_S − 0.3 to V_B + 0.3	V
ST Pin Voltage	V_{ST}	18 − 10	−0.3 to 600	V
Operating Ambient Temperature	T_{OP}	−	−40 to 85	°C
Storage Temperature	T_{STG}	−	−40 to 125	°C
Junction Temperature	T_J	−	150	°C

* Surge voltage withstand (Human body model) of No.14, 15, 16 and 18 is guaranteed 1000 V. Other pins are guaranteed 2000 V.

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25 °C, V_{CC} is 19 V.

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Start Circuit and Circuit Current							
Operation Start Voltage	$V_{CC(ON)}$		2 − 10	15.8	17.0	18.2	V
Operation Stop Voltage (1)	$V_{CC(OFF)}$		2 − 10	7.8	8.9	9.8	V
Startup Current Biasing Threshold Voltage(1)	$V_{CC(BIAS)}$		2 − 10	9.0	9.8	10.6	V
Circuit Current in Operation	$I_{CC(ON)}$		2 − 10	—	—	10.0	mA
Circuit Current in Non-Operation (2)	$I_{CC(OFF)}$	V_{CC} = 11 V	2 − 10	—	0.7	1.5	mA
Startup Current (2)	I_{ST}		18 − 10	3.0	6.0	9.0	mA
Protection Operation Release Threshold Voltage(1)	$V_{CC(P.OFF)}$		2 − 10	7.8	8.9	9.8	V
Circuit Current in Protection	$I_{CC(P)}$	V_{CC} = 10 V	2 − 10	—	0.7	1.5	mA
Oscillator							
Minimum Frequency	$f_{(MIN)}$		11 – 10 16 − 15	27.5	31.5	35.5	kHz
Maximum Frequency	$f_{(MAX)}$		11 – 10 16 − 15	230	300	380	kHz
Minimum Dead-Time	$t_{d(MIN)}$		11 – 10 16 − 15	0.04	0.24	0.44	µs
Maximum Dead-Time	$t_{d(MAX)}$		11 – 10 16 − 15	1.20	1.65	2.20	µs
Externally Adjusted Minimum Frequency 1	$f_{(MIN)ADJ1}$	R_{CSS} = 30 kΩ	11 – 10 16 − 15	69	73	77	kHz
Externally Adjusted Minimum Frequency 2	$f_{(MIN)ADJ2}$	R_{CSS} = 77 kΩ	11 – 10 16 − 15	42.4	45.4	48.4	kHz
Feedback Control							
FB Pin Oscillation Start Threshold Voltage	$V_{FB(ON)}$		3 – 10	0.15	0.30	0.45	V
FB Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		3 – 10	0.05	0.20	0.35	V
FB Pin Maximum Source Current	$I_{FB(MAX)}$	V_{FB} = 0 V	3 – 10	−300	−195	−100	µA
FB Pin Reset Current	$I_{FB(R)}$		3 – 10	2.5	5.0	7.5	mA
Soft-start							
CSS Pin Charging Current	$I_{CSS(C)}$		5 – 10	−120	−105	−90	µA
CSS Pin Reset Current	$I_{CSS(R)}$	V_{CC} = 11V	5 – 10	1.1	1.8	2.5	mA
Maximum Frequency in Soft-start	$f_{(MAX)SS}$		11 – 10 16 − 15	400	500	600	kHz
Standby							
MODE Pin Standby Release Threshold Voltage	$V_{MODE(NRM)}$		9 – 10	4.5	5.0	5.5	V
MODE Pin Standby Threshold Voltage	$V_{MODE(STB)}$		9 – 10	1.35	1.50	1.65	V
MODE Pin Sink Current	$I_{MODE(SNK)}$		9 – 10	3	10	17	µA

(1) $V_{CC(OFF)} = V_{CC(P.OFF)} < V_{CC(BIAS)}$ always.

(2) $I_{START} = I_{ST(OFF)} - I_{CC(OFF)}$, where, I_{START} is VCC pin sink current in startup.

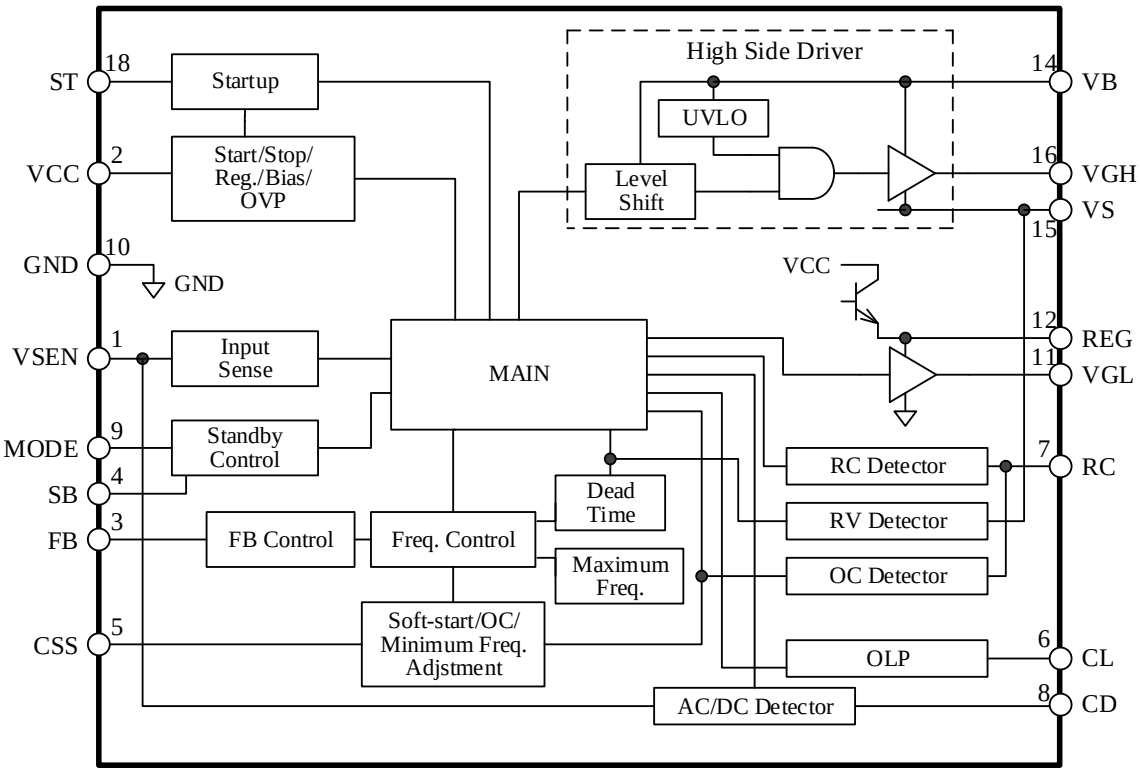
Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
MODE Pin Clamp Voltage	$V_{MODE(CLAMP)}$		9 – 10	7.0	8.5	10.0	V
SB Pin Oscillation Start Threshold Voltage	$V_{SB(ON)}$		4 – 10	0.15	0.30	0.45	V
SB Pin Oscillation Stop Threshold Voltage	$V_{SB(OFF)}$		4 – 10	0.05	0.20	0.35	V
SB Pin Standby Threshold Voltage	$V_{SB(STB)}$		4 – 10	0.5	0.6	0.7	V
SB Pin Source Current (H)	$I_{SB(SRC)H}$		4 – 10	−19.0	−15.0	−11.0	µA
SB Pin Source Current (L)	$I_{SB(SRC)}$		4 – 10	−7.5	−5.0	−2.5	µA
SB Pin Sink Current (H)	$I_{SB(SNK)H}$		4 – 10	9.0	12.5	16.0	µA
SB Pin Sink Current (L)	$I_{SB(SNK)}$		4 – 10	2.5	5.0	7.5	µA
Overload Protection (OLP)							
CL pin OLP Threshold Voltage	$V_{CL(OLP)}$		6 – 10	3.9	4.2	4.5	V
CL Pin Source Current 1	$I_{CL(SRC)1}$		6 – 10	−29	−17	−5	µA
CL Pin Source Current 2	$I_{CL(SRC)2}$		6 – 10	−180	−135	−90	µA
CL Pin Sink Current	$I_{CL(SNK)}$		6 – 10	10	30	50	µA
Input Undervoltage Protection (UVP)							
VSEN Pin Threshold Voltage (On)	$V_{SEN(ON)}$		1 – 10	1.150	1.200	1.250	V
VSEN Pin Threshold Voltage (Off) 1	$V_{SEN(OFF)1}$		1 – 10	0.955	1.000	1.045	V
VSEN Pin Threshold Voltage (Off) 2	$V_{SEN(OFF)2}$		1 – 10	—	0.8	—	V
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$		1 – 10	5.3	5.6	5.9	V
VSEN Pin Clamp Voltage	$V_{SEN(CLAMP)}$		1 – 10	10.0	—	—	V
VSEN pin Threshold Voltage for AC Line Detection 1	$V_{SEN(AC)1}$		1 – 10	2.56	2.70	2.84	V
VSEN Pin Threshold Voltage for AC Line Detection 2	$V_{SEN(AC)2}$		1 – 10	—	2.4	—	V
CD Pin Clamp Voltage for DC Mode	$V_{CD(DC)}$		8 – 10	1.85	2.00	2.15	V
CD Pin Threshold Voltage 1	V_{CD1}		8 – 10	2.8	3.0	3.2	V
CD Pin Source Current	$I_{CD(SRC)}$	V_{CD} = 0 V	8 – 10	–12.0	–10.2	–8.5	µA
CD Pin Reset Current	$I_{CD(R)}$	V_{CD} = 2 V	8 – 10	1.0	2.5	4.0	mA
Reset Detection							
Maximum Reset Time	$t_{RST(MAX)}$		11 – 10 16 – 15	4	5	6	µs
Driver Circuit Power Supply							
VREG Pin Output Voltage	V_{REG}		12 – 10	9.6	10.0	10.8	V
High-side Driver							
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		14 – 15	5.7	6.8	7.9	V
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		14 – 15	5.5	6.4	7.3	V
Driver Circuit							
VGL,VGH Pin Source Current 1	$I_{GL(SRC)1}$ $I_{GH(SRC)1}$	V_{REG} = 10.5V V_B = 10.5V V_{GL} = 0V V_{GH} = 0V	11 – 10 16 – 15	—	–540	—	mA

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
VGL,VGH Pin Sink Current 1	$I_{GL(SNK)1}$ $I_{GH(SNK)1}$	V_{REG} = 10.5V V_B = 10.5V V_{GL} = 10.5V V_{GH} = 10.5V	11 – 10 16 – 15	—	1.50	—	A
VGL,VGH Pin Source Current 2	$I_{GL(SRC)2}$ $I_{GH(SRC)2}$	V_{REG} = 11.5 V V_B = 11.5 V V_{GL} = 10 V V_{GH} = 10 V	11 – 10 16 – 15	−140	−90	−40	mA
VGL,VGH Pin Sink Current 2	$I_{GL(SNK)2}$ $I_{GH(SNK)2}$	V_{REG} = 11.5 V V_B = 11.5 V V_{GL} = 1.5 V V_{GH} = 1.5 V	11 – 10 16 – 15	140	230	360	mA
Current Resonant and Overcurrent Protection (OCP)							
Capacitive Mode Detection Voltage 1	V_{RC1}		7 – 10	0.02	0.10	0.18	V
				−0.18	−0.10	−0.02	V
Capacitive Mode Detection Voltage 2	V_{RC2}		7 – 10	0.20	0.30	0.40	V
				−0.40	−0.30	−0.20	V
RC Pin Threshold Voltage (Low)	$V_{RC(L)}$		7 – 10	1.80	1.90	2.00	V
				−2.00	−1.90	−1.80	V
RC Pin Threshold Voltage (High speed)	$V_{RC(S)}$		7 – 10	2.62	2.80	2.98	V
				−2.98	−2.80	−2.62	V
CSS Pin Sink Current (Low)	$I_{CSS(L)}$		5 – 10	1.1	1.8	2.5	mA
CSS Pin Sink Current (High speed)	$I_{CSS(S)}$		5 – 10	13.0	20.5	28.0	mA
Overvoltage Protection (OVP)							
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 10	30.0	32.0	34.0	V
REG Pin OVP Threshold Voltage	$V_{CC(REG)}$		12 – 10	11.5	12.4	13.5	V
Thermal Shutdown (TSD)							
Thermal Shutdown Temperature	$T_{J(TSD)}$		—	140	—	—	°C
Thermal Resistance							
Junction to Ambient Thermal Resistance	θ_{J-A}		—	—	—	95	°C/W

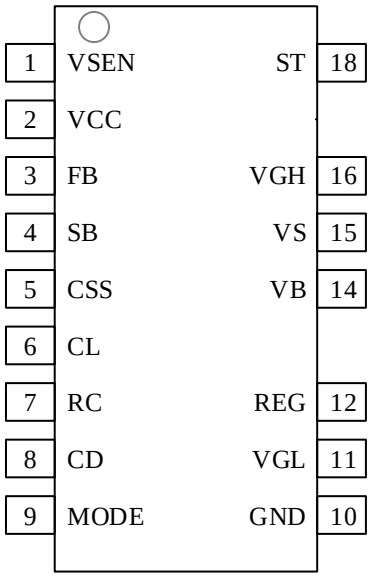
3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Package Weight		—	0.27	—	g	

4. Block Diagram



5. Pin Configuration Definitions



Number	Name	Function
1	VSEN	The mains input voltage protection signal input
2	VCC	Supply voltage input for the IC, and overvoltage protection (OVP) signal input
3	FB	Feedback signal input for constant voltage control
4	SB	Standby control capacitor connection
5	CSS	Soft-start capacitor connection
6	CL	Overload detection capacitor connection
7	RC	Resonant current detection signal input, and overcurrent protection (OCP) signal input
8	CD	Delay time setting capacitor connection
9	MODE	Standby mode change signal input
10	GND	Ground
11	VGL	Low-side gate drive output
12	REG	Supply voltage output for gate drive circuit
13	—	(Pin removed)
14	VB	Supply voltage input for high-side driver
15	VS	Floating ground for high-side driver
16	VGH	High-side gate drive output
17	—	(Pin removed)
18	ST	Startup current input

6. Typical Application

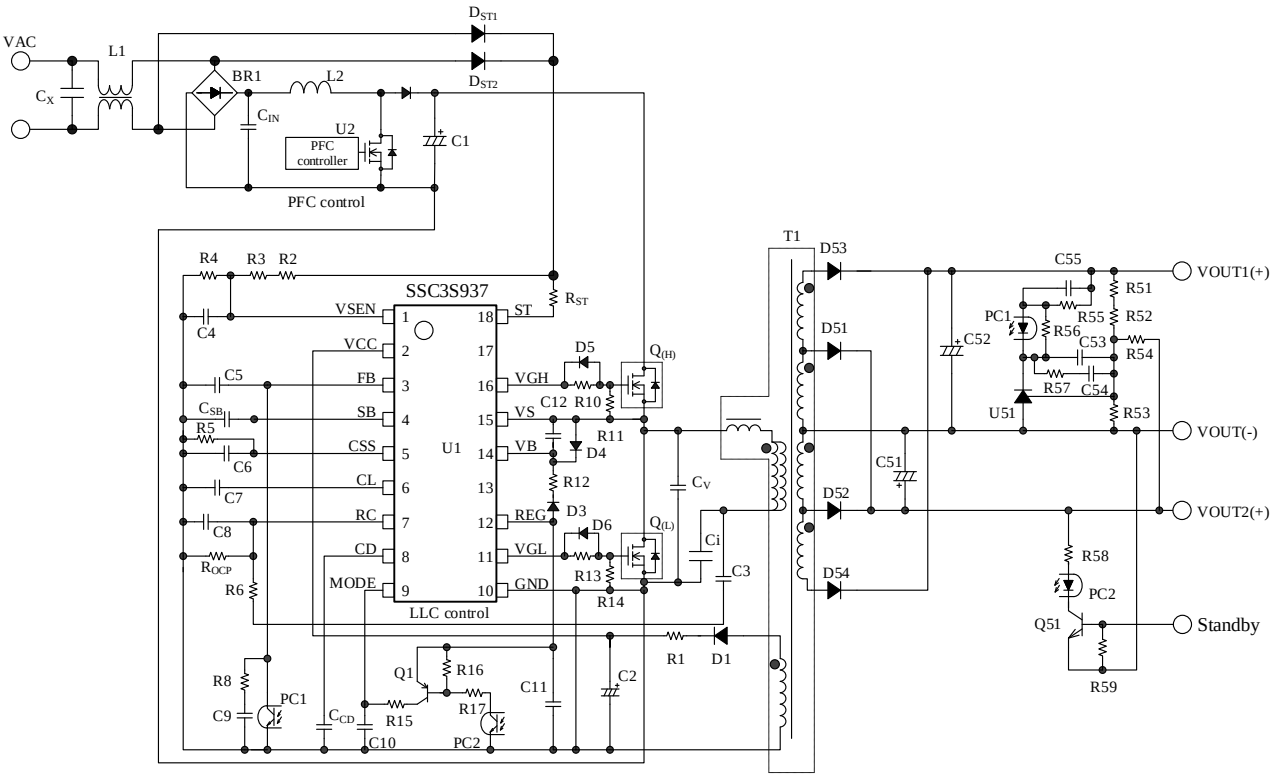


Figure 6-1. Typical Application (AC Input Mode)

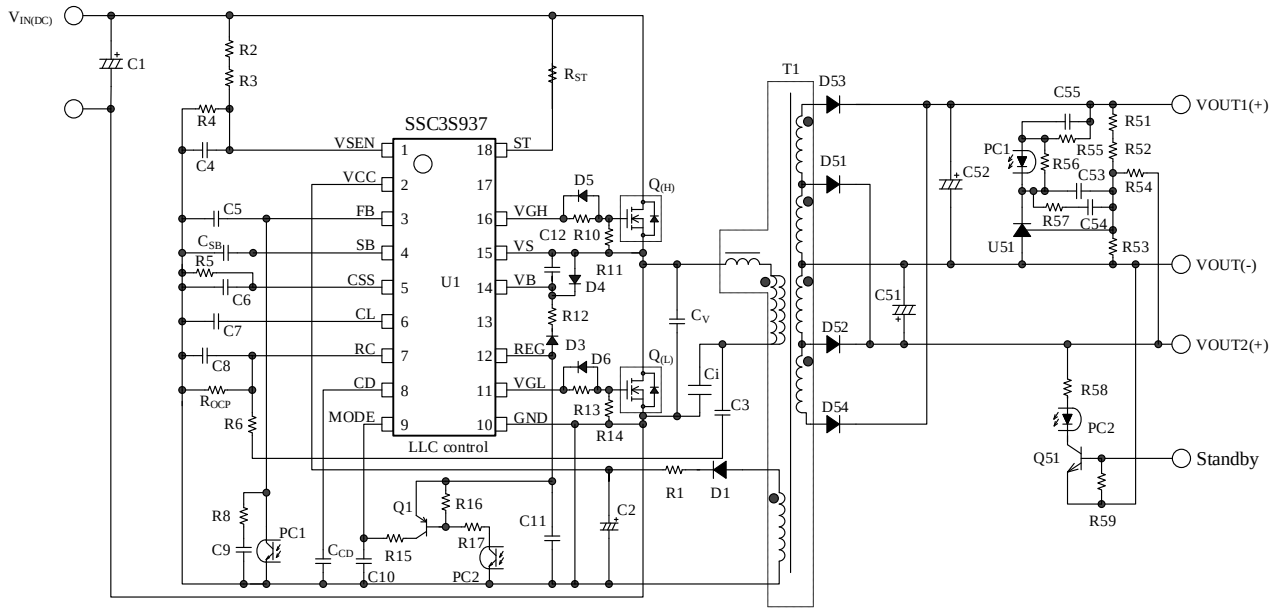
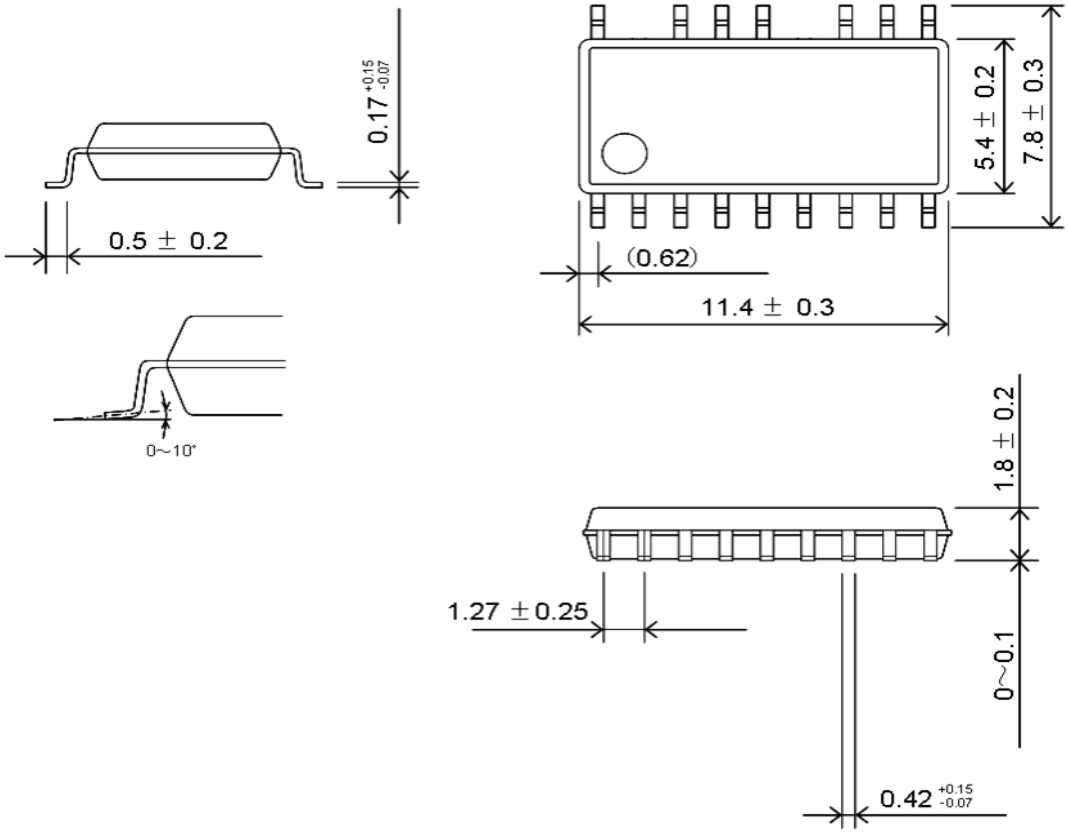


Figure 6-2. Typical Application (DC Input Mode)

7. Physical Dimensions

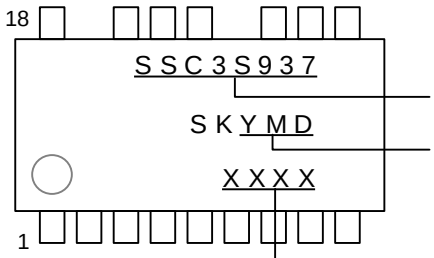
● SOP18



NOTES:

- All dimensions in millimeters
- Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Soldering Iron: 350 °C / 3.5 s, 1 time
  Soldering should be at a distance of at least 1.5 mm from the body of the product.

8. Marking Diagram



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is a period of days:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

9. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−). $Q_{(H)}$ and $Q_{(L)}$ indicate a high-side power MOSFET and a low-side power MOSFET respectively. Ci and C_V indicate a current resonant capacitor and a voltage resonant capacitor, respectively.

9.1 Resonant Circuit Operation

Figure 9-1 shows a basic RLC series resonant circuit.

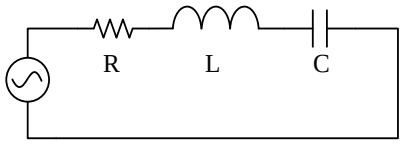


Figure 9-1. RLC Series Resonant Circuit

The impedance of the circuit, Ż, is as the following Equation.

$$\dot{Z} = R + j\left(\omega L - \frac{1}{\omega C}\right), \quad (1)$$

where ω is angular frequency; and ω = 2πf.
Thus,

$$\dot{Z} = R + j\left(2\pi fL - \frac{1}{2\pi fC}\right). \quad (2)$$

When the frequency, f, changes, the impedance of resonant circuit will change as shown in Figure 9-2.

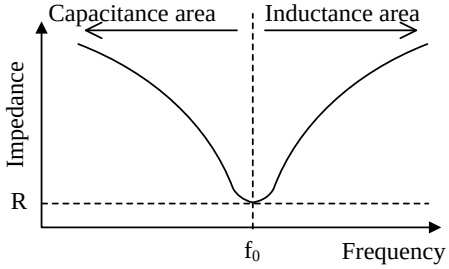


Figure 9-2. Impedance of Resonant Circuit

When 2πfL = 1/2πfC, Ż of Equation (2) becomes the minimum value, R (see Figure 9-2). In the case, ω is calculated by Equation (3).

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}} \quad (3)$$

The frequency in which Ż becomes minimum value is called a resonant frequency, f_0. The higher frequency area than f_0 is an inductance area. The lower frequency area than f_0 is a capacitance area.

From Equation (3), f_0 is as follows:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (4)$$

Figure 9-3 shows the circuit of a current resonant power supply. The basic configuration of the current resonant power supply is a half-bridge converter. The switching devices, $Q_{(H)}$ and $Q_{(L)}$, are connected in series with V_{IN}. The series resonant circuit and the voltage resonant capacitor, C_V, are connected in parallel with $Q_{(L)}$. The series resonant circuit is consisted of the following components: the resonant inductor, L_R; the primary winding, P, of a transformer, T1; and the current resonant capacitor, C_i. The coupling between the primary and secondary windings of T1 is designed to be poor so that the leakage inductance increases. This leakage inductance is used for L_R. This results in a downsized of the series resonant circuit. The dotted mark with T1 describes the winding polarity, the secondary windings, S1 and S2, are connected so that the polarities are set to the same position as shown in Figure 9-3. In addition, the winding numbers of each other should be equal. From Equation (1), the impedance of a current resonant power supply is calculated by Equation (5). From Equation (4), the resonant frequency, f_0, is calculated by Equation (6).

$$\dot{Z} = R + j\left\{\omega(L_R + L_P) - \frac{1}{\omega Ci}\right\}, \quad (5)$$

$$f_0 = \frac{1}{2\pi\sqrt{(L_R + L_P) \times Ci}}, \quad (6)$$

where:
R is the equivalent resistance of load,
L_R is the inductance of the resonant inductor,
L_P is the inductance of the primary winding P, and
Ci is the capacitance of current resonant capacitor.

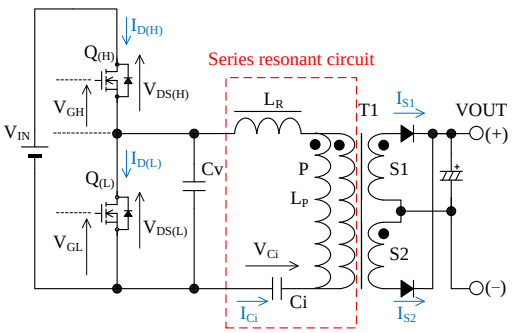


Figure 9-3. Current Resonant Power Supply Circuit

In the current resonant power supply, $Q_{(H)}$ and $Q_{(L)}$ are alternatively turned on and off. The on and off times of them are equal. There is a dead time between the on periods of $Q_{(H)}$ and $Q_{(L)}$. During the dead time, $Q_{(H)}$ and $Q_{(L)}$ are in off status.

In the current resonant power supply, the frequency is controlled. When the output voltage decreases, the IC decreases the switching frequency so that the output power is increased to keep a constant output voltage. This must be controlled in the inductance area ($f_{SW} < f_0$). Since the winding current is delayed from the winding voltage in the inductance area, the turn-on operates in a ZCS (Zero Current Switching); and the turn-off operates in a ZVS (Zero Voltage Switching). Thus, the switching losses of $Q_{(H)}$ and $Q_{(L)}$ are nearly zero. In the capacitance area ($f_{SW} < f_0$), the current resonant power supply operates as follows: When the output voltage decreases, the switching frequency is decreased; and then, the output power is more decreased. Therefore, the output voltage cannot be kept constant. Since the winding current goes ahead of the winding voltage in the capacitance area, $Q_{(H)}$ and $Q_{(L)}$ operate in the hard switching. This results in the increases of a power loss. This operation in the capacitance area is called the capacitive mode operation. The current resonant power supply must be operated without the capacitive mode operation (for more details, see Section 9.11).

Figure 9-4 describes the basic operational waveforms of current resonant power supply (see Figure 9-3 about the symbol in Figure 9-4). For the description of current resonant waveforms in normal operation, the operation is separated into a period A to F. In the following description:

$I_{D(H)}$ is the current of $Q_{(H)}$,
$I_{D(L)}$ is the current of $Q_{(L)}$,
$V_{F(H)}$ is the forwerd voltage of $Q_{(H)}$,
$V_{F(L)}$ is the forwerd voltage of $Q_{(L)}$,
I_L is the current of L_R,
V_{IN} is an input voltage,
V_{Ci} is Ci voltage, and
V_{CV} is C_V voltage.

The current resonant power supply operations in period A to F are as follows:

1) Period A
When $Q_{(H)}$ is on, an energy is stored into the series resonant circuit by $I_{D(H)}$ that flows through the resonant circuit and the transformer (see Figure 9-5). At the same time, the energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

2) Period B
After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 9-6).

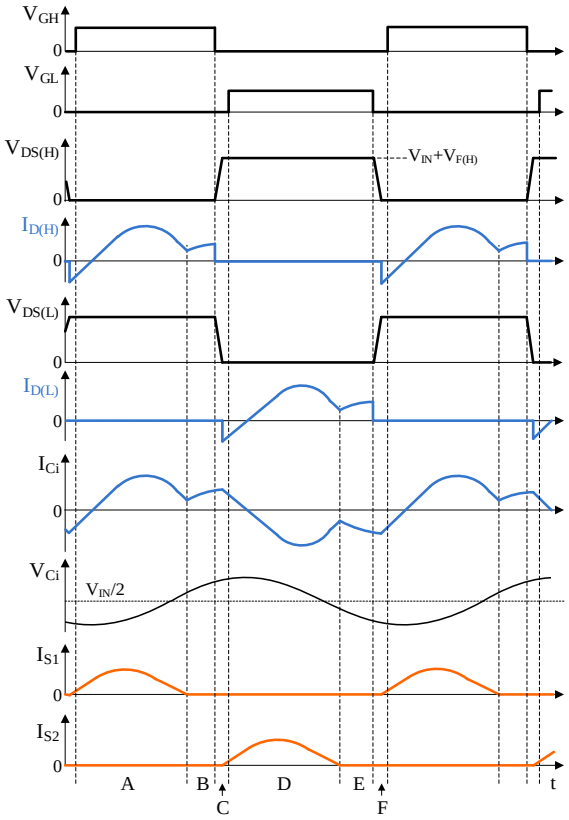


Figure 9-4. The Basic Operational Waveforms of Current Resonant Power Supply

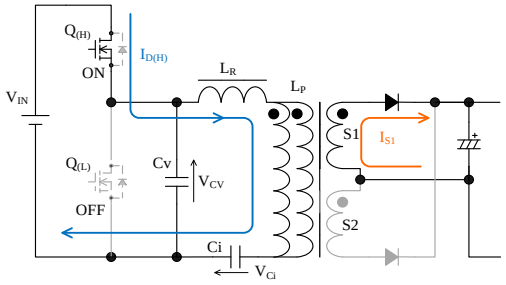


Figure 9-5. Operation in period A

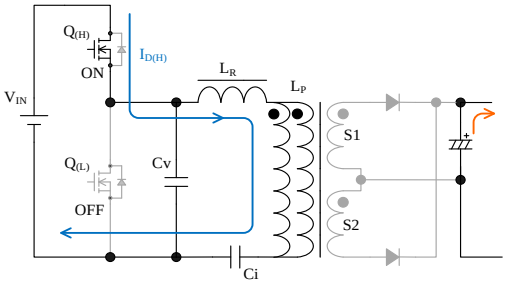


Figure 9-6. Operation in Period B

3) Period C

C is the dead-time period. $Q_{(H)}$ and $Q_{(L)}$ are in off status. When $Q_{(H)}$ turns off, C_V is discharged by I_L that is supplied by the energy stored in the series resonant circuit applies (see Figure 9-7). When V_{CV} decreases to $V_{F(L)}$, $-I_{D(L)}$ flows through the body diode of $Q_{(L)}$; and V_{CV} is clamped to $V_{F(L)}$. After that, $Q_{(L)}$ turns on. Since $V_{DS(L)}$ is nearly zero at the point, $Q_{(L)}$ operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

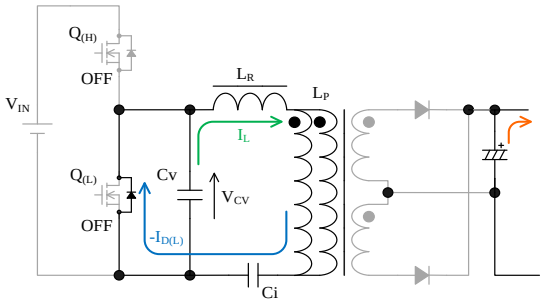


Figure 9-7. Operation in Period C

4) Period D

Immidiately after $Q_{(L)}$ turns on, $-I_{D(L)}$, which was flowing in Period C, continues to flow through $Q_{(L)}$ for a while. Then, $I_{D(L)}$ flows as shown in Figure 9-8; and V_{Ci} is applied the primary winding voltage of the transformer. At the same time, energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

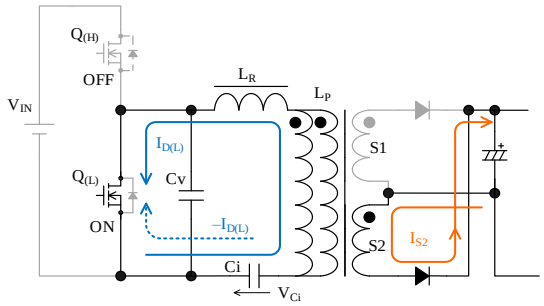


Figure 9-8. Operation in Period D

5) Period E

After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 9-9).

6) Period F

F is the dead-time period. $Q_{(H)}$ and $Q_{(L)}$ are in off status.

When $Q_{(L)}$ turns off, C_V is charged by $-I_L$ that is supplied by the energy stored in the series resonant circuit applies (see Figure 9-10). When V_{CV} decreases to $V_{IN} + V_{F(H)}$, $-I_{D(H)}$ flows through body diode of $Q_{(H)}$; and V_{CV} is clamped to $V_{IN} + V_{F(H)}$. After that, $Q_{(H)}$ turns on. Since $V_{DS(H)}$ is nearly zero at the point, $Q_{(H)}$ operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

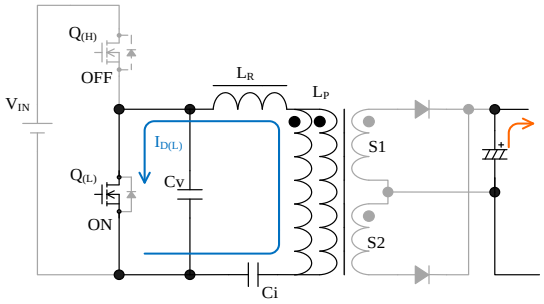


Figure 9-9. Operation in Period E

7) After the period F

Immidiately after $Q_{(H)}$ turns on, $-I_{D(H)}$, which was flowing in Period F, continues to flow through $Q_{(H)}$ for a while. Then, $I_{D(H)}$ flows again; and the operation returns to the period A. The above operation is repeated to transfer energy to the secondary side from the resonant circuit.

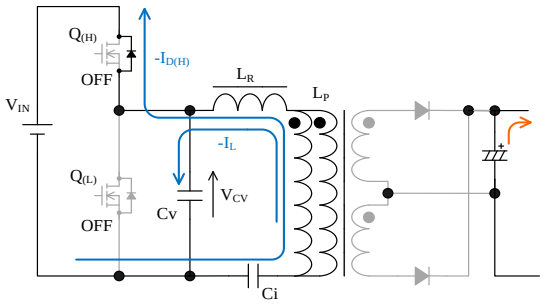


Figure 9-10. Operation in Period F

9.2 Startup Operation

Figure 9-11 shows the VSEN and VCC pins and their peripheral circuit. The IC incorporates its own startup circuit. When an input voltage is supplied, the constant startup current regulated inside the IC (I_{ST} = 6.0 mA) starts charging the C2 connected to the VCC pin. When the VCC pin voltage increase to $V_{CC(ON)}$ = 17.0 V or more, and then the IC starts switching operation, the VCC pin voltage is the rectified auxiliary winding voltage, V_D, as shown in Figure 9-11. After the power startup sequence ends, the startup circuit turns off automatically to eliminate the power dissipation by itself.

The IC can operate with the AC or DC input power supply. The IC determines whether the input is AC or DC by the VSEN pin voltage during the startup period. The switching start timing of the AC or DC input is as follows:

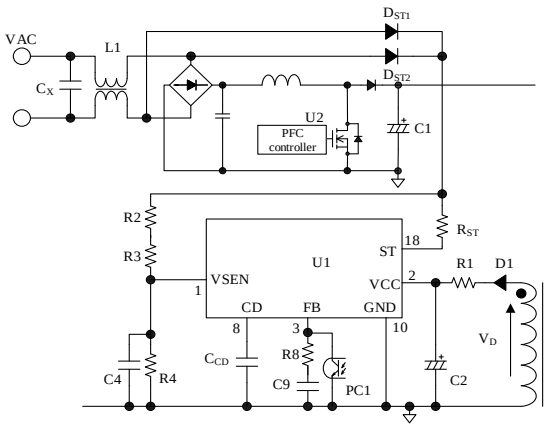


Figure 9-11. VSEN and VCC Pins Peripheral Circuit

● **AC Input Mode**

Figure 9-12 shows the startup operational waveforms in the AC input mode. When an AC input is supplied, the VCC pin voltage, V_{CC}, is increased by the constant startup current. When the IC detects the rising edge of the VSEN pin voltage, V_{SEN}, after $V_{CC} \geq V_{CC(BIAS)}$ = 9.8 V, the IC determines to be the AC input mode. The IC has the following two threshold voltages for the rising edge detection: $V_{SEN(OFF)1}$ = 1.000 V and $V_{SEN(AC)1}$= 2.70 V. The internal threshold voltages are automatically shifted according to which of the VSEN pin threshold voltages has been detected: $V_{SEN(OFF)2}$ = 0.8 V when $V_{SEN(OFF)1}$, and $V_{SEN(AC)2}$ = 2.4 V when $V_{SEN(AC)1}$. This is how the IC ensures its stable detection of AC input voltages.

When $V_{CC} \geq V_{CC(BIAS)}$ = 9.8 V, the IC starts to charge CD pin capacitor, C_{CD}, by $I_{CD(SRC)}$ = –10.2 µA. When the IC detects the rising edge of V_{SEN}, C_{CD} is discharged. When the CD pin voltage decrease to about 0.3 V, the IC charges C_{CD} by $I_{CD(SRC)}$ again. In this way, the IC repeats the charging or discharging of C_{CD}, by the two threshold voltages.

After that, when $V_{CC} \geq V_{CC(ON)}$ = 17.0 V, and IC detects the rising edge of V_{SEN}, the internal circuit starts to operate. Then, the IC generates the REG pin voltage, and starts to charge the FB pin capacitor, C9. When the FB pin voltage increase to $V_{FB(ON)}$ = 0.30 V or more, the VGH and VGL pins start switching operation.

When the AC input, the capacitance of C_{CD} should be set as the CD pin voltage is less than $V_{CD(DC)}$ = 2.00 V during startup ($V_{CC(BIAS)} \leq V_{CC} \leq V_{CC(ON)}$).

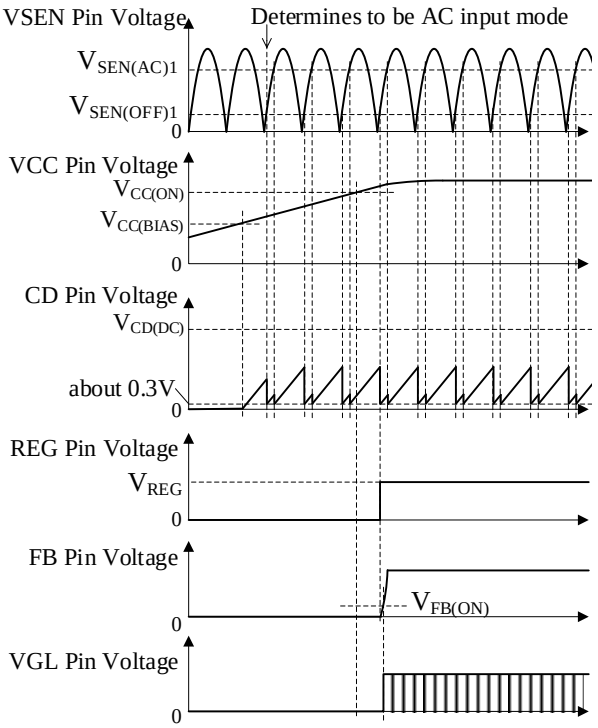


Figure 9-12. Startup Operational Waveforms in AC Input Mode

● **DC Input Voltage**

Figure 9-13 shows the startup operational waveforms in the DC input mode. When an DC input is supplied, the VCC pin voltage, V_{CC}, is increased by the constant startup current. When $V_{CC} \geq V_{CC(BIAS)}$ = 9.8 V, the IC starts to charge CD pin capacitor, C_{CD}, by $I_{CD(SRC)}$ = –10.2 µA. When the CD pin voltage reaches $V_{CD(DC)}$ = 2.00 V without V_{SEN} rising edge detection, the IC determines to be the DC input mode. The CD pin voltage is clamped by $V_{CD(DC)}$.

When all the following conditions are met, the VGH and VGL pins start switching operation.

- VSEN pin voltage ≥ $V_{SEN(ON)}$ = 1.200 V.
- CD pin voltage is clamped by $V_{CD(DC)}$ = 2.00 V.
- VCC pin voltge ≥ $V_{CC(ON)}$ = 17.0 V.
- FB pin voltage ≥ $V_{FB(ON)}$ = 0.30 V.

If V_{CC} becomes ≥$V_{CC(ON)}$ under the CD pin voltage is <$V_{CD(DC)}$, the IC starts to charge the FB pin capacitor, C9, after the CD pin voltage is clamped. When the FB

pin voltage increase to $V_{FB(ON)}$ or more, the VGH and VGL pins start switching operation.

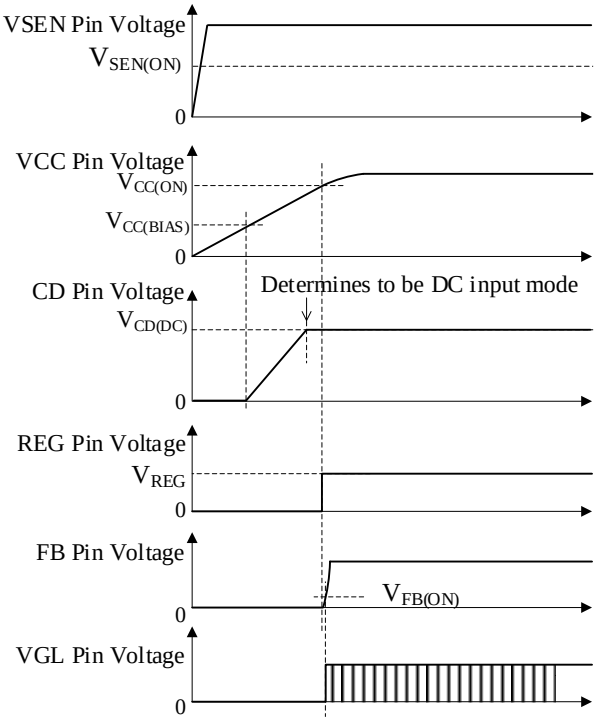


Figure 9-13. Startup Operational Waveforms in DC Input Mode

9.3 Undervoltage Lockout (UVLO)

Figure 9-14 shows the relationship of V_{CC} and I_{CC}.

After the IC starts operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the IC stops switching operation by the undervoltage lockout (UVLO) function and reverts to the state before startup again.

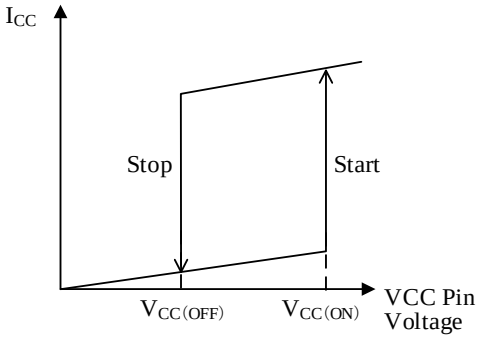


Figure 9-14. V_{CC} vs. I_{CC}

9.4 Bias Assist Function

Figure 9-15 shows the VCC pin voltage behavior during the startup period.

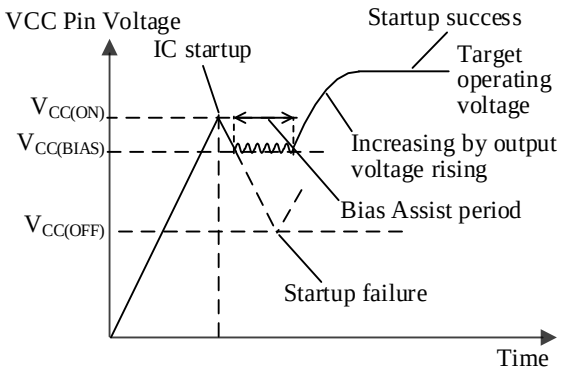


Figure 9-15. VCC Pin Voltage during Startup Period

When the conditions of Section 9.2 are fulfilled, the IC starts operation. Thus, the circuit current, I_{CC}, increases, and the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, V_D, increases in proportion to the output voltage rise. Thus, the VCC pin voltage is set by the balance between dropping due to the increase of I_{CC} and rising due to the increase of the auxiliary winding voltage, V_D.

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the IC stops switching operation and a startup failure occurs.

In order to prevent this, when the VCC pin voltage decreases to the startup current threshold biasing voltage, $V_{CC(BIAS)}$ = 9.8 V, the bias assist function is activated.

While the bias assist function is activated, any decrease of the VCC pin voltage is counteracted by providing the startup current, I_{ST}, from the startup circuit.

It is necessary to check the startup process based on actual operation in the application, and adjust the VCC pin voltage, so that the startup failure does not occur.

If VCC pin voltage decreases to $V_{CC(BIAS)}$ and the bias assist function is activated, the power loss increases.

Thus, VCC pin voltage in operation should be set more than $V_{CC(BIAS)}$ by the following adjustments.

- The turns ratio of the auxiliary winding to the secondary-side winding is increased.
- The value of C2 in Figure 6-1 is increased and/or the value of R1 is reduced.

During all protection operation, the bias assist function is disabled.

9.5 Soft Start Function

Figure 9-16 shows the soft start operational waveforms.

The IC has soft start function to reduce stress of peripheral component and prevent the capacitive mode operation.

During the soft start operation, C6 connected to the CSS pin is charged by the CSS Pin Charge Current, $I_{CSS(C)}$ = −105 μA. The oscillation frequency is varied by the CSS pin voltage. The switching frequency gradually decreases from $f_{(MAX)SS}$* = 500 kHz at most, according to the CSS pin voltage rise. At same time, output power increases. When the output voltage increases, the IC is operated with an oscillation frequency controlled by feedback.

When the IC becomes any of the following conditions, C6 is discharged by the CSS Pin Reset Current, $I_{CSS(R)}$ = 1.8 mA.

- The VCC pin voltage decreases to the operation stop voltage, $V_{CC(OFF)}$ = 8.9 V, or less.
- After AC input voltage turns off, thr CD pin voltage increases to V_{CD1} = 3.0 V or more.
- Any of protection operations in protection mode (OVP, HVP, OLP or TSD) is activated.

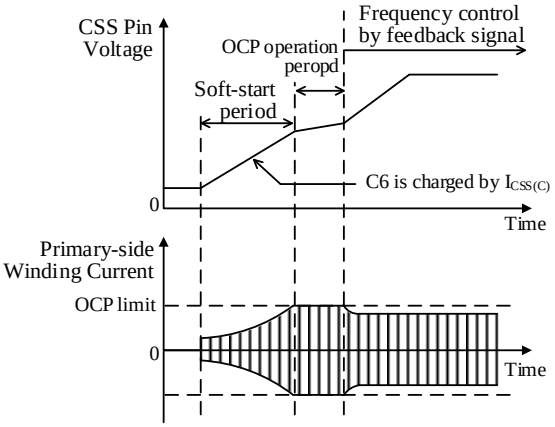


Figure 9-16. Soft-start Operational Waveforms

9.6 Minimum and Maximum Switching Frequency Setting

The minimum switching frequency is adjustable by the value of R5 (R_{CSS}) connected to the CSS pin. The relationship of R5 (R_{CSS}) and the externally adjusted minimum frequency, $f_{(MIN)ADJ}$, is shown in Figure 9-17.

The $f_{(MIN)ADJ}$ should be adjusted to more than the resonant frequency, f_0, under the condition of the minimum mains input voltage and the maximum output power. The maximum switching frequency, f_{MAX}, is determined by the inductance and the capacitance of the resonant circuit. The f_{MAX} should be adjusted to less than the maximum frequency, $f_{(MAX)}$ = 300 kHz.

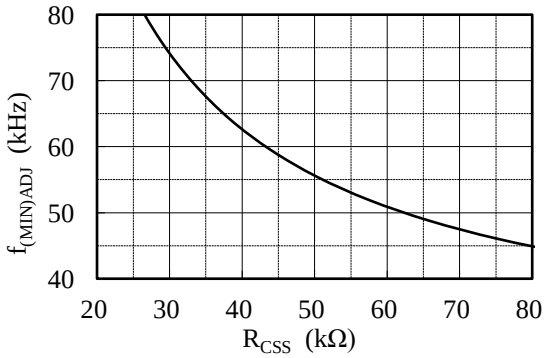


Figure 9-17. R5 (R_{CSS}) vs. $f_{(MIN)ADJ}$

9.7 High-side Driver

Figure 9-18 shows a bootstrap circuit. The bootstrap circuit is for driving to $Q_{(H)}$ and is made by D3, R12 and C12 between the REG pin and the VS pin.

When $Q_{(H)}$ is OFF state and $Q_{(L)}$ is ON state, the VS pin voltage becomes about ground level and C12 is charged from the REG pin.

When the voltage of between the VB pin and the VS pin, V_{B-S}, increases to $V_{BUV(ON)}$ = 6.8 V or more, an internal high-side drive circuit starts operation. When V_{B-S} decreases to $V_{BUV(OFF)}$ = 6.4 V or less, its drive circuit stops operation. In case the both ends of C12 and D4 are short, the IC is protected by $V_{BUV(OFF)}$. D4 for protection against negative voltage of the VS pin

- D3
  D3 should be an ultrafast recovery diode of short recovery time and low reverse current. When the maximum mains input voltage of the apprication is 265VAC, it is recommended to use ultrafast recovery diode of V_{RM} = 600 V

- C11, C12, and R12
  The values of C11, C12, and R12 are determined by total gate charge, Qg, of external MOSFET and voltage dip amount between the VB pin and the VS pin in the burst oscillation mode of the standby mode change.
  C11, C12, and R12 should be adjusted so that the voltage between the VB pin and the VS is more than $V_{BUV(ON)}$ = 6.8 V by measuring the voltage with a high-voltage differential probe.
  The reference value of C11 is 0.47μF to 1 μF.
  The time constant of C12 and R12 should be less than 500 ns. The values of C12 and R22 are 0.047μF to 0.1

* The maximum frequency during normal operation is $f_{(MAX)}$ = 300 kHz.

μF, and 2.2 Ω to 10 Ω.
C11 and C12 should be a film type or ceramic capacitor of low ESR and low leakage current.

- D4
  D4 should be a Schottky diode of low forward voltage, V_F, so that the voltage between the VB pin and the VS pin must not decrease to the absolute maximum ratings of −0.3 V or less.

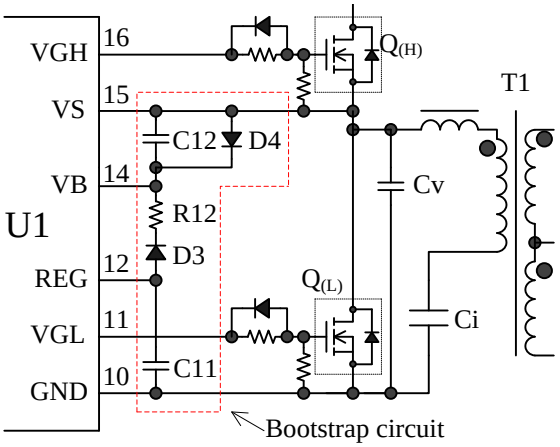


Figure 9-18. Bootstrap Circuit

9.8 Constant Voltage Control Operation

Figure 9-19 shows the FB pin peripheral circuit. The FB pin is sunk the feedback current by the photo-coupler, PC1, connected to FB pin. As a result, since the oscillation frequency is controlled by the FB pin, the output voltage is controlled to constant voltage (in inductance area).

The feedback current increases under slight load condition, and thus the FB pin voltage decreases. While the FB pin voltage decreases to the oscillation stop threshold voltage, $V_{FB(OFF)}$ = 0.20 V, or less, the IC stops switching operation. This operation reduces switching loss, and prevents the increasing of the secondary output voltage. In Figure 9-19, R8 and C9 are for phase compensation adjustment, and C5 is for high frequency noise rejection.

The secondary-side circuit should be designed so that the collector current of PC1 is more than 195 μA which is the absolute value of the maximum source current, $I_{FB(MAX)}$. Especially the current transfer ratio, CTR, of the photo coupler should be taken aging degradation into consideration.

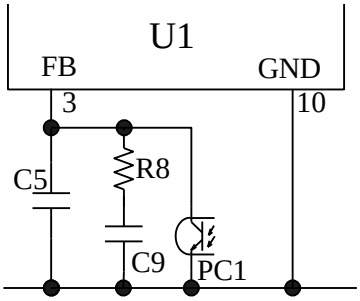


Figure 9-19. FB Pin Peripheral Circuit

9.9 Standby Function

The IC has the standby function that improves efficiency in light load operation. In standby mode, the IC operation shifts to the burst oscillation as shown in Figure 9-20.

The burst oscillation has periodic non-switching intervals. Thus, the burst oscillation mode reduces switching losses. Generally, to improve efficiency under light load conditions, the frequency of the burst oscillation mode becomes just a few kilohertz. In addition, the IC has the Soft-on and the soft-off function in order to suppress rapid and sharp fluctuation of the drain current during the burst oscillation mode. thus, the audible noises can be reduced (see Section 9.9.2). The operation of the IC changes to the standby operation by the external signal (see Section 9.9.1).

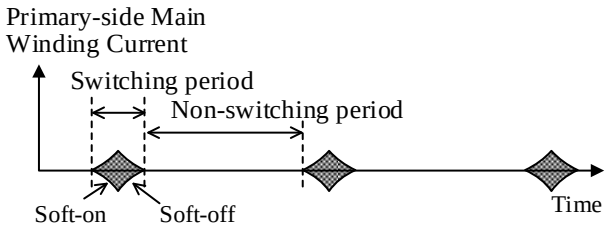


Figure 9-20. Standby Operational Waveforms

9.9.1 Shifting with External Signal

Figure 9-21 shows the standby signal input circuit example. Figure 9-22 shows the standby operational waveforms. When the standby pin shown in Figure 9-21 is set to low level, Q1 turns off, and the MODE pin capacitor, C10, is discharged by the sink current, $I_{MODE(SNK)}$ = 10 μA. When the MODE pin voltage decrease to the MODE Pin Standby Threshold Voltage, $V_{MODE(STB)}$ = 1.50 V, the IC shifts to standby mode. In the standby mode, the IC stops a switching operation while the following conditions are fulfilled:

MODE pin voltage ≤ $V_{MODE(STB)}$ of 1.50 V,
FB pin voltage ≤ $V_{FB(OFF)}$ of 0.20 V, and
SB pin voltage ≤ $V_{SB(OFF)}$ of 0.20 V.

When the standby pin is set to the high level and the SB pin voltage increases to Standby Release Threshold Voltage, $V_{MODE(NRM)}$ = 5.0 V, or more, the IC returns to normal operation.

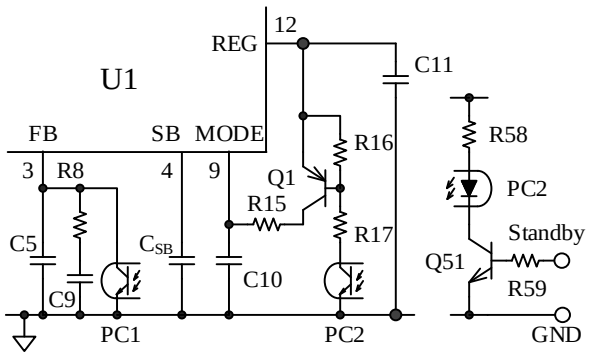


Figure 9-21. Standby Signal Input Circuit Example

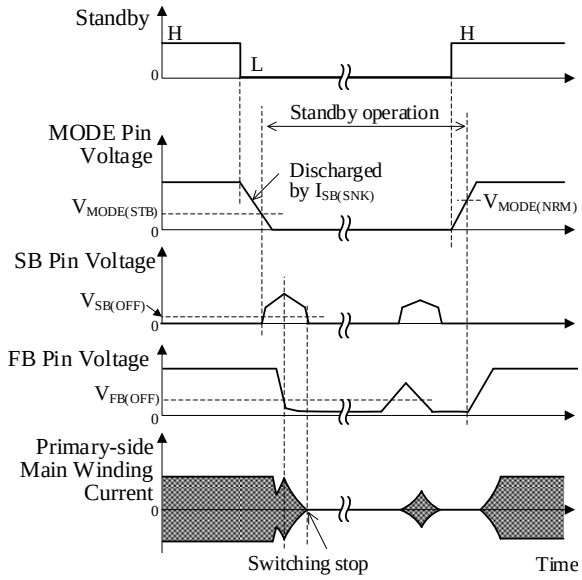


Figure 9-22. Standby Operational Waveforms

9.9.2 Burst Oscillation Operation

In standby operation, the IC operates burst oscillation where the peak drain current is suppressed by soft-on and soft-off function in order to reduce audible noise from transformer. During burst oscillation operation, the switching oscillation is controlled by the SB pin voltage.

Figure 9-23 shows the burst oscillation operational waveforms.

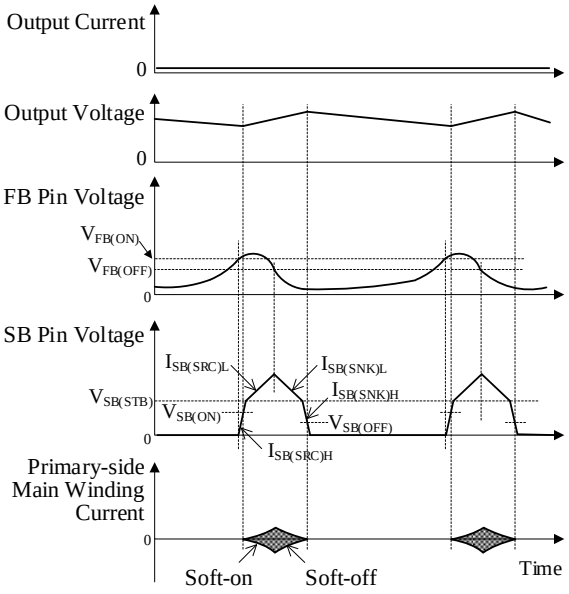


Figure 9-23. Burst Oscillation Operational Waveforms

When the SB pin voltage decreases to $V_{SB(OFF)}$ = 0.20 V or less and the FB pin voltage decreases to $V_{FB(OFF)}$ = 0.20 V or less, the IC stops switching operation, and then the output voltage decreases. Since the output voltage decreases, the FB pin voltage increases. When the FB pin voltage increases to the oscillation start threshold voltage, $V_{FB(ON)}$ = 0.30 V, the SB pin voltage gradually increases because the SB pin capacitor, C_{SB}, is charged by $I_{SB(SRC)H}$ = −15.0 µA. When the SB pin voltage increases to the oscillation start threshold voltage, $V_{SB(ON)}$ = 0.30 V, the IC resumes switching operation, and then the output voltage increases (Soft-on). When the SB pin voltage exceeds $V_{SB(STB)}$ = 0.6 V or more, the charge current of C_{SB} switches to $I_{SB(SRC)L}$ = −5.0 µA. After that, when FB pin voltage decrease to the oscillation stop threshold voltage, $V_{FB(OFF)}$ = 0.20 V, C_{SB} is discharged by $I_{SB(SNK)L}$ = 5.0 µA, and then the SB pin voltage decreases. When the SB pin voltage decreases to less than $V_{SB(STB)}$ = 0.6 V, the discharge current of C_{SB} switches to $I_{SB(SNK)H}$ = 12.5 µA. When the SB pin voltage decreases to $V_{SB(OFF)}$ = 0.20 V again, the IC stops switching operation, and then the output voltage decreases (Soft-off).

The SB pin discharge time in the soft-on and soft-off function depends on the value of C_{SB}. Increasing the C_{SB} value causes the output ripple voltage increase and/or the VCC pin voltage decrease due to the peak drain current reduction and burst period increase. If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.8 V, the power loss increases because the bias assist function is always activated (see Section 9.4).

When adjust the value of C_{SB}, be sure to check the input power, the output ripple voltage, and the VCC pin voltage. The reference value of C_{SB} is about 470 pF to 0.047 µF.

9.10 Automatic Dead Time Adjustment Function

A dead time is a period of time when both of the high- and low-side power MOSFETs turn off. When the dead time is shorter than a voltage resonant period as in Figure 9-24, the power MOSFETs turn on or off during the voltage resonant period. In such case, switching loss increases due to hard switching by the power MOSFETs.

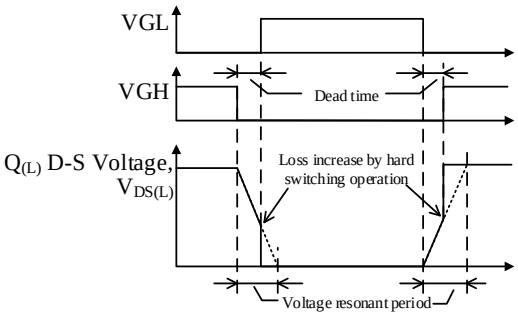


Figure 9-24. ZVS Failure Operation Waveform

To prevent such hard switching, the IC has the automatic dead time adjustment function that the IC detects voltage resonant periods and automatically controls the zero voltage switching (ZVS) operations of $Q_{(H)}$ and $Q_{(L)}$. Even though voltage resonant periods differ according to the power supply specifications (input voltage, output power, etc.), the IC requires no dead time adjustment based on individual power supply specifications because of this function.

As shown in Figure 9-25, a dead time period is determined by the dv/dt period that is defined by the rising and falling voltage waveforms of $V_{DS(L)}$, the drain-to-source voltage of the low-side power MOSFET. The dv/dt period is detected by the VS pin. The ZVS operations of the high- and low-side power MOSFETs are automatically controlled based on this detection system. Note that the automatic dead time adjustment function operates within the period ranging from $t_{d(MIN)}$ = 0.24 µs to $t_{d(MAX)}$ = 1.65 µs.

Also, actual operations must be checked to ensure that power MOSFETs operate with the zero current switching (ZCS) under the following conditions (i.e., check if a period in which drain current flows through a body diode exists for about 600 ns, as in Figure 9-26):

- When an output power is minimum in a maximum input voltage specification.
- When an output power is maximum in a minimum input voltage specification.

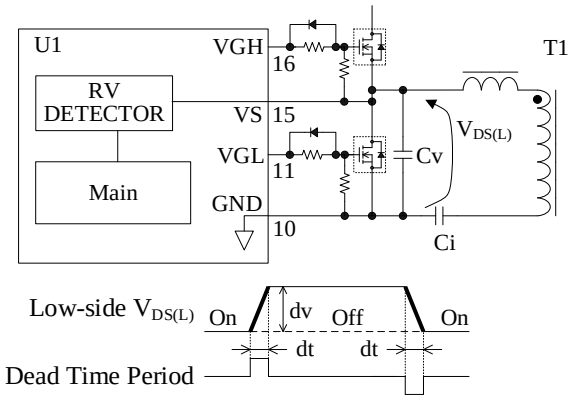


Figure 9-25. VS Pin and Dead Time Period

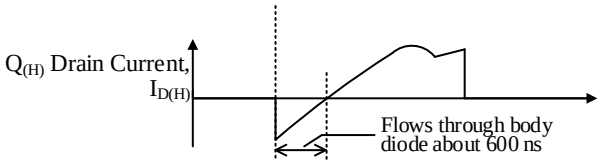


Figure 9-26. Point to Be Checked in ZCS

9.11 Capacitive Mode Detection Function

The current resonant power supply must operate in the inductive area shown in Figure 9-27. In the capacitive area, the power supply enters capacitive mode (see Section 9.1). To prevent such operation, it is generally required to set a minimum oscillation frequency higher than f_0 defined for each power supply specification. The IC has the capacitive mode detection function that constantly maintains its frequency higher than f_0, thereby requiring no setting of minimum oscillation frequencies. Accordingly, enhanced design-friendliness will be added to your application. In addition, using resonant frequency of near f_0 increases the transformer use efficiency.

The RC pin detects a resonant current to determine if a capacitive operation has occurred. When the capacitive mode is detected, the C7 connected to CL pin is charged by $I_{CL(SRC)1}$ = −17 µA. When the CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated and the switching operation stops. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 9.19). As shown in Figure 9-29 and Figure 9-30, the threshold voltage for the capacitive mode detection changes according to the load ranges: V_{RC1} = ±0.10 V or V_{RC2} = ±0.30 V. The capacitive mode detection function is described further below.

- **Period in Which the $Q_{(H)}$ is On**
  Figure 9-28 illustrates the RC pin waveform in the inductive area; Figure 9-29 and Figure 9-30 illustrate the RC pin waveforms in the capacitive area.
  In the inductive area, the RC pin voltage does not

cross over +VRC from high to low during the $Q_{(H)}$ turn-on period (see Figure 9-28).
Conversely, in the capacitive area, the RC pin voltage crosses over the threshold, $+V_{RC1}$ or $+V_{RC2}$, from high to low. At this point, a capacitive mode operation is detected. Then, $Q_{(H)}$ is turned off, whereas $Q_{(L)}$ is turned on (see Figure 9-29 and Figure 9-30).

- **Period in Which the $Q_{(L)}$ is On**
  Contrary to the $Q_{(H)}$case, in the capacitive area, the RC pin voltage crosses over the threshold, $-V_{RC1}$ or $-V_{RC2}$, from low to high during the $Q_{(L)}$ turn-on period. At this point, a capacitive mode operation is detected. Then, $Q_{(L)}$ is turned off, whereas $Q_{(H)}$ is turned on.

Based on the capacitive mode detection on a pulse-by-pulse basis, the IC prevents any capacitive operation by synchronizing the operating frequency with the capacitive mode frequency. R_{OCP}, C3, and R6 must be set so that the absolute value of the RC pin voltage is higher than $|V_{RC2}| = 0.30$ V and is maintained within its absolute maximum rating of ±6 V. In addition to the peripheral component settings required for the OCP function (Section 9.18), the following operations prone to be capacitive mode must be taken into account when you set these components: startup, supply input voltage turn-off, output shorted, and dynamic load effect on a power system.

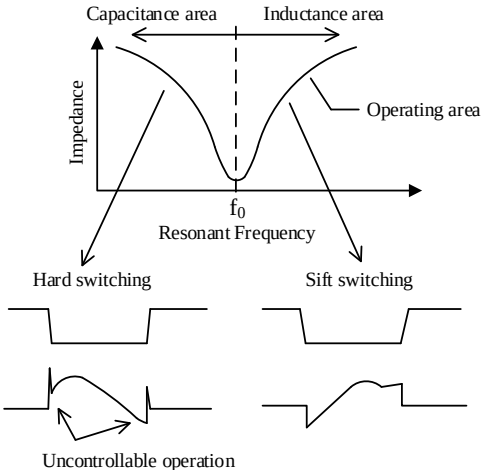


Figure 9-27. Operating Area of Resonant Power Supply

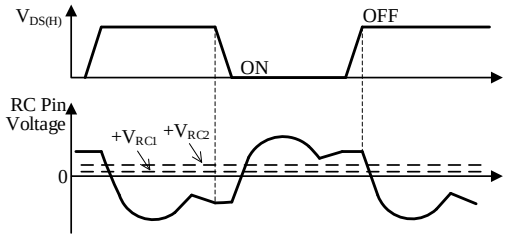


Figure 9-28. RC Pin Voltage in Inductance Area

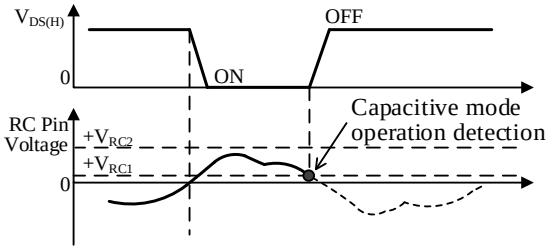


Figure 9-29. High-side Capacitive Mode Detection in Light Load

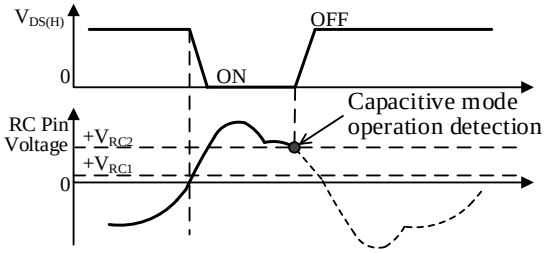


Figure 9-30. High-side Capacitive Mode Detection in Heavy Load

9.12 X-capacitor Discharge Function for AC Input Mode

Generally, a line filter is inserted in the input side of a switching power supply, as illustrated in Figure 9-31.

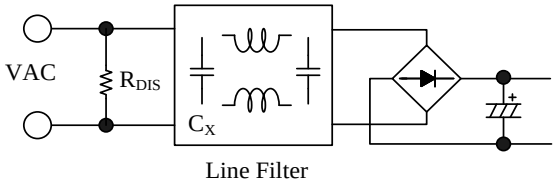


Figure 9-31. Typical Line Filter Circuit

As per IEC 62368-1 safety requirements, the voltage across the capacitor of line filter (i.e., X-capacitor, CX) of ≥300 nF must be decreased to 60 V or less within 2 seconds after AC input voltage cutoff.

Therefore, the discharge resistor, R_{DIS}, is connected in parallel with C_X, as a common approach to meet the requirements. While the AC input voltage is applied, R_{DIS} constantly consumes power. However, the IC implements the X-capacitor discharge function to remove such commonly used R_{DIS}, thus enhancing its circuit efficiency. Power dissipation in R_{DIS}, P_{RDIS}, can be obtained by Equation (7), below:

$$P_{RDIS} = \frac{V_{AC(RMS)}{}^2}{R_{DIS}} \quad (7)$$

Let $V_{AC(RMS)}$ be the effective value of the AC input

voltage.

Hence, if the combined resistance of R_{DIS} = 1 MΩ and the AC input voltage = 265 V, P_{RDIS} becomes about 70 mW.

After an AC input voltage cutoff, the VSEN pin voltage becomes almost constant and the two thresholds, $V_{SEN(OFF)1}$ and $V_{SEN(AC)1}$, are no longer detectable. Then, the CD pin capacitor, C_{CD}, is discharged by $I_{CD(SRC)}$ = –10.2 μA, and the CD pin voltage increases. When the CD pin voltage reaches to V_{CD1} = 3.0 V, the X-capacitor is discharged by the constant current, I_{ST} = 6.0 mA.

The time until the CD pin voltage reaches to V_{CD1} from the cutoff of AC input voltage is delay time, t_{DLY}.

The maximum value of t_{DLY}, t_{DLY_MAX}, can be set by the capacitor of CD pin and is calculated by Equation (9) in Section 9.17.2.

As shown in Figure 9-32, D_{ST1}, D_{ST2}, and R_{ST} are connected to the ST pin from AC input line. The recommend value of R_{ST} is 5.6 kΩ to 10 kΩ. R_{ST} is set at high resistance such that high voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; configure R_{ST} with some serial resistors to reduce each applied voltage.

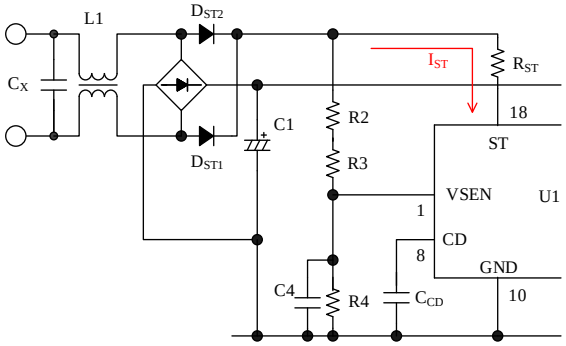


Figure 9-32. ST Pin Peripheral Circuit for AC Input Mode

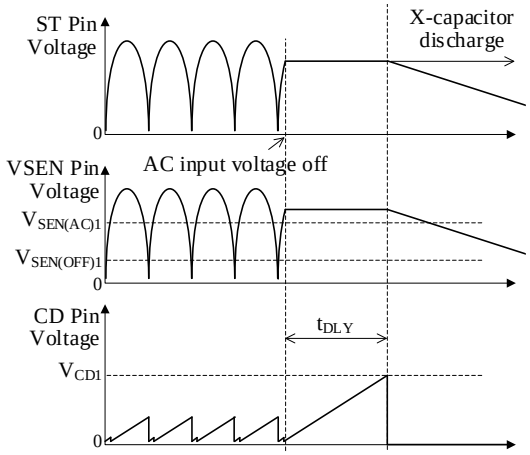


Figure 9-33. X-capacitor Discharge Function Operational Waveform of AC Input Mode

9.13 Input Capacitor Discharge Function for DC Input Mode

After a DC input voltage cutoff, along with the decrease in the input voltage, the voltages of the ST and VSEN pins also decrease. When the VSEN pin voltage decreases to $V_{SEN(OFF)1}$ = 1.000 V or less, the input capacitor is immediately discharged by the constant current, I_{ST} = 6.0 mA.

R_{ST} is connected to the ST pin from DC input line. R_{ST} is 5.6 kΩ to 10 kΩ. R_{ST} is set at high resistance such that high DC voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; configure R_{ST} with some serial resistors to reduce each applied voltage.

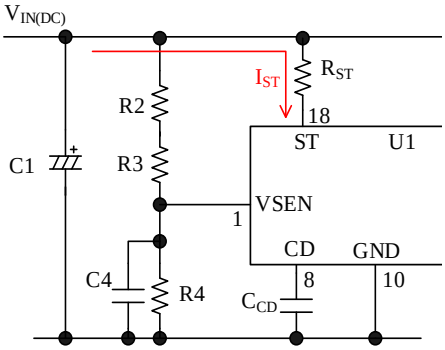


Figure 9-34. ST Pin Peripheral Circuit for DC Input Mode

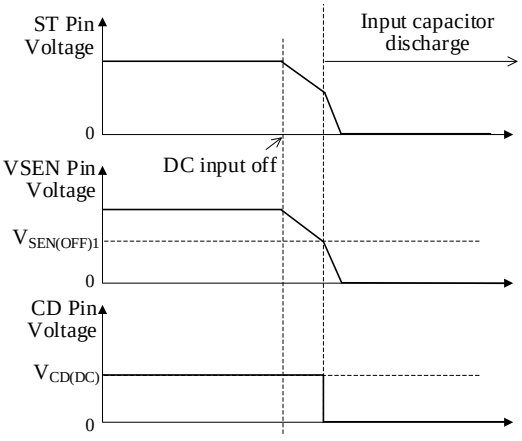


Figure 9-35. Input Capacitor Discharge Function Operational Waveform of DC Input Mode

9.14 Reset Detection Function

In a condition where the output feedback control remains inactive (e.g., during power startup), unbalanced circulating currents for resonant operation control will be incurred. This unbalanced circulating current can cause a hard switching operation that increases the stress of the power MOSFET. The unbalanced circulating current occurs when the power MOSFET turns on at a negative current with the circulating current being not reset during an on-time. The circulating current is a current that flows through the primary side for carrying out a resonant operation. To prevent the hard switching operation, the IC has the reset detection function.

Figure 9-37 represents a high-side operation and the drain current waveforms at each case; normal resonant operation and reset failure. The reset detection function prevents hard-switching operations by extending an on-time until the absolute value of the RC pin voltage increases to $|V_{RC1}| = 0.10$ V or more.

If the on-time is extended longer than the maximum Rest Time, $t_{RST(MAX)} = 5$ µs, the on-time immediately ends and the power MOSFET turns off (see Figure 9-36).

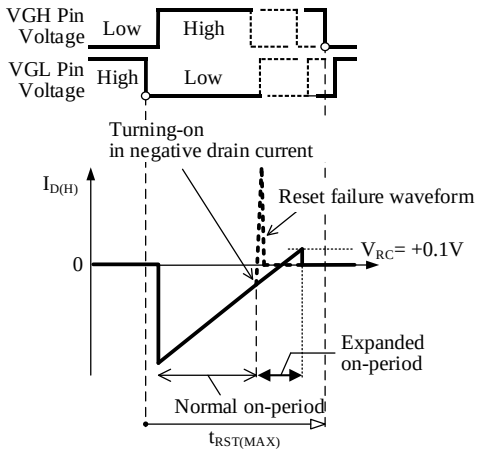


Figure 9-36. Typical Reset Detection during High-side Turn-on Period

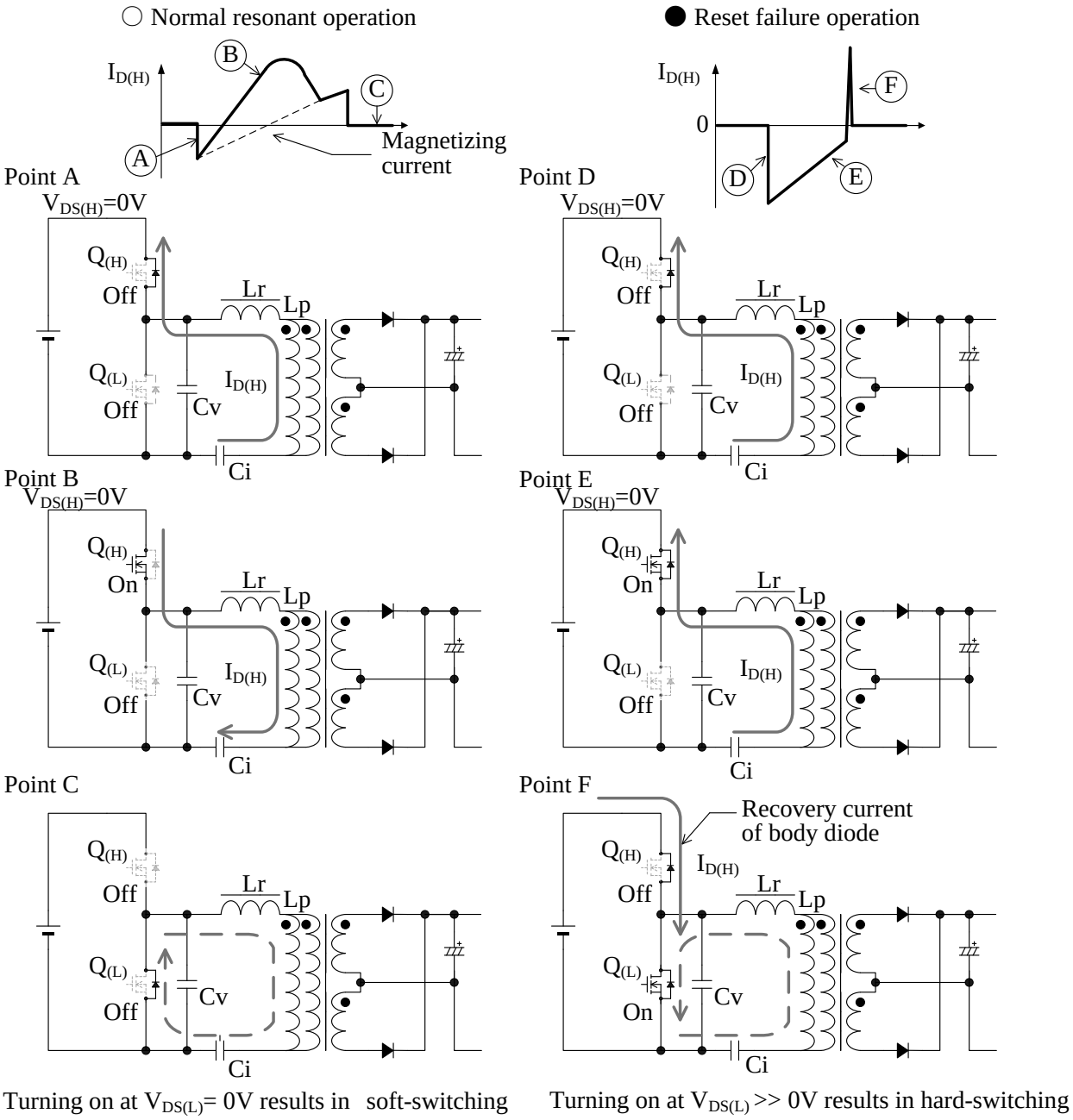


Figure 9-37. High-side Operation and Drain Current Waveforms at Normal Resonant Operation and Reset Failure

9.15 VCC Pin Overvoltage Protection (VCC_OVP)

When the voltage between the VCC and GND pins increases to $V_{CC(OVP)}$ = 32.0 V or more, the VCC pin overvoltage protection (VCC_OVP) is activated. Then, the IC stops its switching operation. When the VCC_OVP activates, the bias assist function is disabled and VCC pin voltage decreases. Then the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.9 V, the undervoltage lockout (UVLO) function is activated, and the IC reverts to the state before startup again.

After that, the startup circuit activates, and the VCC pin voltage increases to $V_{CC(ON)}$ = 17.0 V, and the IC starts operation. The IC repeats the restart and stop during the VCC_OVP operation. When the causes of the VCC_OVP condition are eliminated, the IC automatically returns to normal operation.

When the VCC pin voltage is supplied through the auxiliary winding of the transformer, the VCC pin voltage is proportional to the output voltage. As a result, the VCC pin can detect a secondary-side overvoltage condition caused by abnormality (e.g., when an output voltage detection circuit is open). The approximate value of the secondary-side output voltage, $V_{OUT(OVP)}$, at the VCC_OVP activation can be calculated by Equation (8) below.

$$V_{OUT(OVP)} = \frac{V_{OUT(NRM)}}{V_{CC(NRM)}} \times 32(V) \quad (8)$$

where, $V_{OUT(NRM)}$ is the secondary-side output voltage in normal operation, and $V_{CC(NRM)}$ is VCC pin voltage in normal operation.

9.16 REG Pin Overvoltage Protection (REG_OVP)

The IC has REG pin overvoltage protection (REG_OVP) for the overvoltage of the REG pin.

Figure 9-38 shows the REG_OVP operational waveforms. When the REG pin voltage increases to the REG Pin OVP Threshold Voltage, $V_{REG(OVP)}$ = 12.4 V, the REG_OVP is activated. Then, the IC stops switching operation and fixes the REG pin voltage to ground level.

When the REG_OVP activates, the bias assist function is disabled and VCC pin voltage decreases. Then the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.9 V, the undervoltage lockout (UVLO) function is activated, and the IC reverts to the state before startup again.

After that, the startup circuit activates, and the VCC pin voltage increases. When the VCC pin voltage reaches to $V_{CC(ON)}$ = 17.0 V, the VCC pin voltage decreases because the IC starts operation. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the FB pin voltage increases and switching operation starts.

When the switching operation starts at the RC pin voltage within V_{RC1} = ±0.10 V, the CL pin capacitor, C7, is rapidly charged by $I_{CL(SRC)2}$ = −135 μA. When the CL pin voltage reaches to $V_{CL(OLP)}$ = 4.2 V, the IC stops switching operation. Then, the IC restarts after the VCC pin voltage decreases to $V_{CC(OFF)}$. In this way, the IC repeats an intermittent operation by the CL pin protection and the UVLO. The IC repeats the restart and stop during the VCC_OVP operation. When the causes of the REG_OVP condition are eliminated, the IC automatically returns to normal operation.

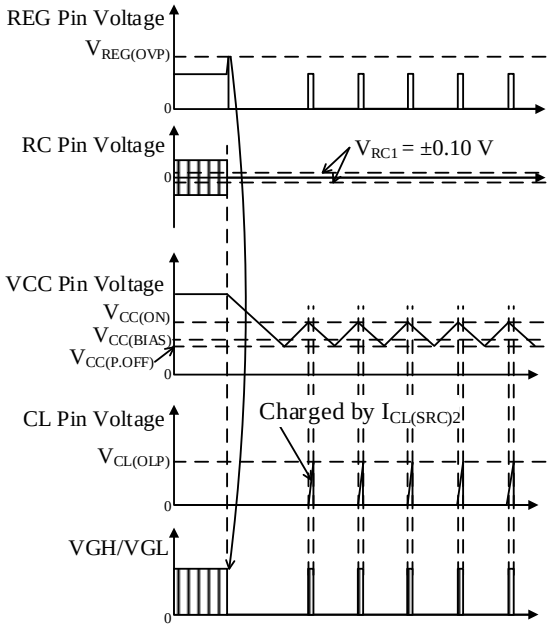


Figure 9-38. REG_OVP Operational Waveforms

9.17 Input Voltage Protection

The input voltage protection includes two protections: the high-voltage protection (HVP) for higher supply input voltages, and the undervoltage protection (UVP) for lower supply input voltages. These protections suppress the component overheating and thermal damage caused by overcurrent or overvoltage.

The VSEN pin is used for detecting an input voltage. According to the levels that the VSEN pin voltage reaches, the IC turns on and off its switching operation. Sections 9.17.1 and 9.17.2 describe the two functions, HVP and UVP, respectively.

9.17.1 Input Overvoltage Protection (HVP)

When the VSEN pin voltage, V_{VSEN}, increases along with an input voltage rise from its steady-state level and reaches the VSEN pin HVP threshold voltage, $V_{SEN(HVP)}$ = 5.6 V or more, the high-voltage protection (HVP) is activated. Then, the switching operation stops.

During the HVP operation, the intermittent operation by UVLO is repeated. When $V_{VSEN} \leq V_{SEN(HVP)}$ after the input voltage lowers, the IC returns to its normal operation.

9.17.2 Input Undervoltage Protection (UVP)

The IC has the undervoltage protection (UVP). The following subsections contain the operations of the AC and DC input modes.

- **AC Input Mode**

Figure 9-39 illustrates the VSEN pin and its peripheral circuit, whereas Figure 9-40 depicts operational waveforms of the input voltage protection.

Along with an AC input voltage fall from its steady-state level, the VSEN pin voltage, V_{VSEN}, decreases. When the VSEN pin voltage decreases to $V_{SEN(OFF)1}$ = 1.000 V or less, and when this condition persists for the delay time, t_{DLY} or longer, even with the IC being in an operation state (i.e., $V_{CC(OFF)} \leq V_{CC}$), the switching operation stops.

When $V_{CC} \geq V_{CC(ON)}$ and $V_{VSEN} \geq V_{SEN(ON)}$ of 1.200 V after the AC input voltage rises, the IC returns to its normal operation.

The maximum delay time, t_{DLY_MAX}, can be calculated by Equation (9).

$$t_{DLY\_MAX} = \frac{V_{CD1} \times C_{CD}}{|I_{CD(SRC)}|} \quad (9)$$

Where,

V_{CD1} is CD Pin Threshold Voltage 1 (3.0 V),

C_{CD} is the capacitance value of CD pin connected capacitor (about 0.1µF to 0.47µF), and

$I_{CD(SRC)}$ is CD Pin Source Current (–10.2 µA)

For example, if C_{CD} is 0.1µF,

$$t_{DLY\_MAX} = \frac{3.0\ V \times 0.1\mu F}{|-10.2\ \mu A|} \approx 29.4\ ms$$

If an input resistance or a forward voltage of a rectifier diode is not factored into, the equation below determines a reference effective value of the AC input voltage at which the HVP or UVP is activated:

$$V_{AC(OP)} = \frac{1}{\sqrt{2}} \times V_{SEN(TH)} \times \left(1 + \frac{R2 + R3}{R4}\right) \quad (10)$$

Where, $V_{DC(OP)}$ is the effective value of AC input voltage which HVP and UVP are activated, and $V_{SEN(TH)}$ is the VSEN pin threshold voltage of (see Table 9-1).

Table 9-1. VSEN Pin Threshold Voltage

Parameter	Symbol	Value (Typ.)
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$	5.6 V
VSEN Pin Threshold Voltage (On)	$V_{SEN(OFF)1}$	1.000 V
VSEN Pin Threshold Voltage (Off)	$V_{SEN(ON)}$	1.200 V

As shown in Figure 9-39, the input voltage, divided by the detection resistors is applied to the VSEN pin.

The reference value of R2 is about 10 MΩ. The resistors of R2 and R3 are set at high resistance such that high voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; configure R2 and R3 with some serial resistors to reduce each applied voltage.

The reference capacitance of C4, the noise filter capacitor shown in Figure 9-39 is 1000 pF to 0.01 µF. R2 to R4, and C4 should be selected based on operation performance in an actual application.

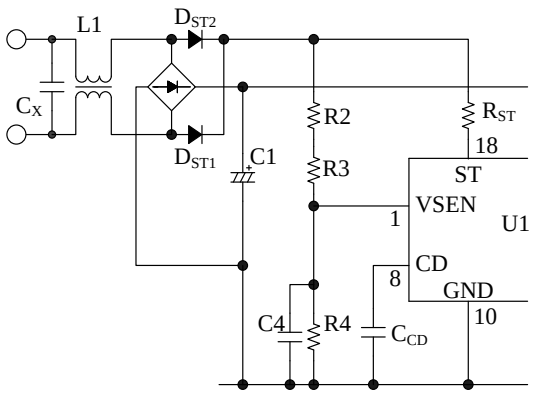


Figure 9-39. VSEN Pin Pherepheral Circuit

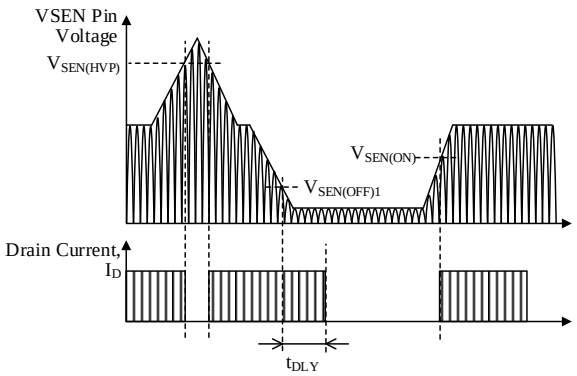


Figure 9-40. Input Voltage Protection Operational Waveforms

● **DC Input Mode**

Along with a DC input voltage fall from its steady-state level, the VSEN pin voltage decreases. When the VSEN pin voltage, V_{VSEN}, decreases to the off threshold, $V_{SEN(OFF)1}$ = 1.000 V or less, even with the IC being in an operation state (i.e., $V_{CC(OFF)} \leq V_{CC}$), the switching operation stops immediately.

When $V_{CC} \geq V_{CC(ON)}$ and $V_{VSEN} \geq V_{SEN(ON)}$ of 1.200 V after the DC input voltage rises, the IC returns to its normal operation.

9.18 Overcurrent Protection (OCP)

The overcurrent protection (OCP) detects the peak drain current of the power MOSFET on a pulse-by-pulse basis, and limits the output power.

The value of the shunt capacitor, C3, shown in Figure 9-41, is set to be considerably smaller than that of the current resonant capacitor, Ci. Thus, the loss of detection resistor R_{OCP} is minimized because the detection current which is shunted from the primary-side winding is low. And this allows R_{OCP} to be smaller in size.

There is no simplified method to obtain an accurate value of resonant current with parameters such as input and output conditions of the power supply. Therefore, R_{OCP}, R6 and C3 must be adjusted based on the operational performance checked with an actual board. Here are reference constants for R_{OCP}, C3, R6, and C8 and their adjustment methods:

● C3 and R_{OCP}

C3 is 100pF to 330pF (around 1 % of Ci value);
R_{OCP} is around 100 Ω.
Given the current of the high-side power MOSFET in on state as $I_{D(H)}$. R_{OCP} is calculated by Equation (11).
The detection voltage across R_{OCP} is also used for the capacitive mode detection described in Section 9.11. Therefore, R_{OCP} and C3 require adjustments for using in both the overcurrent detection and capacitive mode detection.

$$R_{OCP} \approx \frac{|V_{RC(L)}|}{I_{D(H)}} \times \left(\frac{C3 + Ci}{C3}\right) \quad (11)$$

● R6 and C8

These are used for reducing high-frequency noises. R6 is 100 Ω to 470 Ω; C6 is 100 pF to 1000 pF.

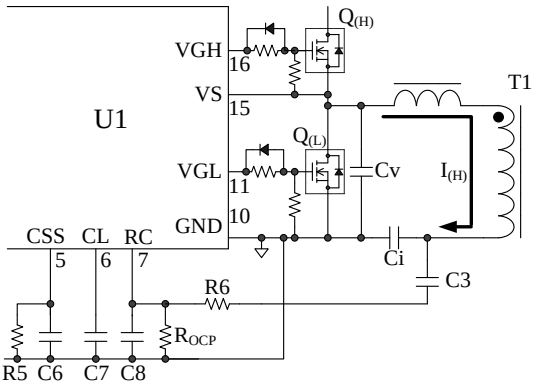


Figure 9-41. RC Pin Peripheral Circuit

The OCP includes two types that are activated at different current levels.

9.18.1 Overcurrent Protection 1 (OCP1)

When the current through the power MOSFET increases and the absolute value of the RC pin voltage rises above $|V_{RC(L)}|$ = 1.90 V, the overcurrent protection 1 (OCP1) is activated, and CSS pin capactor, C6, is discharged by sink current, $I_{CSS(L)}$ = 1.8 mA. Then, the IC increases the switching frequency to suppress the output power. When the absolute value of the RC pin voltage decrease to $\leq |V_{RC(L)}|$ during discharging C6, the IC stops to discharge of C6.

9.18.2 Overcurrent Protection 2 (OCP2)

The overcurrent protection 2 (OCP2) protects the power MOSFET from having large currents. When the absolute value of the RC pin voltage rises above $|V_{RC(S)}|$ = 2.80 V, the OCP2 is activated to immediately invert the on/off states of the power MOSFETs. At the same time, and CSS pin capactor, C6, is discharged by $I_{CSS(S)}$ = 20.5 mA, and the switching frequency is promptly increased for suppressing the output power. When the output power decreases and the RC pin voltage decreases to $|V_{RC(S)}|$ or less, the IC shifts into the OCP1 operation.

9.19 Overload Protection (OLP)

Figure 9-42 shows the overload protection (OLP) operational waveforms. When the absolute value of RC pin voltage increases to $|V_{RC(L)}|$ = 1.90 V by increasing of output power, the overcurrent protection 1 (OCP1) is activated. After that, the CL pin capacitor, C7, is charged by $I_{CL(SRC)1}$ = −17 μA. When the OCP1 state continues and the CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated. When the CL pin voltage becomes the threshold voltage of OLP, $V_{CL(OLP)}$ = 4.2 V, the OLP is activated and the switching operation stops. During the OLP operation, the IC repeats the intermittent operation by UVLO. When the causes of the OLP condition are eliminated, the IC automatically returns to normal operation.

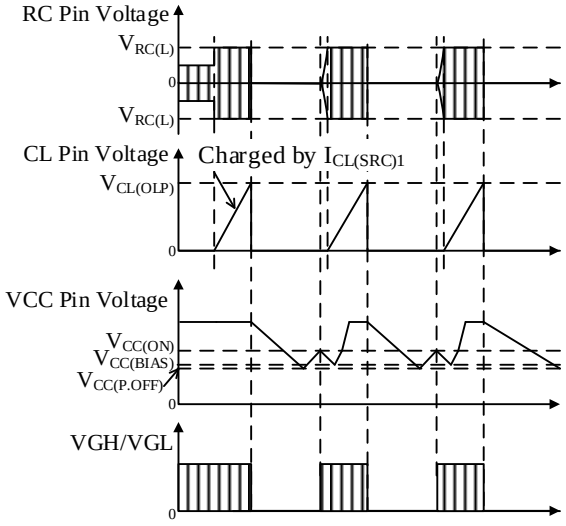


Figure 9-42. OLP Operational Waveforms

9.20 Thermal Shutdown (TSD)

When the control circuit temperature reaches the Thermal Shutdown Temperature $T_{J(TSD)}$ = 140 °C (min.), the thermal shutdown (TSD) is activated. Then, the IC stops their switching operations. After the switching operation stops, the VCC pin voltage decreases. In the condition where $V_{CC(P.OFF)}$ = 8.9 V and the control circuit temperature falls below $T_{J(TSD)}$, TSD is released and the IC restarts.

10. Design Notes

10.1 External Components

Take care to use the proper rating and proper type of components.

10.1.1 Input and Output Electrolytic Capacitors

Apply proper design margin to ripple current, ripple voltage, and temperature rise. A low-ESR capacitor is recommended to reduce ripple voltage, in terms of designing switch-mode power supplies.

10.1.2 Resonant Transformer

The resonant power supply uses the leakage inductance of a transformer. Therefore, to reduce influences from eddy current and skin effect, use a bundle of fine litz wires as the wire of the transformer.

10.1.3 Current Detection Resistor, R_{OCP}

High-frequency switching currents flow through the current detection resistor, R_{OCP}; therefore, be sure to use a resistor with low internal inductance and allowable power dissipation.

10.1.4 Current Resonant Capacitor, Ci

Because large resonant current flows through Ci, it should be a capacitor that supports high-current applications with small losses such as a polypropylene film capacitor. High-frequency current flows through Ci; therefore, capacitor-specific frequency characteristics must also be taken into account.

10.1.5 Gate Pin Peripheral Circuit

The VGH and VGL pins are gate drive outputs for external power MOSFETs. These peak source and sink currents are –540 mA and 1.50 A, respectively.

To make a turn-off speed faster, connect the diode, D_S, as shown in Figure 10-1. When R_A and D_S is adjusted, the following contents should be taken into account: the power losses of power MOSFETs, gate waveforms (for a ringing reduction caused by a pattern layout, etc.), and EMI noises. To prevent the malfunctions caused by steep dv/dt at turn-off of power MOSFETs, connect R_{GS} of 10 kΩ to 100 kΩ between the gate and source pins of the power MOSFET with a minimal length of PCB traces. When these gate resistances are adjusted, the gate

waveforms should be checked that the dead time is ensured as shown in Figure 10-2.

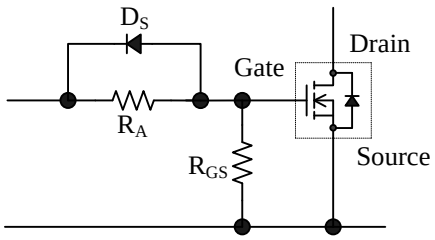


Figure 10-1. Power MOSFET Peripheral Circuit

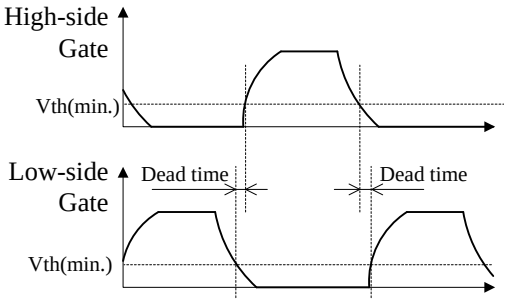


Figure 10-2. Dead Time Confirmation

10.2 PCB Trace Layout and Component Placement

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. High-frequency and high-voltage current loops (see Figure 10-3) should be as small and wide as possible in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

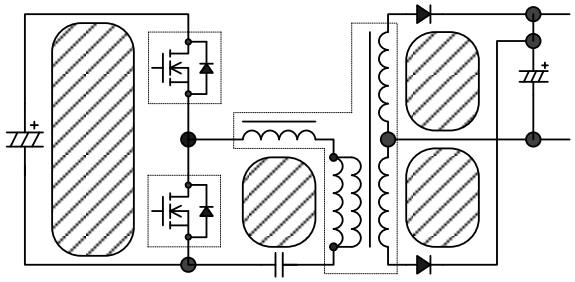


Figure 10-3. High-frequency Current Loop

The following considerations should be taken into account in designing pattern

layouts for your application. Figure 10-4 is a peripheral circuit example of the IC.

1) Main Circuit Trace Layout
Main traces where switching currents pass through should be as wide and looped small as possible.

2) Logic Ground Trace Layout
If a large current flows through a logic ground, electric potential across the logic ground may vary and thus cause the IC to malfunction. Logic ground traces should be designed as close as possible to the GND pin, at a single-point ground (or star ground) that is separated from the main circuit.

3) Peripheral Connections to VCC Pin
Traces connected to the VCC pin should be looped small as possible because the pin supplies power to the IC. If the IC and the electrolytic capacitor C2 are distant from each other, connect the film capacitor C_f (about 0.1 μF to 1.0 μF) between the VCC and GND pins with a minimal length of traces.

4) Components for Logic Control System
These components should be placed close to the IC, and be connected to the corresponding pin of the IC with as short trace as possible.

5) Peripheral Connections to VB Pin
The components of the bootstrap circuit connected between the VCC and VB pins (D3, R12) should be placed as close as possible to the IC. The capacitor, C21, connected between the VB and VS pins should also be placed with a minimal length of traces.

6) Secondary Rectifier Smoothing Circuit
This is the secondary-side main circuit in which switching current flows, should be wide and looped small as possible.

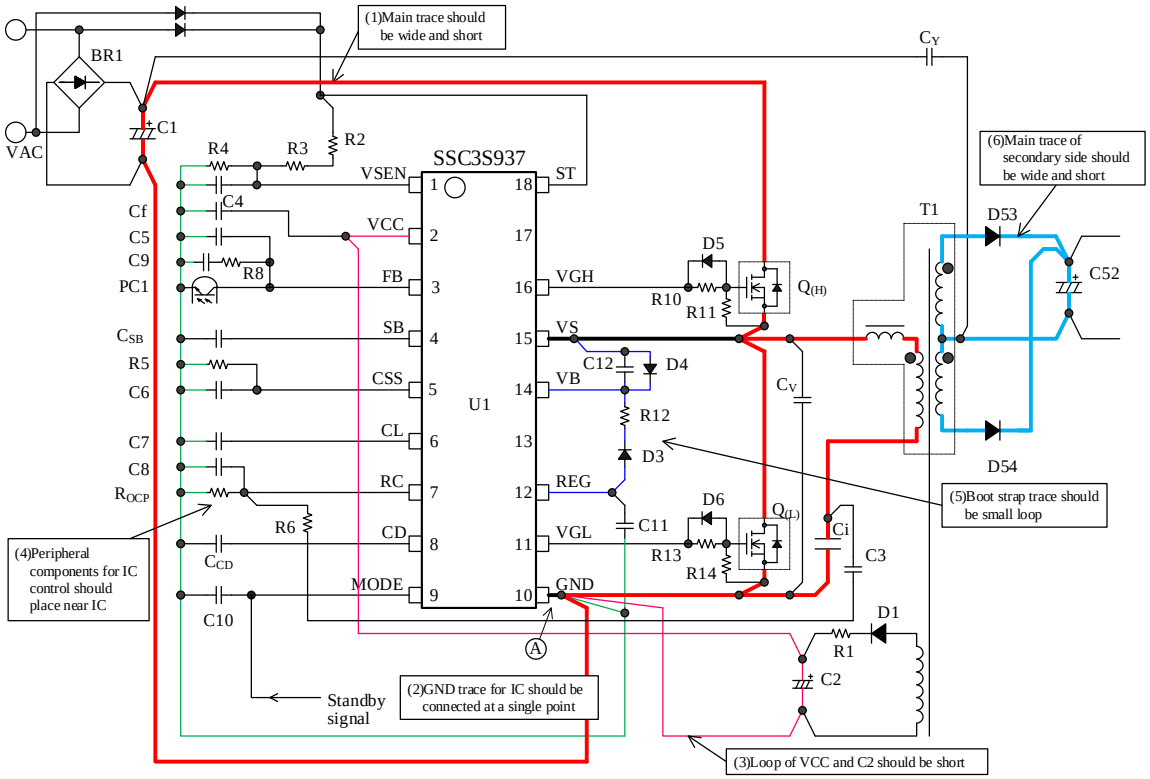


Figure 10-4. Example Connections to IC and Its Peripheral Circuit

11. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of circuit using SSC3S937.

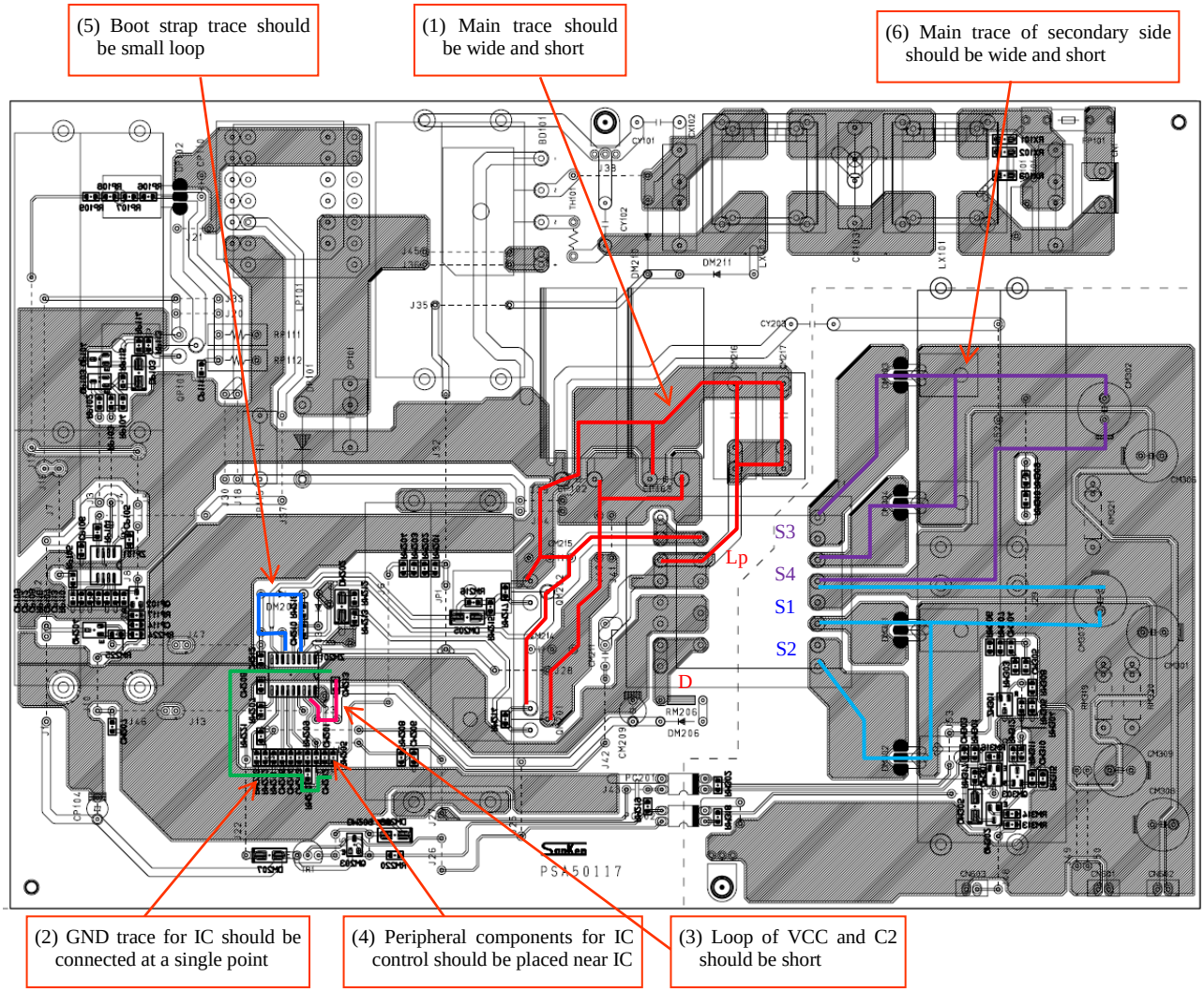


Figure 11-1. PCB Pattern Layout Example

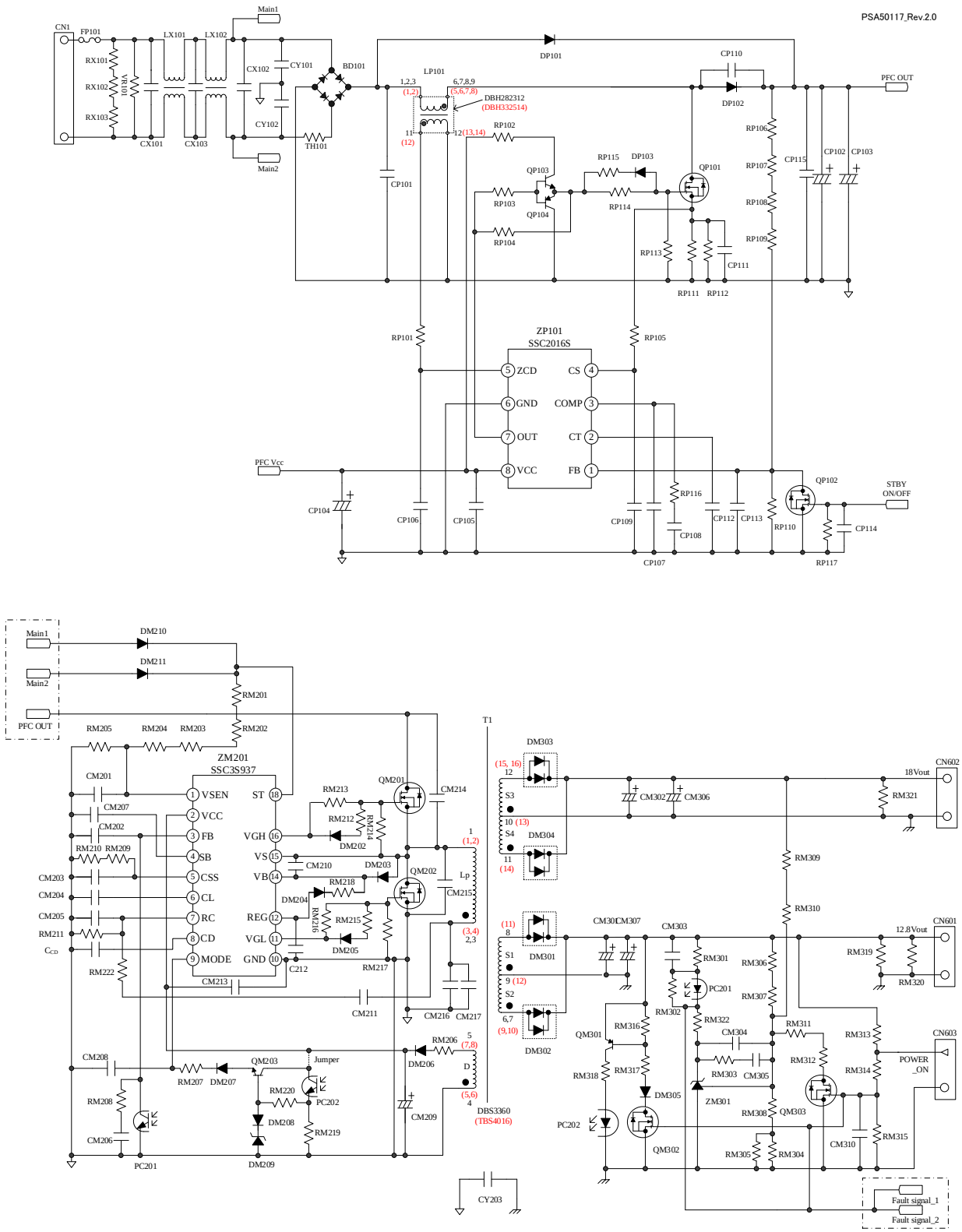


Figure 11-2. PCB Pattern Layout Example Circuit

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