STA7130MPR Series Driver ICs for 2-Phase Stepper Motor Unipolar Drives

Introduction

The STA7130MPR series are driver ICs for driving unipolar mode, 2-phase stepper motors. These drivers are designed for low-voltage (up to 44 V output) motor applications. The series provides a range of maximum output currents from 1 to 2 A, in pin-compatible proprietary (model STA) packages, allowing system optimization with reduced printed circuit board requirements. The logic section provides four modes of operation: forward and reverse normal drive rotation, outputs-off free spin (coast), and electronic braking.

The innovative multi-chip internal structure separates the main logic IC (MIC) from the four output N-channel power MOSFETs. This results in lower thermal resistance and greater efficiency. PWM control allows constant-current control of output while reducing heat generation and power losses by synchronous rectification. The rich set of protection features helps to realize low component counts, and high performance-to-cost power management.

Not to scale

Figure 1. STA7130MPR series packages are 18-pin, fully molded ZIPs, with offset pins for through hole mounting.

Features and Benefits

- Power supply voltages, V_{BB}: 46 V(max), 10 to 44 V normal operating range
- Maximum output currents: 1 A, 1.5 A, 2 A
- Clock-in drive between 2 phase and 2W1-2 step (full to eighth step modes)
- Built-in Detection Resistance feature for motor current detection
- All STA7130MPR series variants are pin-compatible
- ZIP type 18-pin molded package (STA package)
- Self-excitation PWM current control with fixed off-time: automatic 3-level PWM off-time shifting, based on the current setting ratio
- Built-in synchronous rectification circuit reduces losses at PWM switching
- Synchronous PWM chopping function prevents motor noise in Hold mode
- Sleep mode for reducing the IC input current in stand-by state
- Built-in protection circuitry against opens/shorts in motor coil

The product lineup for the STA7130MPR series provides the following:

Part Number	Maximum Output Current (A)	Detection Resistance	Protection (OCP, TSD, Open/Short Load)
STA7130MPR	1	○	○
STA7131MPR	1.5	○	○
STA7132MPR	2	○	○

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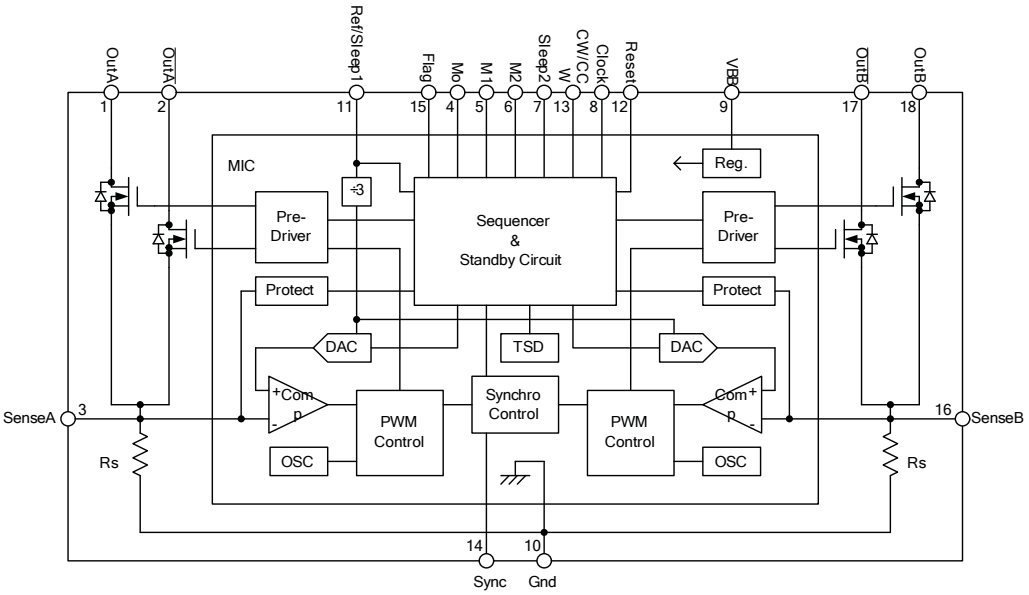
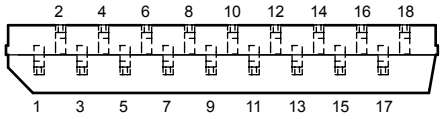
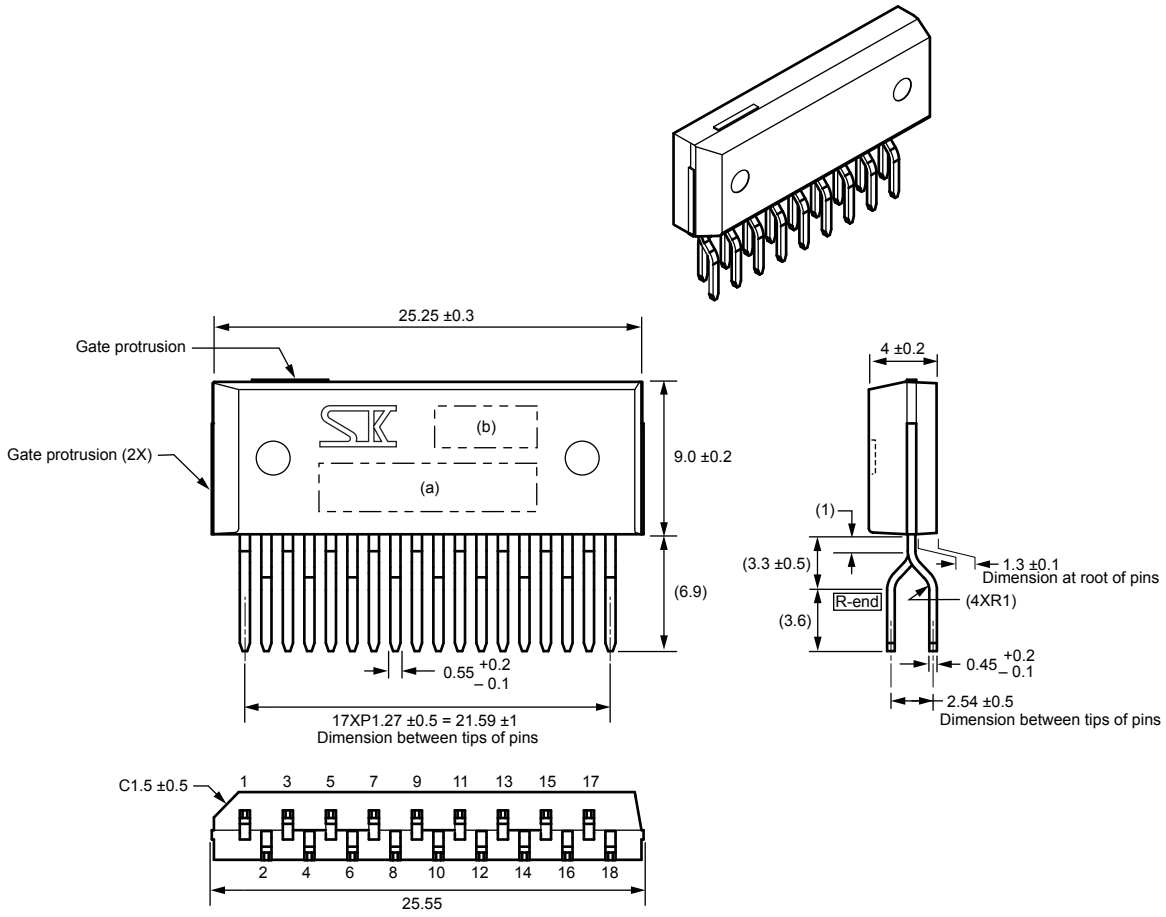
Functional Block Diagrams





Pin Number.	Symbol	Function
1	OutA	Output of phase A
2	$\overline{\text{OutA}}$	Output of phase $\overline{\text{A}}$
3	SenseA	Phase A current sensing
4	Mo	Monitor output in 2-phase-excitation state
5	M1	Motor current excitation control input
6	M2	
7	Sleep2	Sleep2 setup input
8	Clock	Step clock input
9	VBB	Power supply (motor power supply)
10	Gnd	Product ground
11	Ref/Sleep1	Control current and Sleep1 setup input
12	Reset	Reset for internal logic
13	CW/CCW	Forward/reverse switch input
14	Sync	Synchronous PWM control switch input
15	Flag	Protection circuits monitor output
16	SenseB	Phase B current sensing
17	$\overline{\text{OutB}}$	Output of phase $\overline{\text{B}}$
18	OutB	Output of phase B

Package Outline Drawing



Pin core material: Cu
Pin plating: Ni, with solder dip

Dimensions in millimeters

Branding codes:
(a) Type: 713xMPR
Where: x is the current rating
(0 = 1 A, 1 = 1.5 A, or 2 = 2 A)
(b) Lot Number: *YMDD*
Where: Y is the last digit of the year of manufacture
M is the month (*1* to *9, O, N, D*)
DD is the date

Leadframe plating Pb-free. Device composition includes high-temperature solder (Pb >85%), which is exempted from the RoHS directive.

Absolute Maximum Ratings, valid at T_A = 25°C

Characteristic	Symbol	Notes		Rating	Unit
Motor Power Supply Voltage	V_M			46	V
Main Power Supply Voltage	V_{BB}			46	V
Output Current	I_O	STA7130MPR	Control current value	1.0	A
		STA7131MPR		1.5	A
		STA7132MPR		2.0	A
Logic Input Voltage	V_{LI}			–0.3 to 6	V
Logic Output Voltage	V_{LO}			–0.3 to 6	V
REF Input Voltage	V_{REF}			–0.3 to 6	V
Sense Voltage	V_{RS}			±1	V
Allowable Power Dissipation	P_D	No heatsink		3.5	W
Junction Temperature	T_J			150	°C
Operating Ambient Temperature	T_A			–20 to 80	°C
Storage Temperature	T_{STG}			–30 to 150	°C

Recommended Operating Conditions

Characteristic	Symbol	Conditions	Min.	Max.	Unit
Motor Power Supply Voltage	V_M		–	44	V
Main Power Supply Voltage	V_{BB}		10	44	V
Case Temperature	T_C	Measured at the root of pin 10; no heatsink	–	85	°C

ELECTRICAL CHARACTERISTICS[1] valid at T_A = 25°C, V_{BB} = 24 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Main Power Supply Current	I_{BB}	Operating	–	–	10	mA
	I_{BBS}	In Sleep1 or Sleep2 mode	–	–	3	mA
MOSFET Breakdown Voltage	V_{DSS}	V_{BB} = 44 V, I_D = 1 mA	100	–	–	V
Output MOSFET On Resistance	$R_{DS(on)}$	STA7130MPR	–	0.1	0.13	Ω
		STA7131MPR	–	0.7	0.85	Ω
		STA7132MPR	–	0.25	0.4	Ω
Output MOSFET Body Diode Forward Voltage	V_F	STA7130MPR	–	0.18	0.24	V
		STA7131MPR	–	0.85	1.1	V
		STA7132MPR	–	0.95	1.2	V
Maximum Input Frequency	f_{clk}	Input clock duty cycle = 50%	250	–	–	kHz
Logic Input Voltage	V_{IL}		0	–	0.7	V
	V_{IH}		2.3	–	5.5	V
Logic Input Current	I_{IL}		–	±1	–	µA
	I_{IH}		–	±1	–	µA
Logic Output Voltage	V_{LO}	I_{LO} = 5 mA	–	–	0.8	V
Logic Output Current	I_{LO}	V_{LO} = 0.8 V	–	–	5	mA
Ref/Sleep1 Pin Input Voltage	V_{REF}		0.1	–	0.9	V
	V_{REFS}	In Sleep1 mode; output off, I_{BBS} in specification, sequencer enabled	2.0	–	5.5	V
Ref/Sleep1 Pin Input Current	I_{REF}		–	±10	–	µA
Reference Voltage Ratio[2]	Mode F	V_{REF} / 3 ≈ V_{SENSE} = 100%	–	100	–	%
	Mode E		–	98.1	–	%
	Mode C		–	92.4	–	%
	Mode A		–	83.1	–	%
	Mode 8		–	70.7	–	%
	Mode 6		–	55.5	–	%
	Mode 4		–	38.2	–	%
	Mode 2		–	19.5	–	%
Sense Voltage	V_{SENSE}	Reference Voltage Ratio = 100%	V_{REF} / 3 – 0.03	V_{REF} / 3	V_{REF} / 3 + 0.03	V
Sense Resistor[3]	R_S	STA7130MPR	0.296	0.305	0.314	Ω
		STA7131MPR	0.199	0.205	0.211	Ω
		STA7132MPR	0.150	0.155	0.160	Ω
PWM Minimum On-Time (Blanking Time)	$t_{on(min)}$		–	1.5	–	µs
PWM Off-Time	t_{POFF1}	Mode 8, A, C, E, or F	–	11.5	–	µs
	t_{POFF2}	Mode 4 or 6	–	8.5	–	µs
	t_{POFF3}	Mode 2	–	7	–	µs

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ELECTRICAL CHARACTERISTICS[1] (continued) valid at T_A = 25°C, V_{BB} = 24 V; unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Sleep-to-Enable Recovery Time	t_{SE}	From Sleep1 or Sleep2 mode		100	–	–	µs
Switching Time	t_{con}	From input clock edge to output on		–	1.4	–	µs
	t_{coff}	From input clock edge to output off		–	0.7	–	µs
Overcurrent Detection Voltage[4]	V_{OCP}	Motor coil short-circuited		0.65	0.7	0.75	V
Overcurrent Detection Current	I_{OCP}	STA7130MPR	Measured as V_{OCP} / R_S	–	2.3	–	A
		STA7131MPR		–	3.5	–	A
		STA7132MPR		–	4.6	–	A
Load Disconnection Detect Time	t_{OPP}	Starting from PWM-off edge		–	2	–	µs
Thermal Shutdown Temperature	T_{TSD}	Measurement point on the unbranded side of the device case (at a saturation temperature)		–	125	–	ºC

[1]The polarity value for current specifies a sink as "+ ," and a source as "−," referencing the IC.
[2]The Reference Voltage Ratio proportions are the same as the SLA7070M series for corresponding modes.
[3]Includes the inherent bulk resistance (approximately 5 mΩ) of the resistor itself.
[4]$V_{SENSE} \geq V_{OCP}$ always.

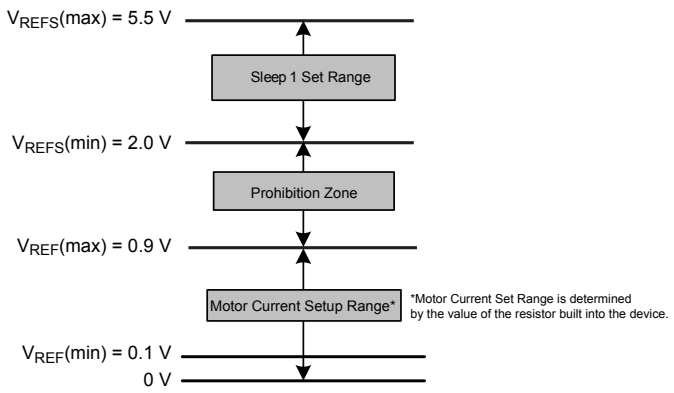


Figure 1. Reference Voltage Setting (V_{REF}, Ref/Sleep1 Pin). Please pay extra attention to the change-over between the Motor Current Setup range, and the Sleep1 Set range. V_{OCP} = 0.7 V is equivalent to V_{REF} = 2.1 V, but will be as a state of Sleep1.

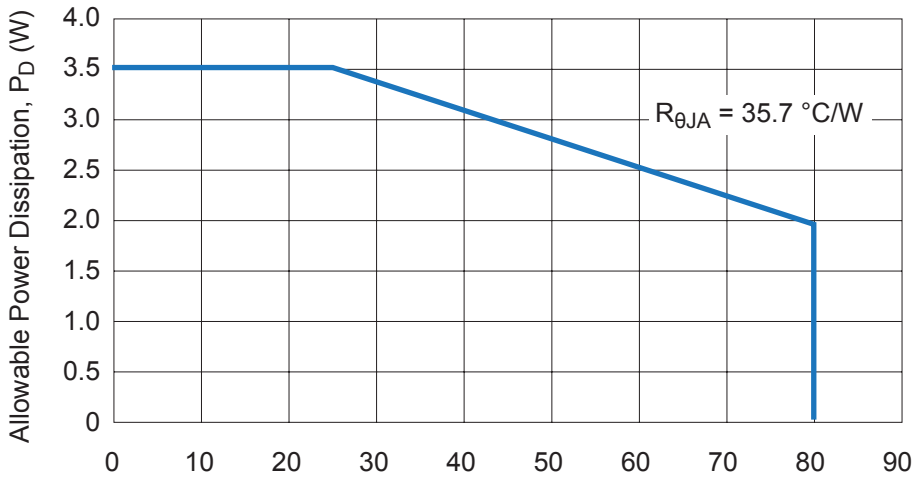


Figure 2. Allowable Power Dissipation

Typical Application Drawing

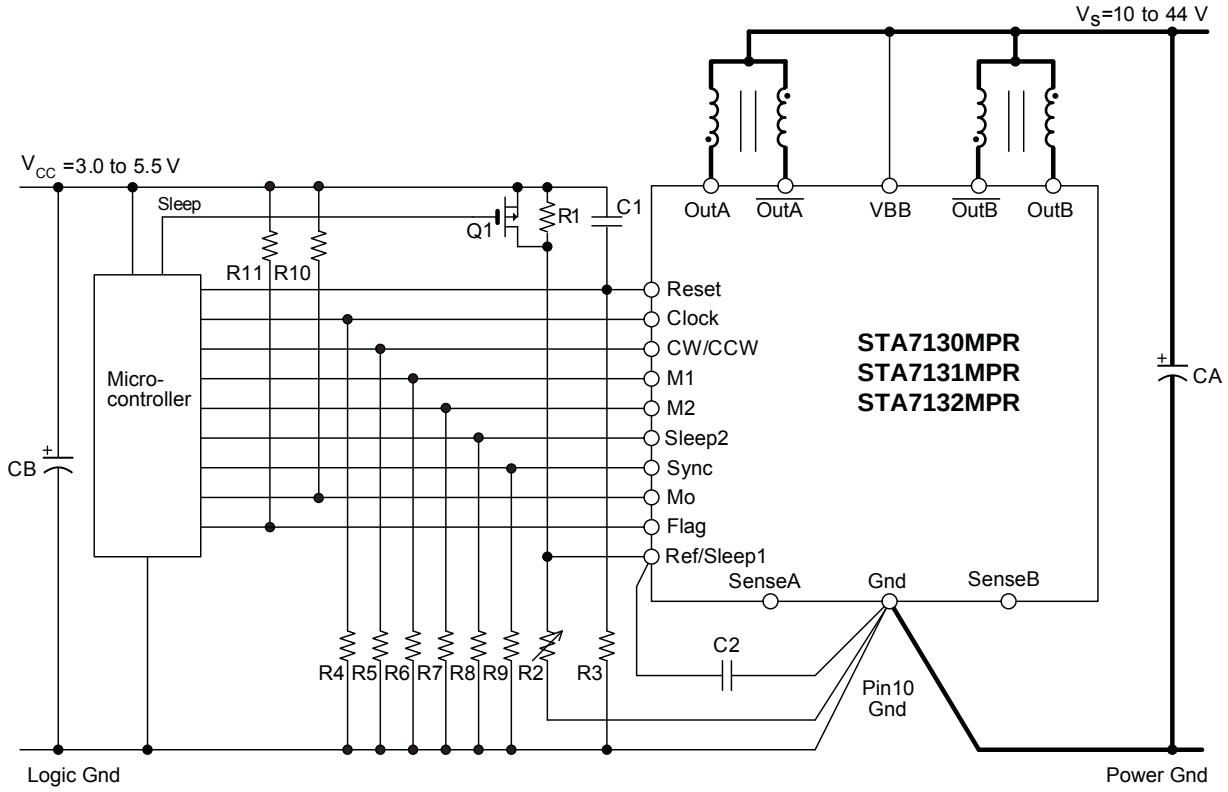


Figure 3. Typical Application Circuit

External Component Typical Values
(for reference use only):

Component	Value	Component	Value
R1	10 kΩ	CA	100 µF / 50 V
R2	1 kΩ (varistor)	CB	10 µF / 10 V
R3	10 kΩ	C1, C2	0.1 µF
R4 to R9*	1 to 10 kΩ		
R10 to R11	5.1 to 10 kΩ		

*Not required if corresponding device input pin open.

- Take precautions to avoid noise on the VDD line and the Logic Gnd line; noise levels greater than 0.5 V on the VDD line may cause device malfunction, so be careful when laying out Gnd traces.
  Noise can be reduced by separating the Logic Gnd and the Power Gnd on the PCB from the device Gnd pin (pin 10).
- If unused, the logic input pins CW / CCW, M1, M2, Sleep2, Reset, and Sync must be pulled up to V_{DD} or pulled down to Gnd. If those unused pins are left open, the device malfunctions.
- If unused, the logic output pins Mo and Flag must be kept open.

Truth Tables

Logic Input Pins

Table 1 shows the truth table for the logic input pins of the STA7130MPR series.

• The Reset function is asynchronous. If the input on the Reset pin is set high, the internal logic circuits are reset. At this point, if the Ref/Sleep1 pin is kept low, then the motor outputs turn on at the starting point of excitation. Note that the output disable function is not available when the Reset pin is high.

• Voltage at the Ref/Sleep1 pin controls the PWM current and the Sleep1 function.

▫ For normal operation, V_{REF} should be less than 1.5 V (low level).

▫ For Sleep1 mode, V_{REF} should be greater than 2.0 V (high level). This turns off (disables) the outputs, stops the internal linear circuits, and reduces the main power supply current, I_{BB}. The logic control circuits remain active, and will respond to a signal on the Clock input.

• Voltage at the Sleep2 pin controls the Sleep2 function. When the Sleep2 pin is pulled high, the outputs are turned off (disabled), the internal linear circuits are stopped, and the main power supply current, I_{BB}, is reduced, similar to the Sleep1 state. In addition, however, the logic control circuits are disabled (Hold mode), and the device will not respond to a signal on the Clock input. When awaking from the Sleep2 state, delay at least 100 µs before sending a Clock pulse (see figure 4).

Setting the Sleep2 pin high releases any protection states in effect. Alternatively, cycle the VDD power supply.

Excitation Mode Input Pins

Table 2 shows the logic of the pins (M1 and M2) that set the commutation mode.

Monitor Output Pins

The STA7130MPR series provides two device status monitor outputs:

• Mo pin – motor output sequencing

• Flag pin – protection function operation

Table 3 shows the logic for the monitor pins. The monitor outputs are open drain, so an external pull-up resistor rated at 5.1 to 10 kΩ must be connected (see Typical Application Drawing section).

Table 2. Motor Phase Excitation Mode Truth Table

Pin Name		Excitation Mode
M1	M2	
L	L	2 phase excitation (mode F, full step)
H	L	1-2 phase excitation (mode F, half step)
L	H	W1-2 phase (quarter step)
H	H	2W1-2 phase (eighth step)

Table 3. Monitor Output Truth Table

Pin Name	Low Level	High Level
Mo	Other than 2-phase excitation timing	2-phase excitation timing
Flag	Normal operation	Protection circuit operation

Table 1. Logic Input Truth Table

Pin Name	Low Level	High Level	Clock Default
Reset	Normal operation	Logic reset	 (Positive edge)
CW/CCW	Forward rotation (CW)	Reverse rotation (CCW)	
M1, M2	Commutation control		
Sleep2	Normal operation	Sleep2 function (Reset protection functions)	
Ref/Sleep1	Normal operation	Sleep1 function	
Sync	Asynchronous PWM control	Synchronous PWM control	

Logic Input Pin Structure

The low pass filter incorporated with the logic input pins (Reset, Clock, CW/CCW, M1, M2, Sleep2, and Sync) improves noise rejection. These are MOS inputs and are high impedance. Apply a fixed input level, either low or high.

Input Logic Timing

The timing considerations described in the following sections are illustrated in figure 4.

Clock Signal

The internal sequencer logic switches on a positive (rising) edge of a Clock input signal.

The Clock pulse width should be longer than 2 µs in both the positive and negative phases, which corresponds to a clock response frequency of 250 kHz. Note: Although in standard configuration only the positive edge is used for output switch timing, it is necessary to control the pulse widths both before and after each Clock signal edge, in order to maintain proper stepping operation.

CW/CCW, M1, and M2 Signals

The CW/CCW, M1, and M2 signals are also timed relative to the Clock input signal edges, and setup and hold time intervals are required. Switching of these inputs should occur at least 1 µs before or after the Clock signal switching pulse edge (positive edge for standard configuration, and positive or negative edge for W option). If either interval is shorter than 1 µs, the sequencer logic circuitry can malfunction.

Awakening from Sleep1 and Sleep2 Mode

When awaking from the Sleep1 and Sleep2 state, after setting the corresponding Sleep1 or Sleep2 input low, a delay, t_{SE}, of at least 100 µs is required before sending a Clock pulse.

Reset Signal

The Reset pulse width, that is, the time the high voltage level is maintained on the Reset pin, must greater than 2 µs.

If a Reset release (falling edge) and Clock edge occur simultaneously, the internal logic might cause an unexpected operation. Therefore, a greater than 5 µs delay is required between the falling edge of the Reset input and the next edge of the Clock input.

Rotation Direction and Mode Change

When a change is made to the rotation direction or excitation mode using the CW/CCW, M1, and M2 inputs, the changes are implemented at the next switching edge of the Clock input. Depending on the state of the motor when the Clock switching edge is received, the motor might be unable to respond and an out-of-step operation could occur. Therefore, please perform sufficient evaluation of the switching sequence with the motor in the application.

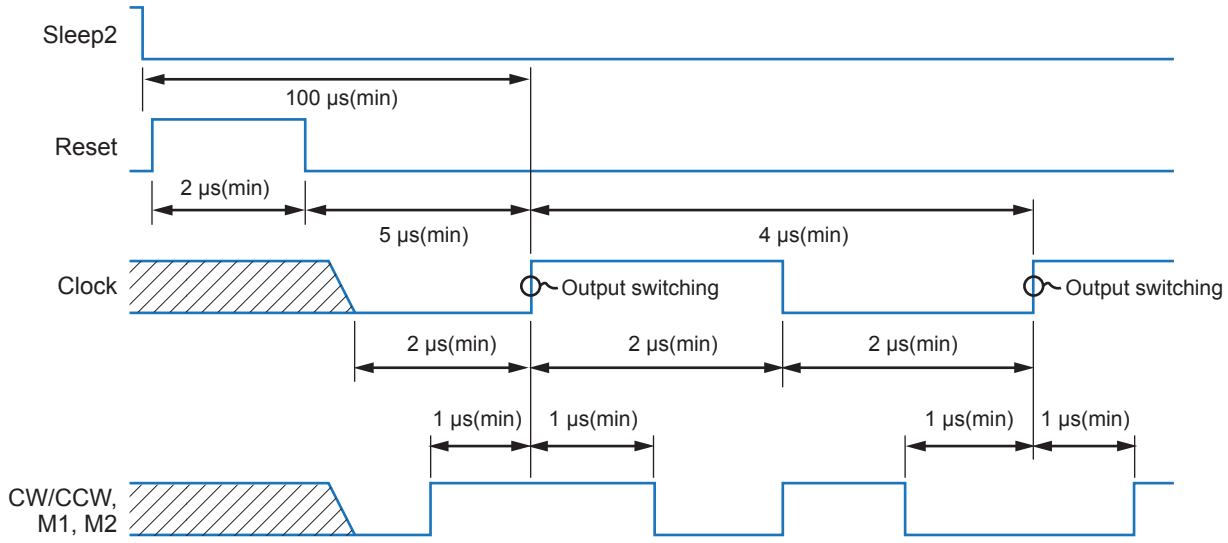
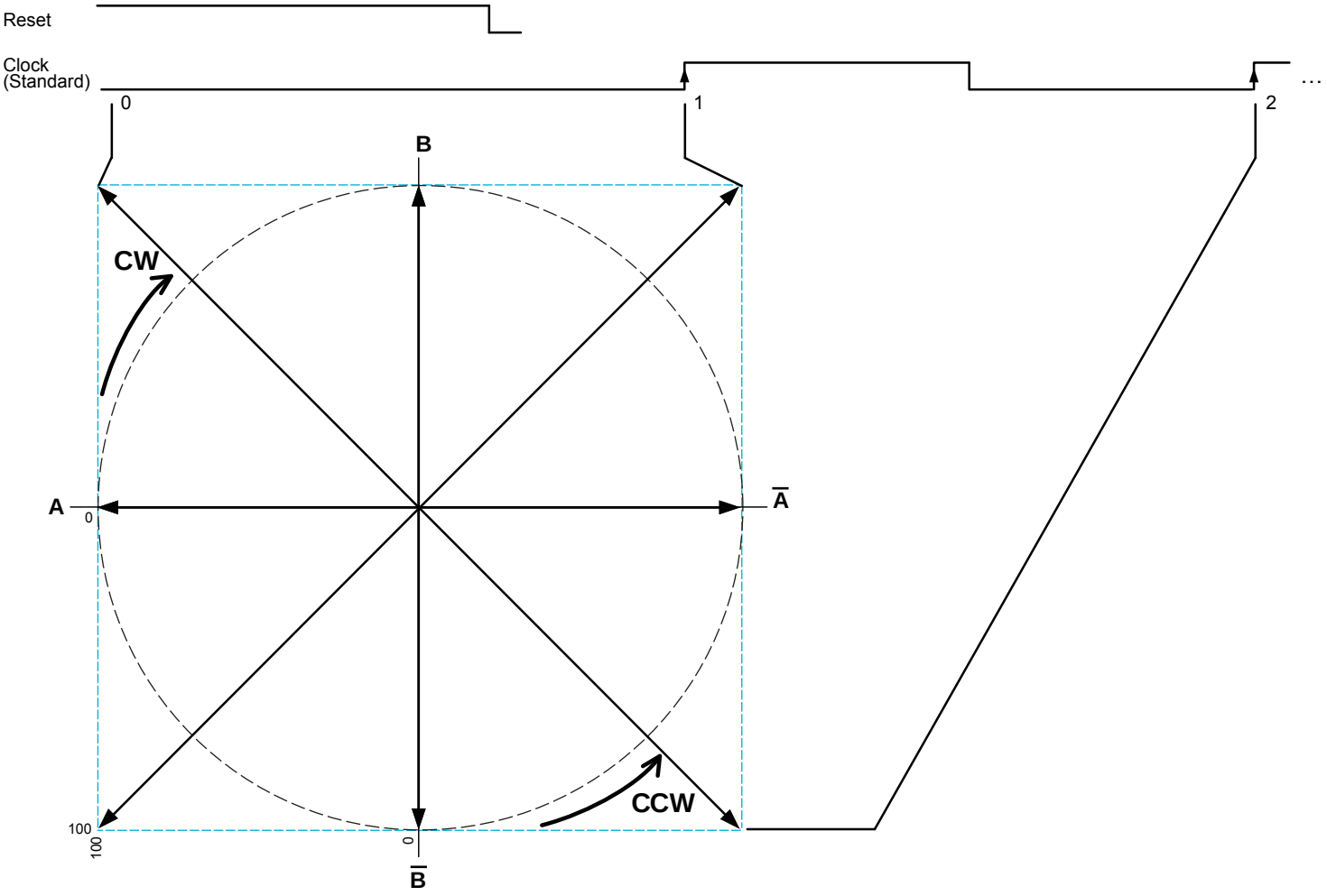


Figure 4. Clock timing diagrams

Stepping Sequence Diagrams

2 Phase Excitation (Full Step)

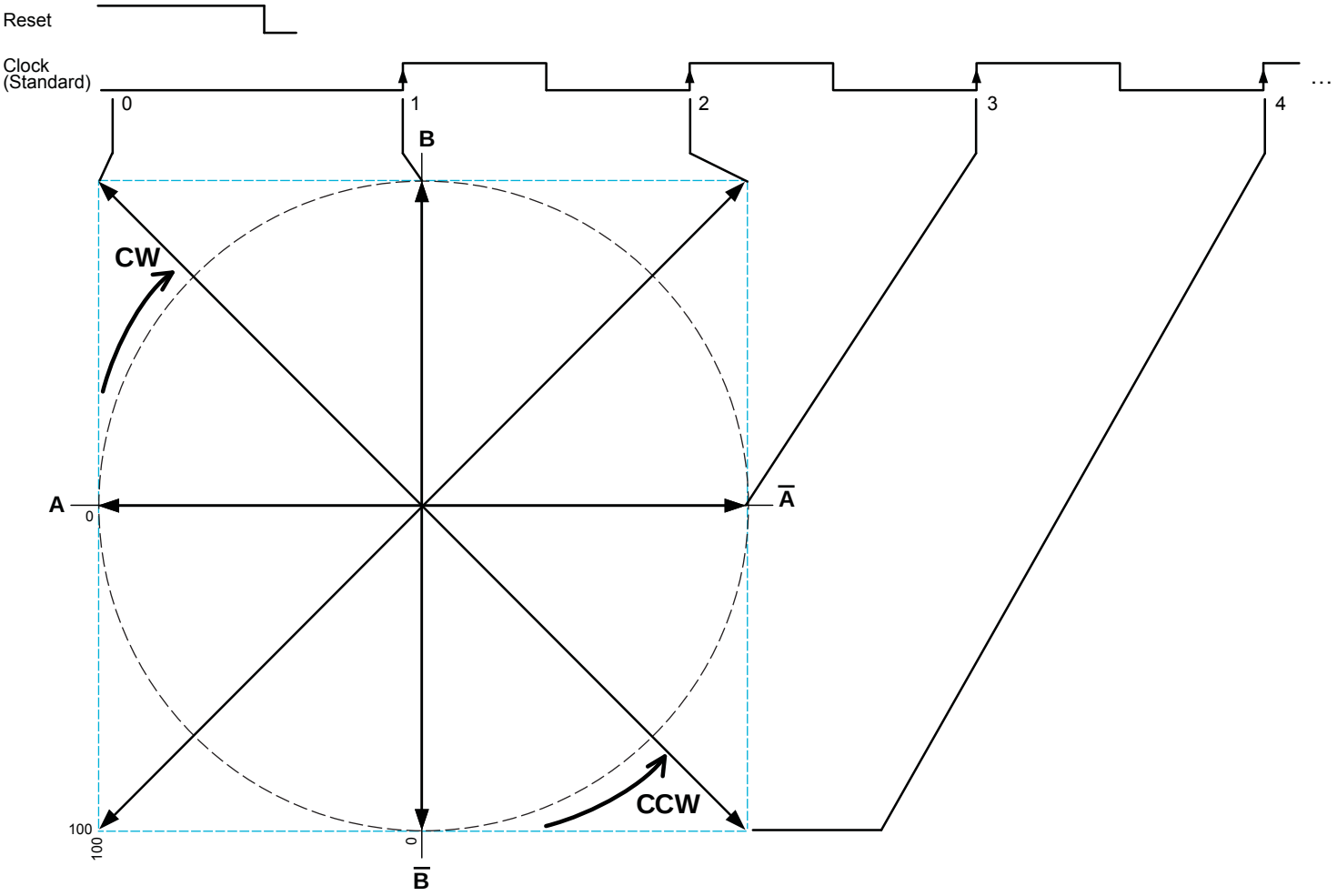


Excitation Mode Selection

M1	M2
Low	Low

Shows the state to which the stepping sequence progresses at each switching edge of the Clock input

1-2 Phase Excitation (Half Step)

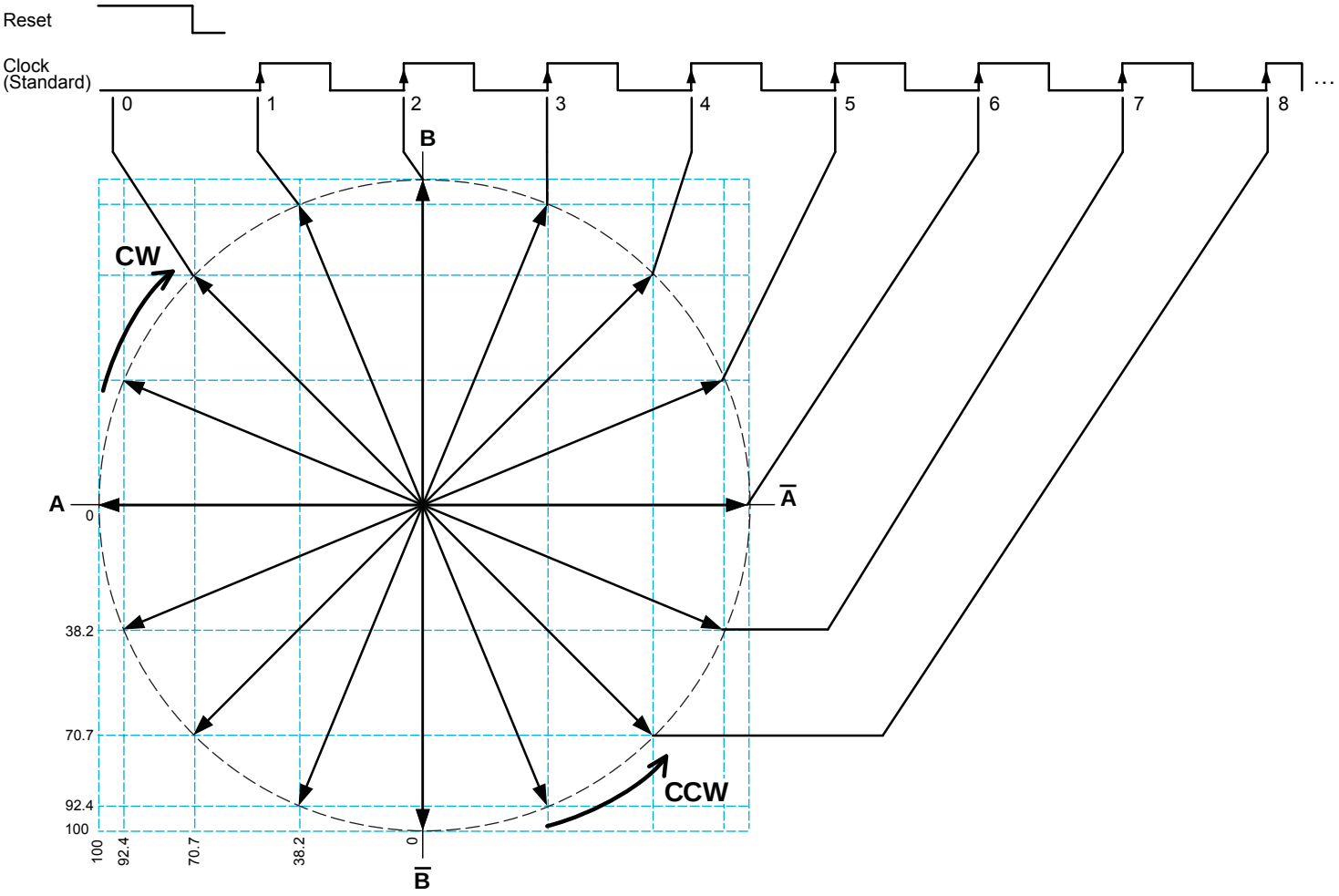


Excitation Mode Selection

M1	M2
High	Low

Shows the state to which the stepping sequence progresses at each switching edge of the Clock input

W1-2 Phase Excitation (Quarter Step)

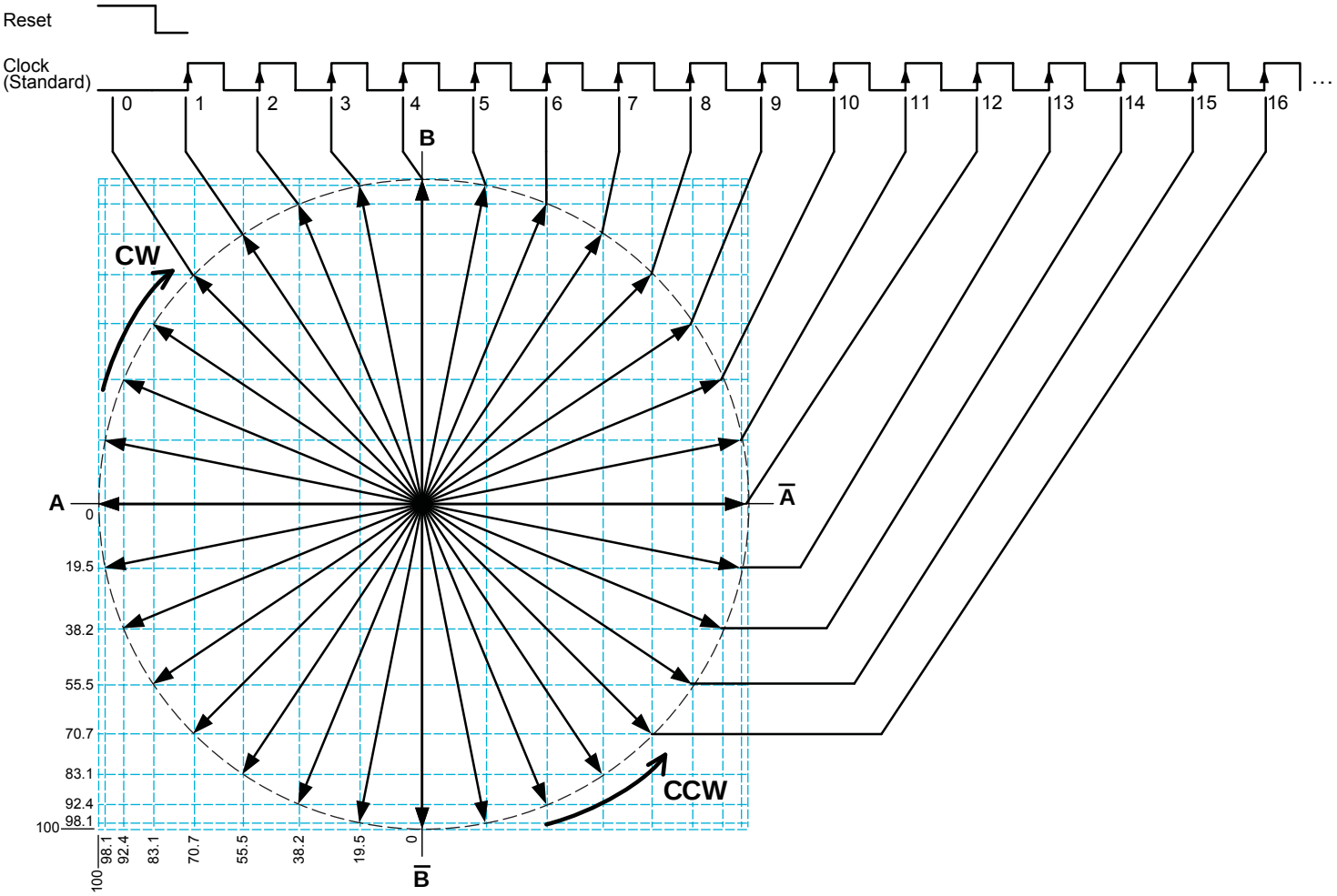


Excitation Mode Selection

M1	M2
Low	High

Shows the state to which the stepping sequence progresses at each switching edge of the Clock input

2W1-2 Phase Excitation (Eighth Step)



Excitation Mode Selection

M1	M2
High	High

Shows the state to which the stepping sequence progresses at each switching edge of the Clock input

Excitation Change Sequencing

The excitation state of the STA7130MPR outputs represent the relative position of the motor, according to the Excitation Mode Sequence shown in table 4. When the Clock signal is received, the position changes to the next step in the sequence (set by the M1 and M2 pins). The direction of position change is set by the CW/CCW pin.

Table 4. Excitation Mode States

Direction	Internal Sequence State[a]				Excitation Mode Sequence			
	Phase A		Phase B		2 Phase (Full Step)	1-2 Phase (Half Step)	W1-2 Phase (Quarter Step)	2W1-2 Phase (Eighth Step)
	PWM	Mode	PWM	Mode				
Counter Clockwise (CCW)	A	8	B	8	√	√	√	√
	A	6	B	A				√
	A	4	B	C			√	√
	A	2	B	E				√
	–	–	B	F		√	√	√
	$\overline{A}$	2	B	E				√
	$\overline{A}$	4	B	C			√	√
	$\overline{A}$	6	B	A				√
	$\overline{A}$	8(F)[b]	B	8(F)[b]	√	√	√	√
	$\overline{A}$	A	B	6				√
	$\overline{A}$	C	B	4			√	√
	$\overline{A}$	E	B	2				√
	$\overline{A}$	F	–	–		√	√	√
	$\overline{A}$	E	$\overline{B}$	2				√
	$\overline{A}$	C	$\overline{B}$	4			√	√
	$\overline{A}$	A	$\overline{B}$	6				√
	$\overline{A}$	8(F)[b]	$\overline{B}$	8(F)[b]	√	√	√	√
	$\overline{A}$	6	$\overline{B}$	A				√
	$\overline{A}$	4	$\overline{B}$	C			√	√
	$\overline{A}$	2	$\overline{B}$	E				√
	–	–	$\overline{B}$	F		√	√	√
	A	2	$\overline{B}$	E				√
	A	4	$\overline{B}$	C			√	√
	A	6	$\overline{B}$	A				√
Clockwise (CW)	A	8(F)[b]	$\overline{B}$	8(F)[b]	√	√	√	√
	A	A	$\overline{B}$	6				√
	A	C	$\overline{B}$	4			√	√
	A	E	$\overline{B}$	2				√
	A	F	–	–		√	√	√
	A	E	B	2				√
	A	C	B	4			√	√
	A	A	B	6				√

[a]The Reference Voltage Ratio proportions are the same as the SLA7070M series for corresponding modes.
[b]Internal Sequence State is Mode 8 for W1-2 Phase and 2W1-2 Phase sequencing, and is Mode F for 2 Phase and 1-2 Phase sequencing.

Individual Circuit Descriptions

Monolithic Control IC (MIC)

• ***Sequencer Logic*** The single Clock input is used for step timing. Direction is controlled by the CW/CCW input. Excitation mode is controlled by the combination of the M1 and M2 input logic levels. For details, refer to the individual truth table and logic timing descriptions.

• ***PWM Control*** Each pair of outputs is controlled by a fixed off-time PWM current-control circuit. The internal oscillator (OSC) sets the off-time. Its operation mechanism is identical to that of the SLA7070M series.

• ***Synchronous Control*** This function prevents abnormal motor noise when the STA7130MPR series is in Hold state. It synchronizes PWM chopping timing between the A and B output phases. Setting the Sync input to logic high sends a timing signal that synchronizes the chopping off-time of both phases A and B.

This function is only recommended for synchronizing 2-Phase (full/half step sequence) excitation in Hold state. Use in non-2-phase operations may result in no synchronization or greatly reduced phase control currents, caused by the mismatch of timing signal values and PWM off-cycles.

We do not recommend using this function while the motor is in rotation, because it may interfere with motor current control, reduce motor torque, and raise motor vibrations.

• ***DAC (D-to-A Converter)*** The sequencer logic controls the generation of an internal reference standard through the individual output phase DACs. The standard voltage amounts to:

$$V_{REF} /3 \times \text{Mode Ratio}$$

Where internal V_{SENSE} is a factor. The Reference Voltage Ratio for the various modes are given in the Electrical Characteristics table.

• ***Regulator Circuit*** The integrated regulator circuit is used in powering the pre-driver for the output MOSFET gates and for other internal linear circuits.

• ***Protection Circuit*** A built-in protection circuit against motor coil opens or shorts is provided. Protection is activated by sensing voltage on the internal R_S resistors; therefore, an overcurrent condition which results from the the Outx pins or Sensex pins, or both, shorting to Gnd cannot be detected by this means. Protection against motor coil opens is available only during PWM operation; therefore, it does not work at constant voltage driving, when the motor is rotating at high speed. Operation of the protection circuit disables all of the outputs. To come out of protection mode, set the Sleep2 pin high, or cycle the VDD power supply.

• ***TSD circuit*** This circuit protects the device by shifting the outputs to Disable mode when the temperature of the device control IC (MIC) rises and becomes higher than threshold value, T_{TSD}. To come out of protection mode, set the Sleep2 pin high, or cycle the VDD power supply.

Output MOSFET Chips

The value of the built-in output MOSFET chips varies according to the current rating of the STA7130MPR variant.

Sense Detection Resistance

The sense resistance varies according to the current rating of the STA7130MPR variant, as follows:

Output Current (A)	R_S Resistance (Ω typ)
1	0.305
1.5	0.205
2	0.155

Each resistance shown above includes the inherent resistance (approximately 5 mΩ) in the resistor itself.

Functional Description

PWM Control

Blanking Time

An operating waveform on a Sensex pin, when driving a motor, is shown in figure 5. After PWM switching from off to on, ringing noise (spiked waveforms) can be observed for several microseconds on the Sensex pins. Ringing noise can be generated by various causes, such as capacitance between motor coils and inappropriate placement of motor wiring.

PWM current control of each output phase is performed using a comparator with inputs from the voltage detection circuit, V_{RS}, and the DAC output voltage to switch the PWM pulse from on to off. If the ringing noise on the sense resistor pin exceeds V_{TRIP}, the comparator would turn off PWM repeatedly (referred to as *seeking*) as shown in figure 6. To prevent this phenomenon, the device is set to disregard signals from the current-sense comparator for a certain period, the *blanking time*, immediately after PWM turns on (figure 7).

• ***Blanking time and seeking phenomenon*** When a motor is driven by the device, the seeking phenomenon may occur, generating noise from a torque reduction or the motor may become audibly louder. Although current control can be improved by shortening blanking time, the degree of margin for suppressing ringing noise decreases commensurately. The STA7130MPR series offers two blanking times: the standard variant duration is 1.5 µs, and the B option offers a duration of 3.0 µs. Using the variant with the longer, B option may solve the ringing problem.

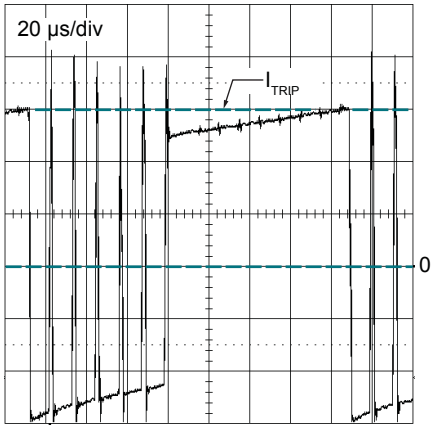


Figure 6. Example of a Sensex terminal waveform during seeking phenomenon

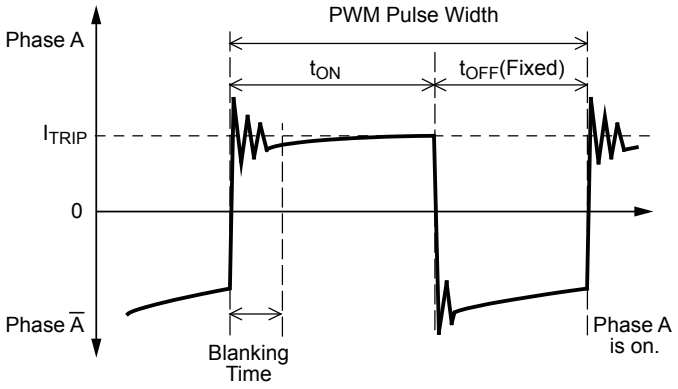


Figure 7. Sensex pin waveform during PWM control

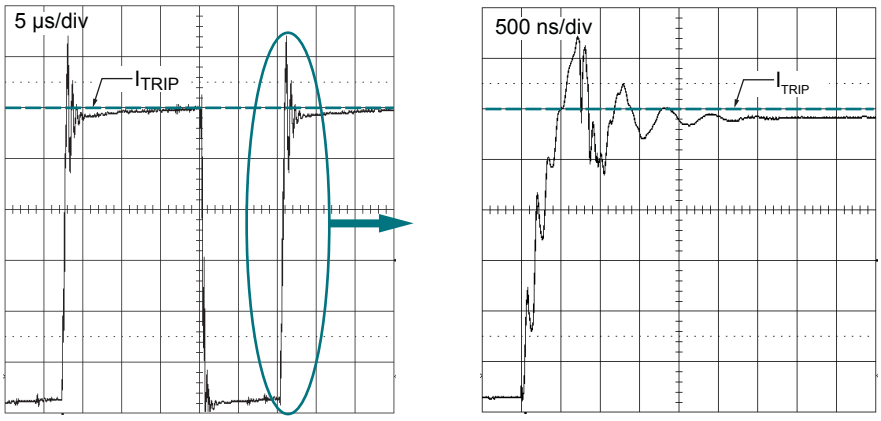


Figure 5. Operating waveforms on the Sensex pins during PWM chopping (circled area of left panel is shown in expanded scale in right panel)

• ***Blanking time tradeoffs*** The tradeoffs from different blanking times are shown in table 5. This comparison is based on the case where drive conditions, such as a motor, motor power supply voltage, Ref input voltage, and a circuit constant, were kept the same; in other words, while only the blanking time was changed.

▫ Minimize PWM on-time. Even if the on-time is shortened in order to reduce the current level, the minimum on-time could not be less than the blanking time. The minimum PWM on-time refers to the time the output MOSFET actually is turned on. In other words, the blanking time would set a minimum on-time, so *short* is selected in table 5).

▫ Minimize Coil current. This corresponds to the coil current during PWM minimum on-time, such as when the coil current is reduced when the power is reduced. In that case the shorter blanking time will allow a greater reduction in current.

Table 5. Characteristic Comparison by the Difference in Blanking Time

Parameter	Better Performance	
Internal Blanking Time Setting	Short	Long
Minimum PWM on-time	Short	← ←
Ringing noise suppression	→ →	Large
Minimum coil current	Low	← ←
Coil current waveform distortion at a high rotation rate (especially with microstepping)	→ →	Large

▫ Coil current waveform distortion during high rotation rate. During microstepping, the I_{Trip} value (the internal reference voltage splitting ratio) changes with each Clock input, to predetermined values approximating a sine wave. Because PWM control of the motor coil current is set according to the I_{trip} value, the coil current is also in sine wave form.

Due to the inductance characteristics of the coils, some amount of time is required for the device to settle the coil current at the targeted values. In general, if the relationship between this convergence time, t_{conv}, and the period, t_{clk}, of the input Clock is $t_{conv} < t_{clk}$, the range of the coil current level will follow the the I_{trip} value in any mode. The limiting value of t_{conv} on the low side is determined by: the power supply voltage, the circuit time constant, and the minimum on-time. The limiting value of t_{conv} on the high side is determined by: the power supply voltage and the coil circuit time constant.

When the frequency of the Clock input is raised, because t_{clk} becomes correspondingly small, the case can be expected in which the coil current cannot be raised to the I_{trip} value within a single clock period. In this case, the waveform amplitude of the coil current degenerates from the sine wave form, a condition referred to as *waveform distortion*.

Figure 8 shows the waveform distortion at two different blanking times (both samples have the same power supply voltage, current preset value, motor, and so forth). As the circled sections show, the Sensex pin waveforms at 1.7 µs blanking time closely follow

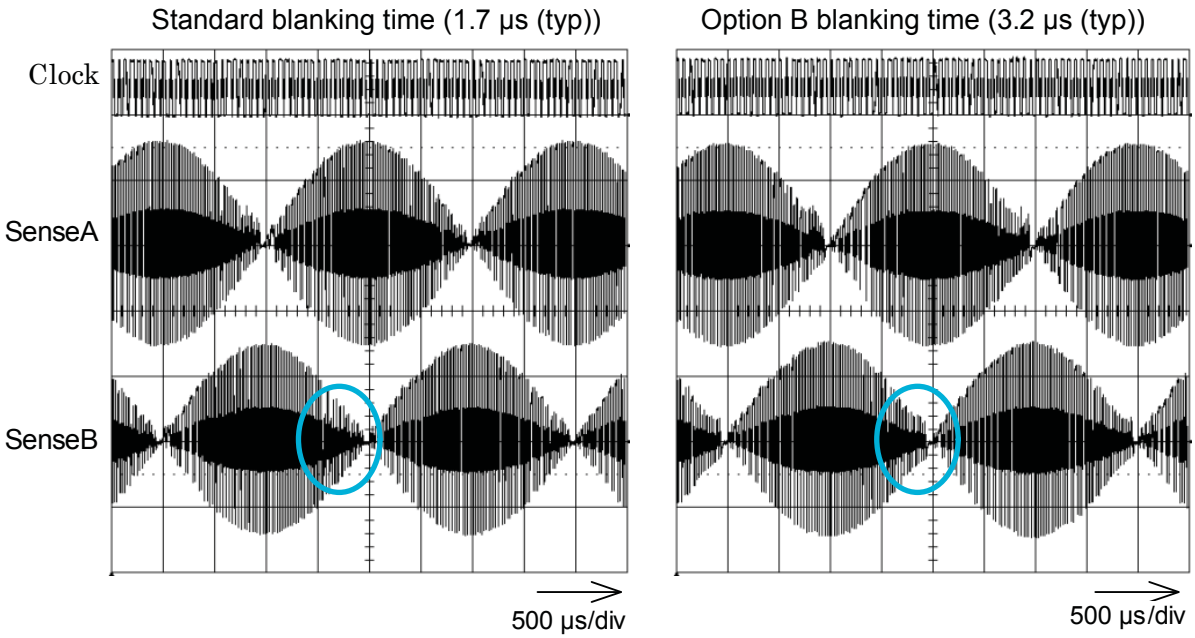


Figure 8. Operating waveforms on the Sensex pins during high rotation rate

a sinusoidal waveform envelope, but with a blanking time of 3.0 µs, the waveforms have begun to degenerate.

In table 5 the preference for long blanking time means that the wave distortion will be less where the blanking time is longer, assuming the same drive conditions, while the wave distortion will be larger where the blanking time is shorter, if the Clock frequency is the same. In addition, despite such waveform distortion being confirmed, it is uncertain that the motor characteristic will be affected. Therefore, please make a final judgment after evaluating very thoroughly.

PWM Off-Time

The PWM off-time is controlled at a fixed time by an internal oscillator (similar to the SLA7070MPRT series). It is switched to one of three levels (see the Electrical Characteristics table) according to the switching sequence selected. In addition, the series provides a function that decreases losses occurring when the PWM turns off. This function dissipates back EMF stored in the motor coil at MOSFET turn-on, as well as at PWM turn-on (referred to as *synchronous rectification*).

Figure 9 shows the difference in back EMF generation between the SLA7060M series and STA7130MPR series. The SLA7060M series performs on–off operations using only the MOSFETs on the PWM-on side, but the SLA7130MPR series also performs on–off operations using the MOSFETs on the PWM-off side. To prevent simultaneous switching of the MOSFETs at synchronous rectification operation, the IC has a dead time of approximately 0.5 µs. During dead time, the back EMF regeneration current-flows through the body diode of the MOSFET.

Protection Functions

The STA7130MPR series includes a motor coil short-circuit protection circuit, a motor coil open protection circuit, and an overheating protection circuit. An explanation of each protection circuit is provided below.

• ***Motor Coil Short-Circuit Protection (Load Short) Circuit***. This protection circuit, built into the STA7130MPR series, begins to operate when the device detects an increase in the sense resistor voltage level, V_{RS}. The voltage at which motor coil short-circuit protection starts its operation, V_{OCP}, is set at approximately 0.7 V.

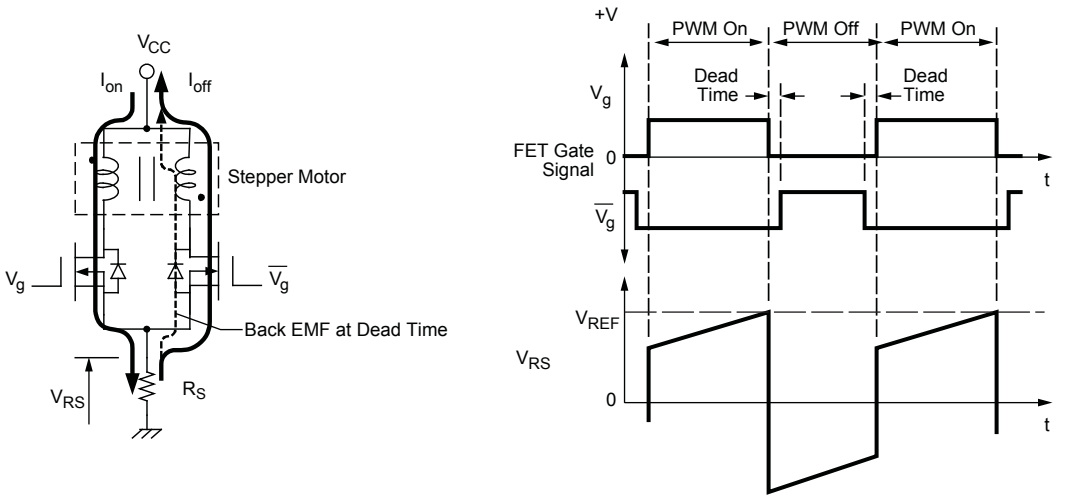


Figure 9. Synchronous rectification operation; Back EMF flows into body diode during Dead Time.

The outputs are disabled at the time the protection circuit starts, where V_{RS} exceeds V_{OCP}. (See figure 10.)

• ***Motor Coil Open Protection*** Driver destruction can occur when one output pin (motor coil) is disconnected in a unipolar drive during operation. This is because a MOSFET reconnected after disconnection will be in the avalanche breakdown state, where very high energy is added with back EMF when PWM is off. With an avalanche state, an output cancels the energy stored in the motor coil where the resistance between the drain and source of the MOSFET is reached (the condition which caused the breakdown).

Although MOSFETs with a certain amount of avalanche energy tolerance rating are used in the STA7130MPR series, avalanche energy tolerance falls as temperature increases.

Because high energy is added repeatedly whenever PWM operation disconnects the MOSFET, the temperature of the MOSFET rises, and when the applied energy exceeds the tolerance, the driver will be destroyed. Therefore, a circuit which detects this avalanche state and protects the driver is provided in the STA7130MPR series. The operation is shown in figure 11.

As explained above, when the motor coil is disconnected, the accumulated voltage in the MOSFET causes a reverse current to flow during the PWM off-time. For this reason, V_{RS} that is negative during the PWM off-time in a normal operation becomes positive when the motor coil is disconnected. Thus, a disconnected motor is detectable by sensing that V_{RS} in the PWM off-time is positive.

In the STA7130MPR series, in order to avoid detection malfunctions, when a state of motor disconnection is detected 3 times continuously, the protection functions are enabled (figure 12).

Note: When the breakdown of an output is confirmed by the occurrence of surge noise after PWM turn-off, the protection feature may operate and continue after the breakdown condition lasts beyond the overload disconnection undetected time (t_{opp}), even if the load is not actually disconnected. In that case, please review the placement of the motor, wiring, and so forth to improve and to settle the breakdown time within the load disconnection undetected time (t_{opp}) (application variations also must be taken into consideration). If the breakdown is not confirmed, operation continues normally. Moreover, the device may be made to operate normally by inserting a capacitor for surge noise suppression between the Outx and Gnd pins as one possible corrective strategy.

• ***Overheating Protection*** When the product temperature rises and exceeds T_{TSD}, the protection circuit starts operating and all the outputs are set to Disable mode.

Note: This product has multichip composition (one IC for control, four MOSFETs, and two chip resistors). Although the location which actually detects temperature is the control IC (MIC), because the main heat sources are the MOSFET chips and the chip resistors, which are separated by a distance from the control IC, some delay will occur while the heat propagates to the control IC. For this reason, because a rapid temperature change cannot be detected, please perform worst-case thermal evaluations in the application design phase.

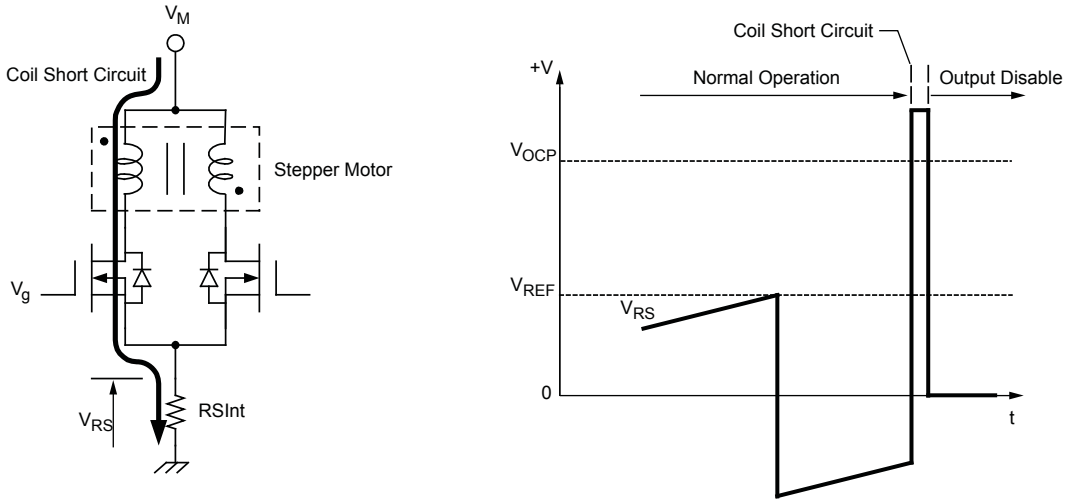


Figure 10. Motor coil short circuit protection circuit operation. Overcurrent that flows without passing the sense resistor is undetectable.

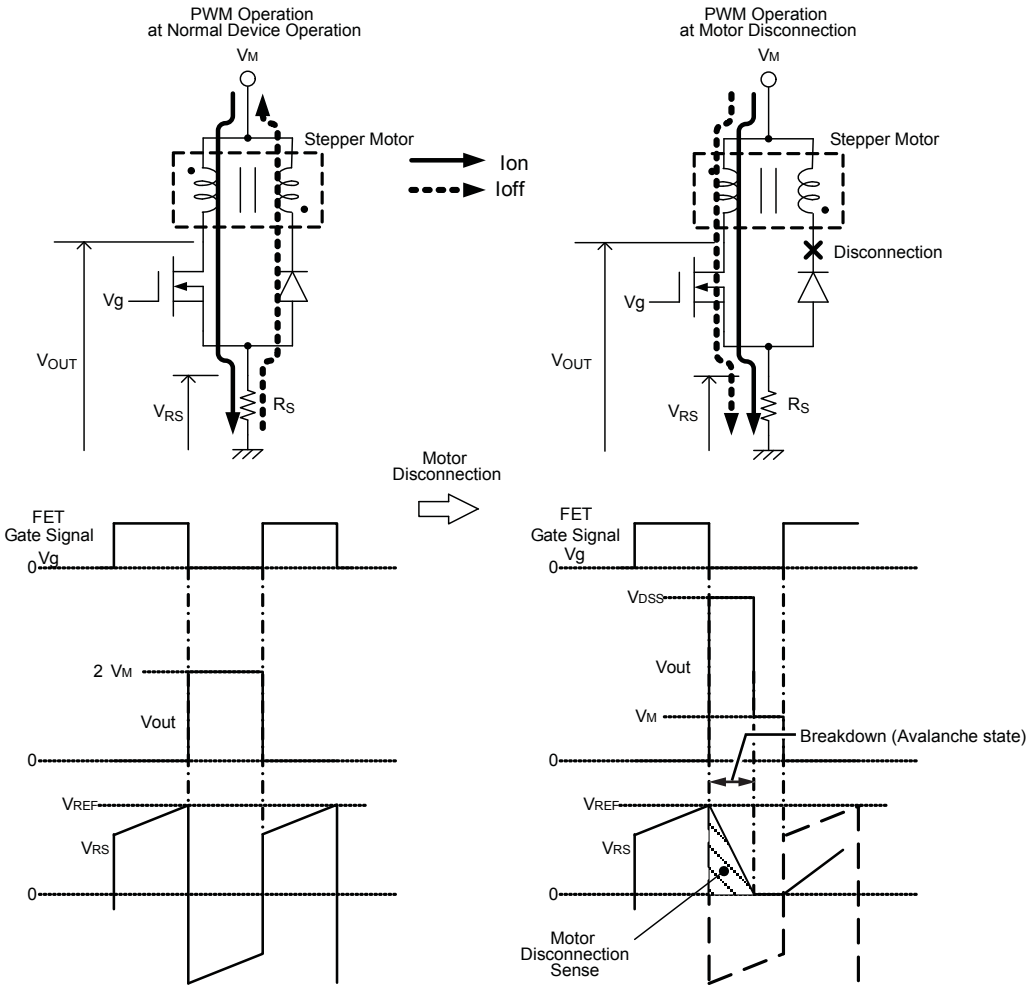


Figure 11. Load open circuit protection circuit operation. Overcurrent that flows without passing the sense resistor is undetectable.

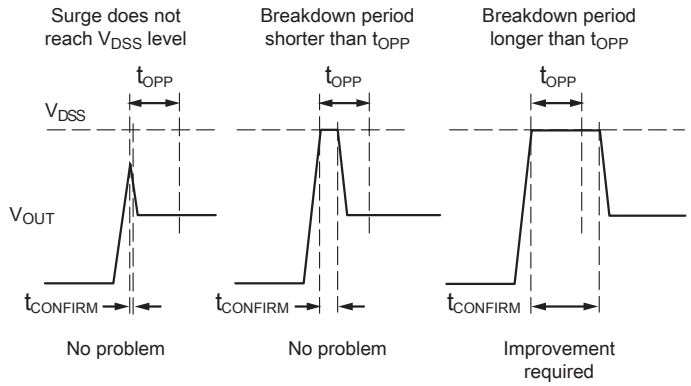


Figure 12. Coil Open Protection

Application Information

Motor Current Ratio Setting (R1 , R2, RS)

The setting calculation of motor current, I_O, for the STA7130MPR series is determined by the ratios of the external components R1 and R2, and current sense resistors, R_S. The following is a formula for calculating I_O:

$$I_O = \frac{R_2}{R_1 + R_2} \times V_{DD} \times \frac{1}{3} \times \frac{1}{R_S} \quad (1)$$

Given:

$$V_{REF} = \frac{R_2}{R_1 + R_2} \times V_{DD} \quad (2)$$

if V_{REF} is set less than 0. 1 V, normal product variations, impedances of the wiring pattern, and similar factors may influence the IC and the possibility of less accurate current sensing becomes high.

The standard voltage for current I_{Trip} that the STA7 130MPR series controls is partially divided by the internal DAC:

$$I_{Trip} = \frac{V_{REF}}{R_S} \times \frac{1}{3} \times \text{Mode Ratio} \quad (3)$$

Lower Limit of Control Current

The STA7130MPR series uses a self-oscillating PWM current control topology in which the of -time is fixed. As energy stored in motor coil is eliminated within the fixed PWM of -time, coil current flows intermittently, as shown in figure 13. Thus, average current decreases and motor torque also decreases.

The point at which current starts flowing into the coil intermittently is considered as the lower limit of the control current, I_O(min), where I_O is the target current level. The lower limit of control current varies with conditions of the motor or other factors, but can be estimated from the following formula:

$$I_{O(min)} = \frac{V_M}{R} \left[\frac{1}{\exp\left(\frac{-t_{OFF}}{t_c}\right)} - 1 \right] \quad (4)$$

where

V_M is the motor supply voltage,

$R_{DS(on)}$ is the MOSFET on-resistance,

R_m is the motor winding resistance,

L_m is the motor winding inductance,

t_{OFF} is the PWM of -time, and

t_C is calculated as:

$$t_c = L_m / R \ , \quad (5)$$

where

$$R = R_m + R_{DS(on)} + R_S \quad (6)$$

Even if the control current value is set at less than the lower limit of the control current, there is no setting at which the IC fails to operate. However, control current will worsen against setting current.

Avalanche Energy

In the unipolar topology of the STA7130MPR series, a surge voltage (ringing noise) that exceeds the MOSFET capacity to withstand might be applied to the IC. To prevent damage, the

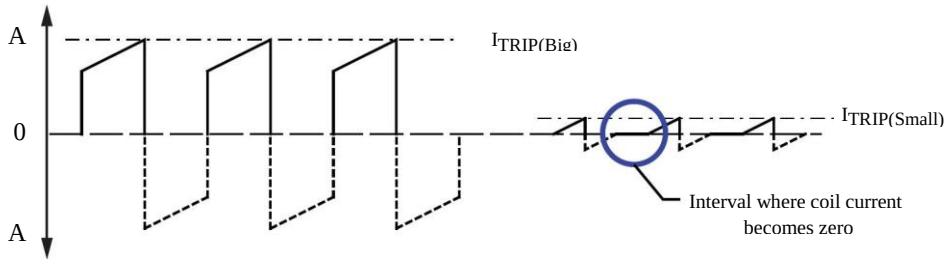


Figure 13. Control current lower limit model waveform

STA7130MPR series is designed with a built-in MOSFET having sufficient avalanche resistance to withstand this surge voltage. Therefore, even if surge voltages occur, users will be able to use the IC without any problems. However, in cases in which the motor harness is long or the IC is used above its rated current or voltage, there is a possibility that an avalanche energy could be applied that exceeds Sanken design expectations. Thus, users must test the avalanche energy applied to the IC under actual application conditions.

The following procedure can be used to check the avalanche energy in an application.

Refer to figure 14, to determine the test point. For the purposes of this example, use the following values:

$V_{DS(AV)}$ = 140 V,

I_D = 1 A, and

t = 0.5 µs.

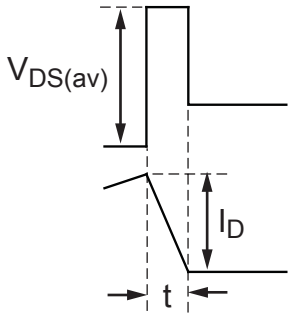


Figure 14. Test point definition

The avalanche energy, E_{AV} can be calculated as follows:

$$E_{AV} = V_{DS(AV)} \times {}^{1}/_{2} \times I_D \times t \quad (7)$$

$$= 140\ (V) \times {}^{1}/_{2} \times 1\ (A) \times 0.5 \times 10^{-6}\ (\mu s)$$

$$= 0.035\ (mJ)$$

By comparing the E_{AV} calculated with the graph shown in figure 15, the application can be evaluated if it is safe for the IC, by being within the avalanche energy-tolerated does range of the MOSFET.

Motor Supply Voltage (V_M) and Main Power Supply Voltage (V_{BB})

Because the STA7130MPR series has a structure that separates the control IC (MIC) and the power MOSFETs, the motor supply and main power supply are separated electrically. Therefore, it is possible to drive the IC using different power supplies and different voltages for motor supply and main power supply. However, extra caution is required because the supply voltage ranges differ between the two purposes.

Internal Logic Circuits

Resetting the Internal Sequencer

When power is applied to the main power supply (VBB) the internal reset function operates and the sequencer circuit initializes. The motor driver outputs are set to the excitation Home state.

To reset the internal sequencer after the motor has been in operation, a reset signal must be input on the Reset pin. In a case in which external reset control is not necessary, and the Reset pin is not used, the Reset pin must be pulled to logic low on the application circuit board.

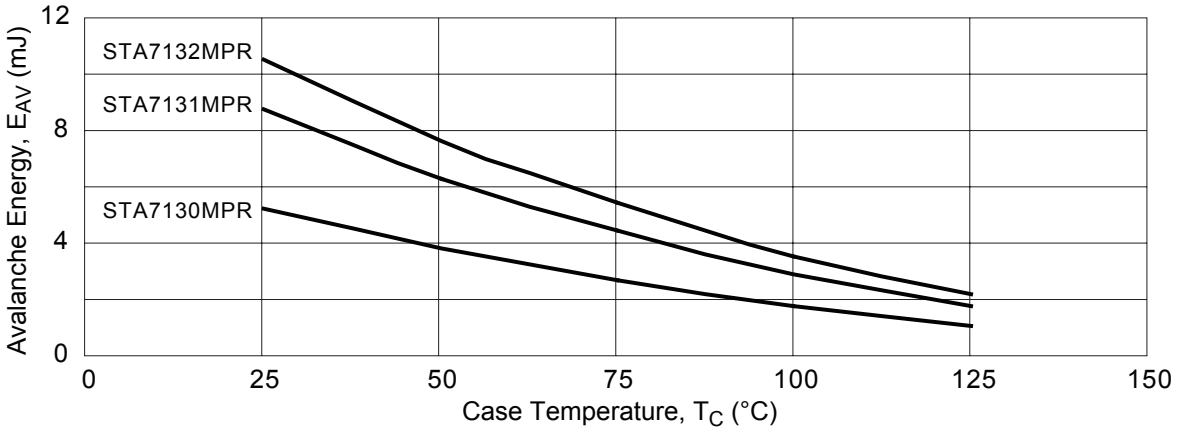


Figure 15. STA7130MPR iterated avalanche energy tolerated level, E_{AV}(max)

Clock Input

If the Clock input signal stops, excitation changes to the motor Hold state. At this time, there is no difference to the IC if the Clock input signal is at the low level or the high level. The STA7130MPR series is designed to move one sequence increment at a time, according to the current stepping mode, when a positive Clock pulse edge is detected.

Chopping Synchronous Circuit

The STA7130MPR series has a chopping synchronous function to protect from abnormal noise that may occasionally occur during the motor Hold state. This function can be operated by setting the Sync pin at high level. However, if this function is used during motor rotation, control current does not stabilize, and therefore this may cause reduction of motor torque or increased vibration. So, Sanken does not recommend using this function while the motor is rotating. In addition, the synchronous circuit should be disabled in order to control motor current properly in case it is used other than in dual excitation state (Modes 8 and F) or single excitation Hold state.

In normal operation, generally the input signal for switching can be sent from an external microcomputer. However, in applications where the input signal cannot be transmitted adequately such as due to the limitations of a port, the methods described below can be used.

The schematic diagram in figure 16 shows how the IC is designed so that the Sync signal can be generated by using the Clock input signal. When a logic high signal is received on the Clock pin, the internal capacitor, C, is charged, and the Sync signal is set to logic low level. However, if the Clock signal cannot rise above logic low level (such as when the circuit between the microcomputer and the IC is not adequate), the capacitor is discharged by the internal resistor, R, and the Sync signal is set to logic high, causing the IC to shift to synchronous mode.

The RC time constant in the circuit should be determined by the minimum clock frequency used. In the case of a sequence that keeps the Clock input signal at logic high, an inverter circuit must be added. In a case where the Clock signal is set at an undetermined level the edge detection circuit shown in figure 17 can be used to prepare the signal for the Clock input, allowing correct processing by the circuit shown in figure 16.

Output Disable (Sleep1 and Sleep2) Circuits

There are two methods to set this IC at motor free-state (coast, with outputs disabled). One is to set the Ref/Sleep1 pin to more than 2 V (Sleep1), and the other is to use the Sleep2 pin. In either way, the IC will change to Sleep mode, decreasing circuit current. The difference between the two methods is that, in Sleep1 mode, the internal sequencer remains enabled. In Sleep2 mode, the internal sequencer is in the Hold state, meaning that if a Clock signal pulse is received, the sequencer remains in the Hold state. Further, the Sleep2 state is used to clear any protection states in effect.

When awaking to normal operating mode (motor rotation) from Disable (Sleep1 or Sleep2) mode, set an appropriate delay time from cancellation of the Disable mode to the initial Clock input edge (positive or negative for W option). In doing so, consider not only the rise time for the IC, but also the rise time for the motor excitation current. A delay of at least 100 µs is required (see figure 18).

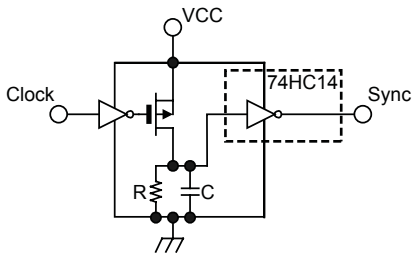


Figure 16. Clock signal shutoff detection circuit

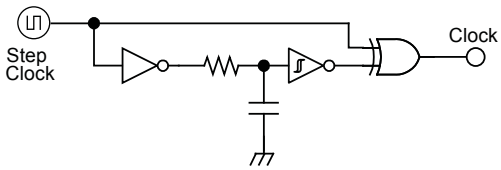


Figure 17. Clock signal edge detection circuit

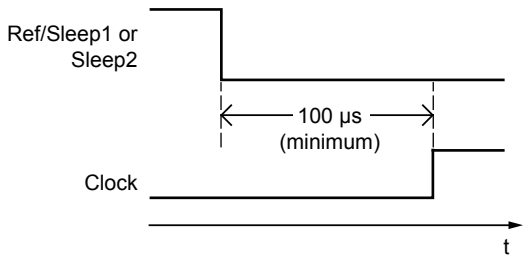


Figure 18. Timing delay between Disable mode cancellation and the next Clock input

Ref/Sleep1 Pin

The Ref/Sleep1 pin provides access to the following functions:

• Standard voltage setting for output current level setting

• Output Enable-Disable control input

These functions are further described in the Truth Table section, and in the discussion of output disabling, above. In addition, please observe the following:

• The output control current value changes with changes in the V_{REF} setting. Caution is required to avoid inducing losses.

• The output enable-disable function control voltage affects the control current values, and caution is required to avoid inducing losses. In addition an output may fail to settle and repeatedly swtich between enabled and disabled states.

Logic Input Pins

If a logic input pin (Clock, Reset, CW/CCW, M1, M2, or Sync) is not used (fixed logic level), the pin must be tied to VDD or Gnd. Please do not leave them floating, because there is possibility of undefined effects on IC performance when they are left open.

Logic Output Pins

The M_O and Flag output pins are designed as monitor outputs, and inside of the IC both are configured as open drain outputs. If used, both must be pulled up to VDD using a 5.1 to 10 kΩ external resistor (see figure 19). If either or both pins are unused, let the unused pins float.

Thermal Design

It is not practical to calculate the power dissipation of the STA7130MPR series accurately, because that would require factors that are variable during operation, such as time periods and excitation modes during motor rotation, input frequencies and sequences, and so forth. Given this situation, it is preferable to perform an approximate calculation at worst conditions. The following is a simplified formula for calculation of power dissipation:

$$P_D = I_O^2 \times (R_{DS(on)} + R_S) \times 2 \quad (8)$$

where

P_D is the power dissipation in the IC,

I_O is the operating output current,

$R_{DS(on)}$ is the resistance of the output MOSFET, and

R_S is the output current sense resistance.

Based on the P_D calculated using the above formula, junction temperature, ΔT_J , of the device can be estimated using figure 20. At this time, if junction temperature does not exceed 150°C in the worst condition (the maximum of ambient air temperature of operation), there will be no problem. However, as a last judgment, product heat generation in actual operation should be measured, to confirm a loss and junction temperature from figure 20.

When the device is used with a heatsink attached, device package thermal resistance, $R_{\theta JA}$, changes the variable used in calculating ΔT_{j-a}. The value of $R_{\theta FIN}$ is calculated from the following formula:

$$R_{\theta JA} \approx R_{\theta JC} + R_{\theta Fin} = R_{\theta JA} - R_{\theta CA} + R_{\theta Fin} \quad (9)$$

where $R_{\theta j-a}$ is the thermal resistance of the heatsink. ΔT_{j-a} can be calculated with using the value of $R_{\theta JA.}$

The following procedure should be used to measure product temperature and to estimate junction temperature in actual operation:

First, measure the temperature rise at the center of the back surface of the device case (ΔT_{c-a}).

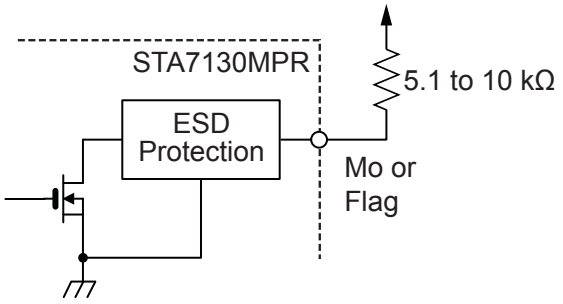


Figure 19. Mo pin and Flag pin equivalent circuit

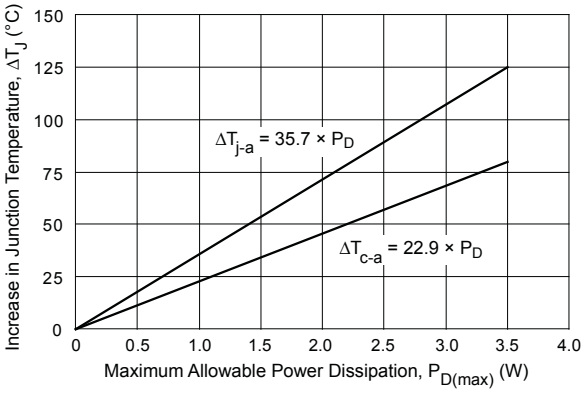


Figure 20. Temperature increase

Second, estimate the loss (P_D) and junction temperature (T_j) from the temperature rise with reference to figure 20, the temperature increase graph. At this point, the device temperature rise ($\Delta T_{c\text{-}a}$) and the junction temperature rise (ΔT_j) can be estimated under the following equation:

$$\Delta T_J \approx \Delta T_{c\text{-}a} + P_D \times R_{\theta j\text{-}c} \quad (10)$$

Notes

The STA7130MPR series is designed as a multichip package, with separate power elements (MOSFET), control IC (MIC), and sense resistance. Consequently, because the control IC cannot accurately detect the temperature of the power elements (which are the primary sources of heat), the device does not provide a protection function against overheating. For thermal protection, users must conduct sufficient thermal evaluations to be able to ensure that the junction temperature does not exceed the warranty level (150°C).

This thermal design information is provided for preliminary design estimations only. The thermal performance of the device will be significantly determined by the conditions of the application, in particular the state of the mounting PCB, heatsink, and the ambient air. Before operating the device in an application, the user must experimentally determine the actual thermal performance.

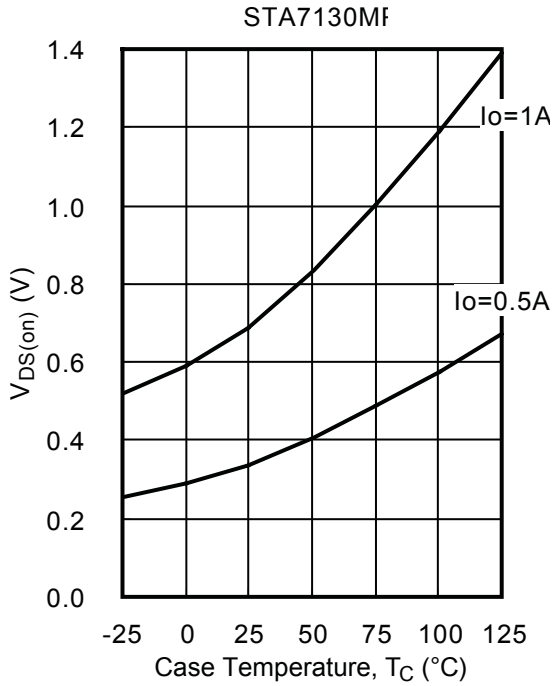
The maximum recommended case temperatures (at the center back surface) for the devices are:

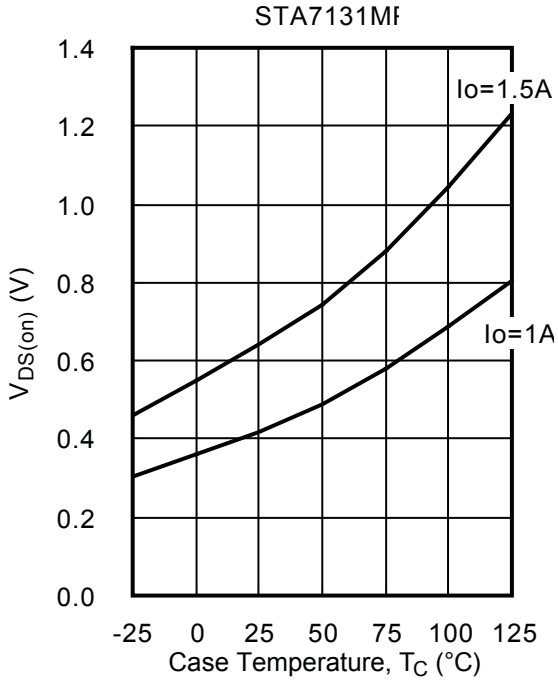
• With no external heatsink connection: 85°C

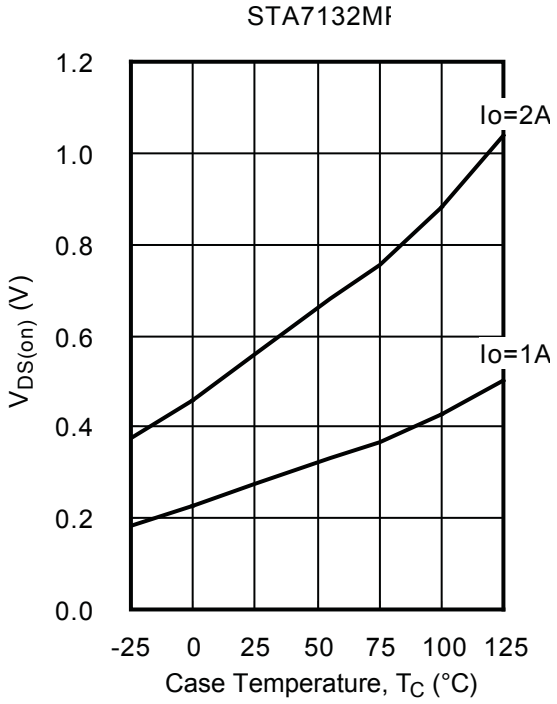
• With external heatsink connection: 75°C

Characteristic Performance

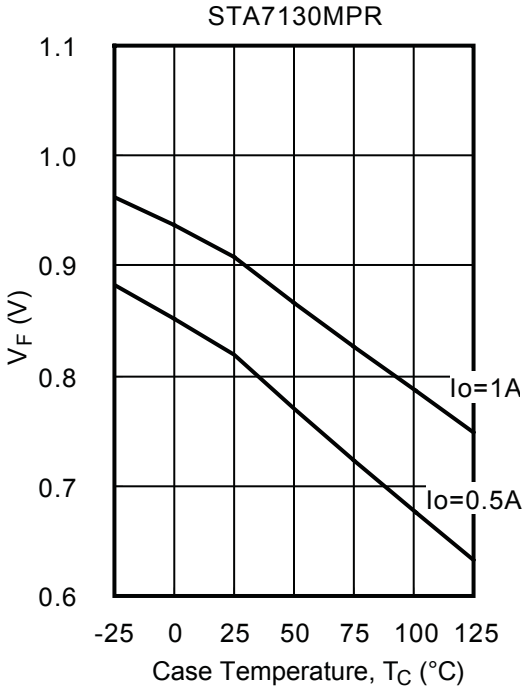
Output MOSFET On-Voltage, $V_{DS(on)}$, Characteristics

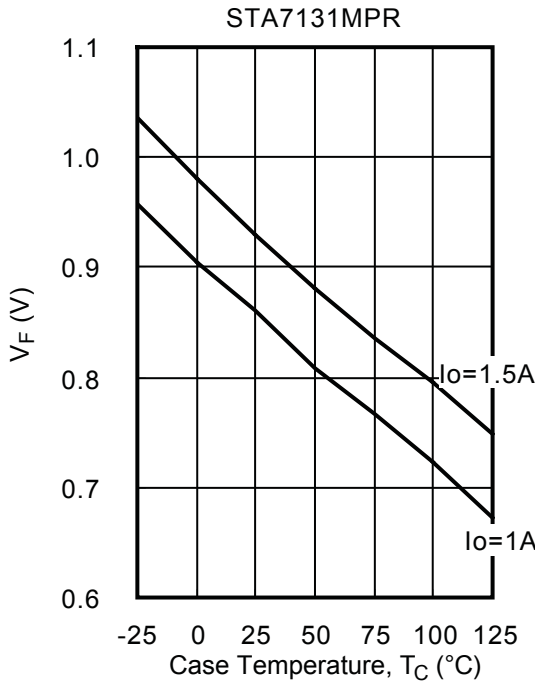


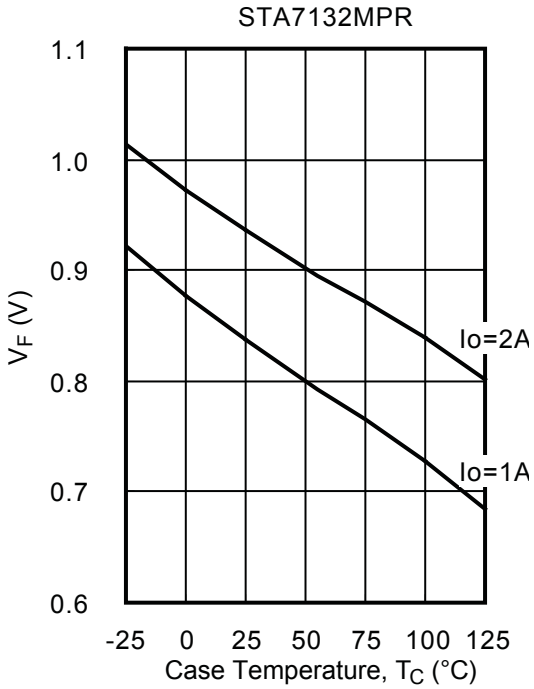




Output MOSFET Body Diode Forward Voltage, V_F, Characteristics







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