STR-L6400 Series Application Note (Ver. 1.4)

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1. General Descriptions

The STR-L6400 series devices comprise an integrated MOSFET and a multifunction controller chip for quasi-resonant switching power supply applications.

In normal operation, the quasi-resonant operation mode coupled with the bottom-skip functions achieves high efficiency and low noise. In standby operation, the burst operation mode ensures lower power consumption.

The controller circuit is common in the STR-Y6400 series, using the compact 7-pin full mold package (TO220F-7L: Sanken designation: FMS207). The STR-L6400 series are using the SIP 10-pin type (Sanken designation: STA-10), providing enough clearance and creepage isolation between high voltage terminals and low voltage terminals. These switchers also provide various protection features that allow power supply designs that are highly reliable and simple－with fewer peripheral components.

2. Features and Production Lineup

- SIP-10pin package
- Built-in Startup circuit (eliminates startup losses and results in low power consumption)
- Multi-mode control enables the high efficiency operation across the full load range
- Automatic Standby mode (improves efficiency by burst-oscillation at light loads, Input wattage Pin < 0.1 W at zero output load condition)
- Bottom-skip mode reduces the switching loss under medium to light loads
- Built-in soft start function reduces the stress applied to power MOSFET during transitions
- Built-in Leading Edge Blanking (LEB) function
- Built-in protection functions for Overcurrent (OCP), Overvoltage (OVP), Overload (OLP), Thermal shutdown (TSD) protection and maximum ON time limitation
- Two-chip structure: a MOSFET and a control IC (the MOSFET has an avalanche energy guarantee)

The production lineup for the STR-L6400 series provides the options shown in the following table.

Product No.	MOSFET V_{DSS}(MIN)[V]	$R_{DS(ON)}$ (MAX)[Ω]	Vin AC [V]	P_{out} [W] (Note 1,2)
STR-L6452	650	3.4	100	22
			220	30
STR-L6472	850	6.5	100	15
			220	25

Note 1: The maximum output power is derived from thermal specifications. The actual output power may be available around 120 – 140% of the above values, respectively, but will be limited by ON duty setting on transformer design or lower output voltage.

Note 2: The condition of the maximum output power is “without heat sink”.

3. Functional Block Diagram and Terminal List

The devices share a common basic electrical configuration, as shown in the functional block diagram in fig.3.
The assignments of terminals in the packages also is common throughout the series, allowing easier design reuse.
The terminal assignments are shown in the Terminal List table in tab.3.

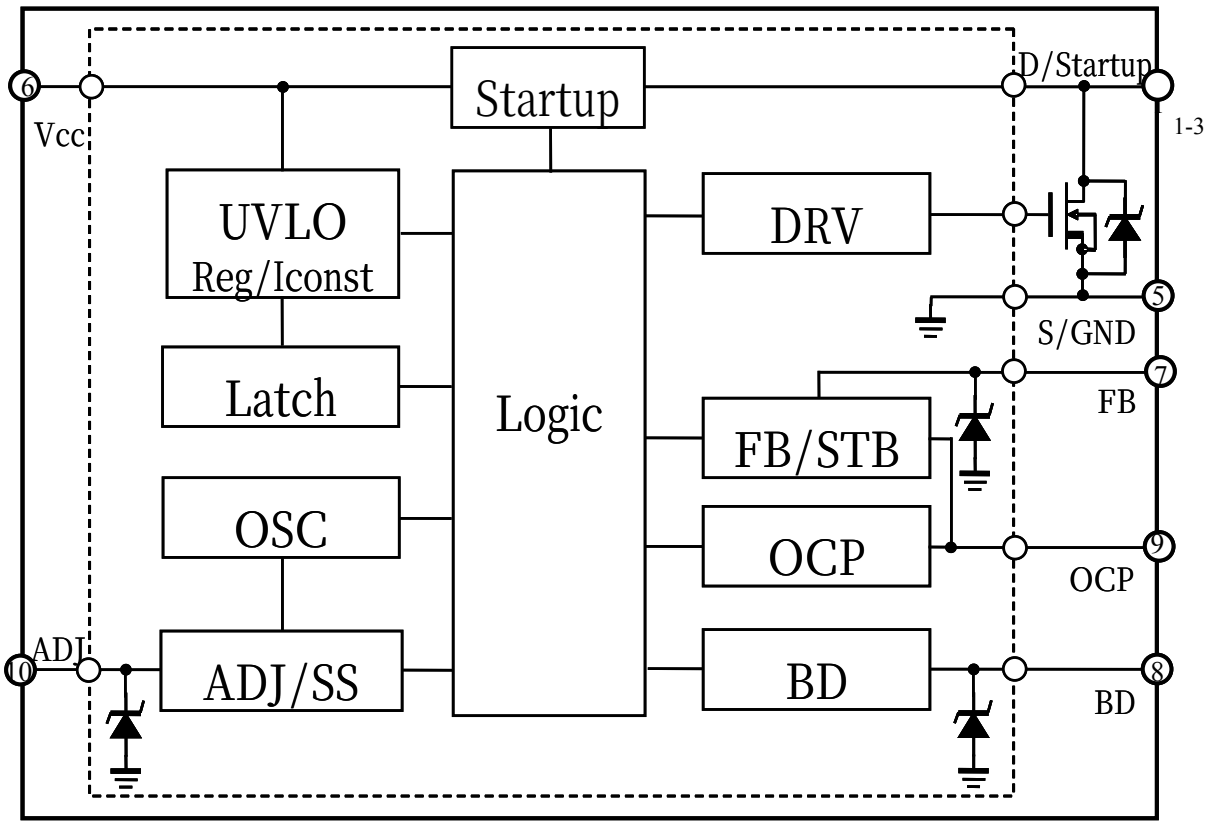


Fig.3 STR-L6400 Series Functional Block Diagram

Terminal List Table

Terminal No.	Symbol	Name	Descriptions
1 - 3	D/Startup	Drain / Start-up Terminal	MOSFET Drain / Start-up current input
5	S/GND	Source / Ground Terminal	MOSFET Source / Ground
6	V_{CC}	Power Supply Terminal	Input of power supply for control circuit
7	FB	Feedback Terminal	Constant voltage control signal input / Standby control input / OLP signal input
8	BD	Bottom Detection / OCP Compensation for AC Input Voltage Terminal	QR signal input / Overcurrent compensation input
9	OCP	OCP Input Terminal	OCP pulse input / Bottom-skip signal input
10	ADJ	Adjustment Terminal	Soft start control / Bottom-skip delay time control / Remote ON/OFF signal input

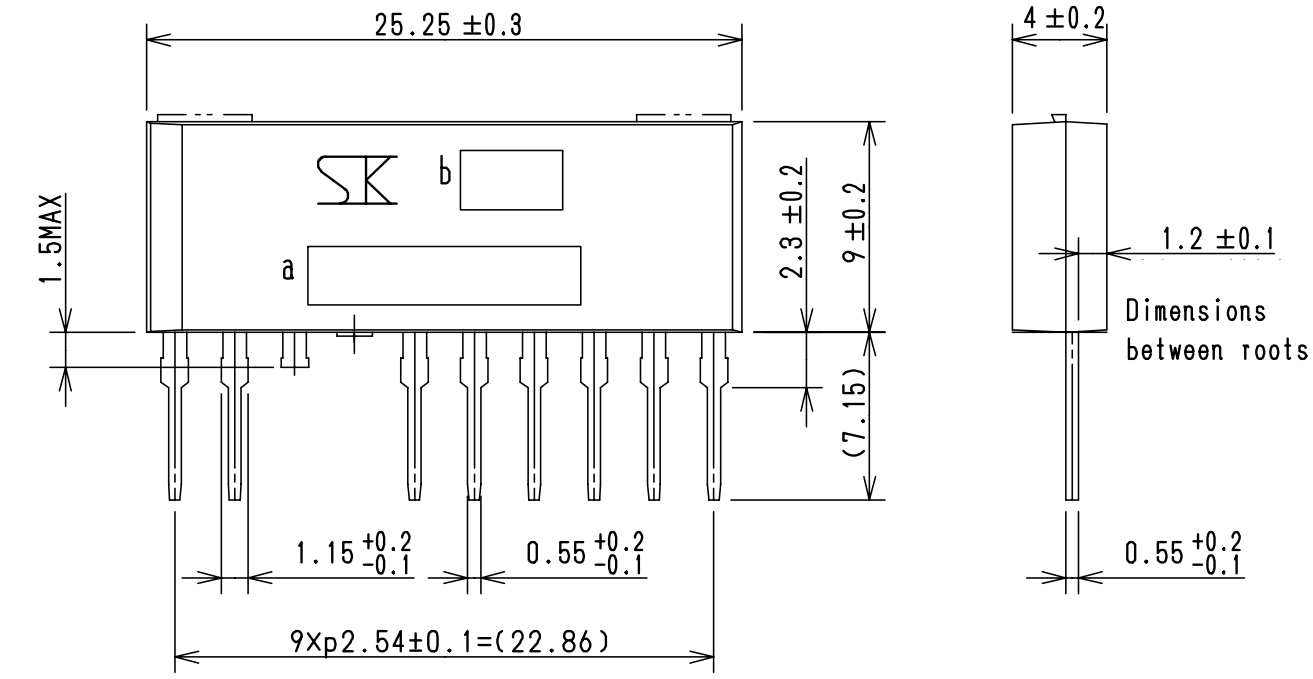
Tab.3 STR-L6400 Series Terminal List table

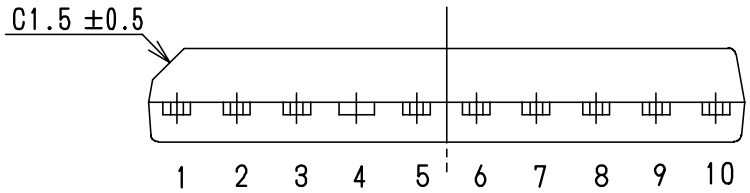
4. Package Information

SIP-10 pin type (Sanken designation: STA-10)

No.4 terminal is removed to provide greater clearance and creepage isolation for the high voltage input (No.1-3) and No.3 terminal is cut.

The package dimensions and branding are shown below, and this lead framing number is LF437.





Dimensions in mm

a. Type Number
b. Lot Number : YMDD
Y is the last digit of the year of manufacture
M is the month(1 to 9, O,N,D)
DD is the 2-digit date

Material of terminal: Cu
Treatment of terminal : Ni plating + solder dip
Weight: Approx. 2.8g

5. Electrical Characteristics (Example: STR-L6472)

The following tables provide electrical characteristics for the STR-L6400 series.

The STR-L6472 is used as an example.

Both absolute maximum ratings and operating characteristics are provided.

Certain details vary among the individual devices.

5.1 Absolute Maximum Ratings, valid at T_a = 25°C

Parameter	Terminal	Symbol	Rating	Unit	Note
Drain Current ※1	1－5	I_{Dpeak}	4.2	A	Single pulse
Maximum Switching Current ※1	1－5	I_{DMAX}	4.2	A	Ta=-30～+125℃
Avalanche Energy ※1	1－5	E_{AS}	40	mJ	Single pulse
		IL_{peak}	1.9	A	V_{DD}=99V, L=20mH
Supply Voltage for Control Circuit	6－5	V_{CC}	32	V	
Startup Terminal Voltage	1－5	$V_{STARTUP}$	-1.0～V_{DSS}	V	
ADJ Terminal Sink Current	10－5	I_{ADJ}	3.0	mA	
FB Terminal Sink Current	7－5	I_{FB}	8.0	mA	
BD Terminal Sink Current	8－5	I_{BDIN}	2.0	mA	
BD Terminal Source Current	8－5	I_{BDOUT}	-2.0	mA	
OCP Terminal Voltage	9－5	V_{OCP}	-1.5～+2.0	V	
Power Dissipation in MOSFET ※1	1－5	P_{D1}	14.7	W	With infinite heat sink
			2.0	W	Without heat sink
Power Dissipation in Control Circuit	—	P_{D2}	0.8	W	
Internal Frame Temperature in Operation	—	T_F	-30～+125	℃	
Operating Ambient Temperature	—	T_{op}	-30～+125	℃	
Storage Temperature	—	T_{stg}	-40～+125	℃	
Channel Temperature	—	T_{ch}	+150	℃	

＊1 Refer to individual device datasheet for details; value differs among devices.

＊ Current characteristics are defined based on IC as Sink:+, Source:－.

5. 2 Electrical Characteristics in MOSFET, valid at T_a = 25°C

Parameter	Terminal	Symbol	Rating			Unit	Note
			MIN	TYP	MAX		
Drain-source Voltage ※1	1 – 5	V_{DSS}	850	—	—	V	
Drain Leakage Current	1 – 5	I_{DSS}	—	—	300	μA	
ON Resistance ※1	1 – 5	$R_{DS(ON)}$	—	—	6.5	Ω	
Switching Time ※1	1 – 5	t_f	—	—	200	nS	
Thermal Resistance ※1	—	θ_{ch-F}	—	2.4	3.1	℃/W	Channel to internal frame

5.3 Control Circuit Electrical Characteristics,

valid at T_a = 25°C, V_{CC}=20V, unless otherwise specified (or noted).

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Power Supply Start-up Operation						
Operation Start Voltage	6－5	$V_{CC(ON)}$	14.4	16.2	18.4	V
Operation Stop Voltage	6－5	$V_{CC(OFF)}$	9.0	10.0	11.3	V
Circuit Current in Operation	6－5	$I_{CC(ON)}$	—	3.5	5.5	mA
Circuit Current in Non-operation	6－5	$I_{CC(OFF)}$	—	10	50	μA
Start-up Circuit Operation Voltage	1－5	$V_{START(ON)}$	55	82	100	V
Start-up Current	6－5	$I_{CC(STARTUP)}$	-2.4	-1.4	-0.5	mA
Start-up Current after OLP Operation	6－5	$I_{CC(STARTOLP)}$	-1.10	-0.50	-0.15	mA
Oscillation Frequency	1－5	f_{OSC}	17.5	21.0	25.0	kHz
Soft Start Operation Stop Voltage	10－5	$V_{ADJ(SS)}$	2.0	2.3	2.6	V
Soft Start Operation Charge Current	10－5	$I_{ADJ(SS)}$	-148	-110	-71	μA
Power-off Threshold Voltage	10－5	$V_{ADJ(OFF)}$	8.2	9.4	10.8	V
Normal Operation						
Bottom-skip Operation Threshold Voltage 1	9－5	$V_{OCP(BS1)}$	-0.720	-0.668	-0.605	V
Bottom-skip Operation Threshold Voltage 2	9－5	$V_{OCP(BS2)}$	-0.485	-0.435	-0.381	V
Bottom-skip Operation Threshold Voltage 3	9－5	$V_{OCP(BS3)}$	-0.205	-0.145	-0.085	V
Bottom-skip Operation Start Voltage	10－5	$V_{ADJ(BS)}$	3.8	4.3	4.8	V
Bottom-skip State Detection Bias Current	10－5	$I_{ADJ(BS)}$	-27	-20	-13	μA
BD Terminal Upper Clamp Voltage	8－5	$V_{BD(HC)}$	—	6.3	—	V
BD Terminal Lower Clamp Voltage	8－5	$V_{BD(LC)}$	—	-0.075	—	V
QR Operation Threshold Voltage 1	8－5	$V_{BD(TH1)}$	0.12	0.31	0.60	V
QR Operation Threshold Voltage 2	8－5	$V_{BD(TH2)}$	0.01	0.15	0.32	V
Maximum Feedback Current	7－5	$I_{FB(MAX)}$	-315	-225	-135	μA
Standby Operation						
Standby State Detection Voltage	7－5	$V_{FB(STBIN)}$	1.40	1.63	1.85	V
Standby State Start Voltage	10－5	$V_{ADJ(STB)}$	5.7	6.2	6.8	V
Standby Operation Threshold Voltage	7－5	$V_{FB(STBOP)}$	0.80	1.00	1.25	V
Minimum T_{ON} period (Normal Operation)	1－5	$T_{ONL(MIN)}$	0.98	1.62	2.19	μS
Minimum T_{ON} period (Input Compensation Operation)	1－5	$T_{ONH(MIN)}$	0.54	0.98	1.40	μS

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Protection Operation						
Maximum T_{ON} period	1－5	$T_{ON(MAX)}$	31	36	41	μS
Leading Edge Blanking Time	1－5	$T_{ON(LEB)}$	-	354	-	nS
Over Current Detection Threshold Voltage (Normal Operation)	9－5	$V_{OCP(H)}$	-0.975	-0.930	-0.875	V
Over Current Detection Threshold Voltage (Input Compensation Operation)	9－5	$V_{OCP(L)}$	-0.904	-0.780	-0.656	V
OCP* Terminal Source Current	9－5	$I_{OCP(O)}$	-260	-130	-40	μA
Input Compensation Detection Threshold Current 1	8－5	$I_{BD(TH1)}$	-575	-500	-425	μA
Input Compensation Detection Threshold Current 2	8－5	$I_{BD(TH2)}$	-565	-450	-375	μA
OLP* Bias Current	7－5	$I_{FB(OLP)}$	-27	-20	-13	μA
OLP* Auto-restart Threshold Voltage	7－5	$V_{FB(OLPAUTO)}$	6.3	6.7	7.3	V
OLP* Latch-off Bias Current	7－5	$I_{FB(OLPLa.OFF)}$	-1.5	-1.0	-0.5	mA
OLP* Latch-off Threshold Voltage	7－5	$V_{FB(OLPLa.OFF)}$	8.6	9.6	10.2	V
OVP* Operation Voltage	6－5	$V_{CC(OVP)}$	26.0	28.5	31.0	V
Latch Circuit Release Voltage ※2	6－5	$V_{CC(La.OFF)}$	6.2	7.5	8.9	V
FB Terminal Maximum Voltage in Feedback Operation	7－5	$V_{FB(MAX)}$	4.90	5.45	6.00	V
Thermal Shut-down Temperature	—	$T_{j(TSD)}$	135	-	-	℃

＊2 Latch circuit is activated by OLP, OVP and TSD functions.

＊ QR : Quasi-resonant, OCP : Overcurrent Protection, OVP : Overvoltage Protection, OLP : Overload Protection

6. Typical Application Circuit

The PCB traces from the D/ST terminals (No.1-2), shall be as wide as possible, in order to enhance thermal dissipation.

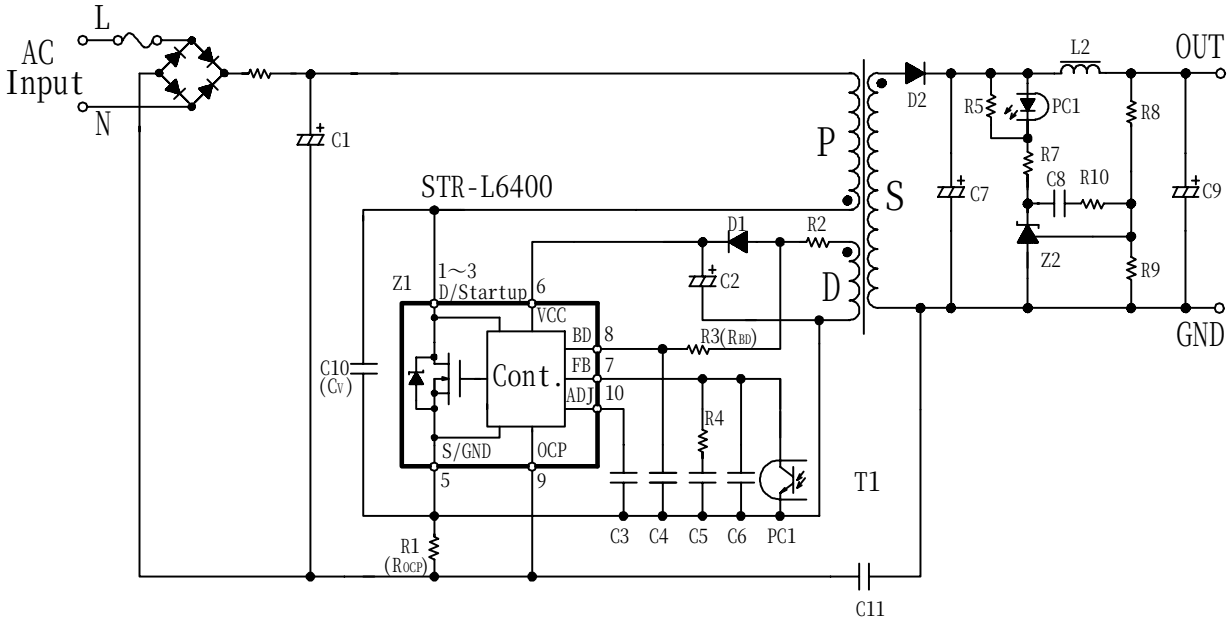


Fig.6 STR-L6400 typical application circuit

7. Functional Descriptions

7.1 V_{CC} (No. 6) Terminal

V_{CC} is the power supply terminal for control circuit.

7. 1. 1 Start-up Circuit

The startup circuit is connected to the drain terminals, D/Startup (No.1-3). During the start-up process, the constant current ($I_{CC(STARTUP)}$ = −1.4 mA typical) charges C2 at V_{CC} terminal (see fig.7-1), and when the startup voltage level ($V_{CC(ON)}$ = 16.2 V typical) is reached, the device starts switching operation.

Hence, the C2 value decides the duration of the startup period, according to the following formula:

$$t_{START} = C2 \times (V_{CC(ON)} - V_{CC(INIT)}) / I_{CC(STARTUP)} \quad \text{--- (1)}$$

where t_{START} is the startup period, in s, and $V_{CC(INIT)}$ is the initial voltage on V_{CC} terminal, in V. C2 shall be 10 to 47 μF, if it is a general power supply application.

After switching operation begins, the startup circuit turns off automatically, to zero its current consumption.

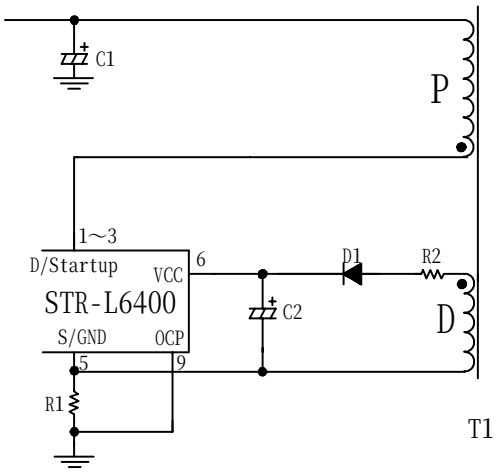


Fig.7-1 V_{CC} peripheral circuit

Fig.7-2 shows the relationship of V_{CC} and I_{CC}.

When V_{CC} terminal voltage reaches $V_{CC(ON)}$, the device starts normal operation and I_{CC} increases. While the device is in operation, if V_{CC} terminal voltage decreases to the shutdown voltage level ($V_{CC(OFF)}$ = 10.0V typical), the undervoltage lockout (UVLO) circuit stops device operation, and the device reverts to the state before startup.

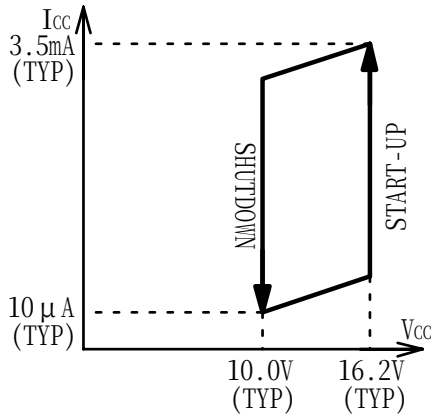


Fig.7-2 Relationship of V_{CC} and I_{CC} at startup and shutdown

As shown in fig.7-3, when the start-up fails because V_{CC} terminal voltage drops below $V_{CC(OFF)}$ = 10.0V (TYP), it will be necessary for C2 to use a larger capacitance. As a larger capacitance causes a longer start-up time, it is necessary to examine about the problems on actual operations.

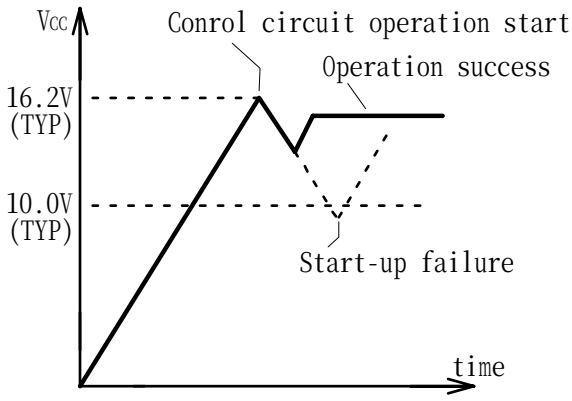


Fig.7-3 V_{CC} behavior at startup

7. 1. 2 Auxiliary Winding

After the device starts normal operation, the voltage from auxiliary winding (D in fig.7-1) becomes a power source to the device. The auxiliary winding voltage needs to be adjusted to approximately 18V, taking into account the turns ratio of

auxiliary winding D, so that V_{CC} terminal voltage becomes:

$$V_{CC(OFF)} = 11.3V(max) < V_{CC} < V_{CC(OVP)} = 26.0\ V(min) \quad \text{--- (2)}$$

within the limits for input and output deviation.

And the bottom point of V_{CC} terminal voltage is recommended 12.5V or higher.

In actual power supply circuits, there are cases in which V_{CC} voltage fluctuates in direct proportion to the output of the SMPS (see fig.7-4). This happens because the circuit current of STR-L6400 series is small, and C2 is charged to a peak by the transient surge voltage that is generated at the moment MOSFET turns off.

To alleviate C2 peak charging, lowering the influence on auxiliary winding D of the surge voltage from the primary winding shall be accomplished. It is effective to add some value R2, of several ohms to several tenths of an ohm, in series with D1 (see fig.7-1). The optimal value of R2 shall be determined using a transformer matching the application, because the proportion of V_{CC} voltage versus the transformer output voltage differs according to transformer structural design.

The proportion of change between V_{CC} voltage and the SMPS output voltage becomes worse if:

- the coupling between the primary winding and the secondary winding of transformer get worse, and/or
- the coupling between the auxiliary winding D and the stabilizing output winding (a winding of the circuit that controls a constant voltage) gets worse.

Considering the above, extra attention is required for the winding location of auxiliary winding D. Fig.7-5 and 7-6 diagram alternative designs for the location of auxiliary winding D.

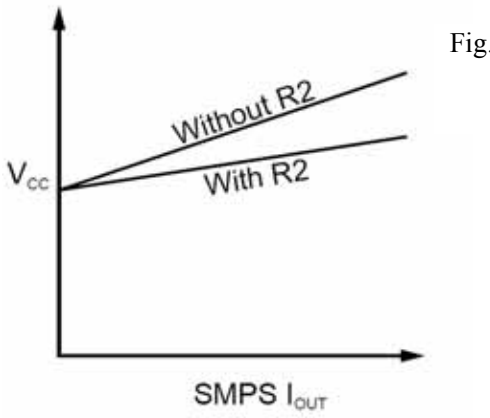


Fig.7-4 Effect of R2 (see fig.7-1) on the proportion of V_{CC} versus the SMPS output current

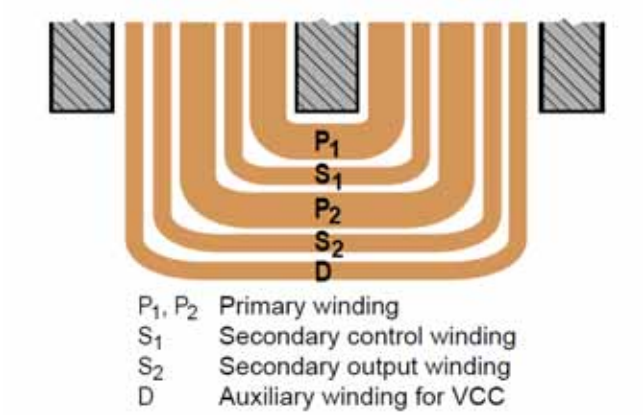


Fig.7-5 Auxiliary winding D remote from primary winding Px

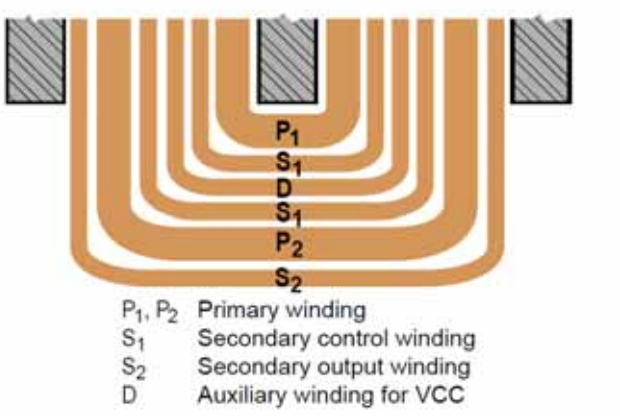


Fig.7-6 Auxiliary winding D within a stabilizing output winding, S1

7. 1. 3 Over Voltage Protection

When more than OVP threshold voltage of $V_{CC(OVP)}$ = 28.5 V (TYP) occurs between V_{CC} terminal and GND terminal, the OVP function starts operation. It shuts down the device with latch mode.

The OVP function can detect overvoltage on the transformer secondary output, because the normal V_{CC} power supply voltage, from the auxiliary winding of transformer, is in proportion to the output voltage.

This provides protection in cases such as a circuit open on the secondary side.

The secondary side output voltage that initiates OVP operation can be calculated approximately from the following formula:

$$Vout(OVP)\ [V] \quad \frac{VOUT\ (normal\ )[V]}{VCC\ (normal\ )[V]} \times 28.5[V]\ (TYP\ ) \quad \text{--- (3)}$$

7. 1. 4 Latch Operation

The fault latch function prevents the device from normal switching while OVP, OLP, TSD protection functions are in operation.

Fig.7-7 shows the transition diagram in OVP operation. When the device switching stops after a protection state is latched, the V_{CC} terminal voltage falls once to $V_{CC(OFF)}$ = 10.0V (TYP). After that, V_{CC} terminal repeats the charge and discharge between $V_{CC(ON)}$ = 16.2V (TYP) and $V_{CC(OFF)}$ = 10.0V (TYP) and prevents V_{CC} voltage excess increase.

Releasing the latch is done by dropping V_{CC} voltage below $V_{CC(La.Off)}$ = 7.5V (TYP) (Latch Circuit Release Voltage), which is normally done by shutting off AC input.

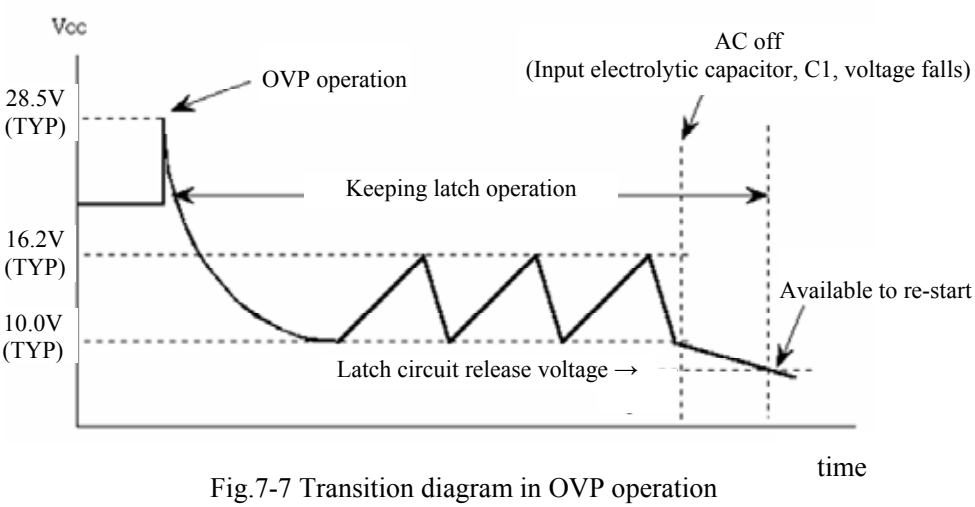


Fig.7-7 Transition diagram in OVP operation

7.2 ADJ (No.10) Terminal

ADJ terminal has 5 functions as below.

① Soft start function

② Delay time setting for QR mode switching

③ Delay time setting for auto standby switching

④ Disabling bottom-skip function / Auto standby function

⑤ External ON /OFF control

7.2.1 Soft Start Function

The built-in soft start function reduces the voltage and current stresses to MOSFET and secondary diode, during the start-up period. Fig.7-8 shows the peripheral circuit for ADJ terminal and the waveforms of MOSFET drain current I_D and ADJ terminal voltage V_{ADJ}.

C3 between ADJ terminal and GND terminals is charged with $I_{ADJ(SS)}$ = －110μA (TYP) (Soft Start Operation Charge Current). The t_{ON} period of MOSFET is limited depending on the ADJ terminal voltage. The soft start operation continues until the ADJ terminal voltage reaches $V_{ADJ(SS)}$ = 2.3V(TYP) (Soft Start Operation Stop Voltage). For reference, in case that C3 is 0.22μF, the soft start period is about 4.6ms (TYP).

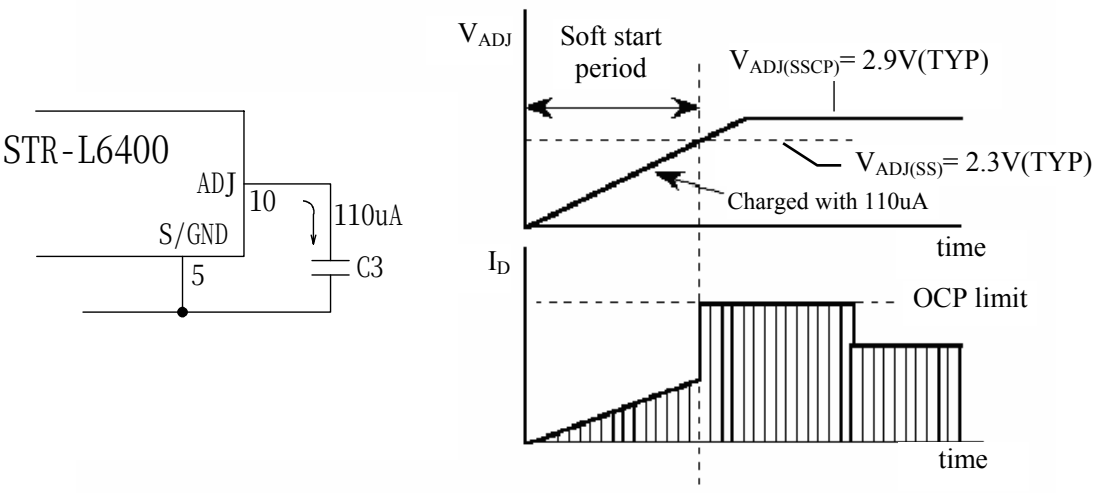


Fig.7-8 ADJ terminal peripheral circuit / Soft start operation at start-up

$V_{ADJ(SSCP)}$ is 2.9V (TYP) on the steady state condition.

7.2.2 Delay Time Setting for QR Mode Switching

STR-L6400 series has the delay time setting for the transit between QR and Bottom-skip mode, between 1 bottom-skip and 2 bottom-skip mode. Therefore, the operation in the same mode is available corresponding for frequent dynamic load changes, and the reduction of audible noise from transformer is achieved with this function. The delay time setting is adjusted using the charge time for soft start capacitor, C3, connected to ADJ terminal as shown in fig.7-8.

Under the load change, only when OCP terminal voltage reaches $V_{OCP(BSX)}$ (Bottom-skip Operation Threshold Voltage) and continues for a delay time, the operation mode is switched.

In case the load condition returns to the previous condition within a delay time, the operation mode is not switched.

As $V_{OCP(BSX)}$ has hysteresis, the same mode is maintained with the hysteresis unless a load change exceeds hysteresis.

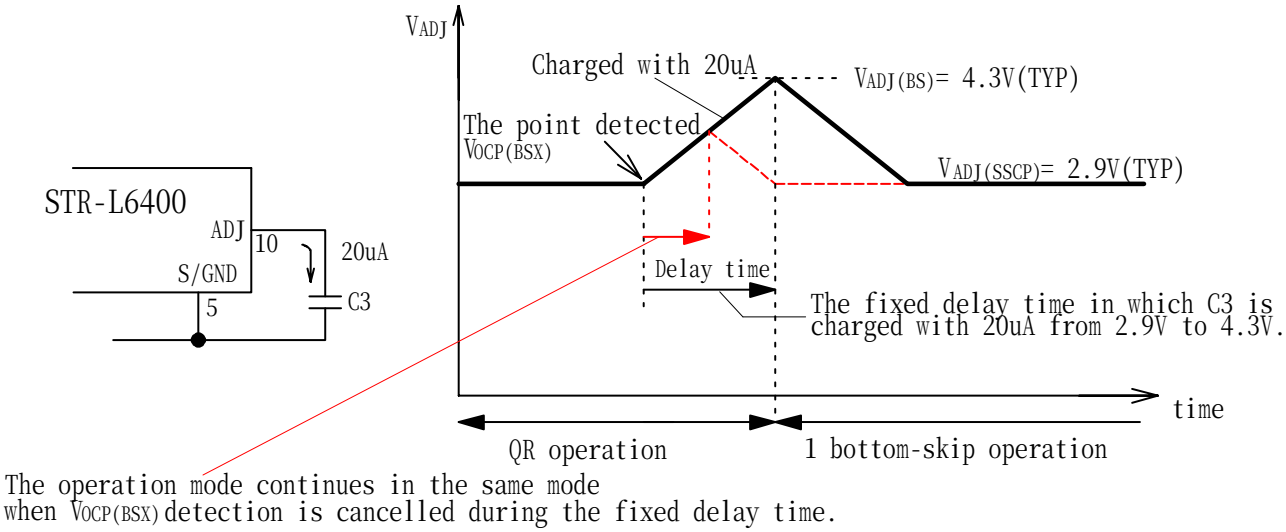


Fig.7-9 Transition diagram under dynamic load change / ADJ terminal peripheral circuit

When C3 is 0.22 μF, the delay time is about 15.4mS.

7.2.3 Delay Time Setting for Auto Standby Switching

STR-L6400 series has the delay time setting for auto standby switching. It is also implemented in the same manner of the delay time setting for QR mode switching in 7.2.2.

Fig.7-10 shows the transition diagram for the switching to auto standby operation.

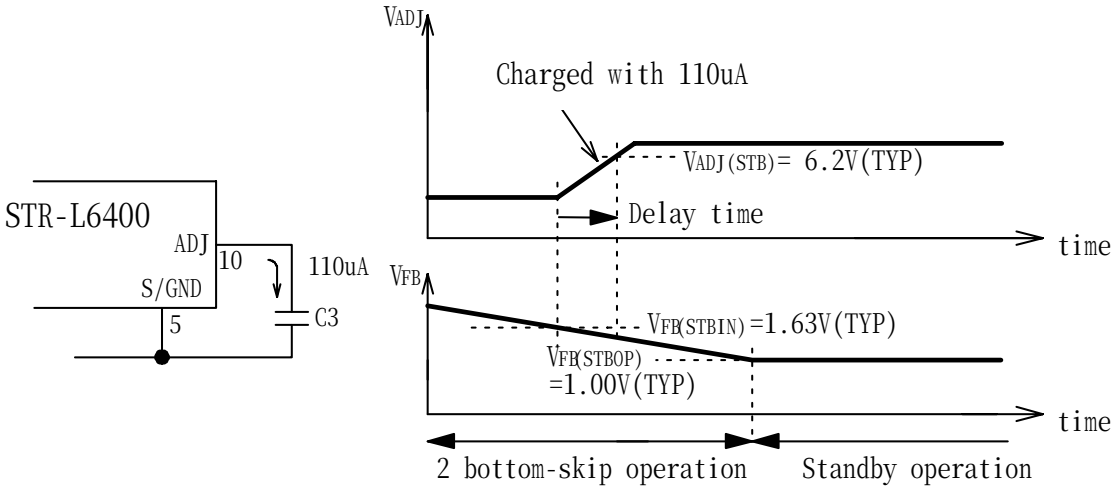


Fig.7-10 Transition diagram for the switching to auto standby operation

In case C3 is 0.22 μF, the delay time is about 6.6mS.

When the load condition changes lighter from low load condition, the feedback current to FB terminal from the photo-coupler is increasing, and the FB terminal voltage is decreasing. If FB terminal voltage falls below

$V_{FB(STBIN)}$ = 1.63V (TYP) (Standby State Detection Voltage), C3 connected to ADJ terminal starts to be charged with $I_{ADJ(SS)}$ = 110μA (TYP) (Soft Start Operation Charging Current). When the ADJ terminal voltage reaches $V_{ADJ(STB)}$ = 6.2V (TYP) (Standby State Start Voltage), the device becomes ready to enter into the burst operation mode. If the load becomes heavier again during the delay time and the FB terminal voltage exceeds $V_{FB(STB)}$ = 1.63V (TYP), the device returns to the bottom-skip operation or the QR operation according to the load conditions, without switching to the burst operation mode.

When the FB terminal voltage continues decreasing and falls below $V_{FB(STBOP)}$ = 1.0V (TYP) (Standby Operation Threshold Voltage), the burst operation mode starts. In addition, when the T_{ON} period reaches $T_{ONL(MIN)}$* / $T_{ONH(MIN)}$* = 1.62μS / 0.98μS (TYP) (Minimum T_{ON} period (Normal Operation) / (Minimum T_{ON} period (Input Compensation Operation), the feedback current is increasing higher. Therefore, the minimum T_{ON} period works for the trigger to enter to standby mode.

The burst operation mode cycle varies on the feedback current according to the load conditions.

※ $T_{ONL(MIN)}$* / $T_{ONH(MIN)}$*: Actual Ton period to standby mode depends on input compensation: refer to 7.4.2.

7.2.4 Disabling Bottom-skip Function / Auto Standby Function

The bottom-skip function and the auto standby function are disabled by connecting external components to ADJ terminal.

Fig.7-11 shows the circuit example for disabling both functions, and fig.7-12 shows only for disabling the auto standby function.

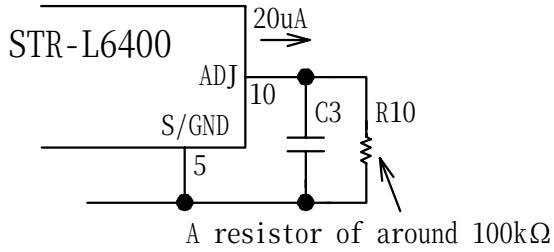


Fig.7-11 Circuit disabling both functions of bottom-skip and auto standby

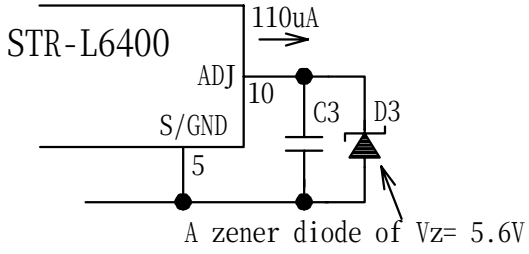


Fig.7-12 Circuit disabling only auto standby function

Disabling Bottom-skip Function

During bottom-skip operation, the ADJ terminal charges C3 with $I_{ADJ(BS)}$ = −20μA (TYP) (Bottom-skip State Detection Bias Current). By connecting a resistor, R10, in parallel with C3 and limiting the terminal voltage increase, the bottom-skip function is disabled. As shown in fig.7-11, by connecting R10 of around 100KΩ, the bottom-skip function is disabled because ADJ terminal voltage is limited at 2V (= 20μA × 100kΩ), which is lower than $V_{ADJ(BS)}$ = 3.8V (MIN) (Bottom-skip Operation Start Voltage).

Disabling Auto Standby Function

To start the burst operation mode, the ADJ terminal voltage shall reach higher than $V_{ADJ(STB)}$ = 6.2V (TYP). However, by connecting a zener diode of V_Z = 5.6V, D3, in parallel with C3, the auto standby function is disabled because ADJ terminal voltage is limited under $V_{ADJ(STB)}$ = 6.2V (TYP). In this case, the voltage difference between V_Z = 5.6V and $V_{ADJ(BS)}$ = 4.3V (TYP) is not enough. It is necessary to take care of the zener voltage accuracy and select the proper zener diode rank.

7.2.5 External ON / OFF Control

The ADJ terminal has the remote ON / OFF control function by applying the external signal. By increasing ADJ terminal voltage to $V_{ADJ(OFF)}$ = 9.4V (TYP) (Power-off Threshold Voltage) and over, the device is stopped (OFF). Fig.7-13 shows the typical circuit example, the external power supply (12－16V) provides ADJ terminal with more than $V_{ADJ(OFF)}$ through R11 (10k – 30KΩ) and a photo-coupler when the photo-coupler turns on by the external signal. And also by continuing to apply the higher voltage than $V_{ADJ(OFF)}$, the device holds OFF state. In this example, if the ON state is activated from the OFF state by turning off the photo-coupler, the operation always starts from discharging the soft start capacitor. As a result, when the ON signal is applied, the ON state begins after the soft start period.

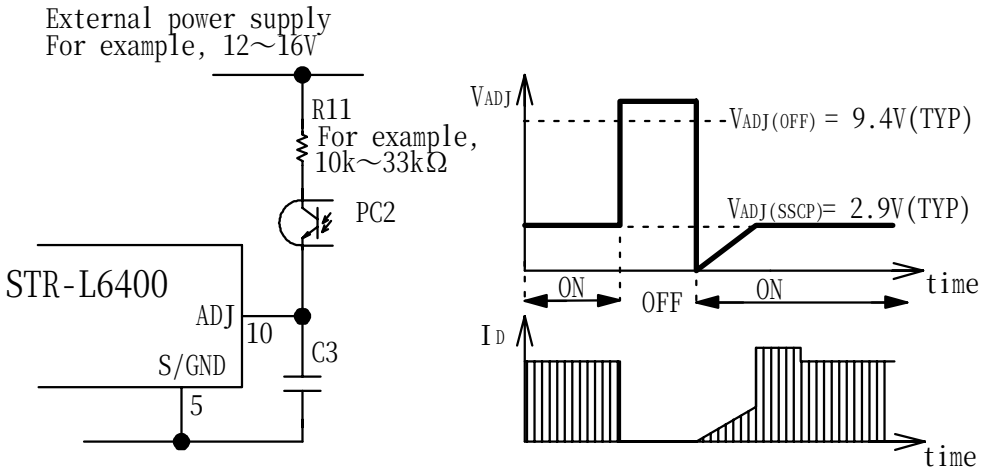


Fig.7-13 Typical circuit for external ON / OFF control

On the circuit design like the above, as the maximum rating of ADJ terminal sink current is = 3.0mA (MAX), the R11 value shall be calculated using the external power supply voltage and ADJ terminal current(below 3mA).

7.3 FB (No. 7) Terminal

FB terminal has 3 functions:

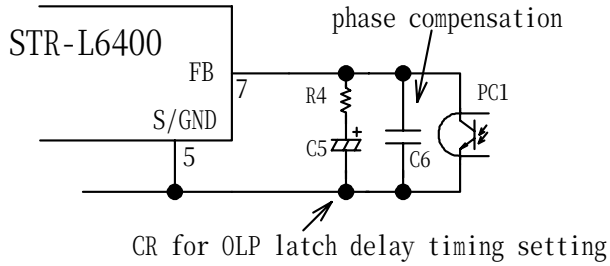
① Output voltage control

② Overload protection (OLP)

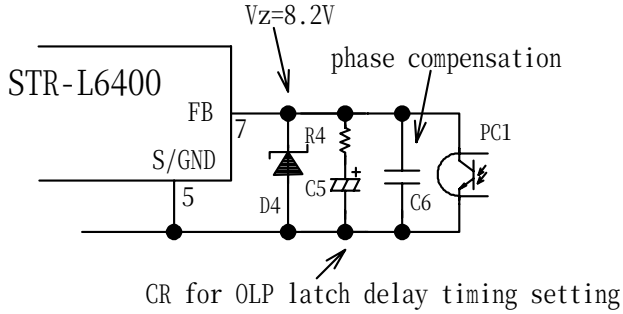
③ Burst operation control for standby mode ⇒ Refer 7.6 Standby Operation

7.3.1 Constant Output Voltage Control

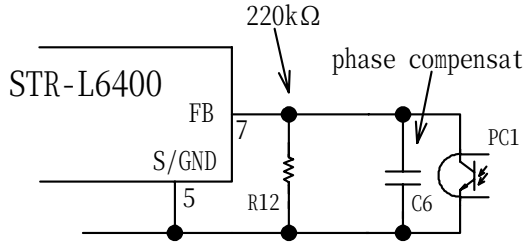
The constant output voltage control is achieved by connecting a photo-coupler to FB terminal and sinking the feedback current. Fig.7-14 shows the peripheral circuit of FB terminal. As the maximum feedback current, $I_{FB(MAX)}$, is –315μA (MIN), the forward current of photo-coupler on secondary side shall be set in consideration of aging degradation of CTR(Current Transfer Ratio) and others.



Normal setting (OLP: Latch shutdown)



Option 1 (OLP: Auto restart)



Option 2 (OLP: Disabling both functions)

Fig.7-14 FB terminal peripheral circuit / OLP operation mode selection

＊As for the values of resistance (R4) and capacitance (C5) for latch delay, generally, around 47kΩ and 4.7μF-10μF are recommended, respectively. The OLP function shall not activate on transient condition (power on and power off), but activate on overload condition. The delay time for OLP shall be adjusted by C5 value when it is shorter.

＊The capacitance (C6) for phase compensation shall be adjusted in the range of 470pF to 0.022μF. (Refer to 7.8, for the detail.)

7.3.2 Overload Protection (OLP) Function

Fig.7-15 shows the transition diagram in OLP operation. When the secondary output is in overload and the overcurrent protection function is activated on primary side, the output voltage decreases. As a result, the secondary error amplifies is cut-off and the feedback current from the photo-coupler is eliminated. At this time, the FB terminal is charged with $I_{FB(OLP)}$ = −20μA (TYP) (OLP Bias Current) during the latch delay time. If the FB terminal voltage reaches $V_{FB(OLPAUTO)}$ = 6.7V (TYP) (OLP Auto-restart Threshold Voltage), the OLP function starts and the oscillation stops. During this period, the V_{CC} terminal voltage decreases. However, after the FB terminal voltage reaches $V_{FB(OLPAUTO)}$ = 6.7V (TYP), the internal bias is switched to $I_{FB(OLPLa.OFF)}$ = −1.0mA(TYP) (OLP Latch-off Bias Current). As a result, the FB terminal voltage rapidly reaches $V_{FB(OLPLa.OFF)}$ = 9.6V (TYP) (OLP Latch-off Threshold Voltage) and the device enters into the latch mode, before V_{CC} terminal voltage falls below $V_{CC(OFF)}$ = 10.0V (TYP) (Operation Stop Voltage). The typical circuit of this operation is shown in the normal setting (OLP: Latch Shutdown) in fig.7-14.

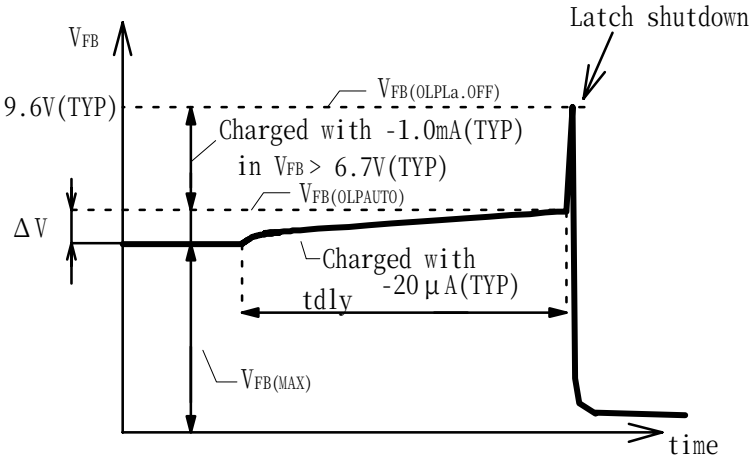


Fig.7-15 Transition diagram in OLP operation

There is the relative relation between $V_{FB(OLPAUTO)}$ and $V_{FB(MAX)}$, and the difference voltage, ΔV, between them is around 1V verified by design.

The tdly charged with −20μA can be calculated approximately from the following formula:

$$tdly \quad \frac{1V \times C5}{20uA} \quad \text{--- (4)}$$

7.3.2-1 Overload Protection (OLP) Function with Auto-restart

The transition diagram of OLP function with auto-restart is shown in fig.7-16. The circuit in "Option 1" in fig.7-14 is for this function with auto-restart. A zener diode of V_Z = 8.2V, D4, is placed between FB terminal and GND terminal, limiting FB terminal voltage not to reach $V_{FB(OLPLa.OFF)}$ = 9.6V (TYP).

As a result, the intermittent operation starts under the overload condition.

When the overload condition is released, the auto-restart is available. As shown in fig.7-16, after the FB terminal voltage reaches $V_{FB(OLPAUTO)}$ = 6.7V (TYP), the oscillation stops. Then the V_{CC} terminal voltage decreases and the auto-restart operation starts. In this operation, as the start-up current decreases to $I_{CC(STARTOLP)}$ = −0.5mA (TYP) (Start-up Current after OLP Operation), the oscillation stop period is extended and the heat generation at switching elements is reduced.

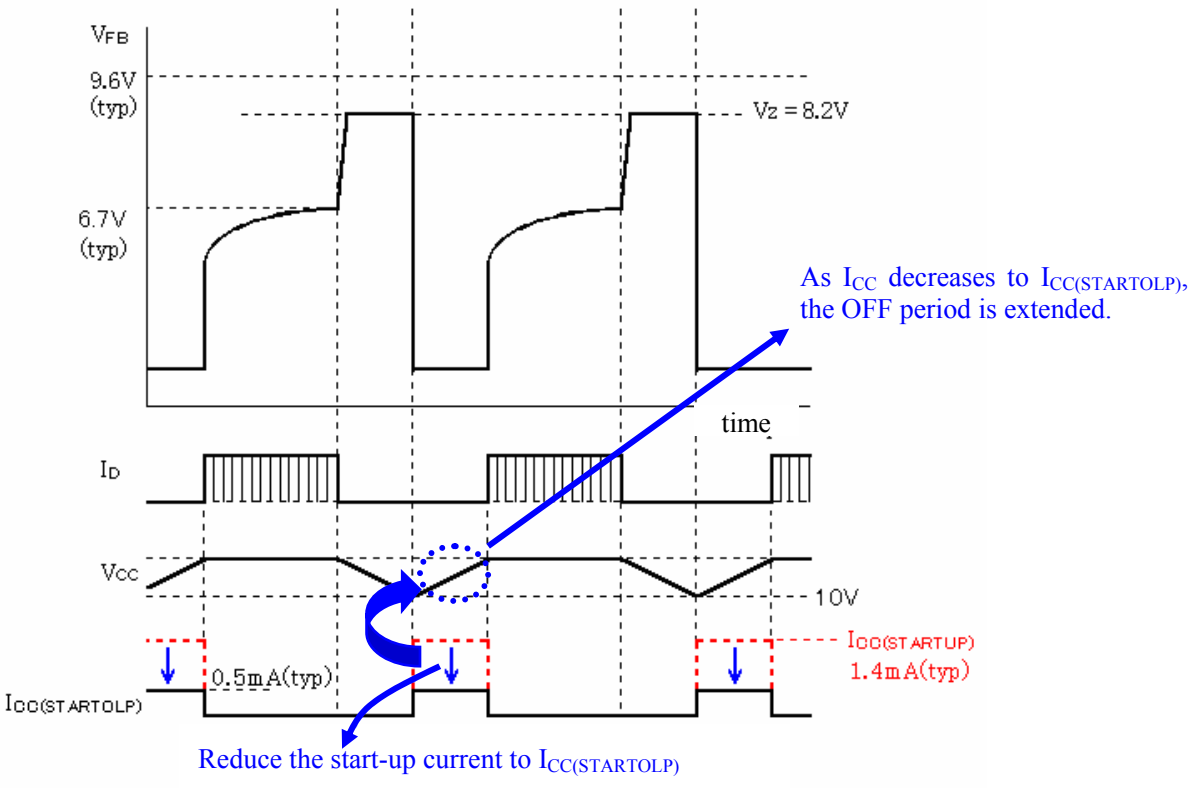


Fig.7-16 Transition diagram in auto-restart operation

7.3.2-2 Disabling OLP Function

The circuit in "Option 2" in fig.7-14 is for disabling OLP function. When R12 (220KΩ or lower) is placed between FB terminal and GND terminal, $I_{FB(OLP)}$ = −20μA (TYP) (OLP Bias Current) flows through R12, and the FB terminal voltage does not reach $V_{FB(OLPAUTO)}$ = 6.7V (TYP). Then the OLP functions (both of the latch operation and the auto-restart operation) are disabled.

When the OLP function is disabled, the output characteristics shall be constant power.

7.4 BD (No 8) Terminal

BD terminal has two separated functions.

① Turn-on timing determination by flyback voltage (plus voltage) of auxiliary winding

② Input compensation by forward voltage (minus voltage) of auxiliary winding

7. 4. 1 Bottom-on Timing (QR Signal)

The bottom-on function* is maintained, not only in the QR mode, but else in the bottom-skip mode.

※Bottom-on Function*: To reduce the switching losses at MOSFET turn-on, by turning-on at each bottom point of V_{DS} waveform of MOSFET.

Fig.7-17 shows the peripheral circuit for BD terminal and auxiliary winding voltage. After limiting the current of plus side (fly-back side) waveform generated on auxiliary winding by R3(R_{BD}), the plus side voltage is input to BD terminal.

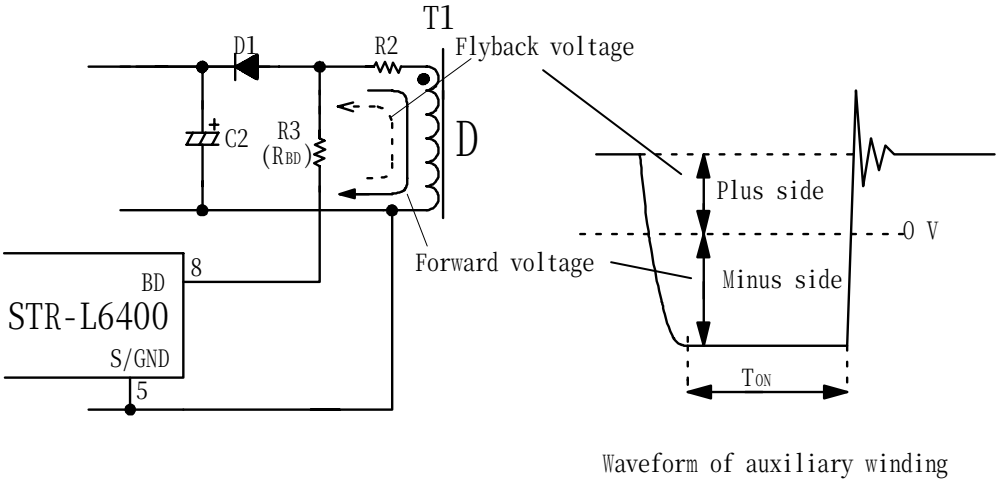


Fig.7-17 BD terminal peripheral circuit and auxiliary winding voltage

By clamping BD terminal voltage internally, the voltage shown in fig.7-18 (example: QR mode under heavy load) is input to BD terminal. During this voltage is input, MOSFET T_{OFF} period continues. After that, the BD terminal voltage falls.

When the falling is detected at $V_{BD(TH2)}$ = 0.15V (TYP) (Quasi-resonant Operation Threshold Voltage 2), MOSFET is turned-on. After the detection of the falling, the BD terminal threshold voltage is set to $V_{BD(TH1)}$ = 0.31V (TYP) (Quasi-resonant Operation Threshold Voltage 1), to prevent malfunctions.

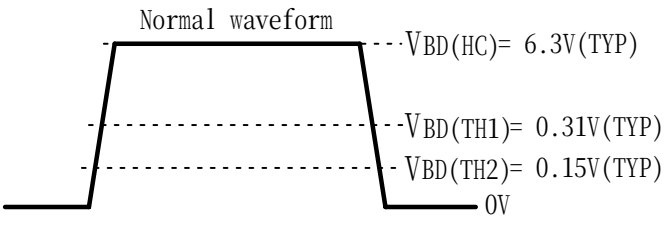


Fig.7-18 BD terminal voltage in QR operation

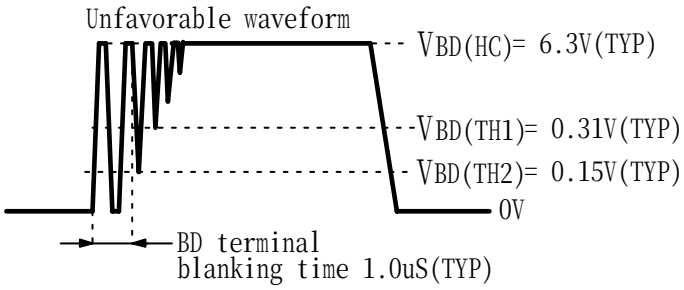


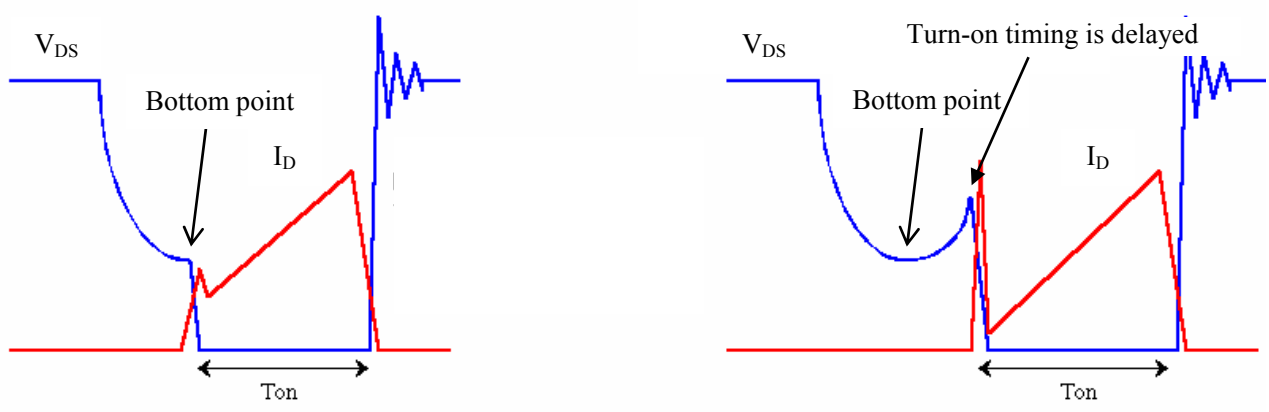
Fig.7-19 BD terminal voltage using a poor coupling transformer

Fig.7-19 shows the BD terminal waveform using a transformer with poor coupling. For example, if the turn ratio (P/S) of primary and secondary winding is large (such as in the low-voltage and high current output specifications), a surge voltage may be generated on BD terminal voltage through auxiliary winding at MOSFET turning-off.

As BD terminal blanking time (1.0 μ S(TYP)) is implemented, the QR signal is not detected during this time. If the surge is applied beyond the blanking time, the MOSFET may be switched with high frequency by the detection of ringing voltage as the QR signal. In this case, the MOSFET loss shall be excessive. If the channel temperature exceeds the maximum rating, the MOSFET destruction is caused. When the high frequency operation occurs, it is necessary to examine the pattern layout (between BD terminal and GND terminal), the transformer design (structure of primary – secondary windings and position of auxiliary winding), the snubber circuit adjustment, the probe position of oscilloscope and others.

Due to the inherent delay at BD terminal, if R3(R_{BD}) value is too large, the turn-on timing shall be delayed as shown in fig.7-20.

As R3(R_{BD}) value is relating to the input compensation of overcurrent protection (OCP) and the input compensation of standby, R3(R_{BD}) value shall be adjusted on actual operations referring the following 7.4.2.



The ideal “bottom-on”: the turn-on timing is at the bottom point of V_{DS} waveform.

The turn-on timing is delayed from the bottom point of V_{DS} waveform due to a large R_{BD}.

Fig.7-20 Waveform Examples at Bottom Point with / without Delay

7. 4. 2 OCP Input Compensation / Standby Input Compensation by R3(R_{BD})

The switching between $V_{OCP(H)}$ / $V_{OCP(L)}$ (Over Current Detection Threshold Voltage), between $T_{ONH(MIN)}$ / $T_{ONL(MIN)}$ (Minimum T_{ON} period) (threshold for standby operation) is achieved by detecting the current which is determined by forward voltage of auxiliary winding and R3(R_{BD}).

The switching is done using the same detection threshold value of $I_{BD(TH1)}$ = －500μA (TYP) (Input Compensation Detection Threshold Current 1).

7.4.2-1 OCP Input Compensation

When the QR mode converter is used in a universal input voltage range, the peak drain current varies because the operating frequency and the input voltage vary (The drain peak current decreases in the higher input voltage range.)

As the value of OCP detection resistor, R1 (R_{OCP}), is fixed, the above influence causes that the OCP operation point shifts to the more overload side in the higher input voltage range. Comparing with the OCP operation point, which is adjusted under the condition of the minimum input voltage of AC100V range and the maximum load, the operation point in AC230V range shall shift around double. To suppress this phenomenon, the OCP threshold voltage is possible to be switched, by sinking the current more than 500μA (TYP) from BD terminal through R3 (R_{BD}) during the T_{ON} period, using the forward (minus) voltage of auxiliary winding shown in fig.7-17.

The OCP threshold voltage is switched as shown below:

① $V_{OCP(H)}$: −0.930V (TYP) when the current through R_{BD} is below 500μA (TYP) during T_{ON} period

② $V_{OCP(L)}$: −0.780V (TYP) when the current through R_{BD} is above 500μA (TYP) during T_{ON} period

＊On usual R3(R_{BD}) design, the OCP operation point shall be $V_{OCP(H)}$ in AC100V input range, and $V_{OCP(L)}$ in AC230V input range.

[Reference Example]

In case of: AC85V - AC264V universal input, 15V / 20W output QR mode converter

・Transformer winding: N_p: 110T (L_p = 3.34mH), N_S (15V): 9T

・Auxiliary winding D: 10T (equivalent to 18V)

・For input compensation around AC160V, the forward voltage is;

$160\sqrt{2}\times(10\,\mathrm{T}/110\,\mathrm{T})=20.57\,\mathrm{V}$

・To flow 500μA at 20.57V,

R3(R_{BD})= 20.57V / 500μA= 41.14kΩ → 39kΩ shall be selected in the E12 / E24 series (Although the impedance between BD terminal and GND terminal gives influence actually, the approximate value shall be calculated.)

・The maximum absolute rating of BD terminal is ±2mA. When R3(R_{BD}) is 39kΩ, the current at the minus side on the auxiliary winding voltage in fig.7-17 is −870μA at maximum input voltage, and the current at the plus side is 300μA because of 18V output (auxiliary winding voltage) and 6.3V (BD terminal clamp voltage). Both of them are confirmed to be within the above range.

7.4.2-2 Standby Input Compensation

As described in 7.2.3, the minimum T_{ON} period works for the trigger to enter to standby mode.

For universal input operation, the T_{ON} period at entering to standby shall be largely different depending on the input conditions. Even if the auto standby is achieved in AC230V input range, the auto standby shall not achieved due to the wider T_{ON} period in AC100V input range, under the same load conditions.

In order to prevent this phenomenon, the minimum T_{ON} period compensation for entering to standby is implemented.

For universal input design, it is recommended the compensation shall be effective around AC140 – AC160V.

Under the load condition to change the mode like standby ⇔ 2 bottom-skip, the T_{ON} period shall be detected to be the following width, in addition to the conditions described in 7.2.3.

① $T_{ONL(MIN)}$: 1.62μs when the current through R_{BD} is below 500μA (TYP) during T_{ON} period
--- AC100V input range

② $T_{ONH(MIN)}$: 0.98μs when the current through R_{BD} is above 500μA (TYP) during T_{ON} period
--- AC230V input range

7. 5 OCP (No. 9) Terminal and Bottom-skip Operation

7.5.1 Connection of OCP Terminal

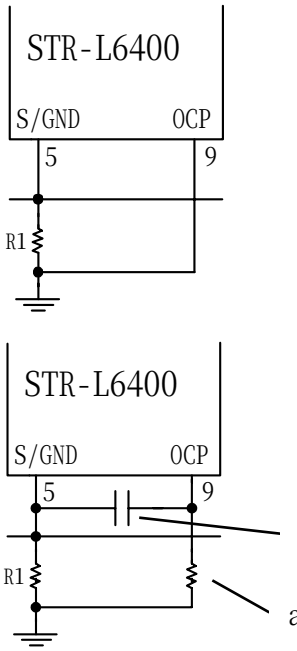
The Overcurrent Protection (OCP) circuit detects each drain peak current level (on a pulse-by-pulse basis) of MOSFET with a OCP detection resistor, R1 (R_{OCP}), and limits the output power of the power supply.

The external circuit is shown in fig.7-21.

At the OCP detection, the leading edge blanking (LEB) function works. During $T_{ON(LEB)}$ = 354ns (TYP) (Leading Edge Blanking Time), the OCP detection is disabled preventing the unstable oscillations.

When coupling capacitance of transformer, drain voltage at MOSFET turning-on, resonance capacitor are higher or the bottom detection is improper, the surge current at MOSFET turning-on may occur like the right side in fig.7-22. If the surge voltage of turn-on portion, which is beyond $T_{ON(LEB)}$ = 354ns (TYP), reaches the OCP terminal voltage (the control value) determined by FB terminal voltage, the oscillation may be unstable.

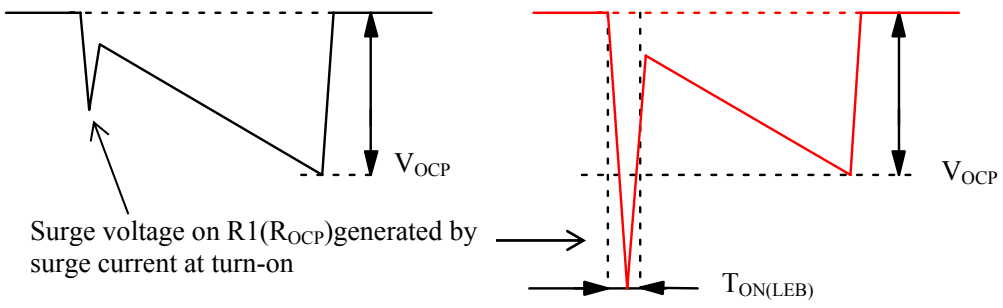
When this phenomena occurs, an external filter with a resistor and a capacitor shown on the lower side in fig.7-21 is recommended. In case of a larger filter resistor, the overcurrent may vary largely, due to the influence of $I_{OCP(O)}$ = −130μA (TYP) (OCP Terminal Source Current) and longer response time. Considering the above, the recommended values are approximately 100Ω and 220pF, respectively.



Generally, a filter circuit is unnecessary, because of the implemented LEB.

A filter circuit is recommended in case LEB does not work properly due to a higher surge current at turn-on.

Fig.7-21 Typical examples for OCP terminal peripheral circuit



In case of small influence of surge voltage at turn-on

In case of large influence of surge voltage at turn-on

Fig.7-22 Waveforms of OCP Terminal Voltage

7.5.2 Bottom-skip Operation

The bottom-skip operation with multi-mode control is available.

The function is to switch between QR operation (under heavy load) and bottom-skip operation (under middle or light load) according to the secondary load condition by detecting the drain current (actually OCP terminal voltage).

Fig.7-23 and 7-24 show the transition diagrams from no load to heavy load, from heavy load to no load, respectively. The multi-mode control changes the modes like standby mode ⇔ 2-bottom-skip mode ⇔ 1-Bottom-skip mode ⇔ QR mode.

In actual operations, there are delay time settings for rapid load changes described in 7.2.2 and 7.2.3. However, fig.7-23 and 7-24 are shown just the conceptual diagrams, and such delays are omitted.

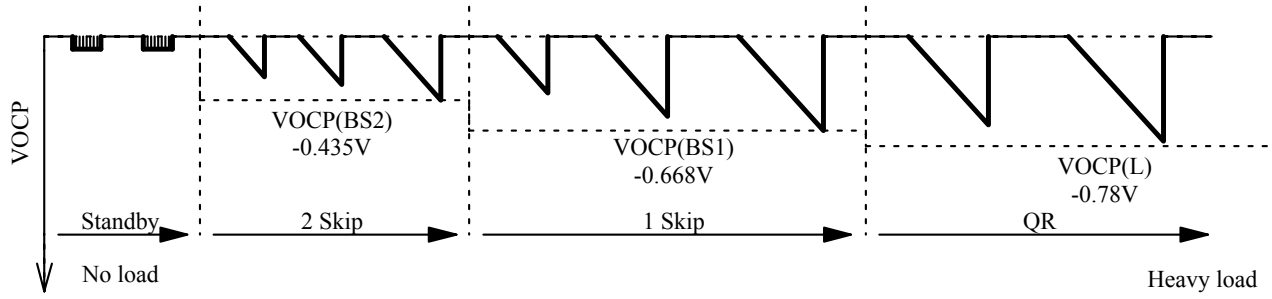


Fig.7-23 Transition diagram from no load to heavy load

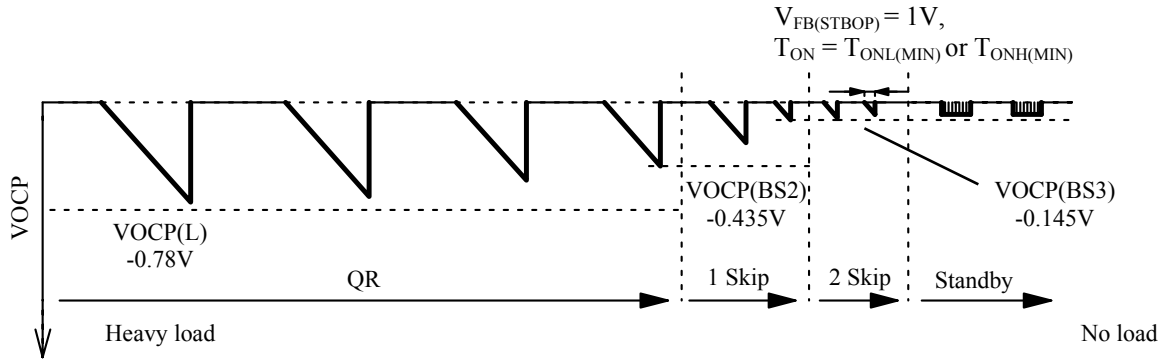


Fig.7-24 Transition diagram from heavy load to no load

As the hysteresis is implemented for each mode switching of the increasing / decreasing load transitions, the oscillation is stable near the switching thresholds and the mode switching is achieved stably.

Fig.7-25 shows the switching hysteresis for each mode switching.

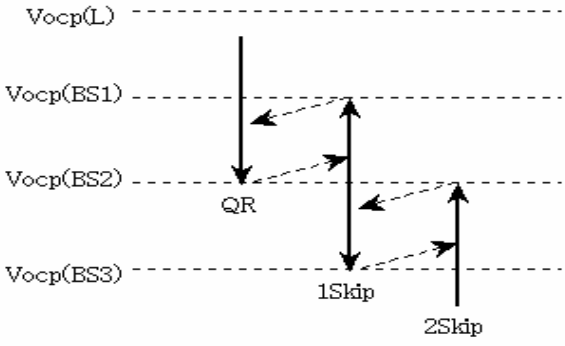


Fig.7-25 Hysteresis for each mode switching

7.6 Standby Operation

FB Terminal Voltage during Standby

As described in 7.2.3, the conditions for entering to standby mode are:

- When the ADJ terminal voltage reaches $V_{ADJ(STB)}$ = 6.2V (TYP) (Standby State Start Voltage), the device becomes ready to enter into the burst operation.
- When the FB terminal voltage falls below $V_{FB(STBOP)}$ = 1.0V (TYP) (Standby Operation Threshold Voltage), the burst operation mode starts.

  Under light load condition, when the T_{ON} period reaches $T_{ONL(MIN)}$/ $T_{ONH(MIN)}$ = 1.62μS / 0.98μS (TYP) (Minimum T_{ON} period (Normal Operation) / (Minimum T_{ON} period (Input Compensation Operation), the feedback current is increasing higher. Therefore, the minimum T_{ON} period works for the trigger to enter to standby mode.

As described in 7.4.2-2, when the input compensation is effective, the minimum T_{ON} period shall be automatically switched; $T_{ONL(MIN)}$ = 1.64μS (TYP) in AC100V input range or 0.98μS (TYP) in AC230V input range.

Fig.7-26 shows the standby operation. During the standby operation, the burst operation mode repeats between oscillation-stop mode and 2-bottom-skip mode.

In the burst operation mode, the energy supply from auxiliary winding synchronizes with the energy supply to the output. As a result, the ripple may be generated on V_{CC} terminal voltage due to burst operation. If the V_{CC} terminal voltage falls below $V_{CC(OFF)}$ = 11.3V (MAX) (Operation Stop Voltage), some adjustments, such as increasing the C2 value between V_{CC} terminal and S /GND terminal, are necessary to stabilize the V_{CC} terminal voltage.

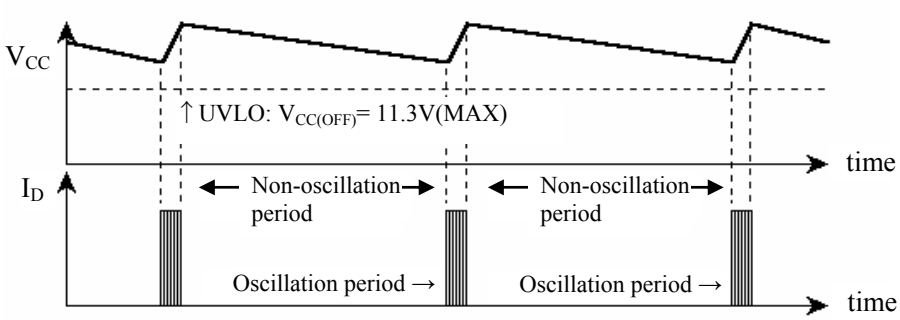


Fig.7-26 Waveform in Standby Operation

7.7 Maximum ON Time Limitation Function

During low input voltage or the transition operation such as power supply ON/OFF, the maximum T_{ON} period is limited to be $T_{ON(MAX)}$ = 36μsec (TYP) (Maximum T_{ON} period) (refer to fig.7-27).

On the power supply design, the confirmation about MOSFET T_{ON} period is necessary, under the condition with minimum input voltage and maximum load condition.

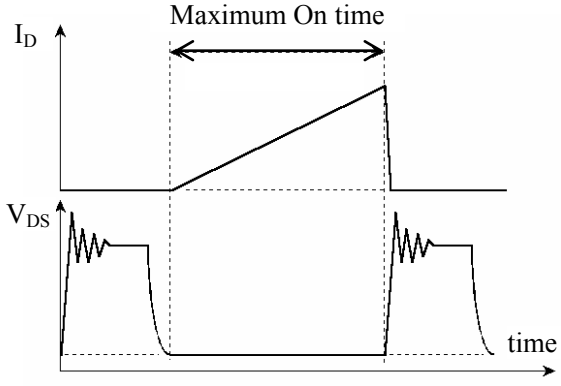


Fig.7-27 Maximum T_{ON} period confirmation

7.8 Phase Compensation

Fig.7-28 shows the circuit diagram for the secondary error amplifier, using a general shunt regulator. As for the phase compensation capacitor, C8, the capacitance shall be adjusted in the range of 0.047 – 0.47μF, and finally determined on actual operations.

In case the load specification is not general, the phase compensation on secondary error amplifier is not enough due to the larger ripples on rectifier capacitor, or the operation is not stable due to the noises to FB terminal, it is recommended to place a capacitor, C6, between FB terminal and GND terminal shown in fig.7-29. As for C6, the capacitance shall be adjusted in the range of 470pF to 0.022μF and finally determined on actual operations.

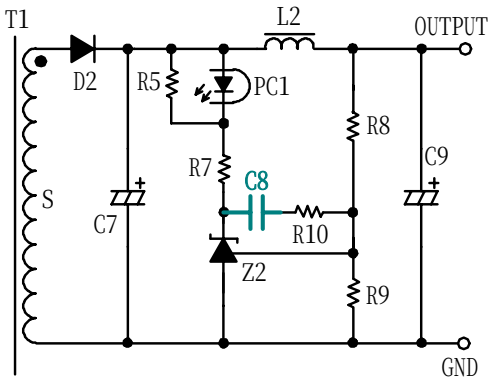
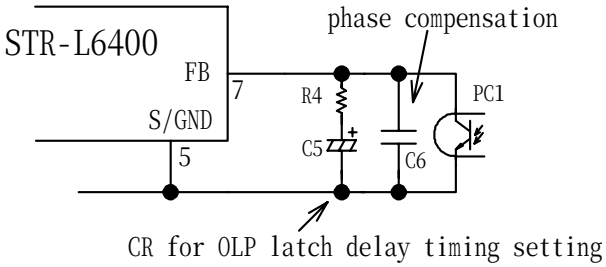


Fig.7-28 Peripheral circuit around secondary shunt regulator



Normal setting (OLP: Latch shutdown)

Fig.7-29 FB terminal peripheral circuit

8. Design Notes

8. 1 External Components

Please take care to use properly rated, including derating as necessary, and proper type of components.

- Input and output electrolytic capacitors. Apply proper derating against ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.
- Transformer. Apply proper derating against core temperature rise from core loss and copper loss.
- Current sensing resistor R1 (R_{OCP}). A high frequency switching current flows to R1 ($_{ROCP}$), and may cause poor operation if a high inductance resistor is used. Choose a low inductance and surge-proof type.

8. 2 Component Layout and Trace Design

PCB circuit trace design and component layout affect proper functioning during operation, EMI noise, and power dissipation. Therefore, where high frequency current traces form a loop, as in fig.8-1, wide, short patterns and small circuit loops are important. In addition, local GND and earth ground traces affect radiated EMI noise, thus the same measures should be taken into account. Switching mode power supplies consist of current traces of high frequency and high voltage, thus trace design and component layouts should be done to comply with all safety guidelines. Furthermore, in the case where a MOSFET is being used as the switching device, take into account the positive thermal coefficient of $R_{DS(on)}$ when preparing a thermal design.

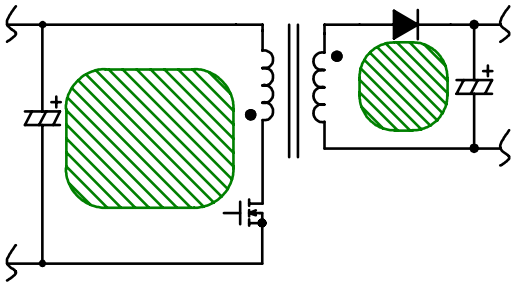


Fig.8-1 High frequency current loops (hatched areas)

(1) S/GND terminal to R1 (R_{OCP}) to C1 to T1 [winding P] to D/ST terminal Trace Layout

This is the main circuit containing the switching current, and thus it should be as wide and as short as possible. In case the distance between C1 and the device is lengthy, an isolation capacitor near the device or the transformer is recommended.

The capacitors may be either electrolytic or film type capacitors, 0.1 μF, in the range considered maximum input voltage.

(2) S/GND terminal to C2 to T1 [winding D] to R2 to D1 to C2 to V_{CC} terminal Trace Layout

This circuit also needs to be as wide and short as possible. In case the distance between C2 and the device is not short, placing a 0.1 μF / 50 V film capacitor between V_{CC} and S/OCP terminals is recommended.

(3) R1 (R_{OCP}) Trace Layout

Place R1 (R_{OCP}) as close as possible to S/GND terminal. There should be a single connection (A in fig.8-2) between the power pattern and the control circuit pattern, and a single connection (B in fig.8-2) between the power pattern and the OCP terminal pattern close to R1 (R_{OCP}), in order to reduce the common impedance of the pattern and to avoid interference from the switching current to the control circuit.

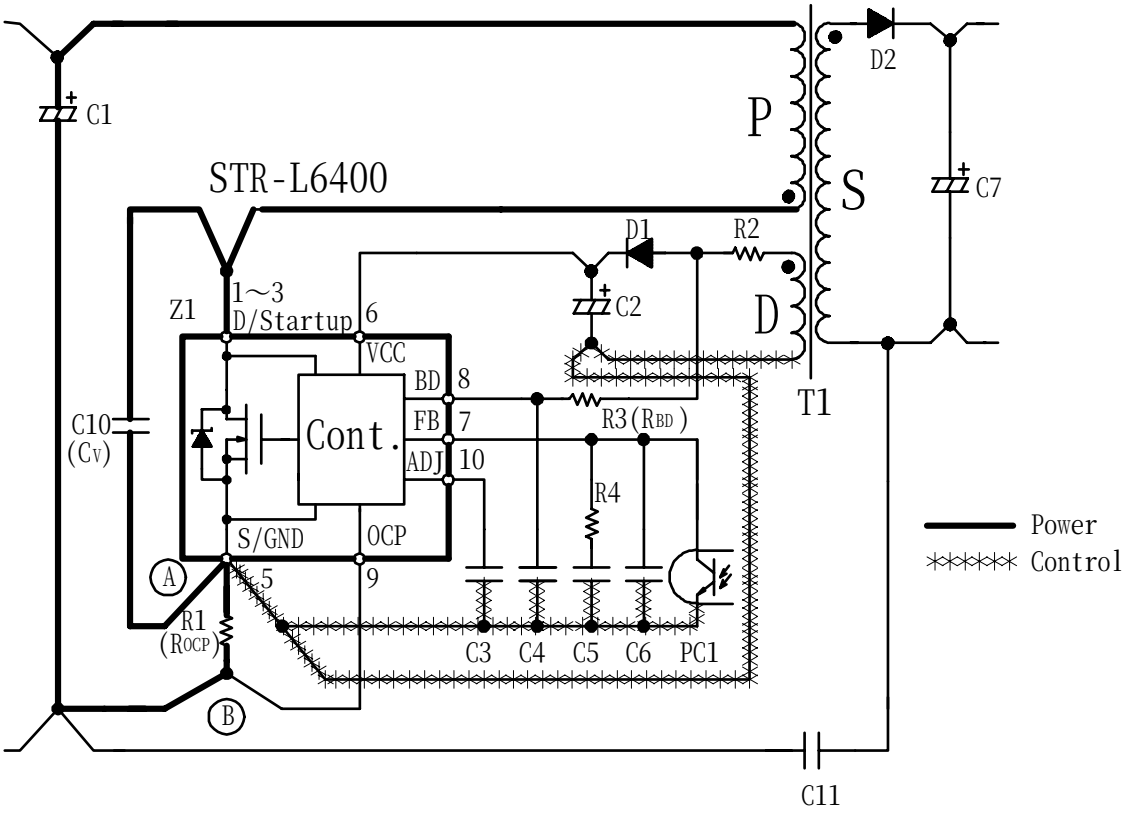


Fig.8-2 External component layout