STR-V600
Application Note Rev.1.1

SANKEN ELECTRIC CO., LTD.

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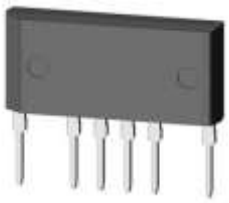
Contents

General Descriptions

The STR-V600 series is a power IC for switching power supplies, incorporating a power MOSFET and a current mode PWM controller IC in one package.
The SIP8L full mold package features low height and creeping distance of 4mm or longer between high and low voltage pin bases.
To achieve low power consumption, the product includes a startup circuit and a standby function in the controller.
The switching modes are automatically changed according to load conditions so that the PWM mode is in normal operation and the burst mode is in light load condition.
The rich set of protection features helps to realize low component counts, and high performance-to-cost power supply.

Package

SIP8L



Features

- SIP8L package (2.54 pitch, straight lead): Creeping distance of 4mm or longer between high voltage and low voltage pin bases. Low height of less than 12 mm from PCB (Printed Circuit Board)
- Current mode PWM control
- Auto Standby function: improves efficiency by burst mode operation in light load
  - Normal operation: PWM mode
  - Light load operation: Burst mode
- No load power consumption < 25 mW
- Brown-In and Brown-Out function: auto-restart, prevents excess input current and heat rise at low input voltage
- Random Switching function: reduces EMI noise, and simplifies EMI filters
- Slope Compensation function: avoids subharmonic oscillation
- Leading Edge Blanking function
- High Speed Latch Release function
- Protection features
  - Overcurrent Protection function (OCP): pulse-by-pulse, with input compensation function
  - Overvoltage Protection function (OVP): latched shutdown
  - Overload Protection function (OLP): auto-restart, with timer
  - Thermal Shutdown function (TSD): latched shutdown

Applications

- Standby power supply
- Home appliances
- Digital appliances
- Office automation (OA) equipment
- Industrial apparatus
- Communication facilities

Product Lineup

Part Number	f_{OSC} (kHz)	Power MOSFET		Output Power, P_{OUT} * (W)	
		V_{DSS} (min) (V)	$R_{DS(ON)}$ (max) (Ω)	230VAC	85 to 265VAC
STR-V653	67	650	1.9	30	23

* The listed output power is based on the thermal ratings, and the peak output power can be 120% to 140% of the value stated here. At low output voltage and short duty cycle, the output power may be less than the value stated here.

1. Absolute Maximum Ratings

- Refer to the datasheet of each product for these details.
- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, Ta is 25 °C

Characteristic	Pins	Symbol	Rating	Unit	Notes
Drain Peak Current	1 − 3	I_{DPEAK}	6.7	A	Single pulse
Avalanche Energy	1 − 3	E_{AS}	99	mJ	Single pulse V_{DD}=99V,L=20mH
		I_{LPEAK}	2.9	A	
S/OCP Pin Voltage	3 − 5	V_{OCP}	−2 to 6	V	
Control Part Input Voltage	8 − 5	V_{CC}	32	V	
FB/OLP Pin Voltage	6 − 5	V_{FB}	−0.3 to 14	V	
FB/OLP Pin Sink Current	6 − 5	I_{FB}	1.0	mA	
BR Pin Voltage	4 − 5	V_{BR}	−0.3 to 7	V	
BR Pin Sink Current	4 − 5	I_{BR}	1.0	mA	
Power Dissipation of MOSFET	1 − 3	P_{D1}	10.8	W	With infinite heat sink
			1.6	W	Without heat sink
Power Dissipation of Control Part	8 − 5	P_{D2}	1.2	W	
Operating Ambient Temperature	−	T_{op}	−30 to +125	°C	
Storage Temperature	−	T_{stg}	−40 to +125	°C	
Channel Temperature	−	T_{ch}	+150	°C	

2. Electrical Characteristics

- Refer to the datasheet of each product for these details.
- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.

2.1 Electrical Characteristics of Control Part

Unless otherwise specified, Ta is 25 °C, V_{CC} is 18 V

Characteristic	Pins	Symbol	Min.	Typ.	Max.	Unit	Notes
Operation Start Voltage	8 − 5	$V_{CC(ON)}$	13.8	15.3	16.8	V	
Operation Stop Voltage (1)	8 − 5	$V_{CC(OFF)}$	7.3	8.1	8.9	V	
Circuit Current in Operation	8 − 5	$I_{CC(ON)}$	−	−	4	mA	V_{CC}=12V
Minimum Startup Voltage	8 − 5	$V_{ST(ON)}$	−	38	−	V	
Startup Current	8 − 5	$I_{STARTUP}$	−3.7	−2.5	−1.5	mA	
Startup Current Supply Threshold Biasing Voltage (1)	8 − 5	$V_{CC(BIAS)}$	8.5	9.5	10.5	V	
Frequency Modulation Deviation	1 − 5	$f_{OSC(AVE)}$	60	67	74	kHz	
Oscillation Frequency Fluctuation Range	1 − 5	Δf	−	5	−	kHz	
Maximum Duty Cycle	1 − 5	D_{MAX}	77	83	89	%	
Minimum On-time	−	$t_{ON(MIN)}$	−	550	−	ns	
Leading Edge Blanking Time	−	t_{BW}	−	330	−	ns	
OCP Compensation Coefficient	−	DPC	−	20	−	mV/μs	
OCP Compensation Duty Cycle Limit	−	D_{DPC}	−	36	−	%	

Characteristic	Pins	Symbol	Min.	Typ.	Max.	Unit	Notes
OCP Threshold Voltage at Zero Duty Cycle	3 − 5	$V_{OCP(L)}$	0.70	0.78	0.86	V	
OCP Threshold Voltage at 36% Duty Cycle	3 − 5	$V_{OCP(H)}$	0.81	0.90	0.99	V	
Maximum Feedback Current	6 − 5	$I_{FB(MAX)}$	−340	−230	−150	µA	
Minimum Feedback Current	6 − 5	$I_{FB(MIN)}$	−30	−15	−7	µA	
FB/OLP Pin Oscillation Stop Threshold Voltage	6 − 5	$V_{FB(OFF)}$	0.85	0.95	1.05	V	
OLP Threshold Voltage	6 − 5	$V_{FB(OLP)}$	7.3	8.1	8.9	V	
OLP Delay Time	6 − 5	t_{OLP}	54	68	82	ms	
OLP Operation Current	8 − 5	$I_{CC(OLP)}$	−	300	600	µA	
FB/OLP Pin Clamp Voltage	6 − 5	$V_{FB(CLAMP)}$	11	12.8	14	V	
Brown-In Threshold Voltage	4 − 5	$V_{BR(IN)}$	5.2	5.6	6	V	
Brown-Out Threshold Voltage	4 − 5	$V_{BR(OUT)}$	4.45	4.8	5.15	V	
BR Pin Clamp Voltage	4 − 5	$V_{BR(CLAMP)}$	6	6.4	7	V	
BR Function Disable Threshold Voltage	4 − 5	$V_{BR(DIS)}$	0.3	0.48	0.7	V	
V_{CC} Pin OVP Threshold Voltage	8 − 5	$V_{CC(OVP)}$	26	29	32	V	
Latch Circuit Holding Current (2)	8 − 5	$I_{CC(LATCH)}$	−	700	−	µA	
Thermal Shutdown Temperature	−	$T_{j(TSD)}$	135	−	−	°C	

(1) $V_{CC(BIAS)} > V_{CC(OFF)}$ always.
(2) A latch circuit is a circuit operated with Overvoltage Protection (OVP) and/or Thermal Shutdown Protection (TSD) in operation.

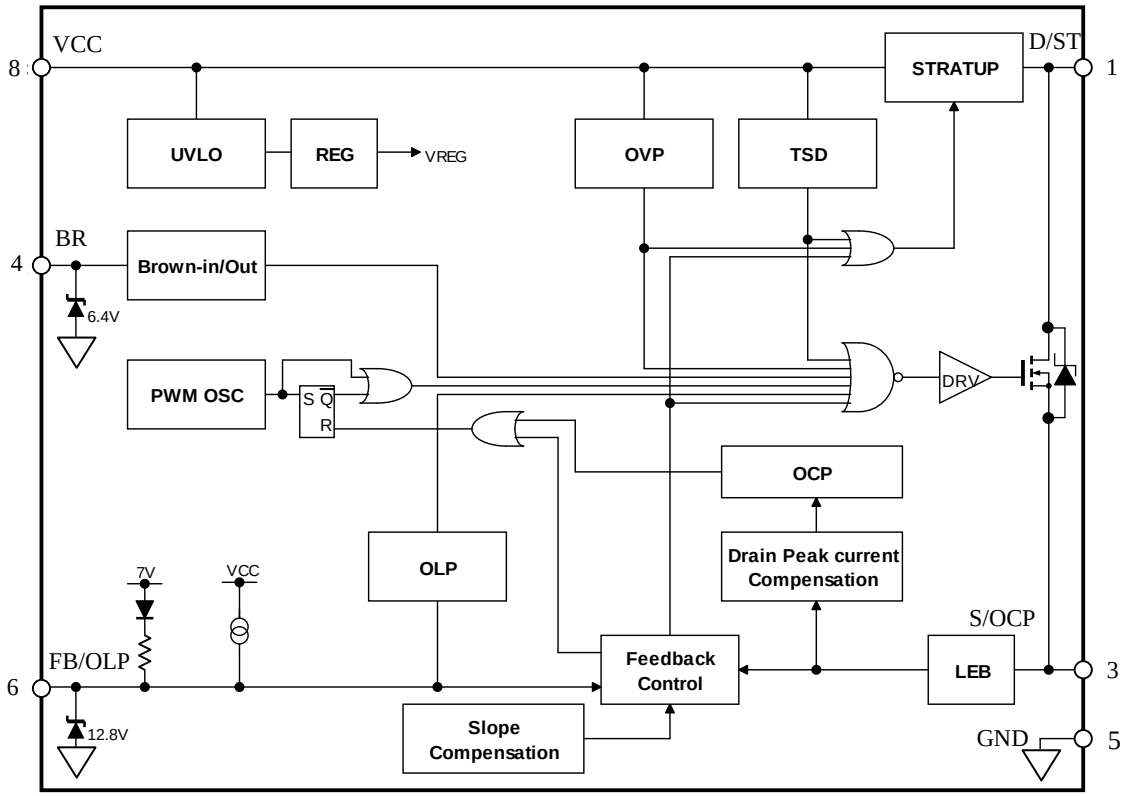
2.2 Electrical Characteristics of MOSFET

Unless otherwise specified, Ta is 25 °C

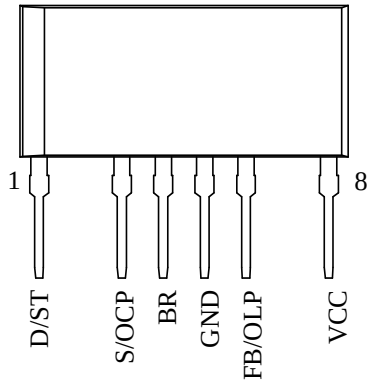
Characteristic	Pins	Symbol	Min.	Typ.	Max.	Unit	Notes
Drain-to-Source Breakdown Voltage	1 – 3	V_{DSS}	650	−	−	V	
Drain Leakage Current	1 – 3	I_{DSS}	−	−	300	µA	
On-Resistance	1 – 3	$R_{DS(ON)}$	−	−	1.9	Ω	
Switching Time	1 – 3	t_f	−	−	250	ns	
Thermal Resistance *	−	θ_{ch-F}	−	−	3.0	°C/W	

* The thermal resistance between the channels of the MOSFET and the internal frame

3. Functional Block Diagram



4. Pin List Table



Number	Name	Function
1	D/ST	MOSFET drain pin and input of the startup current
2	–	(Pin removed)
3	S/OCP	MOSFET source and input of Overcurrent Protection (OCP) signal
4	BR	Input of Brown-In and Brown-Out detection voltage
5	GND	Ground
6	FB/OLP	Feedback signal input for constant voltage control signal and input of Overload Protection (OLP) signal
7	–	(Pin removed)
8	VCC	Power supply voltage input for Control Part and input of Overvoltage Protection (OVP) signal

5. Typical Application Circuit

The following drawings show circuits enabled and disabled the Brown-In/Brown-Out function.
The following design features should be observed:

- The PCB traces from the D/ST pin (pin 1) should be as wide as possible, in order to enhance thermal dissipation.

In applications having a power supply specified such that V_{DS} has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary-side winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

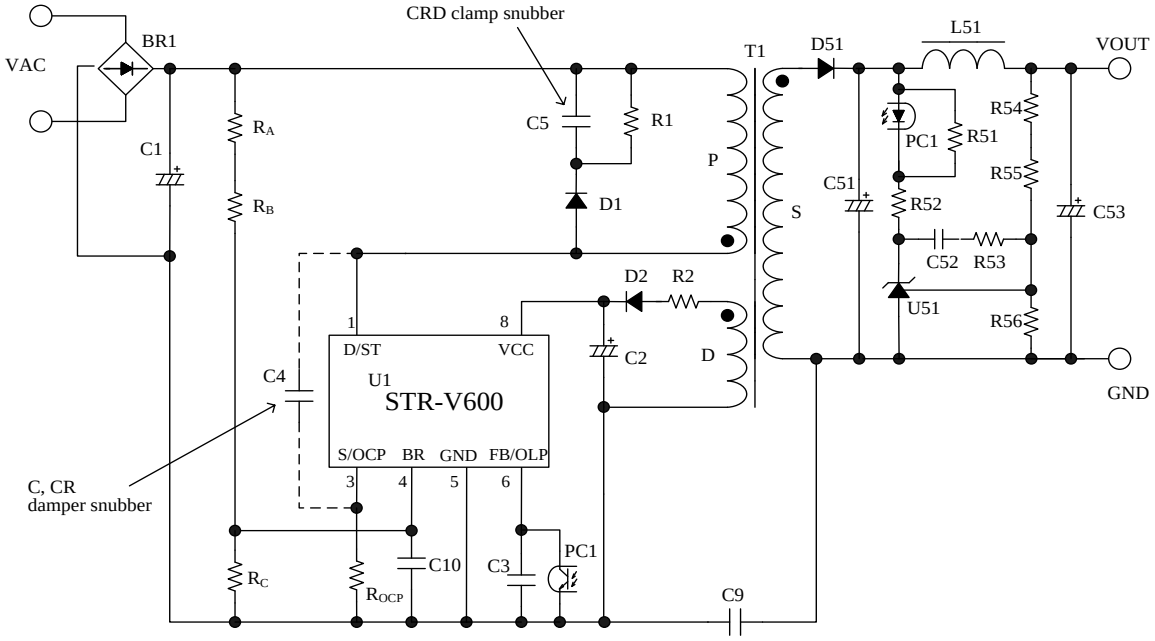


Figure 5-1 Typical application circuit instance, enabled Brown-In/Brown-Out function (DC line detection)

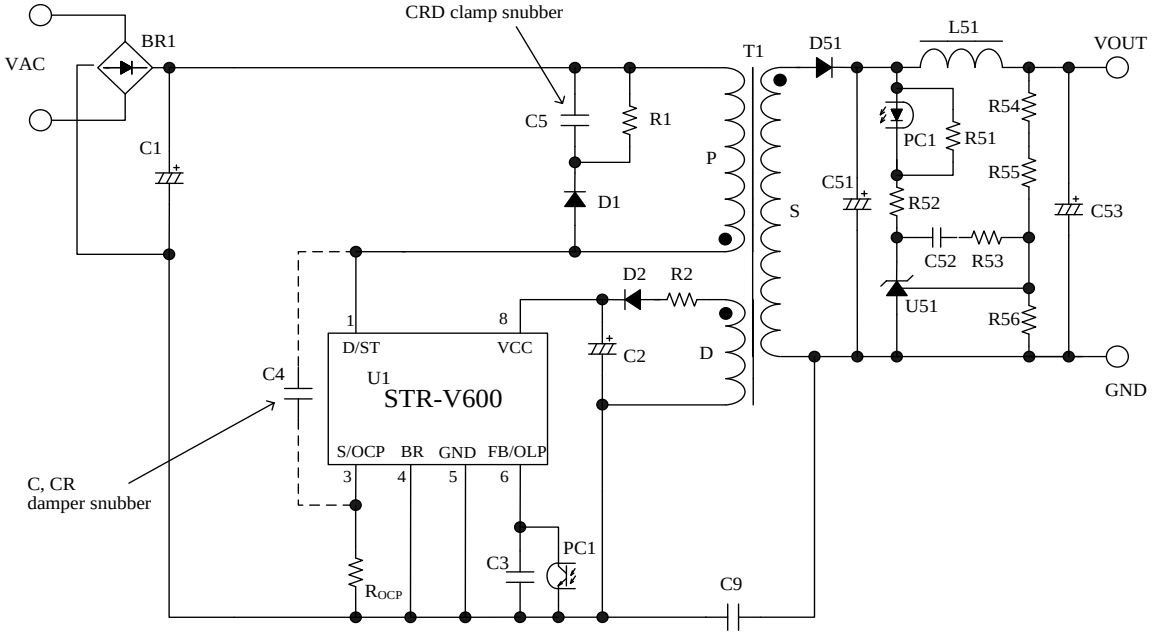
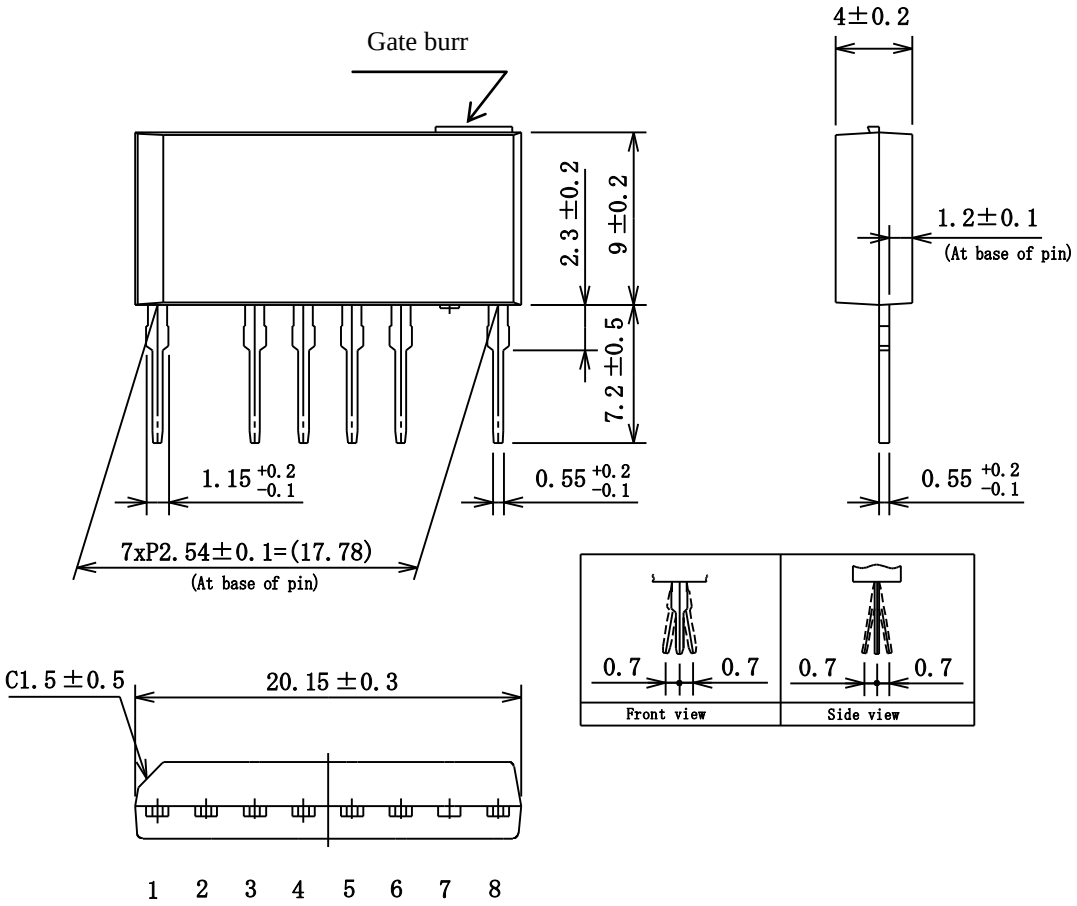


Figure 5-2 Typical application circuit example, disabled Brown-In/Brown-Out function

6. Package Diagram

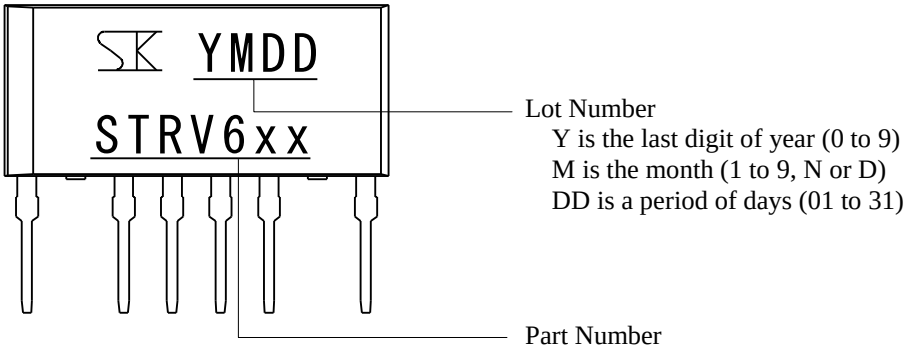
- SIP8L package (2.54 pitch, straight lead)
- The pin 2 removed to provide greater creepage and clearance isolation between the high voltage pins (pins 1: D/ST) and the low voltage pin (pin 3: S/OCP).
- Creeping distance of 4mm or longer between high voltage and low voltage pin bases.
- Low height of less than 12 mm from PCB (Printed Circuit Board)



NOTES:

- Unit: mm
- Gate burr indicates protrusion of 0.3 mm (max).
- Pin treatment Pb-free. Device composition compliant with the RoHS directive.

7. Marking Diagram



8. Functional Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

8.1 Startup Operation

Figure 8-1 shows the VCC pin peripheral circuit, disabled the Brown-In/Brown-Out function by connecting the BR pin trace to the GND pin trace.

In Figure 8-1, the Startup Current, $I_{STARTUP}$, which is a constant current of –2.5 mA, is provided from the IC to capacitor C2 connected to the VCC pin, and it charges C2. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, the IC starts operation. After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

During the IC operation, the rectified voltage from the auxiliary winding voltage, V_D, of Figure 8-1 becomes a power source to the VCC pin.

The winding turns of the winding D should be adjusted so that the VCC pin voltage is applied to equation (1) within the specification of the input voltage range and output load range of the power supply. The target voltage of the winding D is about 18 V.

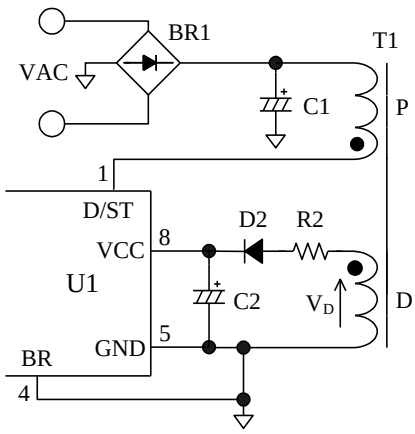


Figure 8-1 VCC pin peripheral circuit

$$V_{CC(BIAS)}(\max) < V_{CC} < V_{CC(OVP)}(\min)$$
$$\Rightarrow 10.5(\mathrm{V}) < V_{CC} < 26.0(\mathrm{V}) \qquad (1)$$

The startup time, t_{START}, is determined by the value of C2, and it is approximately given as below:

$$t_{START} \approx C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left| I_{STARTUP} \right|} \qquad (2)$$

where:

t_{START} is the startup time in s, and

$V_{CC(INT)}$ is the initial voltage of the VCC pin in V.

8.2 Undervoltage Lockout (UVLO) Circuit

Figure 8-2 shows the relationship of V_{CC} and I_{CC}. After the IC starts operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the IC stops switching operation by the UVLO (Undervoltage Lockout) circuit and reverts to the state before startup again.

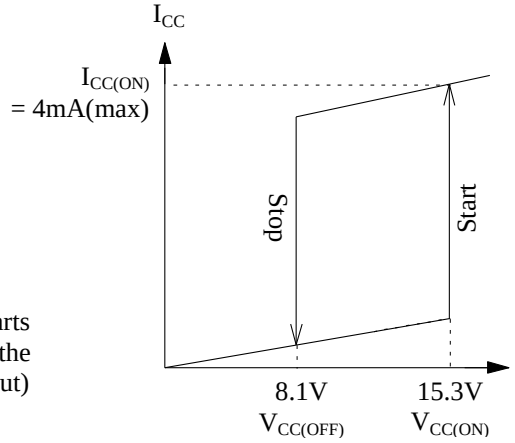


Figure 8-2 V_{CC} versus I_{CC}

8.3 Bias Assist Function

Figure 8-3 shows the VCC pin voltage behavior during the startup period. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, the IC starts operation. Thus, the circuit current, I_{CC}, increases, and the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, V_D, increases in proportion to the output voltage rise. Thus, the VCC pin voltage is set by the balance between dropping due to the increase of I_{CC} and rising due to the increase of the auxiliary winding voltage, V_D.

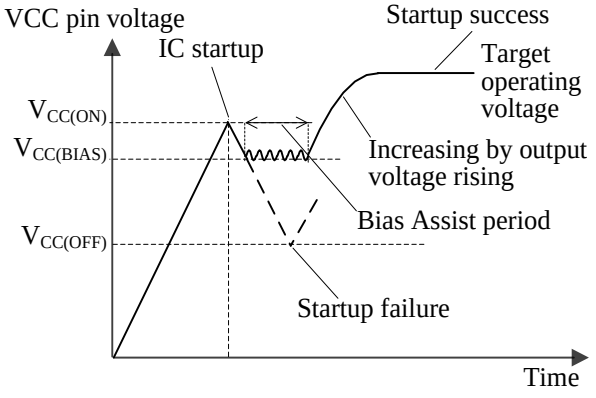


Figure 8-3 VCC pin voltage during startup period

Just at the turning-off of the power MOSFET, a surge voltage occurs at the output winding. If the feedback control is activated by the surge voltage on light load condition at startup, the output power is restricted and the output voltage decreases. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the IC stops switching operation and a startup failure occurs.

In order to prevent this, the Bias Assist function is activated when the VCC pin voltage decreases to the Startup Current Threshold Biasing Voltage, $V_{CC(BIAS)}$ = 9.5 V, during a state of operating feedback control.

While the Bias Assist function is activated, any decrease of the VCC pin voltage is counteracted by providing the Startup Current, $I_{STARTUP}$, from the startup circuit. Thus, the VCC pin voltage is kept almost constant.

By the Bias Assist function, the value of C2 is allowed to be small and the startup time becomes shorter. Furthermore,

because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function becomes shorter.

It is necessary to check and adjust the startup process based on actual operation in the application, so that the startup failure does not occur.

8.4 Constant Voltage Control Operation

The constant output voltage control function uses current mode control (peak current mode), which enhances response speed and provides stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (refer to Section 3 Functional Block Diagram), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure 8-4 and Figure 8-5.

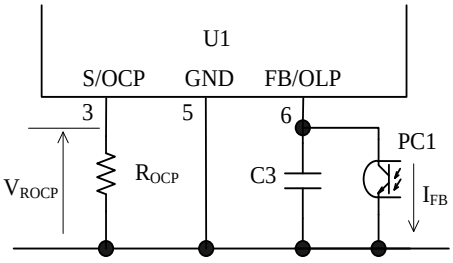


Figure 8-4 FB/OLP pin peripheral circuit

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photocoupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

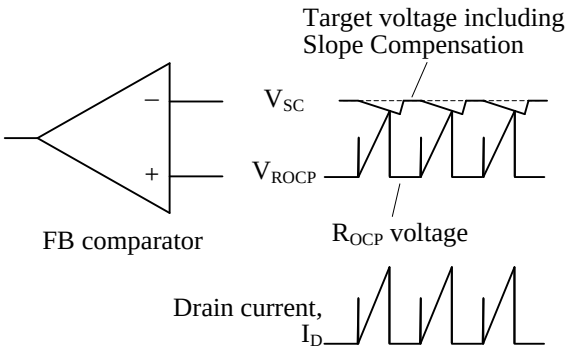


Figure 8-5 Drain current, I_D, and FB comparator operation in steady operation

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.
This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 8-6. This is called the subharmonics phenomenon.
In order to avoid this, the IC incorporates the Slope Compensation function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the on-duty gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.
Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

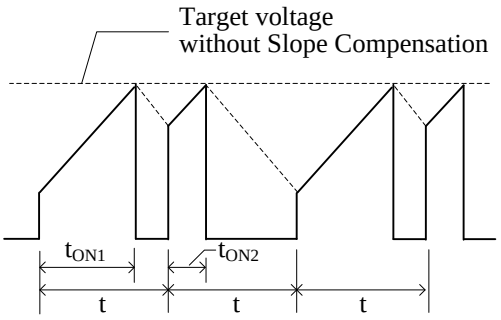


Figure 8-6 Drain current, I_D, waveform in sub-harmonic oscillation

In the current mode control method, the FB comparator and/or the OCP comparator may respond to the surge voltage resulting from the drain surge current in turning-on the power MOSFET. As a result, the power MOSFET may turn off irregularly. In order to prevent this response to the surge voltage in turning-on the power MOSFET, Leading Edge Blanking, t_{BW} = 330 ns, is built-in.

8.5 Auto Standby Mode Function

Auto standby mode is activated automatically when the drain current, I_D, reduces under light load conditions, at which I_D is less than 15% to 20% of the maximum drain current (it is in the Overcurrent Protection state).

The operation mode becomes burst oscillation, as shown in Figure 8-7. Burst mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals.

Generally, in order to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst mode, audible noises can be reduced.

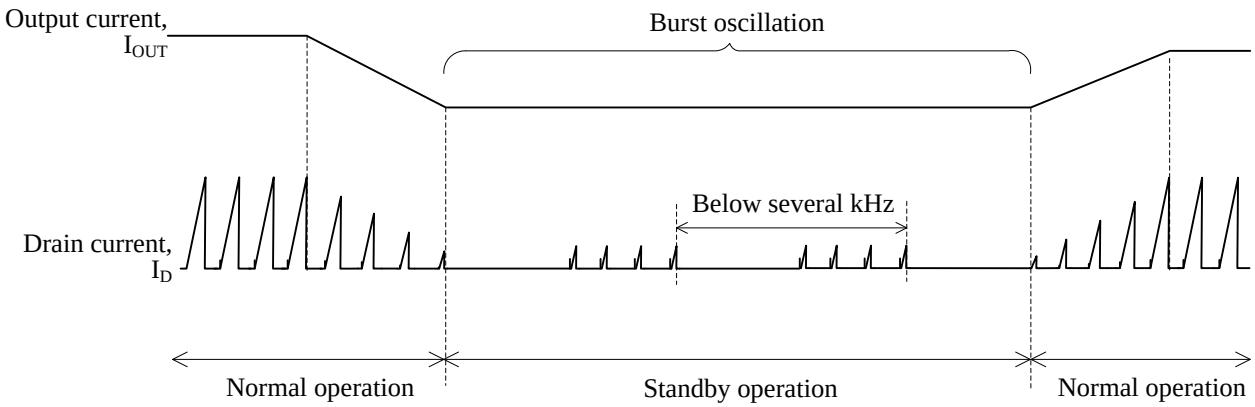


Figure 8-7 Auto Standby mode timing

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.5 V during the transition to the burst mode, the Bias Assist function is activated and stabilizes the standby mode operation, because $I_{STARTUP}$ is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary-side winding and/or reducing the value of R2 in Figure 9-2 (refer to Section 9.1 Peripheral Components for a detail of R2).

8.6 Random Switching Function

The IC modulates its switching frequency randomly within $\Delta f = \pm 5$ kHz superposed on the average operation frequency, $f_{OSC(AVG)}$ = 67 kHz. The conduction noise with this function is smaller than that without this function, and this function can simplify noise filtering of the input lines of power supply.

8.7 Brown-In and Brown-Out Function

This function stops switching operation when it detects low input line voltage, and thus prevents excessive input current and overheating. During Auto Standby mode, this function is disabled.

8.7.1 Disabled Brown-In and Brown-Out Function

When the Brown-In and Brown-Out function is unnecessary, connect the BR pin trace to the GND pin trace so that the BR pin voltage is $V_{BR(DIS)}$ = 0.48 V or less, as shown in Figure 8-8.

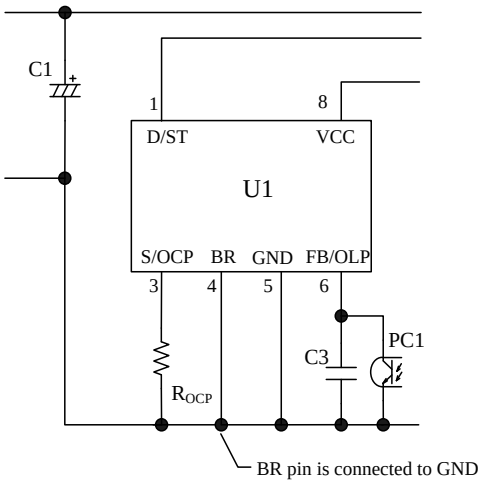


Figure 8-8 The circuit used to disable Brown-In and Brown-Out function

8.7.2 Brown-In and Brown-Out Function by DC Line Detection

The BR pin detects a voltage proportional to the DC input voltage (C1 voltage), with the resistive voltage divider R_A, R_B, and R_C connected between the DC input and GND, plus C10 connected to the BR pin, as shown in Figure 8-9.

This method detects peaks of the ripple voltage of the rectified AC input voltage, and thus it minimizes the influence of load conditions on the detecting voltage.

During the input voltage rising from the stopped state of power supply, when the BR pin voltage increases to $V_{BR(DIS)}$ = 0.48 V or more, this function is enabled. After that, when the BR pin voltage increases to $V_{BR(IN)}$ = 5.6 V or more and the VCC pin voltage increases to $V_{CC(ON)}$ or more, the IC starts switching operation.

During the input voltage falling from the operated state of power supply, when the BR pin voltage decreases to $V_{BR(OUT)}$ = 4.8 V or less for about 68 ms, the IC stops switching operation.

- Component values of the BR pin peripheral circuit:
  - R_A, R_B: A few megohms. Because of high DC voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
  - R_C : A few hundred kilohms
  - C10: 100 p to 1000 pF for high frequency noise rejection

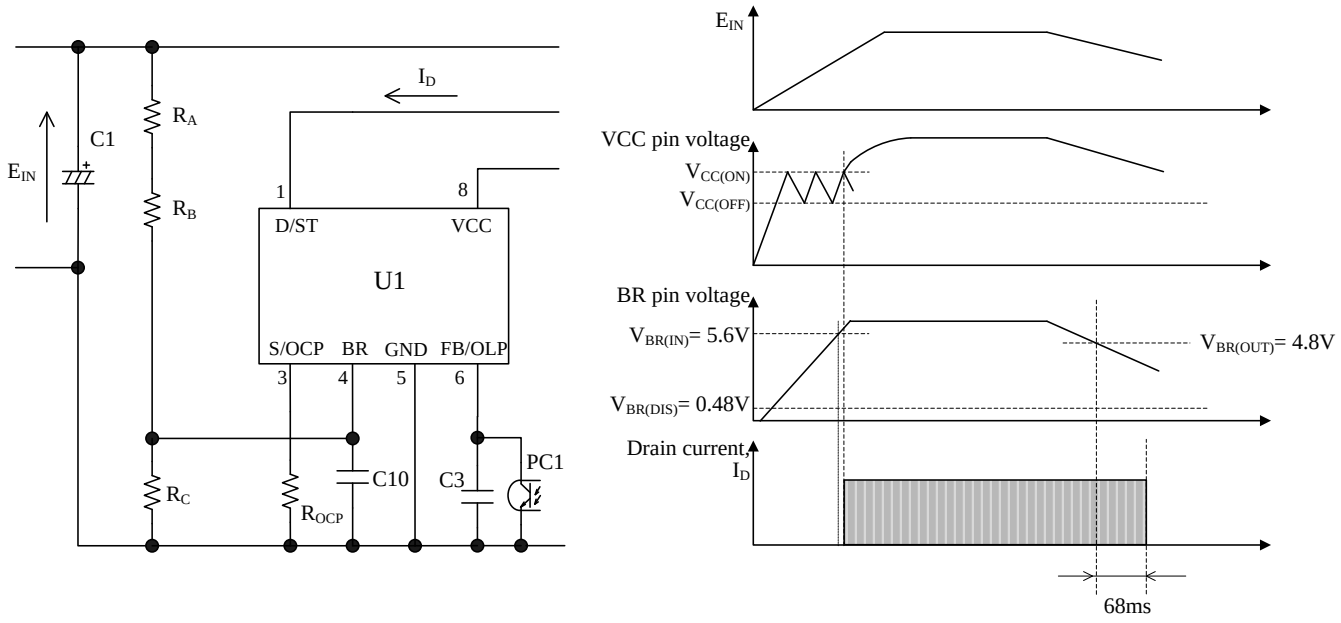


Figure 8-9 Brown-In and Brown-Out function controlled by DC line detection

8.7.3 Brown-In and Brown-Out Function by AC Line Detection

The BR pin detects a voltage proportional to the AC input voltage, with the resistive voltage divider R_A, R_B, and R_C connected between one side of the AC line and GND, plus C10 connected to the BR pin and R9 connected between the BR pin and the VCC pin, as shonw in Figure 8-10. This method detects the AC input voltage, and thus it minimizes the influence from C1 charging and discharging time, or load conditions, on the detecting voltage.
This method is set together with the High-Speed Latch Release function.

During the input voltage rising from the stopped state of power supply, when the BR pin voltage increases to $V_{BR(DIS)}$ = 0.48 V or more, this function is enabled. After that, when the BR pin voltage increases to $V_{BR(IN)}$ = 5.6 V or more and the VCC pin voltage increases to $V_{CC(ON)}$ or more, the IC starts switching operation.
During the input voltage falling from the operated state of power supply, when the BR pin voltage decreases to $V_{BR(OUT)}$ = 4.8 V or less for about 68 ms, the IC stops switching operation.

- Component values of the BR pin peripheral circuit:
  - R_A, R_B : A few megohms. Because of high DC voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
  - R_C : A few hundred kilohms
  - C10: 0.047 μ to 0.47 μF for AC ripple rejection. This should be adjusted according to values of R_A, R_B, and R_C.
  - R9: In order to enable the Brown-In and Brown-Out function, this value must be adjusted so that the BR pin voltage is more than $V_{BR(DIS)}$ = 0.48 V when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V.

- High-Speed Latch Release
  The Brown-In and Brown-Out function by AC line detection shown in Figure 8-10 can quickly release the latch mode when the AC input, VAC, is turned off.
  When the Overvoltage Protection function (OVP) or Thermal Shutdown function (TSD) are activated, the IC stops switching operation in latch mode.
  Releasing the latch mode is done by decreasing the VCC pin voltage below $V_{CC(OFF)}$ = 8.1 V after unplugging the AC input, or by decreasing the BR pin voltage below $V_{BR(OUT)}$ = 4.8 V.
  The method of unplugging the AC input will spend much time until the VCC pin voltage decreases below $V_{CC(OFF)}$ = 8.1 V, because the release time is determined by the discharge time of C1.
  In contrast, the configuration of the BR pin peripheral circuit of Figure 8-10 makes the releasing process faster. Because the BR pin voltage immediately decreases to $V_{BR(OUT)}$ = 4.8 V or less when the AC input, VAC, is turned off, and thus the latch mode is quickly released.

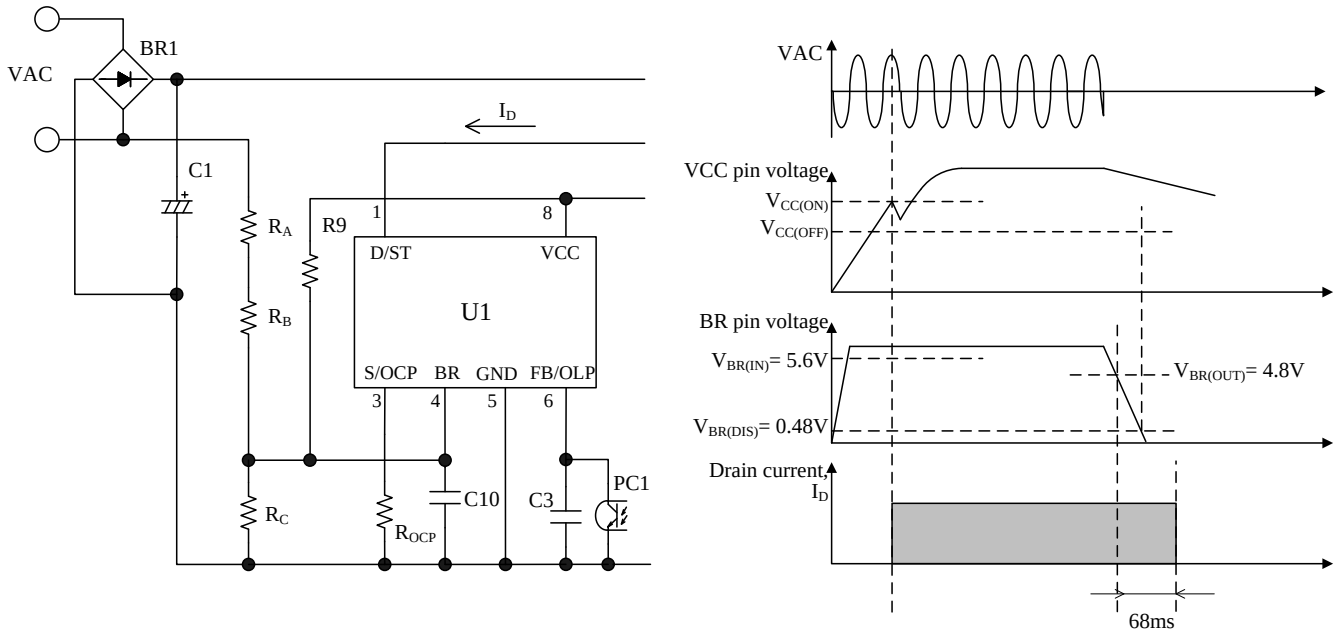


Figure 8-10 Brown-In and Brown-Out function controlled by AC line detection

8.8 Overcurrent Protection Function (OCP)

The OCP function detects each peak drain current level of the power MOSFT by the current detection resistor, R_{OCP}. When the OCP pin voltage increases to the internal OCP threshold voltage, the IC turns off the power MOSFET on pulse-by-pulse basis, and limits the output power.

ICs with PWM control usually have some detection delay time on OCP detection. The steeper the slope of the actual drain current at a high AC input voltage is, the later the actual detection point is, compared to the internal OCP threshold voltage. Thus, the actual OCP point limiting the output current usually has some variation depending on the AC input voltage, as shown in Figure 8-11.

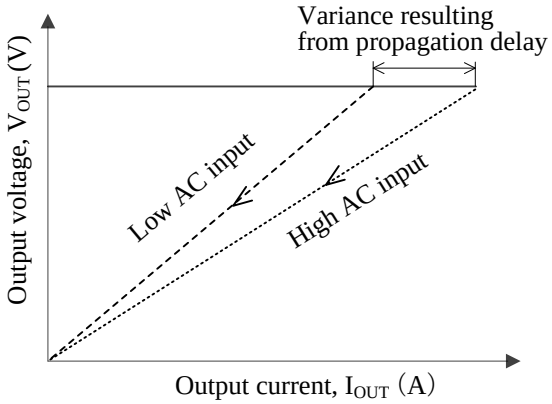


Figure 8-11 Output current at OCP without input compensation

The IC incorporates a built-in Input Compensation function that superposes a signal with a defined slope into the detection signal on the OCP pin as shown in Figure 8-12. When AC input voltage is lower and the duty cycle is longer, the OCP compensation level increases more than that in high AC input voltage. Thus, the OCP point in low AC input voltage increases to minimize the difference of OCP points between low AC input voltage and high AC input voltage, without any additional components.

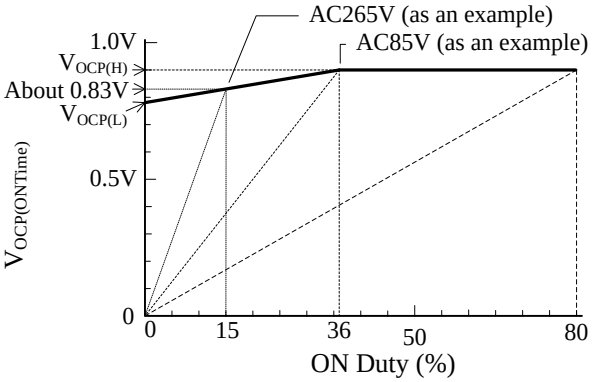


Figure 8-12 Relationship of duty cycle and OCP threshold voltage after compensation

Because the compensation signal level is designed to depend upon the on-time of the duty cycle, the OCP threshold voltage after compensation, $V_{OCP(ONTime)}$, is given as below.
However, when the duty cycle becomes 36 % or more, the OCP threshold voltage after compensation remains at $V_{OCP(H)}$ = 0.9 V, constantly.

$$V_{OCP(ONTime)}(V) = V_{OCP(L)}(V) + DPC(mV/\mu s) \times ONTime(\mu s) \quad (3)$$

where:
$V_{OCP(L)}$ is the OCP threshold voltage at zero duty cycle (V), 0.78 V
DPC is the OCP compensation coefficient (mV/μs), 20 mV/μs, and
ONTime is the on-time of the duty cycle (μs):

$$ONTime = \frac{ONDuty}{f_{OSC(AVG)}}$$

8.9 Overvoltage Protection Function (OVP)

When the voltage between the VCC pin and the GND pin is applied to the OVP threshold voltage, $V_{CC(OVP)}$ = 29 V or more, the Overvoltage Protection function (OVP) is activated and the IC stops switching operation.
When the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.5 V, the startup circuit provides the Startup Current, $I_{STARTUP}$, to the VCC pin, in order to prevent the VCC pin voltage from decreasing to $V_{CC(OFF)}$ = 8.1 V or less. Thus, the IC maintains latch mode.
Releasing the latch mode is done by decreasing the VCC pin voltage below $V_{CC(OFF)}$ = 8.1 V after unplugging the AC input. In the Brown-In and Brown-Out function by AC line detection of Section 8.7.3, releasing the latch mode is done by the High-Speed Latch Release decreasing the BR pin voltage below $V_{BR(OUT)}$ = 4.8 V.

When the auxiliary winding supplies the VCC pin voltage, the OVP function is able to detect an excessive output voltage, such as when the detection circuit for output control is open on the secondary-side, because the VCC pin voltage is proportional to the output voltage.
The output voltage of the secondary-side at OVP operation, $V_{OUT(OVP)}$, is approximately given as below:

$$V_{OUT(OVP)} \approx \frac{V_{OUT}(\text{normal operation})}{V_{CC}(\text{normal operation})} \times 29V \quad (4)$$

8.10 Overload Protection Function (OLP)

Figure 8-13 shows the FB/OLP pin peripheral circuit, and Figure 8-14 shows each waveform for OLP operation.

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current flowing to the photocoupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin, and the FB/OLP pin voltage increases.

When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 8.1 V or more for the OLP Delay Time, t_{OLP} = 68 ms or more, the OLP function is activated and the IC stops switching operation.

When the OLP function is activated, the Bias Assist function is disabled and the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V. Thus, the IC stops switching operation by the UVLO (Undervoltage Lockout) circuit and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, and the IC starts switching operation again.

In this way, the intermittent operation by UVLO is repeated during OLP state.

This operation reduces power stress on the power MOSFET and secondary-side rectifier diode. Furthermore, this reduces power consumption, because the switching period in this intermittent operation is shorter than non-switching interval.

When the fault condition is removed, the IC returns to normal operation automatically.

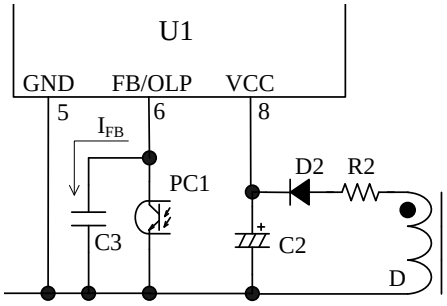


Figure 8-13 FB/OLP pin peripheral circuit

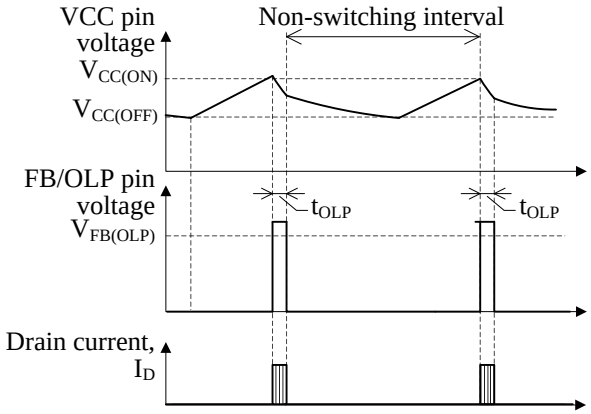


Figure 8-14 OLP operation waveforms

8.11 Thermal Shutdown Function (TSD)

If the temperature of the control part in the IC increases to more than $T_{j(TSD)}$ = 135 °C (min), the Thermal Shutdown function (TSD) is activated and the IC stops switching operation in latch mode, in the same way as Section 8.9 Overvoltage Protection Function (OVP).

Releasing the latch mode is done by decreasing the VCC pin voltage below $V_{CC(OFF)}$ = 8.1 V after unplugging the AC input. In the Brown-In and Brown-Out function by AC line detection of Section 8.7.3, releasing the latch mode is done by High-Speed Latch Release decreasing the BR pin voltage below $V_{BR(OUT)}$ = 4.8 V.

9. Design Notes

9.1 Peripheral Components

Take care to use the proper rating and proper type of components.

- Input and output electrolytic capacitors
  Apply proper design margin to accommodate ripple current, voltage, and temperature rise.
  A low ESR type for output smoothing capacitor, designed for switch-mode power supplies, is recommended to reduce output ripple voltage.

- Current detection resistor, R_{OCP}
  Choose a low inductance and high surge-tolerant type. Because a high frequency switching current flows to R_{OCP} in Figure 9-1, a high inductance resistor may cause poor operation.

- BR pin peripheral circuit
  The Brown-In and Brown-Out function has two types of detection method: AC line or DC line.
  Refer to Section 8.7 Brown-In and Brown-Out Function.

- FB/OLP pin peripheral circuit
  C3, located between the FB/OLP pin and the GND pin in Figure 9-1, performs high frequency noise rejection and phase compensation. C3 should be connected close to these pins. The reference value of C3 is about 2200p to 0.01µF, and should be adjusted based on actual operation in the application.

- VCC pin peripheral circuit
  Figure 9-2 shows the VCC pin peripheral circuit.
  The reference value of C2 is generally 10µ to 47µF (refer to Section 8.1 Startup Operation, because the startup time is determined by the value of C2).
  In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 9-3), and the Overvoltage Protection function (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary-side winding when the power MOSFET turns off.
  For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 9-2). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

- Phase Compensation
  A typical phase compensation circuit with a secondary-side shunt regulator (U51) is shown in Figure 9-4. The reference value of C52 for phase compensation is about 0.047µ to 0.47µF, and should be adjusted based on actual operation in the application.

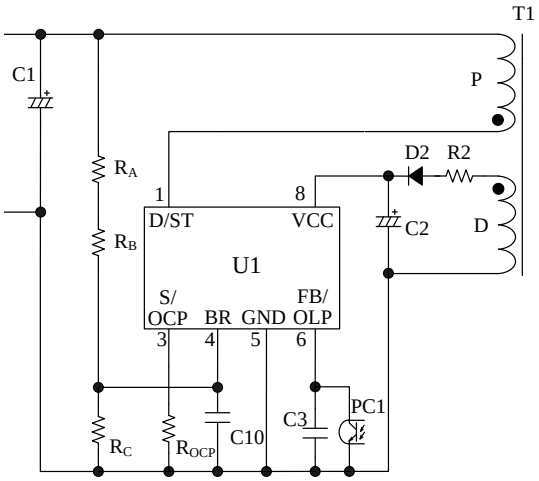


Figure 9-1 IC peripheral circuit

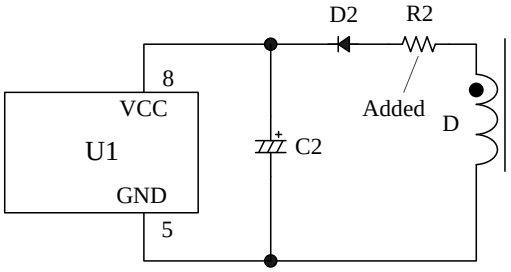


Figure 9-2 VCC pin peripheral circuit

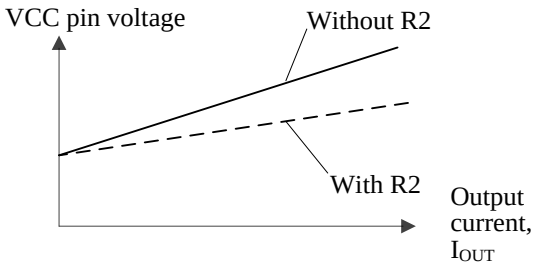


Figure 9-3 V_{CC} versus I_{OUT} with and without resistor R2

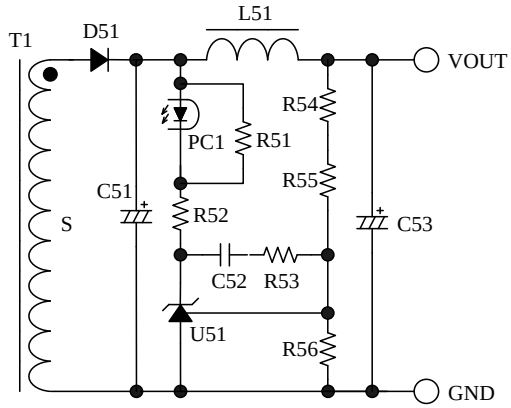


Figure 9-4 Peripheral circuit around secondary-side shunt regulator (U51)

● Transformer

Apply proper design margin to core temperature rise due to core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration. Choose a suitable wire gauge in consideration of the RMS current and a current density of about 3 to 4 A/mm^2. If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

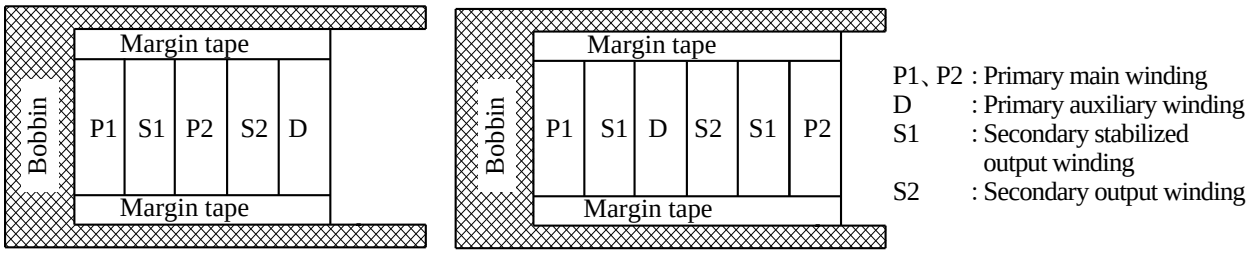
▫ Increase the number of wires in parallel.
▫ Use litz wire.
▫ Thicken the wire gauge

Fluctuation of the VCC pin voltage by I_{OUT} worsens in the following cases, requiring a transformer designer to pay close attention to the placement of the auxiliary winding D:

▪ Poor coupling between the primary-side and secondary-side windings (this causes high surge voltage and is seen in a design with low output voltage and high output current)
▪ Poor coupling between the auxiliary winding D and the secondary-side stabilized output winding where the output line voltage is controlled constant by the output voltage feedback (this is susceptible to surge voltage)

In order to reduce the influence of surge voltage on the VCC pin, Figure 9-5 shows winding structural examples which take into consideration the placement of the auxiliary winding D:

▫ Winding structural example (a): Separating the auxiliary winding D from the primary-side windings P1 and P2. P1 and P2 are windings divided the primary-side winding into two.
▫ Winding structural example (b): Placing the auxiliary winding D within the secondary-side stabilized output winding, S1, in order to improve the coupling of those windings. S1 is a stabilized output winding of secondary-side windings, controlled to constant voltage.



Winding structural example (a) Winding structural example (b)

Figure 9-5 Winding structural examples

9.2 PCB trace layout and Component placement

PCB circuit trace design and component layout significantly affects operation, EMI noise, and power dissipation. Therefore, pay extra attention to these designs. In general, trace loops shown in Figure 9-6 where high frequency currents flow should be wide, short, and small to reduce line impedance.

In addition, earth ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Switch-mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines. Furthermore, because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it when preparing a thermal design.

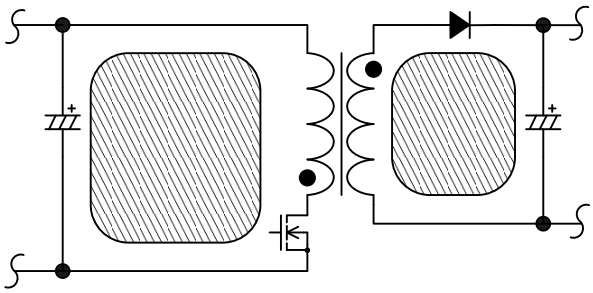


Figure 9-6 High frequency current loops (hatched areas)

Figure 9-7 shows a circuit layout design example for the IC peripheral circuit and secondary-side rectifier-smoothing circuit.

- IC Peripheral Circuit

  (1) S/OCP pin Trace Layout: S/OCP pin to R_{OCP} to C1 to T1 (winding P) to D/ST pin

  This is the main trace containing switching currents, and thus it should be as wide and short as possible. If the IC and C1 are distant from each other, placing a capacitor such as film or ceramic capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

  (2) GND Trace Layout: GND pin to C2 (negative pin) to T1 (winding D) to R2 to D2 to C2 (positive pin) to VCC pin

  This is the trace for supplying power to the IC, and thus it should be as wide and short as possible. If the IC and C2 are distant from each other, placing a capacitor such as film or ceramic capacitor (about 0.1 μ to 1.0 μF) close to the VCC pin and the GND pin is recommended.

  (3) R_{OCP} Trace Layout

  R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 9-7) which is close to the base of R_{OCP}, in order to reduce common impedance, and to avoid interference from switching currents to the control part in the IC.

- Secondary-side Rectifier-Smoothing Circuit Trace Layout: T1 (winding S) to D51 to C51

  This is the trace of the rectifier-smoothing loop, carrying the switching current, and thus it should be as wide and short as possible.

  If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier-smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

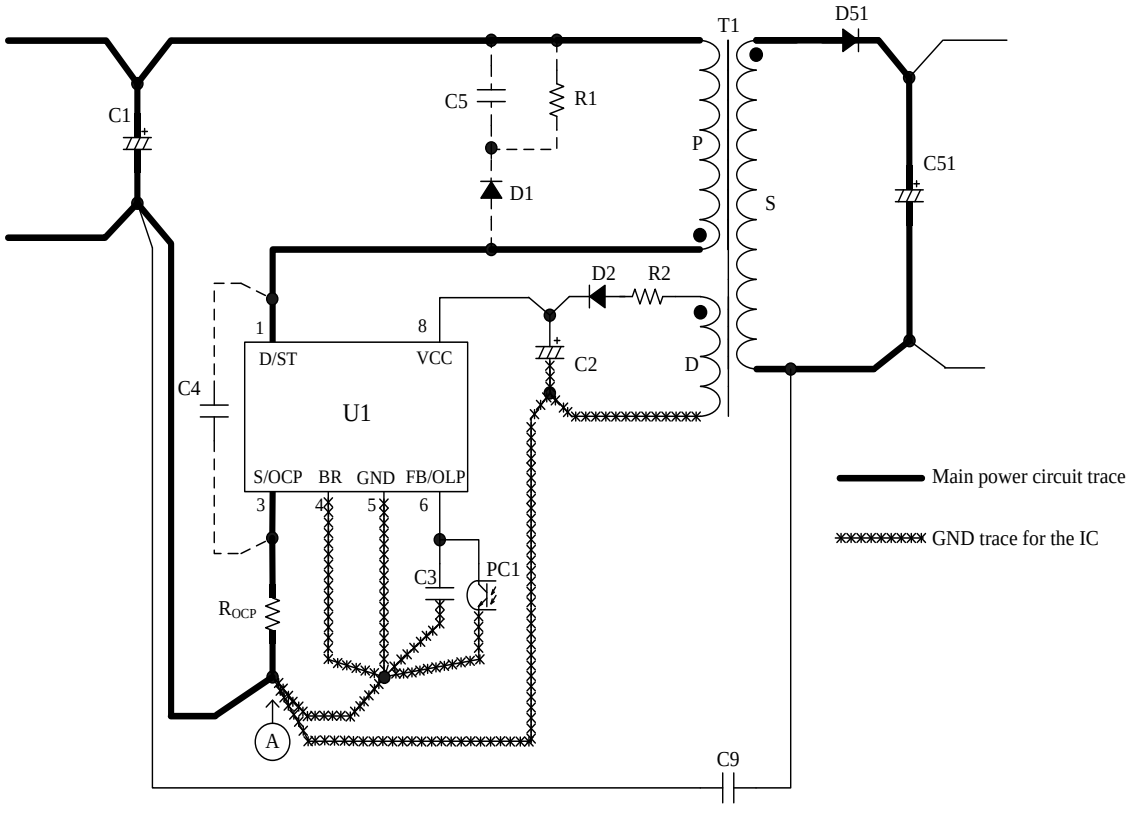


Figure 9-7 Peripheral circuit example around the IC

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