STR2W100D Series PWM Off-Line Switching Regulators

General Description

STR2W100D series are power ICs for switching power supplies, incorporating a power MOSFET and a current mode PWM controller IC in one package.

Including a startup circuit and a standby function in the controller, the product achieves low power consumption, low standby power, and high cost-effectiveness in power supply systems, while reducing external components.

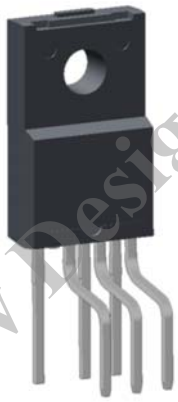


Figure 1. STR2W100D series packages are fully molded TO-220 package types. Pin 2 is deleted for greater isolation.

Features and Benefits

- Current mode PWM control
- Built-in Random Switching function: reduces EMI noise, simplifies EMI filters, and cuts cost by external part reduction
- Built-in Slope Compensation function: avoids subharmonic oscillation
- Built-in Leading Edge Blanking (LEB) function
- Auto Standby function:
  - Input power, P_{IN} < 25 mW at no load
  - Normal load operation: PWM switching
  - Light load operation: Standby mode (Burst oscillation)
- Soft Start function: reduces stress on internal power MOSFET and output rectifier diode
- Protection Functions:
  - Overcurrent Protection function (OCP); Pulse-by-pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
  - Overload Protection function (OLP); Auto restart, built-in timer, reduces heat during overload condition, and no external components required
  - Overvoltage Protection function (OVP); Auto restart
  - Thermal Shutdown function (TSD); Auto restart

Applications

Switching power supplies for electronic devices such as:

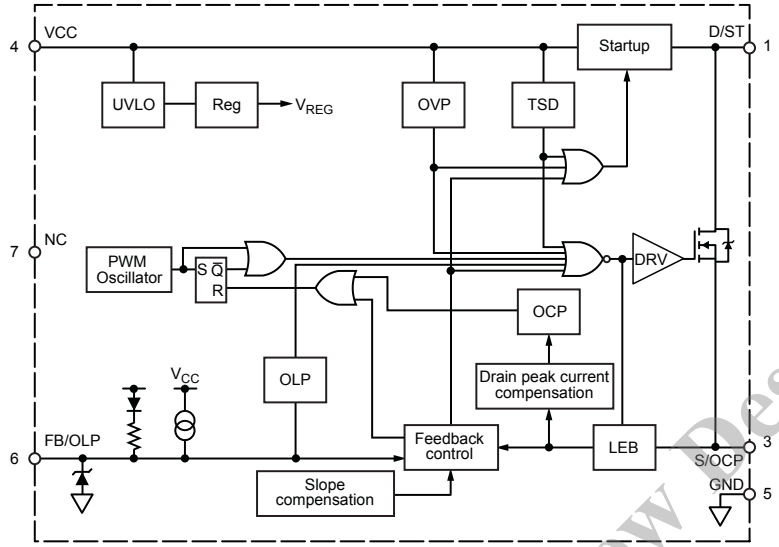
- Home appliances
- Digital appliances
- Office automation (OA) equipment
- Industrial apparatus
- Communication facilities

The product lineup for the STR2W100D series provides the following options:

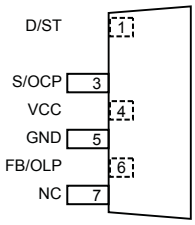
Part Number	f_{OSC} (kHz)	MOSFET		P_{OUT}* (W)	
		V_{DSS}(min) (V)	$R_{DS(on)}$ (max) (Ω)	230 VAC	85 to 265 VAC
STR2W152D	67	650	3.0	60	40
STR2W153D			1.9	90	60

*The listed output power is based on the package thermal ratings, and the peak output power can be 120% to 140% of the value stated here. At low output voltage and short duty cycle, the output power may be less than the value stated here.

Functional Block Diagram



Pin-out Diagram



STR2W100D Pin List Table

Number	Name	Function
1	D/ST	MOSFET drain pin and input of the startup current
3	S/OCP	MOSFET source and input of Overcurrent Protection (OCP) signal
4	VCC	Power supply voltage input for Control Part and input of Overvoltage Protection (OVP) signal
5	GND	Ground
6	FB/OLP	Feedback signal input for constant voltage control signal and input of Overload Protection (OLP) signal
7	NC	No connection

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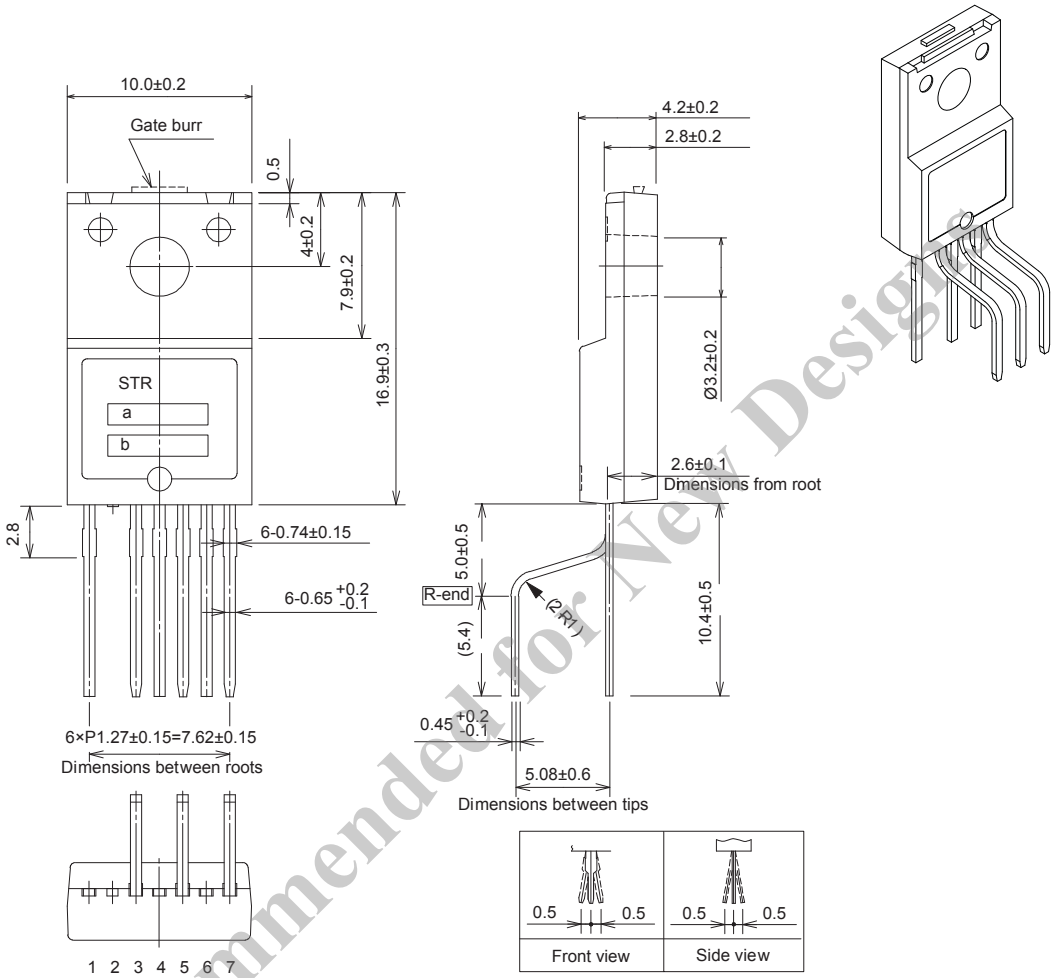
Package Outline Drawing, TO-220F-6L



Unit: mm
Dashed line at gate burr indicates protrusion of 0.3 mm (maximum)
Leadform: LF2003
Pin 2 is deleted in order to ensure creepage and clearance of the high voltage pin (pin 1) and low voltage pin (pin 3)

a. Type Number: 2W1xxD
b. Lot Number:
1st and 2nd letter: Control number
3rd letter: Last digit of year (0-9)
4th letter: Month
1 to 9 for Jan. to Sept.
O for Oct.
N for Nov.
D for Dec.
5th and 6th letter: Day of month (01-31)
7th and 8th letter: Control number

Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Electrical Characteristics

• Refer to the datasheet of each product for these details.

• The polarity value for current specifies a sink as "+ ," and a source as "–," referencing the IC.

Absolute Maximum Ratings Unless specifically noted, T_A is 25°C

Characteristic	Symbol		Notes	Pins	Rating	Unit
Drain Peak Current	I_{DPEAK}	STR2W152D	Single pulse	1−3	6.0	A
		STR2W153D			9.5	A
Maximum Switching Current	I_{DMAX}	STR2W152D	T_A = −20°C to 125°C	1−3	6.0	A
		STR2W153D			9.5	A
Avalanche Energy	E_{AS}	STR2W152D	Single pulse, V_{DD} = 99 V, L = 20 mH	1−3	62	mJ
		STR2W153D			86	mJ
	I_{LPEAK}	STR2W152D			2.3	A
		STR2W153D			2.7	A
S/OCP Pin Voltage	V_{OCP}			3−5	−2 to 6	V
Control Part Input Voltage	V_{CC}			4−5	32	V
FB/OLP Pin Voltage	V_{FB}			6−5	−0.3 to 14	V
FB/OLP Pin Sink Current	I_{FB}			6−5	1.0	mA
MOSFET Power Dissipation	P_{D1}	STR2W152D	With infinite heatsink	1−3	23.8	W
		STR2W153D			26.5	W
		Without heatsink			1.3	W
Control Part Power Dissipation	P_{D2}	V_{CC} × I_{CC}		4−5	0.13	W
Internal Frame Temperature In Operation*	T_F			–	−20 to 115	°C
Operating Ambient Temperature	T_{OP}			–	−20 to 115	°C
Storage Temperature	T_{stg}			–	−40 to 125	°C
Channel Temperature	T_{ch}			–	150	°C

*The recommended internal frame temperature, T_F , is 105°C (max).

Electrical Characteristics of Control Part Unless specifically noted, T_A is 25°C, V_{CC} = 18 V

Characteristic	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Unit
Operation Start Voltage	$V_{CC(ON)}$		4 – 5	13.8	15.3	16.8	V
Operation Stop Voltage*	$V_{CC(OFF)}$		4 – 5	7.3	8.1	8.9	V
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	4 – 5	−	−	2.5	mA
Minimum Start Voltage	$V_{ST(ON)}$		4 – 5	−	40	−	V
Startup Current	$I_{STARTUP}$	V_{CC} = 13.5 V	4 – 5	−3.9	−2.5	−1.1	mA
Startup Current Threshold Biasing Voltage*	$V_{CC(BIAS)}$	I_{CC} = –100 µA	4 – 5	8.5	9.5	10.5	V
Average Operation Frequency	$f_{OSC(AVG)}$		1 – 5	60	67	74	kHz
Frequency Modulation Deviation	Δf		1 – 5	−	5	−	kHz
Maximum Duty Cycle	D_{MAX}		1 – 5	65	74	83	%
Leading Edge Blanking Time	t_{BW}		–	−	390	−	ns
OCP Compensation Coefficient	DPC		–	−	17	−	mV/µs
OCP Compensation Duty Cycle Limit	D_{DPC}		–	−	36	−	%
OCP Threshold Voltage at Zero Duty Cycle	$V_{OCP(L)}$		3 – 5	0.69	0.78	0.87	V
OCP Threshold Voltage at 36% Duty Cycle	$V_{OCP(H)}$		3 – 5	0.79	0.88	0.97	V
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V	6 – 5	−280	−170	−90	µA
Minimum Feedback Current	$I_{FB(MIN)}$		6 – 5	−30	−15	−7	µA
FB/OLP Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$	V_{CC} = 32 V	6 – 5	1.3	1.4	1.5	V
OLP Threshold Voltage	$V_{FB(OLP)}$	V_{CC} = 32 V	6 – 5	7.3	8.1	8.9	V
OLP Operation Current	$I_{CC(OLP)}$	V_{CC} = 12 V	4 – 5	−	230	−	µA
OLP Delay Time	t_{OLP}		1 – 5	54	68	82	ms
FB/OLP Clamp Voltage	$V_{FB(CLAMP)}$		6 – 5	11	12.8	14	V
OVP Threshold Voltage	$V_{CC(OVP)}$		4 – 5	26	29	32	V
Thermal Shutdown Activating Temperature	$T_{J(TSD)}$		−	130	−	−	°C

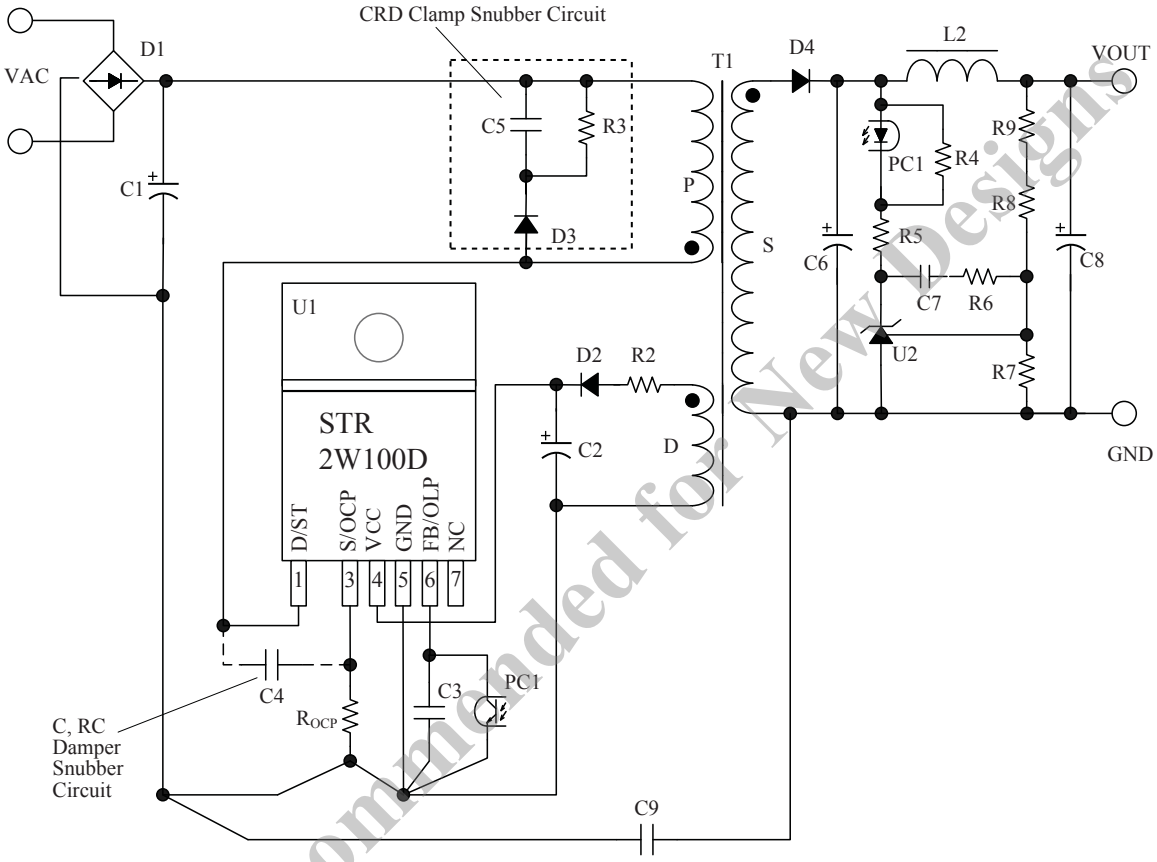
*$V_{CC(BIAS)}$ > $V_{CC(OFF)}$ always.

Electrical Characteristics of MOSFET Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Test Conditions		Pins	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V_{DSS}			1 – 5	650	–	–	V
Drain Leakage Current	I_{DSS}			1 – 5	–	–	300	μA
On-Resistance	$R_{DS(ON)}$	STR2W152D		1 – 5	–	–	3.0	Ω
		STR2W153D			–	–	1.9	Ω
Switching Time	t_f			1 – 5	–	–	250	ns
Thermal Resistance*	$R_{\theta ch-F}$	STR2W152D		–	–	–	2.48	°C/W
		STR2W153D			–	–	1.95	°C/W

*The thermal resistance between the channels of the MOSFET and the internal frame.

Typical Application Circuit



The following design features should be observed:
• The PCB traces from the D/ST pin should be as wide as possible, in order to enhance thermal dissipation.
• In applications having a power supply specified such that V_{DS} has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

Functional Description

All of the parameter values used in these descriptions are typical values, according to the STR2W153D specification, unless they are specified as minimum or maximum.

With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

Startup Operation

Startup Period

Figure 2 shows the VCC pin peripheral circuit. The built-in startup circuit is connected to the D/ST pin, and it generates a constant current, $I_{STARTUP}$ = –2.5 mA to charge capacitor C2 connected to the VCC pin. During this process, when the VCC pin voltage reaches $V_{CC(ON)}$ = 15.3V, the control circuit starts operation. After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

The approximate startup time, t_{START}, is calculated as follows:

$$t_{START} \approx C_2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{STARTUP}|} \quad (1)$$

where:

t_{START} is the startup time in s, and

$V_{CC(INT)}$ is the initial voltage of the VCC pin in V.

C2 should be an electrolytic capacitor, in the range 10 to 47 µF, for general power supply applications.

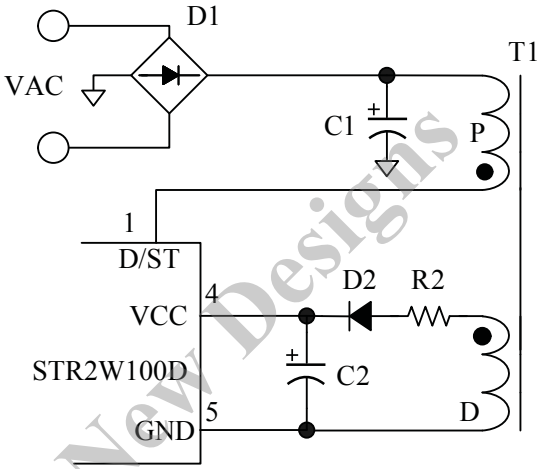


Figure 2. VCC pin peripheral circuit

Undervoltage Lockout (UVLO) Circuit

Figure 3 shows the relationship of V_{CC} and I_{CC}. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, the control circuit starts operation and the circuit current, I_{CC}, increases.

In operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the control circuit stops operation, by the UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup. The voltage from the auxiliary winding, D, in figure 2 becomes a power source to the control circuit after the operation start. The auxiliary winding voltage is targeted to be about 15 to 20 V, taking account of the winding turns of the D winding, so that the VCC pin voltage should become as follows within the specification of input voltage range and the output load range of power supply:

$$V_{CC(BIAS)}(\text{max}) < V_{CC} < V_{CC(OVP)}(\text{min}) \quad (2)$$

$$10.5\ (\text{V}) < V_{CC} < 26.0\ (\text{V})$$

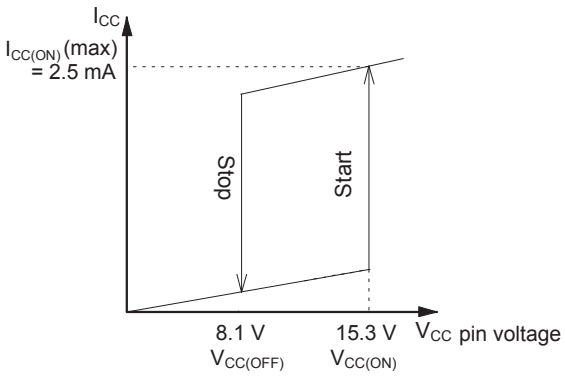


Figure 3. V_{CC} versus I_{CC}

Bias Assist Function

Figure 4 shows the VCC pin voltage behavior during the startup period. When the VCC pin voltage reaches $V_{CC(ON)}$ = 15.3 V, the control circuit starts operation, the circuit current, I_{CC}, increases, and thus the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage increases in proportion to the output voltage rise. And thus, the VCC pin voltage is set by the balance between dropping by the increase of I_{CC} and rising by the increase of the auxiliary winding voltage.

Just at the turning-off of the power MOSFET, a surge voltage occurs at the output winding. If the feedback control is activated by the surge voltage on light load condition at startup, and the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, a startup failure can occur, because the output power is restricted and the output voltage decreases.

In order to prevent this, during a state of operating feedback control, when the VCC pin voltage falls to the Startup Current Threshold Biasing Voltage, $V_{CC(BIAS)}$ = 9.5 V, the Bias Assist function is activated. While the Bias Assist function is operating, the decrease of the VCC voltage is suppressed by a supplementary current from the Startup circuit.

By the Bias Assist function, the use of a small value C2 capacitor is allowed, resulting in shortening startup time. Also, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function can also be shortened. It is necessary to check and adjust the process so that poor starting conditions may be avoided.

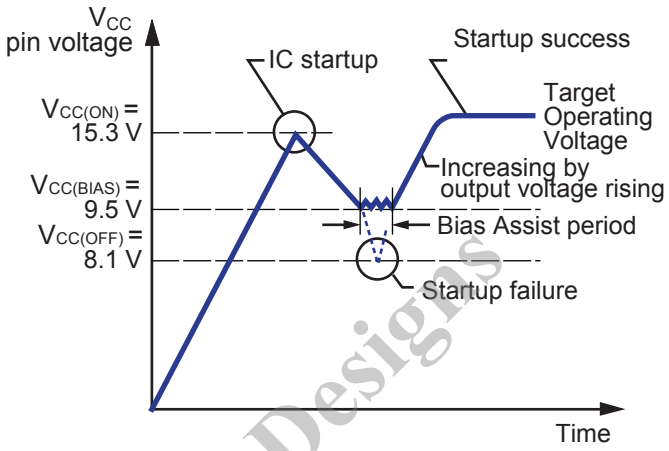


Figure 4. V_{CC} during startup period

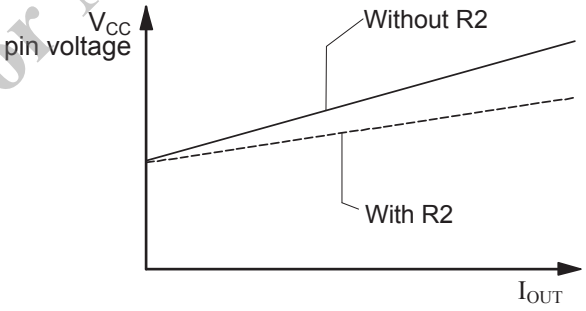


Figure 5. V_{CC} versus I_{OUT} with and without resistor R2

Auxiliary Winding

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output of the SMPS (see figure 5). This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see figure 6). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

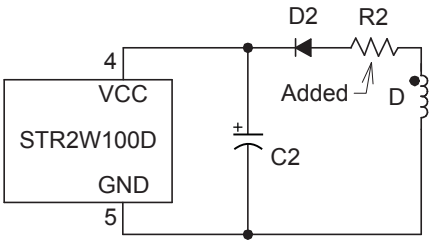


Figure 6. VCC pin peripheral circuit with R2

The variation of VCC pin voltage becomes worse if:

- The coupling between the primary and secondary windings of the transformer gets worse and the surge voltage increases (low output voltage, large current load specification, for example).
- The coupling of the auxiliary winding, D, and the secondary side stabilization output winding (winding of the output line which is controlling constant voltage) gets worse and it is subject to surge voltage.

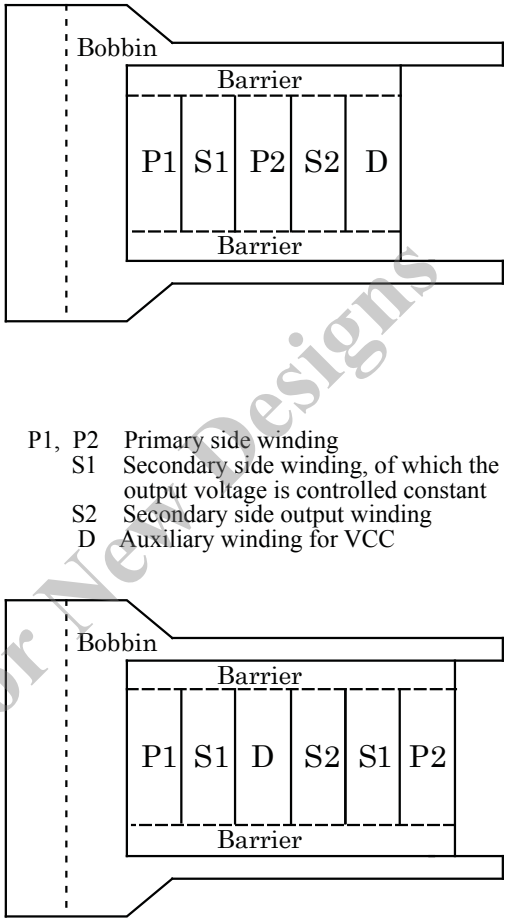
In order to reduce the influence of surge voltages on the VCC pin, alternative designs for the auxiliary winding, D, can be used; as examples of transformer structural designs see figure 7.

- Winding structural example (a): Separating the auxiliary winding D from the primary side windings P1 and P2.

  The primary side winding is divided into two windings, P1 and P2.

- Winding structural example (b): Placing the auxiliary winding D within the secondary winding S1 in order to improve the coupling of those windings.

  The output winding S1 is a stabilized output winding, controlled to constant voltage.



P1, P2 Primary side winding
S1 Secondary side winding, of which the output voltage is controlled constant
S2 Secondary side output winding
D Auxiliary winding for VCC

Figure 7. Winding structural examples

Soft-Start Function

Figure 8 shows the behavior of VCC pin voltage and the drain current during the startup period.

The IC activates the soft start function during the startup period. The soft start operation period is internally fixed to approximately 7 ms, and the overcurrent protection (OCP) threshold voltage steps up in five steps during this period. This reduces the voltage and current stress on the internal power MOSFET and on the secondary-side rectifier. Because the Leading Edge Blanking function (refer to the Constant Output Voltage Control section) is disabled during the soft start period, the on-time may be the LEB time, t_{BW} = 390 ns or less. It is necessary to check and adjust the OLP delay time and the VCC pin voltage during startup in actual operation.

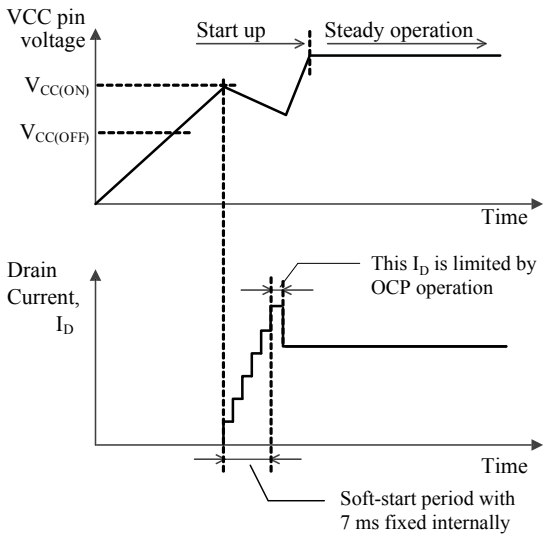


Figure 8. Soft-start operation waveforms at startup

Constant Output Voltage Control

For enhanced response speed and stability, current mode control (peak current mode control) is used for constant voltage control of the output voltage. This IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}. V_{SC} is generated by inputting the FB/OLP pin voltage to the feedback control (see functional block diagram) and adding the slope compensation value (refer to figures 9 and 10).

• **Light load conditions** When load conditions become lighter, the output voltage, V_{OUT}, rises, and the feedback current from the error amplifier on the secondary side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, the peak value of V_{ROCP} is controlled to be low, and the peak drain current, I_D, decreases. This control prevents the output voltage from increasing.

• **Heavy load conditions** When load conditions become greater, the control circuit performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases. This control prevents the output voltage from decreasing.

In the current-mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current. This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in figure 11. It is called the *subharmonics* phenomenon.

In order to suppress the subharmonics phenomenon, the IC incorporates a slope compensation signal to the target voltage, Vsc. Because the compensation signal is a down slope signal, Vsc output on the FB/OLP pin goes down as the duty cycle rises, reducing the controlled drain peak current. Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance during normal operation.

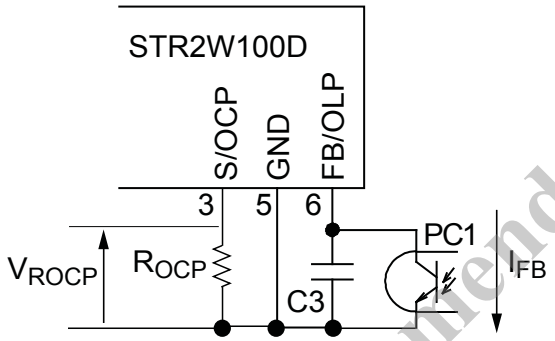


Figure 9. FB/OLP peripheral circuit

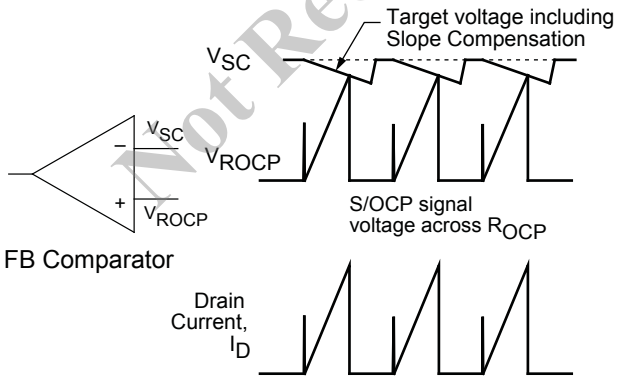


Figure 10. Drain current, I_D, and FB comparator operation in steady operation

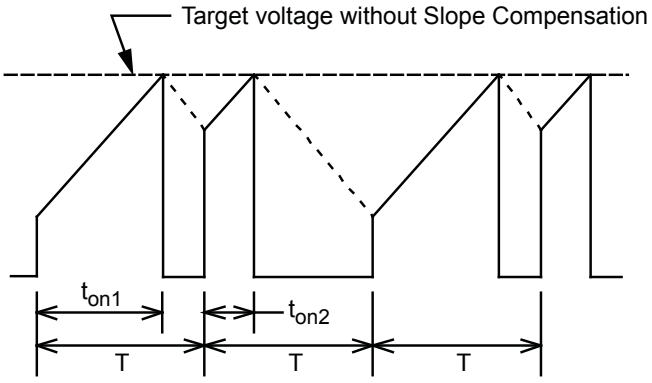


Figure 11. Drain current, I_D, waveform in subharmonic oscillation

In the current-mode control method, the FB comparator and/or the OCP comparator may respond to the surge voltage resulting from the drain surge current in turning-on the power MOSFET, and may turn off the power MOSFET irregularly. Leading Edge Blanking, t_{BW} (390 ns), is built-in to prevent malfunctions caused by surge voltage in turning-on the power MOSFET.

Automatic Standby Mode Function

Automatic Standby mode is activated automatically when the drain current, I_D, reduces under light load conditions at which I_D is less than 25% to 30% of the maximum drain current (it is in the Overcurrent Protection state). The operation mode becomes burst oscillation, as shown in figure 12.

Burst oscillation reduces switching losses and improves power supply efficiency because of periodic non-switching intervals. Generally, to improve efficiency under light load conditions, the frequency of the burst oscillation becomes just a few kilohertz.

During the transition to burst-oscillation, if the VCC pin voltage decreases to $V_{CC(BIAS)}$ (9.5 V), the Bias Assist function is activated and stabilizes the Standby mode operation, because $I_{STARTUP}$ is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist function is always activated during Standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio between the auxiliary winding and secondary winding and/or reducing the value of R2 in figure 6.

Random Switching Function

The IC modulates its switching frequency randomly within Δf (5 kHz) superposed on the Average Operation Frequency, $f_{OSC(AVG)}$ = 67 kHz. The conduction noise with this function is smaller than that without this function, and this function can simplify noise filtering of the input lines of power supply.

Overcurrent Protection Function (OCP)

Overcurrent Protection Function (OCP) detects each peak drain current level of the power MOSFET on pulse-by-pulse basis, and limits the output power. This function incorporates the Input Compensation function to reduce OCP point variation for the AC input voltage, without any additional external components. This OCP function detects the drain current by the current detection resistor, R_{OCP}, which is connected between the S/OCP pin and the GND pin. When the voltage drops on both sides of R_{OCP} increase to the OCP threshold voltage, V_{OCP}, the power MOSFET is turned off.

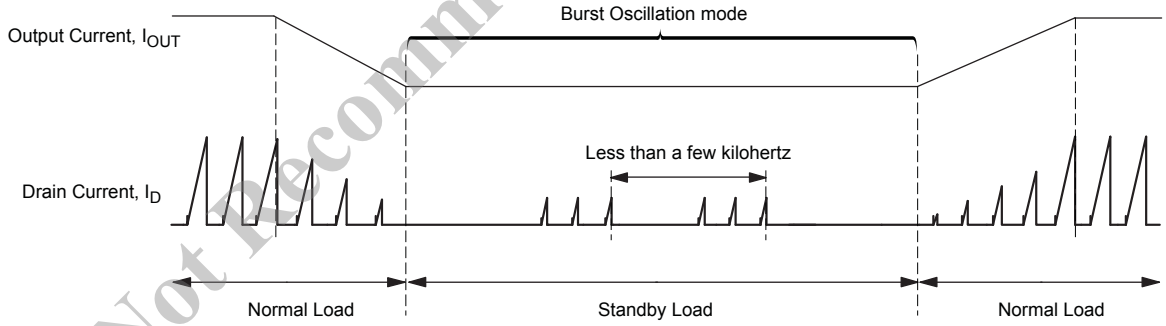


Figure 12. Automatic Standby mode operation

ICs with PWM control usually have some detection delay time on OCP detection. The steeper the slope of the actual drain current at a high AC input voltage is, the later the actual detection point is, compared to the internal OCP threshold voltage, V_{OCP}. And thus the actual OCP point limiting the output current usually has some variation depending on the AC input voltage, as shown in figure 13.

The IC incorporates a built-in Input Compensation function that superposes a signal with a defined slope onto the detection signal on the S/OCP pin as shown in figure 14. When AC input voltage is lower and the duty cycle is longer, the OCP compensation level increases. Thus the OCP point in low AC input voltage increases to minimize the difference of OCP points between low AC input voltage and high AC input voltage.

Because the compensation signal level is designed to depend upon the on-time of the duty cycle, OCP threshold voltage after compensation, $V_{OCP(ontime)}$, is calculated as below. When the duty cycle becomes 36% or more, OCP threshold voltage after compensation remains at $V_{OCP(H)}$ = 0.88 V, constantly.

$$V_{OCP(ontime)}\,(V) = V_{OCP(L)}(V) + DPC\,(mV/\mu s) \times On\ Time\,(\mu s). \quad (3)$$

where:

$V_{OCP(L)}$ is the OCP threshold voltage at zero duty cycle (V),

DPC is the OCP compensation coefficient (mV/µs), and

On Time is the the on-time of the duty cycle (µs): On Time = $(D / f_{OSC(AVG)})$

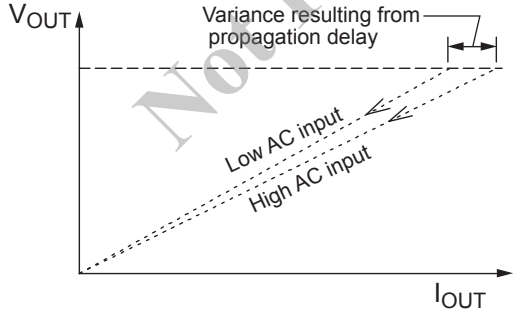


Figure 13. Output current at OCP without input compensation

Overvoltage Protection Function (OVP)

When the voltage between the VCC pin and the GND pin increases to $V_{CC(OVP)}$ = 29 V or more, the OVP function is activated and stops switching operation.

While OVP is active, because the Bias Assist function is disabled, the VCC pin voltage falls below the Operation Stop Voltage, $V_{CC(OFF)}$ (8.1 V). At that time, the UVLO (Undervoltage Lockout) circuit becomes active, stopping the control circuit and then restarting it. Then, when the VCC pin voltage rises due to the startup current and reaches the Operation Start Voltage, $V_{CC(ON)}$ (15.3 V), the control circuit will return to normal operation again. In this manner, the intermittent oscillation mode is operated by the UVLO circuit repeatedly while there is an excess voltage condition. By this intermittent oscillation operation, stress on the internal and external circuits, such as the power MOSFET and the secondary rectifier diode, is reduced. Furthermore, because the switching period is shorter than an oscillation stop period, power consumption under intermittent operation can be minimized. When the fault condition is removed, the IC returns to normal operation automatically.

When the auxiliary winding supplies the VCC pin voltage, the OVP function is able to detect an excessive output voltage, such as when the detection circuit for output control is open on the secondary side, because the VCC pin voltage is proportional to the output voltage.

The output voltage of the secondary side at OVP operation, $V_{OUT(OVP)}$, is calculated approximately as follows:

$$V_{OUT(OVP)} = \frac{V_{OUT}(\text{normal operation})}{V_{CC}(\text{normal operation})} \times 29\ (V) \quad (4)$$

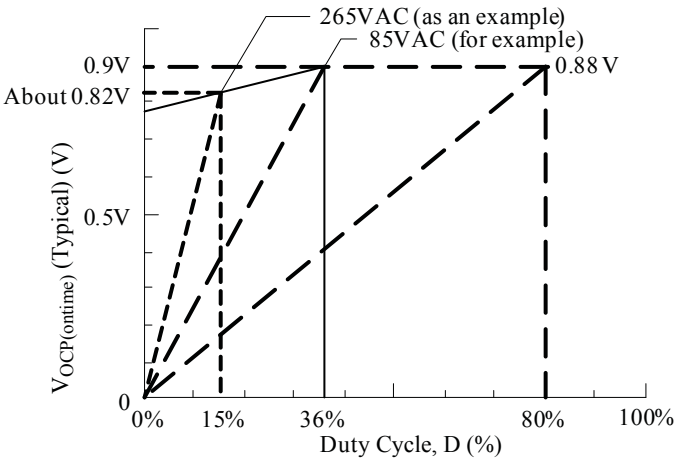


Figure 14. Relationship of duty cycle and V_{OCP} at $f_{OSC(AVG)}$ = 67 kHz

Overload Protection Function (OLP)

When the drain peak current is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler, I_{FB} (see figure 15), becomes zero. As a result, the FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ (8.1 V) or more, and remains at that level for the OLP Delay Time, t_{OLP} (68 ms) or more, the OLP function is activated. It stops switching operation and reduces stress on the power MOSFET, secondary rectifier, and so on.

When the OLP function is activated, the Bias Assist function is disabled, as mentioned in the Overvoltage Protection Function (OVP) section, and intermittent mode operation by the UVLO circuit is performed repeatedly. When the fault condition is removed, the IC returns to normal operation automatically.

Thermal Shutdown Function (TSD)

If the temperature of the Control Part of the IC reaches more than the Thermal Shutdown Activating Temperature $T_{J(TSD)}$ = 130°C (min), the Thermal Shutdown function (TSD) is activated.

During TSD operation, the Bias Assist function is disabled, and intermittent mode operation by the UVLO circuit is performed repeatedly. If the factor causing the overheating condition is removed, and the temperature of the Control Part falls below $T_{J(TSD)}$, the IC returns to normal operation automatically.

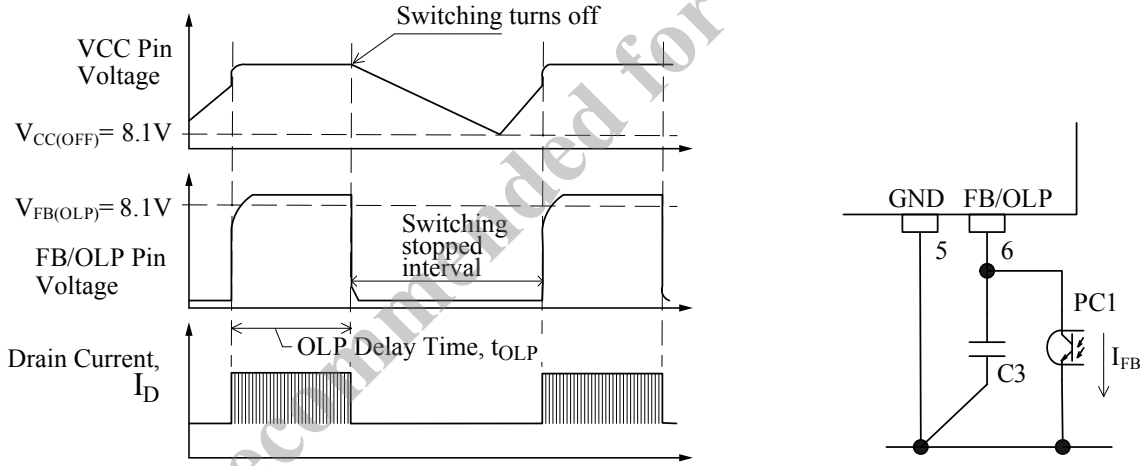


Figure 15. OLP operation waveforms (left), and FB/OLP pin peripheral circuit (right)

Design Notes

Peripheral Components

Take care to use properly rated and proper type of components.

- Input and output electrolytic capacitors
  - Apply proper design margin to ripple current, voltage, and temperature rise.
  - Use of high ripple current and low impedance types, designed for switch-mode power supplies, is recommended, depending on their purposes.
- Transformer
  - Apply proper design margin to core temperature rise by core loss and copper loss.
  - Because switching currents contain high frequency currents, the skin effect may become a consideration.
  - In consideration of the skin effect, choose a suitable wire gauge in consideration of rms current and a current density of about 3 to 4 A/mm^2.
  - If measures to further reduce temperature are still necessary, use paralleled wires or litz wires to increase the total surface area of the wiring.
- Current detection resistor, R_{OCP}
  - A high frequency switching current flows to R_{OCP}, and may cause poor operation if a high inductance resistor is used.
  - Choose a low inductance and high surge-tolerant type.

Phase Compensation

A typical phase compensation circuit with a secondary shunt regulator (U2) is shown in figure 16. The value for C7 is recommended to be about 0.047 to 0.47 µF, and should be selected based on actual operation in the application.

Place C3 between the FB/OLP pin and the GND pin, as shown in figure 17, to perform high frequency noise reduction and phase compensation. The value for C3 is recommended to be about 2200 pF to 0.01 µF.

C3 should be connected close to the FB/OLP pin and the GND pin, and should be selected based on actual operation in the application.

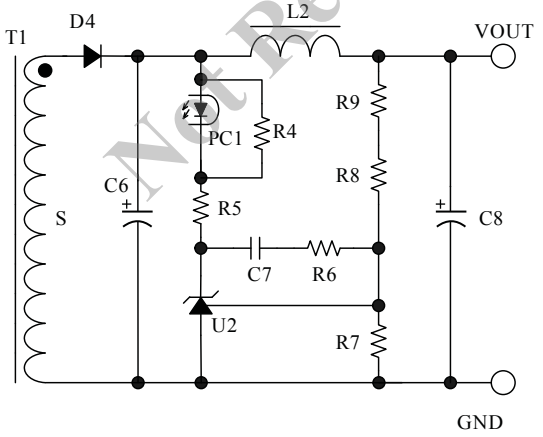


Figure 16. Peripheral circuit around secondary shunt regulator

PCB Trace Layout and Component Placement

PCB circuit trace design and component layout significantly affect operation, EMI noise, and power dissipation. Therefore, pay extra attention to these designs. In general, where high frequency current traces form a loop, as shown in figure 18, wide, short traces, and small circuit loops are important to reduce line impedance. In addition, earth ground traces affect radiated EMI noise, and the same measures should be taken into account.

Switch-mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines. Furthermore, because the incorporated power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it when preparing a thermal design.

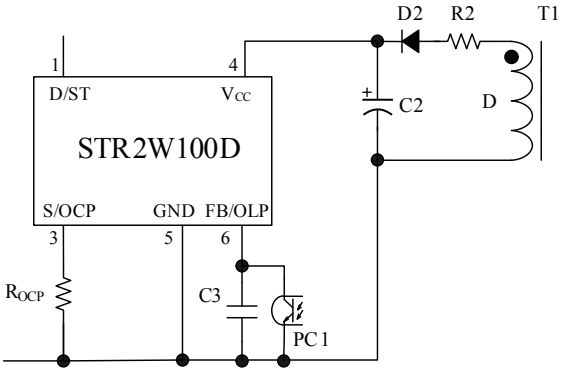


Figure 17. FB/OLP peripheral circuit

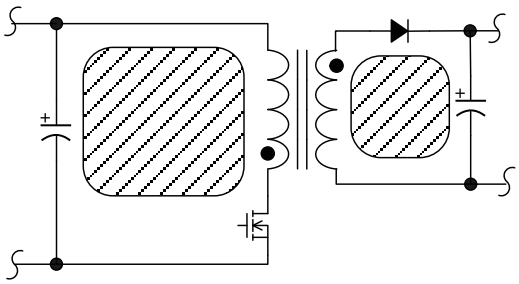


Figure 18. High-frequency current loops (hatched areas)

Figure 19 shows a circuit layout design example.

• S/OCP Trace Layout: S/OCP pin to R_{OCP} to C1 to T1 (winding P) to D/ST pin

This is the main trace containing switching currents, and thus it should be as wide and short as possible.

If C1 and the IC are distant from each other, an electrolytic capacitor or film capacitor (about 0.1 µF and with proper voltage rating) near the IC or the transformer is recommended to reduce impedance of the high frequency current loop.

• GND Trace Layout: GND pin to C2 (negative pin) and T1 (winding D) to R2 to D2 to C2 (positive pin) to VCC pin

This trace also must be as wide and short as possible.

If C2 and the IC are distant from each other, placing a capacitor (approximately 0.1 to 1.0 µF (50 V) film capacitor) close to the VCC pin and the GND pin is recommended.

• R_{OCP} Trace Layout

R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of main trace and the control circuit ground should be connected by a single point ground (A in figure 19) to remove common impedance, and to avoid interference from switching currents to the control circuit.

Figure 19 also shows a circuit layout design example for the secondary side.

(1) Secondary Smoothing Circuit Trace Layout: T1 (winding S) to D4 to C6

This trace should be as wide as possible.

If the loop distance is lengthy, leakage inductance resulting from the long loop may increase surge voltage at turning off a power MOSFET.

Proper secondary trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

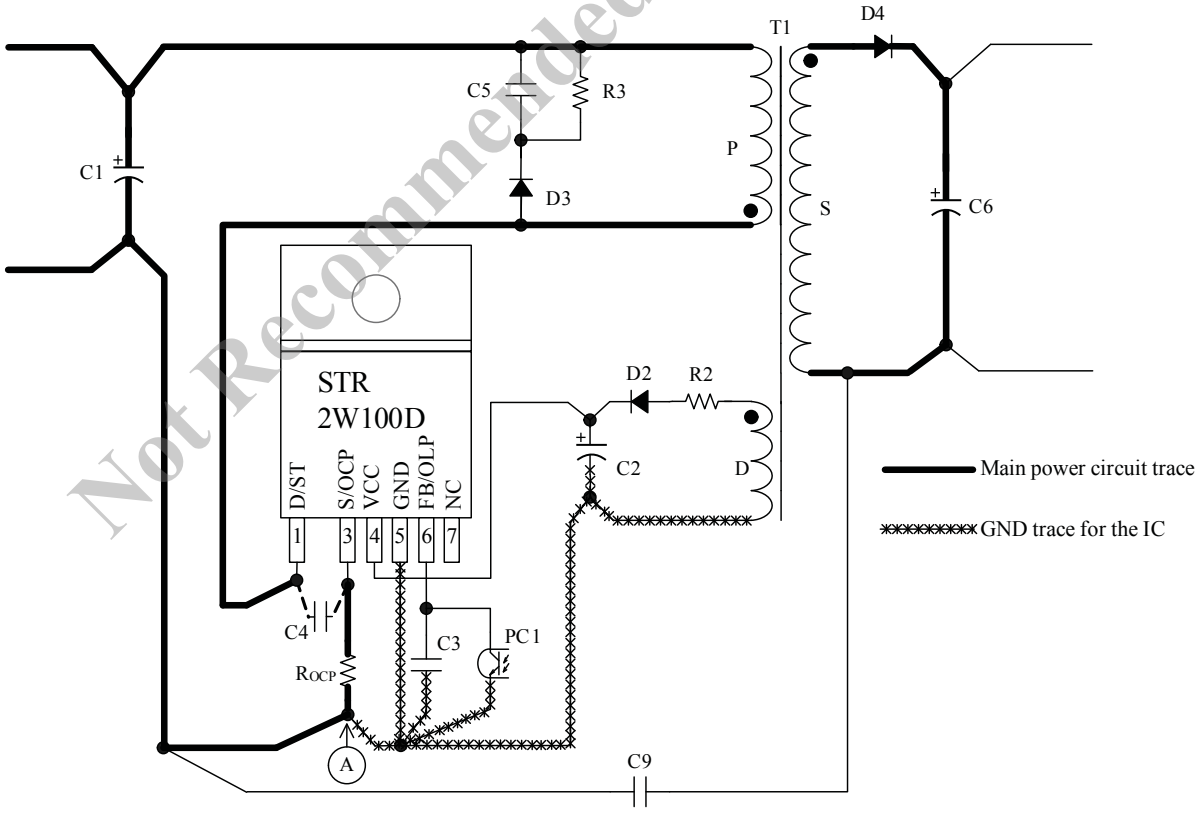


Figure 19. Peripheral circuit example around the IC

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