Development of Novel LDMOS with ESD Robustness for Start-up Circuits

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Abstract A new LDMOS (Lateral Double-diffused MOSFET) with high ESD tolerance for startup circuits of high voltage power supply ICs has been developed by integrating the ESD protection device function into itself, while minimizing the increase in chip area. Since this LDMOS is connected to the startup pin, which is a product pin, it enhances the ESD robustness of the product and contributes significantly to the realization of safer and more reliable high-voltage power supply IC products. In this paper, we report on the features and advantages of two new structures (dual zone and ring zone) of high-function LDMOS for startup circuits that we have developed.

1. Introduction

We offer a lineup of high voltage power supply ICs up to 1,200V that can be used in a variety of industrial applications. In addition, the power supply circuit has been downsized by incorporating a startup circuit, to meet the demand for smaller products.

The startup circuit uses a startup device that integrates a high-voltage Nch LDMOS and a JFET (hereafter, LDMOS for startup circuits), and its drain electrode is connected to the startup pin. Since this startup pin is taken off as a product pin, increasing the ESD (electrostatic discharge) robustness of the startup pin will lead to safer and more reliable products.

Generally, ESD robustness is increased by introducing dedicated ESD protection devices. However, in high voltage power supply ICs, the ESD protection device also requires a large area in order to maintain high voltage characteristics, resulting in an increase in chip area and cost.

Our development work, summarized here, has focused on the LDMOS for startup circuits connected to the startup pin, and has developed a new structure that achieves high tolerance without increasing the chip area, by adding an ESD protection device function to the LDMOS itself.

2. High Performance LDMOS for Startup Circuits

2.1. Development Concept

In this development, the ESD protection device function is built in by forming an ESD protection area in the LDMOS area, and the LDMOS itself for startup circuits is designed to have high tolerance. The ESD protection area uses a structure that promotes parasitic NPN operation, and is provided in parallel with the LDMOS. Figure 1 shows its equivalent circuit. In the event of ESD, the parasitic NPN promotion structure turns on preferentially in the ESD protection area immediately after breakdown and discharges to the GND, thereby protecting the LDMOS and internal circuits from damage.

In this study, two types of structures, dual zone type and ring zone type, were developed based on the arrangement of this ESD protection areas.

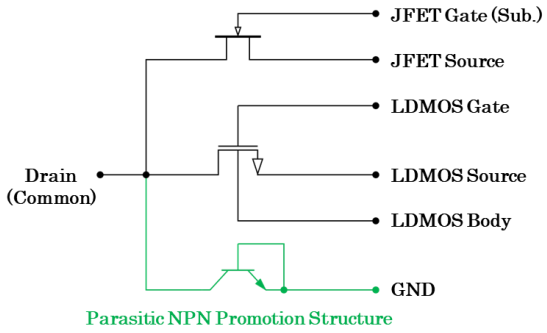

Figure 1: Equivalent Circuit of a High Performance LDMOS for Startup Circuits

2.2. Conventional Type

First of all, the conventional structure of the LDMOS for startup circuits, which is the basis of this development, is described. Figure 2 shows the device schematic of the conventional structure. As mentioned earlier, this device integrates a high voltage Nch LDMOS and a JFET, with the LDMOS area formed in a ring shape around the entire

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circumference, and a JFET area formed in part of the outer area.

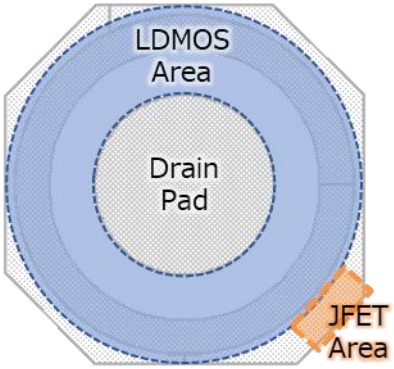


Figure 2: Schematic of a Conventional LDMOS Device

Figure 3 shows the cross-section structural diagram of the LDMOS and JFET areas. LDMOS uses a RESURF structure in the drain drift layer and an MFFP (Multiple Floating Field Plate) , which contributes to stabilization of the surface potential, to achieve high voltage characteristics. The JFET consists of an N-type layer extended from the drain drift layer in the P-type substrate, which is pinched off by a depletion layer extending from the PN junction into the N-type layer as the drain voltage rises.

Since this development is a structural development of the LDMOS area, we will focus only on the LDMOS area below.

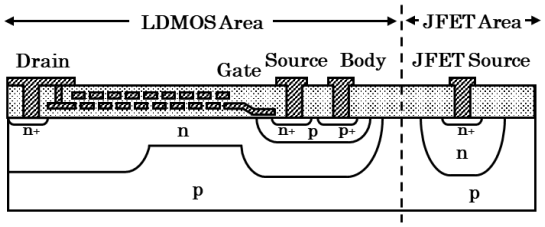


Figure 3:Cross-sectional Schematic of the LDMOS and JFET Areas of a Conventional LDMOS

2.3. Dual Zone Type

Figure 4 shows an device schematic of the dual zone structure. In the conventional structure, the entire circumference is an LDMOS area, but in the dual zone structure, the LDMOS area is bisected. This structure uses one side as LDMOS and the other side as an ESD protection area. The drain is common, but the drift layer and anode electrode of the ESD protection area are separated from the drift layer and low-voltage side electrode of the LDMOS. The LDMOS area is the same as the conventional structure in Figure 2.

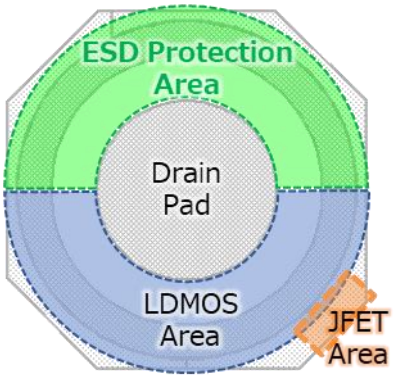


Figure 4: Schematic of a Dual Zone LDMOS Device

Figure 5 shows a cross-section structural diagram of the ESD protection area. It has the same structure as the LDMOS, except for the wiring. All pins on the low voltage side are shorted as anode electrodes and connected to GND to form the parasitic NPN promotion structure. It is possible to form an ESD protection area without additional process step.

The separation between the LDMOS area and the ESD protection area is designed according to the rated voltage between the body and substrate to prevent leakage current between the body layer of the LDMOS and the base layer of the parasitic NPN promotion structure.

Evaluation results confirmed that the ESD (HBM) tolerance was sufficiently higher than 2kV of the JEITA standard class 2. The dual zone type enables a higher tolerance without increasing the device area.

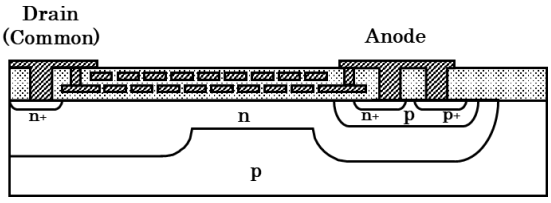


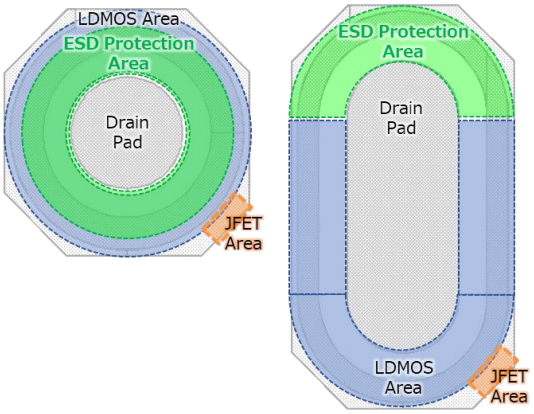
Figure 5: Cross-sectional Schematic of the ESD Protection Area of a Dual Zone Type LDMOS

2.4. Ring Zone Type

Figure 6(a) and (b) show the device schematic of the ring zone type structure and the dual zone type variant structure, respectively. The dual zone structure has succeeded in increasing ESD tolerance as described above, but the current capacity is reduced compared to the conventional structure because a portion of it is used as the ESD protection area. In other words, it cannot support startup circuits that require high current. If the gate width of the LDMOS is extended in the dual zone type to obtain the same current capacity as the

conventional type, the device area increases by 80% or more, as shown in Figure 6(b), requiring a larger chip footprint.

Therefore, we developed a ring zone type in which the ESD protection area is placed inside and the LDMOS area and ESD protection area are formed in concentric circles, as shown in Figure 6(a). By sharing the drift layer between the LDMOS area and the ESD protection area, the LDMOS can flow current using the entire circumference of the device, as in the conventional type, thus providing equivalent current capacity.



(a) Ring zone type (b) Dual zone variant

Figure 6: LDMOS Device Structure Schematics for Ring Zone and Dual Zone Variant

Figure 7 shows a cross-section structural diagram of the ring zone type structure. As with the dual zone type, the ESD protection area is formed with the same structure as the LDMOS, except for the wiring. To ensure high voltage characteristics, the distance between the drain and the anode of the ESD protection area is designed to be the same as that of the conventional type. The low-voltage side electrodes of the LDMOS are located on the outside through the separation. The separation between the LDMOS area and the ESD protection area is designed at the rated voltage between the LDMOS body and the substrate, and also a distance that does not reduce the current by narrowing the current path flowing into the LDMOS channel. Although the device area is increased compared to the conventional type, the increase is limited to 20%, which is a significant reduction in area compared to the 80% increase of the dual zone type.

As a result of the evaluation, ESD (HBM) tolerance well above 2kV was confirmed, as was the case with the dual zone type. Current capacity was confirmed to be equivalent to that of the conventional type, as shown by the *V-I* characteristics in Figure 8. The ring zone type enables both a high tolerance and high current capacity while minimizing the increase in device area.

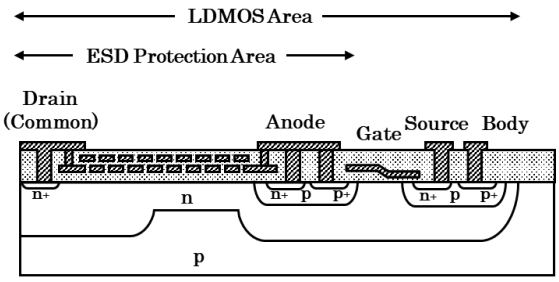


Figure 7: Cross-sectional Schematic of a Ring Zone Type LDMOS

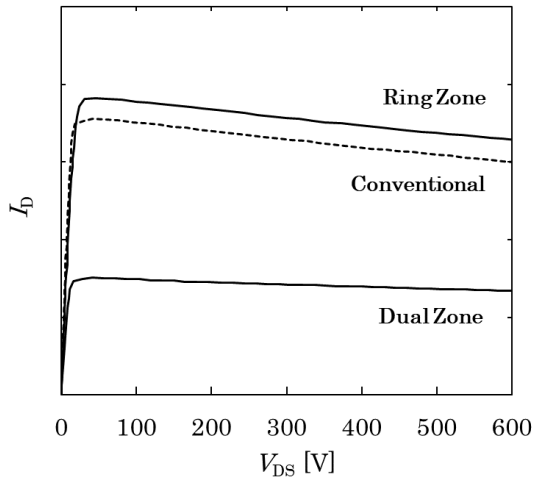


Figure 8: *V*DS-*I*D Curves for Each LDMOS Type

3. Conclusion

A new high-performance LDMOS with high ESD tolerance has been developed by integrating an ESD protection area into an LDMOS for startup circuits. The dual zone type has realized a high tolerance in the startup device itself without increasing the device area. Furthermore, the ring zone type structure minimizes the increase in device area while maintaining a high tolerance and current capacity, which is a challenge for the dual zone type. In the future, we will use these LDMOSs for startup circuits to provide safer and more reliable products, such as high voltage power supply ICs.