Development of the Motor Driver IC SIM1 Series

Kawashima Ryota* **Yamakawa Yuhei***

Abstract The SIM689xM Series offers a wide range of current ratings and is used in inverter-driven white goods. It is assumed that white goods in general will shift to inverters worldwide to promote energy conservation. The market demands a more stable supply and improved quality from this versatile series.

The new SIM1 Series meets these market requirements by adopting the next-generation MIC process to shorten lead time, adding H side OCP (overcurrent protection) to prevent secondary breakdowns, and adding an ESD protection element between LS (low-side power IGBT emitter) and COM (common) to avoid electrostatic breakdown risks during set assembly. In addition, the loss characteristics of some ratings of IGBT products have been optimized and reduced to meet the driving conditions of market applications, thereby broadening the range of applications in which they can be used.

1. Introduction

In recent years, inverter technology, which achieves energy savings, has been advancing in the white goods market, and the need for motor driver ICs has expanded accordingly.

Among our existing motor driver IC products, the SIM689xM series is available in a wide range of ratings from 2A to 10A, and is used in a wide variety of applications. Therefore, as the demand for motor driver ICs increases worldwide in the future, a more stable supply will be required.

Some of the regions where inverter-based products will be newly popularized in the future have poor power supply conditions, and overvoltage due to power supply voltage fluctuations may occur in some of those regions. When overvoltage breakdown occurs, there is a risk of secondary breakdowns spreading, leading to fatal breakdowns such as acoustic or package rupture. To prevent secondary destruction, both the H side and L side of the inverter arm should be able to shut down in case one of them breaks down, so that the other arm can shut down.

As inverter products become more widespread worldwide, set manufacturers are establishing factories in various regions, including emerging countries, to assemble such products in order to ensure mass production. Therefore, there is a risk of destruction by static electricity due to inadequate quality control. Sufficient ESD tolerance is required, including pins to which static electricity may be applied directly to the gates of power elements.

In addition, the existing SIM689xM series has adopted FS-IGBT, a shrink process, in the development process to date, which has expanded the ratings of the power chips that can be mounted from the previous 5A to 10A. However, this series lacks heat dissipation performance because it does not have a down-set structure, which is common for 10A products. Washing machines, which are the main application of this series, require high frequency. Therefore, the adoption of this 10A product has been limited to some small-capacity models with low drive motor current due to the limitation of allowable power dissipation. In terms of current rating, we believe that optimization of the loss characteristics will allow this 10A product to be expanded to a larger capacity model.

To solve these problems, we developed the successor SIM1 Series (Figure 1) in the same package.

DIP40
Mold Dimensions: 36.0 mm × 14.8 mm × 4.0 mm

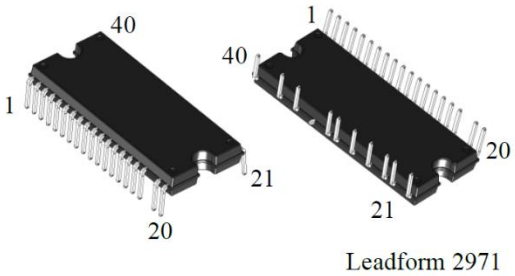

Figure 1: SIM1 Package (Full Mold)

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2. SIM1 Series Configuration

The structure of the product is the same as the conventional product, with four types of chips (power chip, H-side MIC and L-side MIC that control the power chip, and bootstrap diode for current rectification) mounted on a lead frame and molded with high thermal conductivity resin. The package size is the same as the conventional product, 14.8 mm (H) × 36.0 mm (W) × 4.0 mm (D). We have multiple production bases: two in the U.S. and two in Japan for MIC chips, five in Japan and overseas for power chips, and three in Japan, China, and Korea for assembly, to ensure a stable supply even in the event of a disaster. Figure 2 shows the internal block diagram of the SIM1 Series. As for protection functions, the same UVLO (undervoltage lockout), L-side OCP (overcurrent protection), and TSD (thermal shutdown) are provided as in the conventional products. In addition, a new H-side OCP was added. This allows the H side to be shut down even if the Low side breaks down due to overvoltage, preventing secondary destruction.

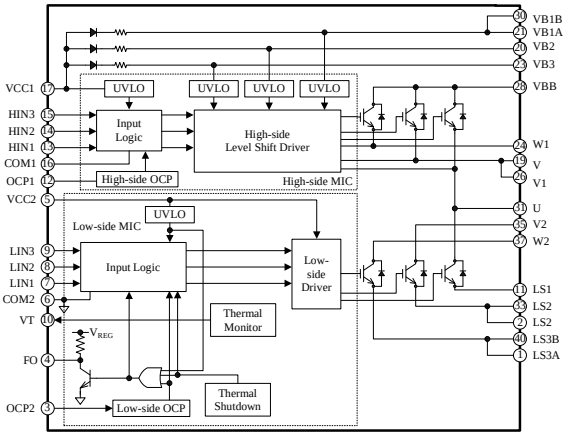

Figure 2: Internal Block Diagram of SIM1 Series

Table 1 shows the main specifications of the SIM1 Series.

In the SIM1 Series, the L-side OCP specification was not changed from the conventional SIM689xM Series, but the H side OCP specification was optimized.

The L-side MIC of the SIM1 Series is equipped with a high-precision temperature monitoring function. The MIC's excellent linearity makes temperature control easy for set manufacturers and provides a temperature monitoring function with a temperature detection accuracy of ±3°C, equivalent to that of a chip thermistor. The temperature monitor output vs temperature characteristics of the SIM1 Series are shown in Figure 3.

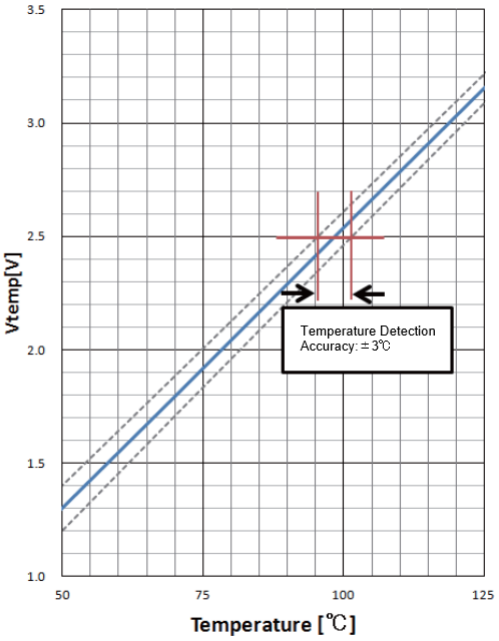

Figure 3: SIM1 Series Temperature Monitor Output vs Temperature Characteristics

Item	Symbol	Specification Value					Unit	Conditions
		SIM1-02D2M	SIM1-03A1M	SIM1-05A1M	SIM1-10F1M	SIM1-10F1A		
Output Power Element	-	SJ-MOS	IGBT				-	
Rated Breakdown Voltage	V_{CES}	600					V	
Rated Output Current	I_O	2.0	3.0	5.0	10.0	10.0	A	
IGBT Output Saturation Voltage TYP/MAX	$V_{CE(SAT)}$	-	1.8/2.3	1.75/2.2	1.65/2.1	2.05/2.5	V	I_C=I_O (Rated Output Current)
MOSFET On-resistance TYP/MAX	$R_{ds(on)}$	3.2/3.6	-	-	-	-	Ω	I_d=I_O (Rated Output Current)/2
Insulation Voltage (MIN)	V_{ISO}	1,500					Vms	Between back surface and lead terminal for AC 1minute
Terminal Spacing	P	1.778					mm	
Thermal Resistance (Junction-to-case)	$R_{(J-C)}$	3.6					°C/W	All elements operate
Thermal Resistance (Joint to Ambient)	$R_{(J-A)}$	25.0					°C/W	
Bootstrap Power Supply Undervoltage Protection	V_{UVHL}	10.0±1.0					V	
	V_{UVHH}	10.5±1.0					V	
Control Power Supply Undervoltage Protection	V_{UVLL}	11.0±1.0					V	
	V_{UVLH}	11.5±1.0					V	
Overheat Protection Operating and Releasing Temperature	T_{DH}	150°C±15°C					°C	
	T_{DL}	120°C±15°C					°C	
H-side Overcurrent Protection Trip Voltage	V_{tripH}	0.7V±10%					V	
L-side Overcurrent Protection Trip Voltage	V_{tripL}	0.5V±8%					V	
H-side Overcurrent Protection Hold Time MIN/TYP	T_{ocpH}	20/25					us	
L-side Overcurrent Protection Hold Time MIN/TYP	T_{ocpL}	5/10					ms	

Table 1: Main Specifications of the SIM1 Series

3. Development of the SIM1 Series

In developing new products, there are four main development concepts to solve the aforementioned issues.

The first is the use of a next-generation process optimized for high-voltage driver ICs to shorten lead times and ensure stable supply. At the same time, we will continue to commonalize MICs by changing the functions of wire options, as well as BCP support for chip and assembly factories.

Second, in addition to the OCP function of the L-side MIC of the existing SIM689xM series, we have added an OCP function to the H-side MIC, to enable upper and lower OCP operation. In regions where power supply conditions are unstable, even if one of the upper and lower arms is damaged by overvoltage, the other arm will always turn off instantly with OCP operation, preventing secondary destruction such as fatal acoustic or package rupture breakdowns.

The third concept is to protect the LS pin, which is connected to the application of static electricity to the gate of the power element with relatively low ESD tolerance, by connecting an ESD protection element installed in the MIC with internal wiring. This avoids the risk of electrostatic breakdown during set assembly.

The fourth concept is to reduce practical losses in 10A-rated IGBTs by optimizing the IGBT process conditions, focusing on washing machine applications where the carrier frequency is set relatively high. This will enable the adoption and deployment of large-capacity models in washing machines, which are the main application of this product.

3.1. Adoption of a next generation MIC process [(1)]

In the development of our high voltage tolerance BCD process, we have made a selling point of the fact that the process can be used for power supply IC applications, such as high voltage tolerance switching regulators, as well as high-voltage drivers, in a single process. In order to reduce element size and improve performance, development has been mainly directed toward reducing design rules, assuming an all-purpose process.

However, in the high-voltage integrated circuits (HVICs) used in IPM, there are few CMOS logic circuits that can benefit from this technology, so it does not offer much advantage. Therefore, we developed a next-generation process targeting IPMs (Intelligent Power Modules), for which supply stability is desired, by reducing epitaxial growth, the number of masks, and the number of processes, and by applying a revised (expanded) design rule. This shortened lead time and satisfied the demand for stable supply.

Table 2 shows an overview of the process and the main devices to be mounted, comparing the current process with the next-generation process. The maximum operating voltage tolerance of CMOS is set to 20V, in accordance with IPM product specifications. Considering the circuit scale of low-voltage CMOS Logic, the gate oxide film was changed from the dual configuration of the current process to a single configuration of 600Å. The CMOS sidewall formation process and silicide process, which are necessary for miniaturization, were eliminated. The guaranteed voltage for high voltage tolerance devices has also been lowered to 700V to meet specifications.

Figure 4 shows a cross-sectional schematic of the diffusion structure for each process. In the next-generation process, N-Well (NW) regions are formed by high-temperature and long-time diffusion in the P-sub. The NW diffusion layer is set at an appropriate depth to prevent P-Well (PW)-Psub punch-through. The absence of an embedded N+-type diffusion layer shortens lead time by reducing epitaxial growth and embedding processes.

The next-generation process reduces the number of wafer fabrication steps by 25% compared to the current process, thereby reducing fabrication lead time and wafer fabrication cost. Significant improvements have been achieved in both production and cost.

Table 2: Outline of Current and Next-generation Processes

	Element Item	Current	Next-generation
Process	Design rule	0.25um	0.50um
	Gate oxide thickness	180Å/800Å	600Å
	Embedded Epi	Applied	Not applied
	Sidewall	Applied	Not applied
	Salicide	Applied	Not applied
	Wiring Structure	2Poly/2Metal	
Device	CMOS	5V/7V	7V
		20V/30V	20V
	NPN	7V/20V/30V	20V/30V
	PNP	7V/20V/40V	なし
	Diode	Various	
	Resistance	Various	
	Capacitor	Various	
	高圧Nch MOS	150V/600V/900V	700V
	高圧Pch MOS	150V/600V	なし
	JFET	900V	700V

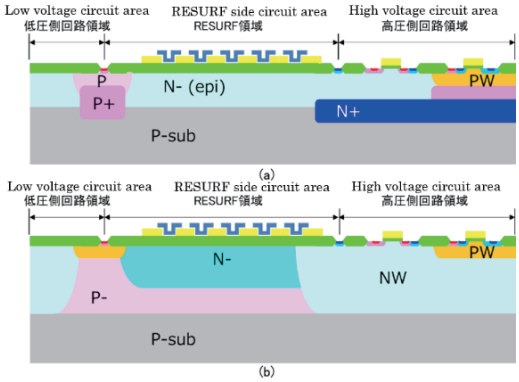

Figure 4: Cross-sectional View of Diffusion Structure
(a) Current process (b) Next-generation process

3.2. H-side OCP function to prevent secondary destruction

Figure 5 shows a circuit diagram around the control pins of SIM1. In the SIM1 Series, the OCP function and OCP pin are also added to the H-side IC. As with the L side, a shunt resistor Rs is connected to the OCP pin to enable the OCP function on the H side. This allows the gate of the H-side power element to be shut down immediately in the event that a short-circuit failure of the L-side power element due to an anomaly turns on the H side and causes an excessive through-current to flow, thereby preventing secondary breakdown of the H-side power element.

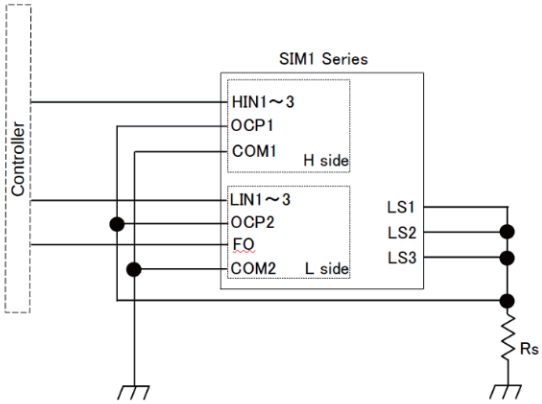

Figure 5: Circuit Diagram Around the Control Pins of SIM1

Here, due to the limitation of the number of SIM1 terminals, the FO (error signal output) pin could not be provided on the H side as shown in Figure 5. However, when the H-side OCP operates, the L-side OCP also always operates to transmit alarm signals from the FO pin to the host controller.

3.3. Optimization of 10A-rated IGBT Process Conditions

Compared to the conventional 10A product SIM6897M, the new 10A product SIM1-10F1M has reduced switching losses through revision of the FS-IGBT process conditions, resulting in reduced losses in washing machine applications driven at a relatively high carrier frequency.

As shown in Figure 6, the *V*ce (sat) – *E*off(switching OFF loss) trade-off characteristic is improved by increasing the size of the FS-IGBT, and reducing the collector dose significantly reduces *E*off while keeping the *V*ce (sat) rise to a minimum. Note that a smaller collector dose results in a smaller tail current at switching OFF (see Figure 7), and thus a smaller *E*off.

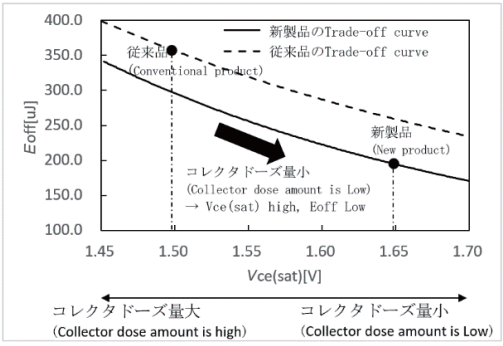

Figure 6: How to Optimize IGBT Process Conditions

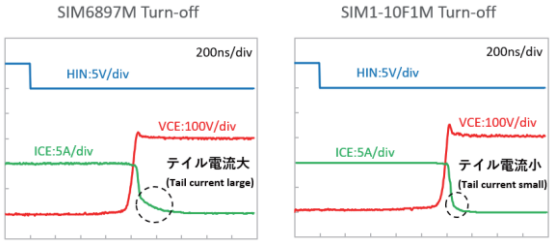

Figure 7: Comparison of SW Waveforms at Turn-off

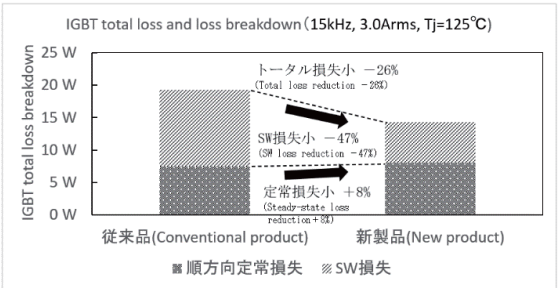

Figure 8: IGBT Total Loss and Loss Content

As shown in Figure 8, when the carrier frequency is high, the switching loss associated with the *E*off reduction decreases. As a result, the IGBT total loss was reduced by 26% compared to the conventional product. This compensates for the lack of heat dissipation performance of the SIM package and enables deployment to high-capacity models.

4. Conclusion

The adoption of the next-generation MIC process to shorten lead times and other measures has made it possible to provide the stable supply required by the growing demand for motor driver ICs in the future.

In addition, the addition of the H-side OCP function prevents the expansion of secondary breakdown after the breakdown of the one-arm power element, and the addition of an ESD protection element between LS and COM avoids the risk of electrostatic breakdown during set assembly. These changes result in a significant improvement in quality over the previous SIM689xM Series, and enable safe use in various regions.

Furthermore, by reducing switching losses, the SIM1 Series has been able to expand its application area beyond that of conventional products by reducing losses through optimization of IGBT process conditions, even in the case of washing machine applications where the carrier frequency is relatively high.

In the future, we will consider improving heat dissipation by adopting a down-set structure, etc., to further expand the area of use.

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Development of BlueFRD1 for Low-noise FRD

Yuya Kambayashi*

Abstract In today's power device market, where efficient power utilization is required, energy loss reduction by fast recovery diodes (FRDs), which are used in a wide range of applications, is essential. Low noise is also important for general-purpose applications. We have developed BlueFRD1, a new platform FRD with low noise and excellent V_F switching-off characteristics due to its new structure.

1. Introduction

The world's electricity consumption will continue to increase in the future due to industrial development. Toward the realization of a sustainable world, power semiconductor devices used in various applications, such as white goods, electric vehicles, and industrial equipment, are required to be smaller and more efficient. Among them, fast recovery diodes (FRDs) are widely used in high-frequency rectifiers, PFC, DC/DC converters, inverters, and switching power supplies, etc., and play an important role in the effective utilization of power.

FRDs are characterized by fast reverse recovery time during switching operation and low energy loss during switching-off. However, short switching operation times are prone to noise due to ringing. This noise may also cause electromagnetic interference in surrounding circuits and equipment. Therefore, if ringing is pronounced, the FRD is rendered less practical for general-purpose applications.

In this paper, we report on the development of an FRD that combines low V_F and low energy loss during switching operation with low noise during recovery operation.

2. Features of BlueFRD1

2.1. What is BlueFRD1?

BlueFRD1 is a new-generation FRD we have developed as a new process platform with improved trade-off characteristics between V_F *and* switching-off loss (=Q_{rr}) and improved ringing generation during switching-off compared to our conventional FRDs.

2.2. Features of BlueFRD1

Figure 1 shows a schematic diagram of the structure of our conventional FRD and BlueFRD1 in this development.

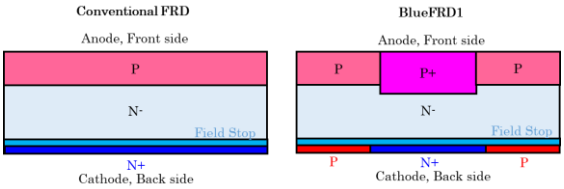

Figure 1: FRD Structure of Our Conventional and Newly-developed Products

The conventional structure is a basic vertical structure diode, consisting of a front anode, back cathode, and field stop layer on an N-layer substrate. In general, thinner N-layers are effective in improving energy loss during switching-off of FRDs. However, simply making the N-layer thinner means that there will be fewer undepleted regions during switching-off operation. Therefore, there is a concern that sudden carrier depletion may easily occur, and noise may be generated by hard recovery. A solution to this problem is to form a P-layer on the cathode. The presence of a P-layer in the cathode provides holes during switching-off operation, reducing carrier depletion and preventing hard recovery. In other words, the thinning of the N-layer and the formation of the cathode P-layer enable both low loss and soft recovery.

However, if a P-layer is formed on the cathode, voltage tolerance degradation due to secondary breakdown is likely to occur. This is because the injection of holes from the cathode P-layer during breakdown causes conductivity modulation, which locally lowers resistance and leads to breakdown due

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to current concentration. BlueFRD1 in this development aims to form a deep anode P-layer (Deep P) in the surface active region and to use the deepest Deep P-layer in the anode diffusion layer as a breakpoint. By installing multiple such Deep P-layers in the active area, the breakdown points are distributed and the occurrence of breakdowns due to localized concentration of current is suppressed. Figure 2 shows a schematic of the current density at breakdown voltage for the basic diode structure and BlueFRD1 structure. In BlueFRD1, the breakdown point changes from the corner section to the Deep P-layer. Another feature of this development is that the positioning of the deep P-layer, the back cathode P-layer, and the N layer is aligned to prevent the secondary breakdown phenomenon from occurring. Align the planar positions of the P-layers on the front and back surfaces so that there is no cathode P-layer directly below the Deep P-layer. This prevents the supply of holes from the cathode P-layer during breakdown at the Deep P-layer.

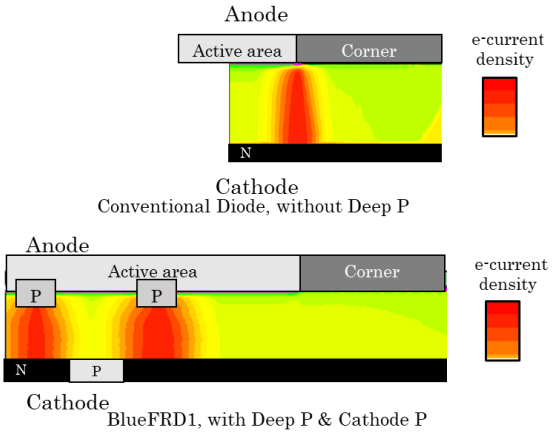

Figure 2: Breakdown Point Schematic, Conventional (top) and BlueFRD1 (bottom)

3. Development Study Details of the BlueFRD1

3.1. Thin Wafer Process Technology

The thinner wafers required for low Q_{rr} entail the risk of mechanical strength degradation and wafer breakage, so it was necessary to review the entire chip manufacturing equipment and manufacturing process, starting from the conventional FRD manufacturing line. A process step to form a P-layer on the backside cathode was also required. We applied our proven thin wafer process technology as a process to stably realize the above [(1), (2), (3)].

3.2. Examination of the BlueFRD1 Structure

In the BlueFRD1 product developed this time, 650V, 50A, the rating for air conditioner PFC applications, was set as the target index. One of the features of the BlueFRD1 structure mentioned earlier is that a Deep P-layer is formed so that it overlaps the cathode N_+ layer. The depth of this Deep P-layer was verified by simulation and the results are shown in Figure 3.

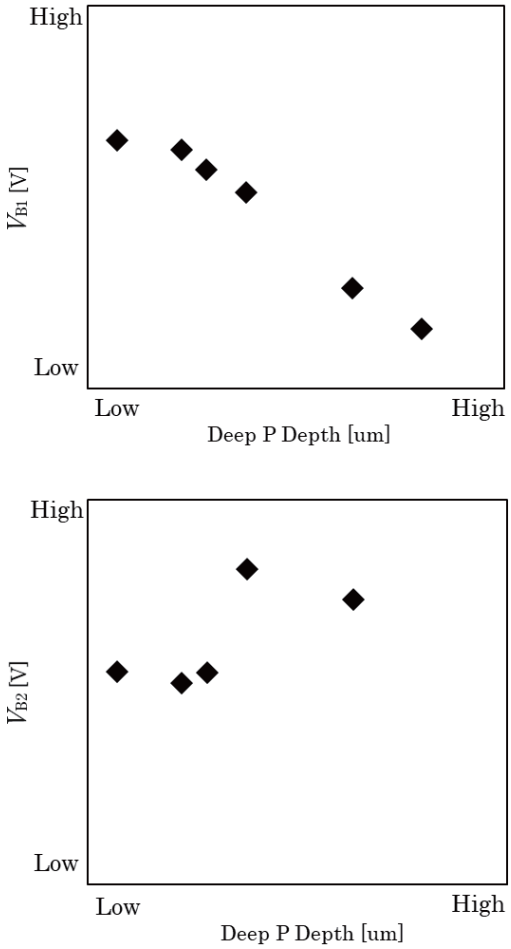

Figure 3: Simulation of Deep P Depth and Voltage Tolerance, Primary Breakdown (top), and Secondary Breakdown (bottom)

The normal static voltage tolerance is V_{B1} for the primary breakdown and V_{B2} for the voltage at which the secondary breakdown occurs. The deeper the Deep P-layer, the closer the distance between the anode and the cathode, and the thinner the drift N-layer, and so the smaller the primary breakdown voltage V_{B1}. However, if Deep P is deep, it is possible to increase the secondary breakdown voltage in line with the design aims. The reason for this is explained by the results from the simulation of hole current density at the depth of Deep P in Figure 4. In conventional diode structures with only anode surfaces, the Hall current density at breakdown is equal

everywhere in the transverse direction at a given depth. During breakdown, electrons move to the cathode side. In the upper part of the cathode P-layer area, electrons move laterally toward the cathode N layer, which has a low barrier. When the voltage drop due to this lateral shift exceeds the barrier, the PN junction is turned on and holes are injected, facilitating secondary breakdown. On the other hand, the deeper the Deep P-layer is, the more electrons flow into the cathode N immediately below it, because the current is concentrated in the Deep P. Therefore, hole injection from the cathode P-layer can be suppressed. As a result, the secondary breakdown voltage can be increased.

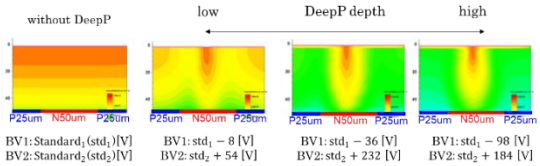

Figure 4: Current Density Simulation at Breakdown

4. Evaluation of the Development of BlueFRD1

4.1. Breakdown Evaluation of BlueFRD1

In Chapter 2, BlueFRD1 was described as being characterized by making secondary breakdown less likely to occur. However, it is difficult to accurately monitor the secondary breakdown voltage as the breakdown current is increased. Therefore, we checked whether avalanche tolerance could be improved in the Unclamped Inductive Switching (UIS) test (Figure 5). The test evaluation samples were the BlueFRD1 development product and a sample with the same chip size and thickness as BlueFRD1, but with only an N-layer for the cathode and with or without a deep P-layer. When the tolerance of the evaluation sample (2), which has a basic diode structure with no Deep P-layer and only an N layer for the cathode, is set to 1, the tolerance of the evaluation sample (1) with the BlueFRD1 structure was increased by approximately 2.8 times. On the other hand, sample (3) with a deep P-layer and only a cathode N increased by only about 1.5 times. Aligning the Deep P-layer with the P-layer of the cathode in addition to forming it is effective in improving avalanche tolerance.

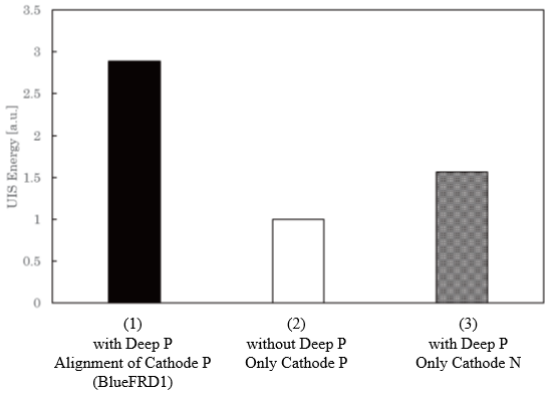

Figure 5: UIS Test Results

4.2. BlueFRD1 Switching-off Characteristics

The V_F-Q_{rr} trade-off characteristics of the developed BlueFRD1 and the conventional product are shown in Figure 6, and the switching-off waveforms are shown in Figure 7.

The conditions under which the switching-off characteristics were obtained in the RRSOA (Reverse Recovery Safe Operating Area) test were: 650V-rated IGBTs on the high side, collector-emitter voltage V_{CE} = 400V, collector current I_C = 50A, gate voltage V_{GE} = +15V/0V, and temperature Ta = 25°C.

Figure 6 shows that BlueFRD1 has improved the V_F-Q_{rr} trade-off curve toward smaller values than the conventional product. In other words, energy loss during switching-off was reduced. Figure 7 also shows that ringing, which had appeared in the conventional product during recovery operations, was reduced in BlueFRD1.

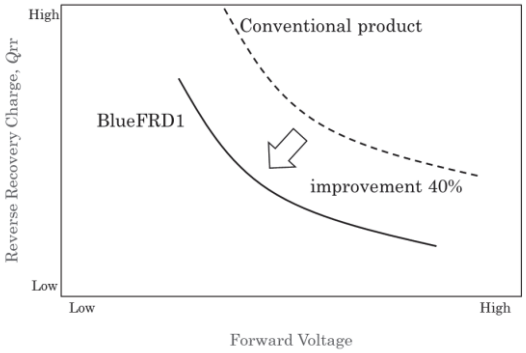

Figure 6: V_F-Q_{rr} Trade Characteristics

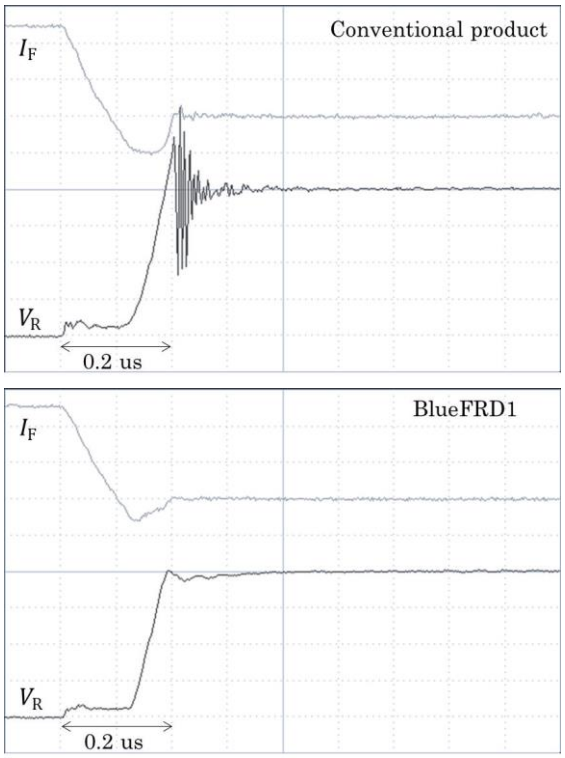

Figure 7: Switching-off Waveforms, Conventional (top) and BlueFRD1 (bottom)

5. Conclusion

By reducing the wafer thickness and optimizing the structure of the diffusion layers on the front and back surfaces, we have developed the BlueFRD1 to have lower energy loss during switching operation and lower noise than conventional products.

BlueFRD1 product development is currently underway. We will promote the technological development of a new generation of FRDs to meet applications that require even lower V_F, higher tolerance, and other properties. And, through responding to the demands of the market, we contribute to the realization of a sustainable world.

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Development of Novel LDMOS with ESD Robustness for Start-up Circuits

Naoto Fujita*

Abstract A new LDMOS (Lateral Double-diffused MOSFET) with high ESD tolerance for startup circuits of high voltage power supply ICs has been developed by integrating the ESD protection device function into itself, while minimizing the increase in chip area. Since this LDMOS is connected to the startup pin, which is a product pin, it enhances the ESD robustness of the product and contributes significantly to the realization of safer and more reliable high-voltage power supply IC products. In this paper, we report on the features and advantages of two new structures (dual zone and ring zone) of high-function LDMOS for startup circuits that we have developed.

1. Introduction

We offer a lineup of high voltage power supply ICs up to 1,200V that can be used in a variety of industrial applications. In addition, the power supply circuit has been downsized by incorporating a startup circuit, to meet the demand for smaller products.

The startup circuit uses a startup device that integrates a high-voltage Nch LDMOS and a JFET (hereafter, LDMOS for startup circuits), and its drain electrode is connected to the startup pin. Since this startup pin is taken off as a product pin, increasing the ESD (electrostatic discharge) robustness of the startup pin will lead to safer and more reliable products.

Generally, ESD robustness is increased by introducing dedicated ESD protection devices. However, in high voltage power supply ICs, the ESD protection device also requires a large area in order to maintain high voltage characteristics, resulting in an increase in chip area and cost.

Our development work, summarized here, has focused on the LDMOS for startup circuits connected to the startup pin, and has developed a new structure that achieves high tolerance without increasing the chip area, by adding an ESD protection device function to the LDMOS itself.

2. High Performance LDMOS for Startup Circuits

2.1. Development Concept

In this development, the ESD protection device function is built in by forming an ESD protection area in the LDMOS area, and the LDMOS itself for startup circuits is designed to have high tolerance. The ESD protection area uses a structure that promotes parasitic NPN operation, and is provided in parallel with the LDMOS. Figure 1 shows its equivalent circuit. In the event of ESD, the parasitic NPN promotion structure turns on preferentially in the ESD protection area immediately after breakdown and discharges to the GND, thereby protecting the LDMOS and internal circuits from damage.

In this study, two types of structures, dual zone type and ring zone type, were developed based on the arrangement of this ESD protection areas.

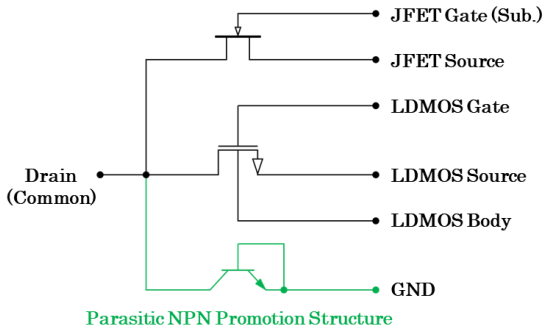

Figure 1: Equivalent Circuit of a High Performance LDMOS for Startup Circuits

2.2. Conventional Type

First of all, the conventional structure of the LDMOS for startup circuits, which is the basis of this development, is described. Figure 2 shows the device schematic of the conventional structure. As mentioned earlier, this device integrates a high voltage Nch LDMOS and a JFET, with the LDMOS area formed in a ring shape around the entire

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Process Engineering Division, Engineering Development Headquarters

circumference, and a JFET area formed in part of the outer area.

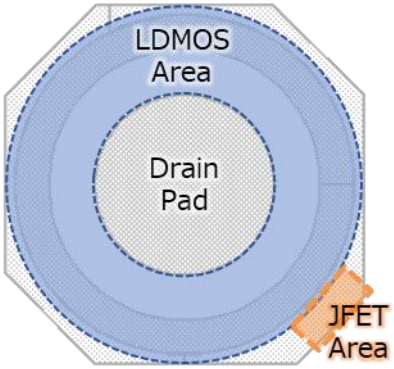


Figure 2: Schematic of a Conventional LDMOS Device

Figure 3 shows the cross-section structural diagram of the LDMOS and JFET areas. LDMOS uses a RESURF structure in the drain drift layer and an MFFP (Multiple Floating Field Plate) , which contributes to stabilization of the surface potential, to achieve high voltage characteristics. The JFET consists of an N-type layer extended from the drain drift layer in the P-type substrate, which is pinched off by a depletion layer extending from the PN junction into the N-type layer as the drain voltage rises.

Since this development is a structural development of the LDMOS area, we will focus only on the LDMOS area below.

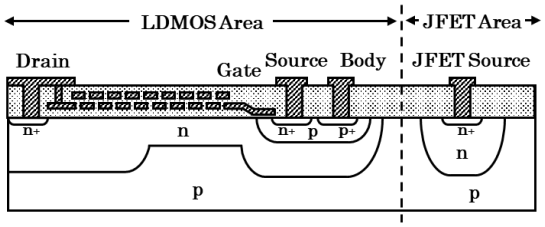


Figure 3:Cross-sectional Schematic of the LDMOS and JFET Areas of a Conventional LDMOS

2.3. Dual Zone Type

Figure 4 shows an device schematic of the dual zone structure. In the conventional structure, the entire circumference is an LDMOS area, but in the dual zone structure, the LDMOS area is bisected. This structure uses one side as LDMOS and the other side as an ESD protection area. The drain is common, but the drift layer and anode electrode of the ESD protection area are separated from the drift layer and low-voltage side electrode of the LDMOS. The LDMOS area is the same as the conventional structure in Figure 2.

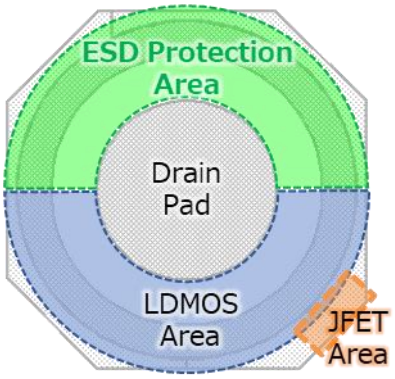


Figure 4: Schematic of a Dual Zone LDMOS Device

Figure 5 shows a cross-section structural diagram of the ESD protection area. It has the same structure as the LDMOS, except for the wiring. All pins on the low voltage side are shorted as anode electrodes and connected to GND to form the parasitic NPN promotion structure. It is possible to form an ESD protection area without additional process step.

The separation between the LDMOS area and the ESD protection area is designed according to the rated voltage between the body and substrate to prevent leakage current between the body layer of the LDMOS and the base layer of the parasitic NPN promotion structure.

Evaluation results confirmed that the ESD (HBM) tolerance was sufficiently higher than 2kV of the JEITA standard class 2. The dual zone type enables a higher tolerance without increasing the device area.

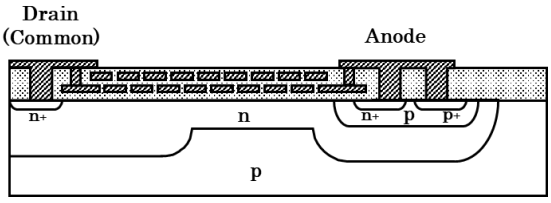


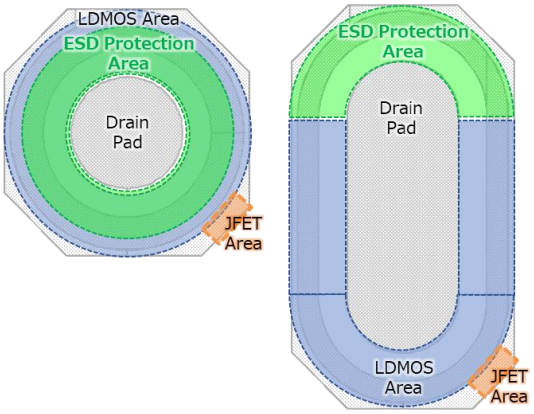
Figure 5: Cross-sectional Schematic of the ESD Protection Area of a Dual Zone Type LDMOS

2.4. Ring Zone Type

Figure 6(a) and (b) show the device schematic of the ring zone type structure and the dual zone type variant structure, respectively. The dual zone structure has succeeded in increasing ESD tolerance as described above, but the current capacity is reduced compared to the conventional structure because a portion of it is used as the ESD protection area. In other words, it cannot support startup circuits that require high current. If the gate width of the LDMOS is extended in the dual zone type to obtain the same current capacity as the

conventional type, the device area increases by 80% or more, as shown in Figure 6(b), requiring a larger chip footprint.

Therefore, we developed a ring zone type in which the ESD protection area is placed inside and the LDMOS area and ESD protection area are formed in concentric circles, as shown in Figure 6(a). By sharing the drift layer between the LDMOS area and the ESD protection area, the LDMOS can flow current using the entire circumference of the device, as in the conventional type, thus providing equivalent current capacity.



(a) Ring zone type (b) Dual zone variant

Figure 6: LDMOS Device Structure Schematics for Ring Zone and Dual Zone Variant

Figure 7 shows a cross-section structural diagram of the ring zone type structure. As with the dual zone type, the ESD protection area is formed with the same structure as the LDMOS, except for the wiring. To ensure high voltage characteristics, the distance between the drain and the anode of the ESD protection area is designed to be the same as that of the conventional type. The low-voltage side electrodes of the LDMOS are located on the outside through the separation. The separation between the LDMOS area and the ESD protection area is designed at the rated voltage between the LDMOS body and the substrate, and also a distance that does not reduce the current by narrowing the current path flowing into the LDMOS channel. Although the device area is increased compared to the conventional type, the increase is limited to 20%, which is a significant reduction in area compared to the 80% increase of the dual zone type.

As a result of the evaluation, ESD (HBM) tolerance well above 2kV was confirmed, as was the case with the dual zone type. Current capacity was confirmed to be equivalent to that of the conventional type, as shown by the *V-I* characteristics in Figure 8. The ring zone type enables both a high tolerance and high current capacity while minimizing the increase in device area.

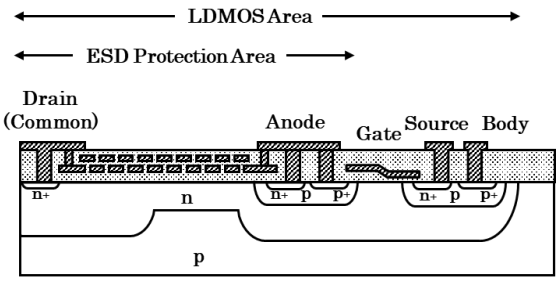


Figure 7: Cross-sectional Schematic of a Ring Zone Type LDMOS

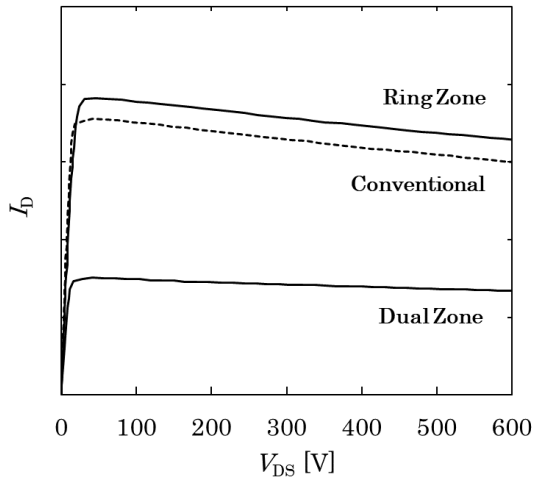


Figure 8: *V*DS-*I*D Curves for Each LDMOS Type

3. Conclusion

A new high-performance LDMOS with high ESD tolerance has been developed by integrating an ESD protection area into an LDMOS for startup circuits. The dual zone type has realized a high tolerance in the startup device itself without increasing the device area. Furthermore, the ring zone type structure minimizes the increase in device area while maintaining a high tolerance and current capacity, which is a challenge for the dual zone type. In the future, we will use these LDMOSs for startup circuits to provide safer and more reliable products, such as high voltage power supply ICs.

Development of Special LEDs Using Phosphors Emitting Near-infrared Light

Yousuke Umetsu*

Abstract Near-infrared light has been considered unnecessary in lighting and displays for it's difficulty of invisibility in human eyes. However, it is important in the fields of plant growth and spectroscopic analysis, and is considered to be applicated in such fields as LEDs. This paper covers our development of various LEDs using phosphors that emit near-infrared light.

1. Introduction

White LEDs are an achievement accomplished by the development of blue LEDs as well as by the development of phosphors. In the visible light region, white LEDs suitable for lighting and LCD backlighting have been developed by controlling the emission spectrum using phosphors emitting light from green to red. In particular, white LEDs for general lighting applications have been spread rapidly since the Great East Japan Earthquake of 2011, and luminous efficiency approached the theoretical limit.

However, from perspective of the near-infrared (NIR) region, there are still some fields where the conversion of existing lamps to LEDs is lagging behind.

As for examples of NIR emitting LEDs, there are LEDs used as sensors for remote controls for audio-visual equipment and opening and closing of automatic doors, as LEDs emitting light at around 840nm or 940nm are used for those applications. In those applications, LEDs with a small full width at half maximum (FWHM) are easy to use, but on the other hand, light sources with a broad band emission in the NIR region are needed.

OCT (optical coherence tomography) is used in ophthalmologic procedures such as glaucoma because it's nondestructive, first and also enables high-resolution observation. A light source with a broad band emission spectrum in the NIR region is needed, and studies have been conducted using blue LEDs and phosphors that emit NIR light[1].

NIR spectroscopy is widely used to sort fruit sugar content and to brand Japanese black beef branding, etc., since it can observe the optical absorption of functional groups such as O-H, C-N, and C-H and analyze various components[2]. Near-infrared spectroscopy requires a light source with a broad emission spectrum from 700 to 2,500nm, and NIR phosphors have been reported to emit NIR emission from 650 to 1,400nm[3].

The characteristics and emission spectra of NIR phosphors and LEDs are shown in Table 1 and Figure 1. According to the Table 1, the FWHM of LEDs has a narrow band of less than 50nm, whereas the FWHM of phosphors is wider than 80nm.

Table 1: Characteristics of NIR Phosphors and LEDs

	Abbreviation	composition	Emission peak	FWHM
Phosphor	CASN	$CaAlSiN_3$:Eu	650nm	90nm
	YGG	$Y_3Ga_5O_{12}$:Cr[4]	711nm	80nm
	SBO	$ScBO_3$:Cr[5]	811nm	138nm
	CCSO	$CaCuSi_4O_{10}$[6]	921nm	109nm
LED	AlGaAs	(Al,Ga)As	840nm	40nm
	GaAs	GaAs	936nm	48nm

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Power Device Development Division, Engineering Development Headquarters

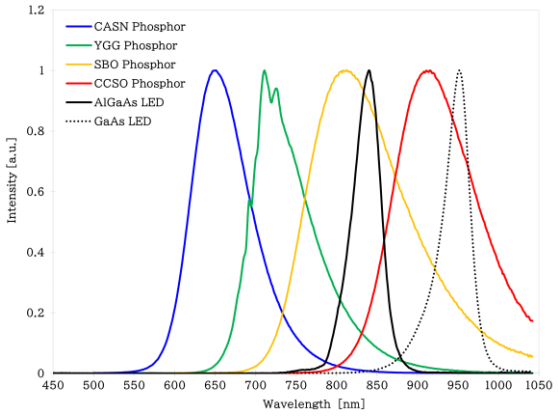

Figure 1: Emission Spectra of NIR Phosphors and LEDs

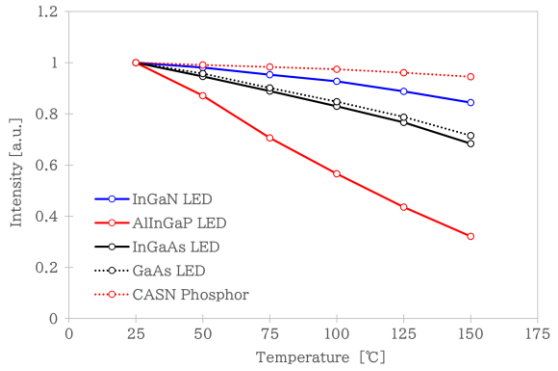

Figure 2: Temperature Dependence of Emission Intensity of LEDs and CASN Phosphor

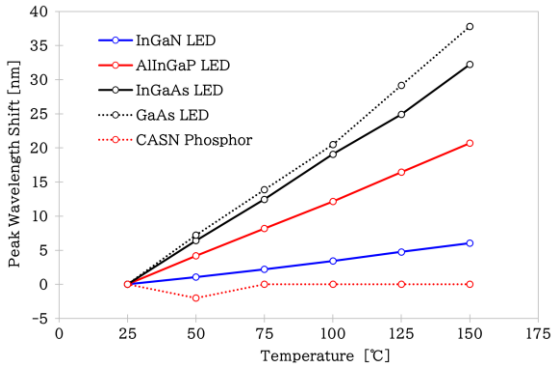

Figure 3: Temperature Dependence of Peak Wavelength Shift of LEDs and CASN Phosphor

Although NIR LEDs have a small decrease in emission intensity output by increasing temperature (Figure 2), they have a large change in emission spectra (Figure 3), which is a major issue.

Most phosphors are composed of a crystal line host matrix and activators, and it is known that the decrease in emission intensity due to temperature rise can be improved by the amount of activators[7]. There are also phosphors, such as CASN phosphors, whose emission spectra change little by increasing temperature (Figure 3).

Based on the above, we developed special LEDs using phosphors with broad band emission spectrum and excellent temperature characteristics.

2. LEDs for Plant Growth

$LiAlO_2$:Fe phosphors that emit light at around 740nm have been long-standing component of fluorescent lamps for plant growth[8]. However, $LiAlO_2$:Fe phosphors cannot be excited by blue light. Although these cannot be applied in blue LEDs.

$(Ba,Sr,Ca)_3MgSi_2O_8$:Eu,Mn phosphors can be excited by visible light. And it emits deep red light[7]. The blue luminescence from Eu^{2+} and the red luminescence from Mn^{2+} overlap sufficiently with the photosynthetic action spectrum of chlorophyll, so they are expected to be used for plant growth[9].

In addition, since the light absorption of phytochrome is located around 650nm and 730nm, LEDs with increased deep red light for plant growth have been developed[10].

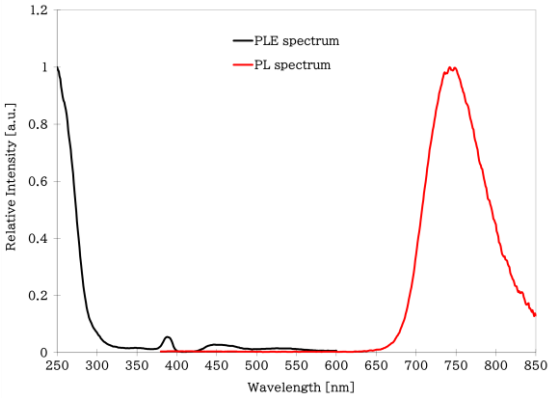

Figure 4: Photoluminescence(PL) Spectrum and Photoluminescence Excitation(PLE) Spectrum of $LiAlO_2$:Fe Phosphors

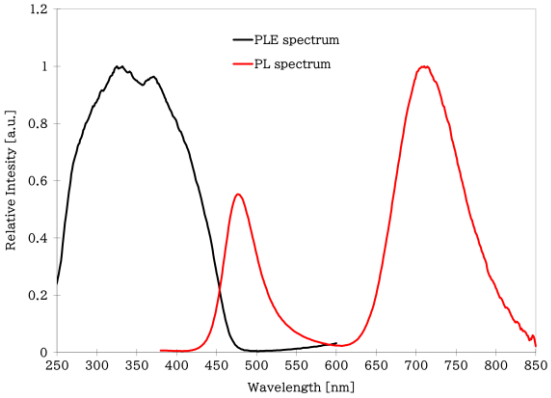

Figure 5: Photoluminescence(PL) Spectrum and Photoluminescence Excitation(PLE) Spectrum of $Ca_3MgSi_2O_8$:Eu,Mn Phosphors

Sunlight has sufficient light with wave lengths above 800nm, but artificial light such as that from fluorescent lamps or white LEDs does not.

The NIR spectroscopy described above uses absorption bands of molecular bonds. The absorption band attributed to the O-H stretching vibration is around 970nm, and the

absorption band attributed to the C-H stretching vibration is around 920nm [11]. Therefore, water molecules and sucrose molecules are thought to cause optical absorption of these NIR lights. By making water molecules and sucrose molecules oscillate, we can expect vigorous circulation of nutrients in the plant, which may promote growth.

In this study, we focused on the NIR region from 920nm to 970nm. As mentioned earlier, the emission of NIR LEDs (GaAs) around 920nm decreases due to the shift in emission to longer wavelengths as the temperature increases. For this reason, we developed a special LEDs for plant growth using phosphors that emit NIR light.

The CCSO phosphors in Table 1 were used to obtain NIR light from 920nm to 970nm. CCSO phosphors have a strong excitation band around 600nm, but cannot be excited by blue light. To obtain NIR light from CCSO phosphors, the first step would be to excite them with a red LEDs. However, as shown in Figures 2 and 3, the current AlInGaP-based red LEDs have poor temperature dependency, resulting in a decrease in light output and a change in the emission spectra.

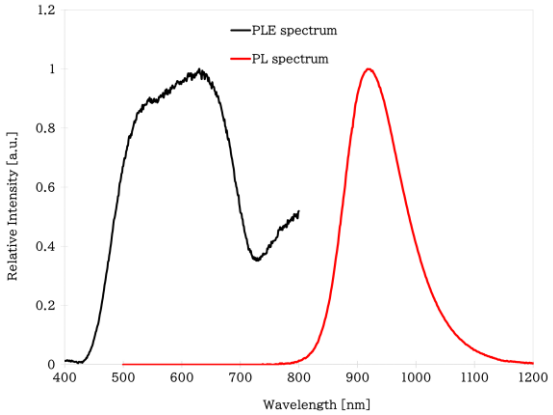

Figure 6: Photoluminescence(PL) Spectrum and Photoluminescence Excitation(PLE) Spectrum of CCSO Phosphors

Therefore, we tried to excite (Sr,Ca)$AlSiN_3$:Eu(SCASN) red phosphors with a blue LEDs, so that its red light emission would cause a CCSO phosphors to emit NIR light.

As a comparison, the emission spectrum of an LED combining a red LED and CCSO phosphor (red LED excitation), and the emission spectrum of an LED combining a blue LED, SCASN phosphor, and CCSO phosphor (blue LED excitation) that we developed, are shown below.

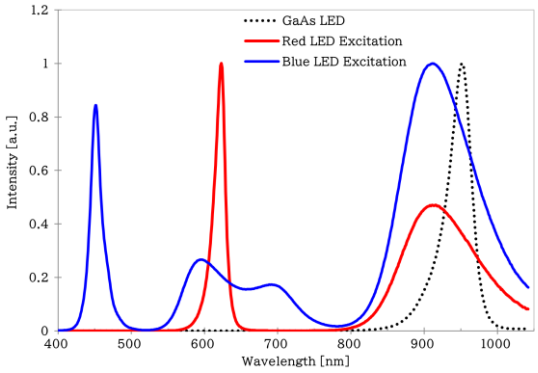

Figure 7: Emission Spectra of LEDs for Plant Growth

Since NIR light is invisible to the human eye, we used *WPE* (Wall Plug Efficiency) to compare luminous efficiency. *WPE* is expressed by the following equation.

$$WPE\ (\%) = (\text{Light output } W) / (\text{Input power } W)$$
$$= (\text{Light output } W) / \{(\text{current } A) \times (\text{voltage } V)\}$$

For measurements of emission spectra, we used CAS-140 (Instrument Systems GmbH). The *WPE* calculation was based on the sum between 380nm and 1,042nm ($\Sigma_{380\text{-}1042}$) for using this spectrometer. Visible light output is the sum between 380nm and 780nm ($\Sigma_{380\text{-}780}$), and NIR light output is the sum between 781nm and 1,042nm ($\Sigma_{781\text{-}1042}$). The results are shown in Table 2.

Table 2: Characteristics of LEDs for Plant Growth

	Current [mA]	Voltage [V]	Input Power [W]	$\Sigma_{380\text{-}780}$ [mW]	$\Sigma_{781\text{-}1042}$ [mW]	$\Sigma_{380\text{-}1042}$ [mW]	WPE [%]
Red LED Excitation	65.0	2.15	0.14	5.2	14.8	20.0	14
Blue LED Excitation	65.0	2.75	0.18	13.3	25.4	38.7	22

The NIR emission ($\Sigma_{781\text{-}1042}$) light output and *WPE* were higher for the blue LED excitation than for the red LED excitation.

The graph of the temperature dependence on the NIR light ($\Sigma_{781\text{-}1042}$) is shown in Figure 8. The blue LED excitation has less decrease in light output at high temperatures.

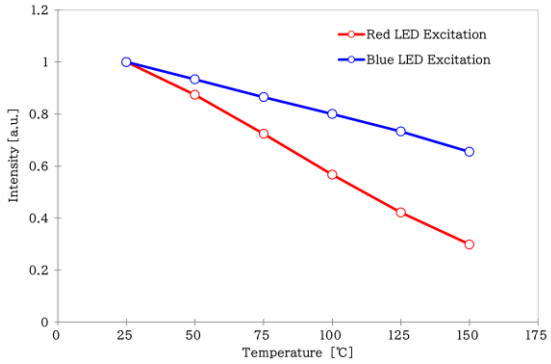

Figure 8: Temperature Dependence of LEDs for Plant Growth

From the above, it was found that the blue LED excitation is superior because it produces strong NIR luminescence and has little output decreasing even at high temperatures[12].

Although it is not known how NIR light around 920-970nm affects plant growth, it contains blue and red Lights necessary for photosynthesis, so we have high expectations for experiments using LEDs for plant growth.

3. LEDs for Halogen Lamp Replacement

Broad band lights are used for spectrophotometers. Which lights has 200nm to 1,000nm spectrum. The phosphors in Figures4 and 5, are measured by spectrophotometer manufactured by FP-6500 (JASCO Corporation). This spectrophotometer has a 150W xenon lamp, and a 20W halogen lamp valued from 350nm to 900nm, enabling measurements in the wavelength range of 220nm to 900nm. The luminescence of xenon lamps does not stabilize after using lighting time of more than 1,000 hours, so it is recommended to use less than 1,000 hours.

Light sources for spectroscopic analysis require correction of the device and measurement of calibration curve each time the lamp is replaced. In addition, LEDs are desired for reasons such as miniaturization, power saving, and minimum heat emission.

The required emission spectra differs depending on the application, but since the luminous efficiency of LEDs is low in the ultraviolet (UV) region from 220 to 350nm, the target wavelength for this work is from 360 to 1,000nm, and we have developed three types of LEDs (Types (a) to (c)) as halogen lamps replacement.

Details of the LEDs and phosphors (a) to (c) are shown in Tables 3 and 4. Emission spectra shown in Figure 9 is comparing ultra-high color rendering LED[13], and a halogen lamp.

Table 3: Configuration of LEDs

	UV Region		Visible light Region			NIR Region		
Type (a)	-	-	Blue LED	Phosphor A	Phosphor B	Phosphor C	-	-
Type (b)	-	-	Blue LED	Phosphor A	Phosphor B	Phosphor C	Phosphor D	Phosphor E
Type (c)	UV-LED	Phosphor F	Blue LED	Phosphor A	Phosphor B	Phosphor C	Phosphor D	Phosphor E

Table 4: List of Material Characteristics of Used for Type(a) to (c) LEDs

	Composition	Emission peak	
UV-LED	InGaN	363nm	UV Region
Phosphor F	$(Sr,Mg)_2P_2O_7:Eu^{2+}$	397nm	
Blue LED	InGaN	435nm	Visible light Region
Phosphor A	$Lu_3(Al,Ga)_5O_{12}:Ce^{3+}$	486nm	
Phosphor B	$(Sr,Ca)AlSiN_3:Eu^{2+}$	642nm	
Phosphor C	$ScBO_3:Cr^{3+}$	810nm	NIR Region
Phosphor D	$Y_3Ga_5O_{12}:Cr^{3+},Nd^{3+}$	878nm, 1,067nm	
Phosphor E	$Y_3Ga_5O_{12}:Cr^{3+},Yb^{3+}$	1,030nm	

Table 5: WPE of LEDs (Types (a), (b))

	Current [mA]	Voltage [V]	Input Power [W]	$\sum_{380\text{-}780}$ [mW]	$\sum_{781\text{-}1042}$ [mW]	$\sum_{380\text{-}1042}$ [mW]	WPE [%]
Ultra-high color rendering LED	32.5	5.45	0.18	91.0	0.4	91.4	51
Type (a)	65.0	2.85	0.19	42.5	9.5	52.0	28
Type (b)	65.0	2.85	0.19	26.2	14.1	40.3	22

The sharp emission spectrum above 850nm caused by phosphors D and E is due to the 4f-4f transition of rare earth ions Nd^{3+} and Yb^{3+}, and the emission peak changes extremely small compared to the NIR LED in Figure 3 because of the 4f inner shell transition.

As shown in Figure 10, phosphor D has sharp spectra around 1,067nm due to Nd^{3+} ion. Light whose peak wavelength is above 1,042nm cannot be measured by this spectrophotometer. Considering that Type (b) also emits light with wavelengths above 1,042nm, the *WPE* of Type (b) is even higher than that of Table 5.

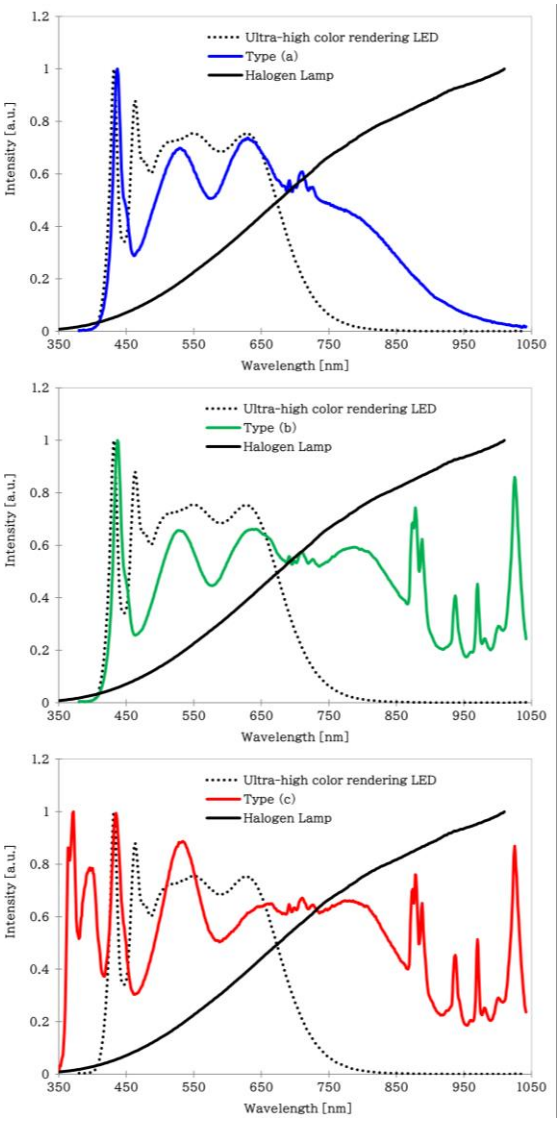

Figure 9: Emission Spectra of Type(a) to (c) LEDs Comparing Ultra-high Color Rendering LED, and Halogen Lamp

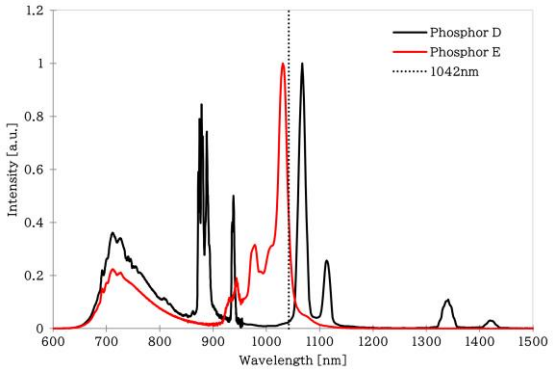

Figure 10: Photluminescence(PL) Spectra of Phosphor D and E

Although there is a concavity in the emission spectrum in Figure 9, the emission intensity is more than 10% of the main peak in the targeted wavelength region[14]. The emission spectra can be adjusted by changing type and amount of phosphors, making it possible to create LEDs that meet market needs. We expect those to be used for spectroscopic analysis.

4. LEDs for Vehicle Paint Inspection and Stage Lighting

Sunlight contains a large amount of NIR light, but fluorescent lamps and white LEDs contain almost no NIR light. Artificial lighting has been improved to reduce intensity of light from red region to NIR region, because these emission have poor visual sensitivity[15, 16, 17].

For the lighting used in painting process of automobile bodies, replacement with LEDs is not progressed, because the objects illuminated by artificial lighting are not be shown similarly comparing to ones with sunlight

To make human facial color and expression be reflected, NIR (far-red) light is necessary, although its visual sensitivity is poor. Halogen lamps are used persistently in stage lighting for it's ability to realistically reflect facial expressions.

We have now developed LEDs emphasizing NIR (far-red) light as LEDs for vehicle paint inspection and stage lighting. We used YGG phosphor, of which emission peak is 711nm, as shown in Table 1,

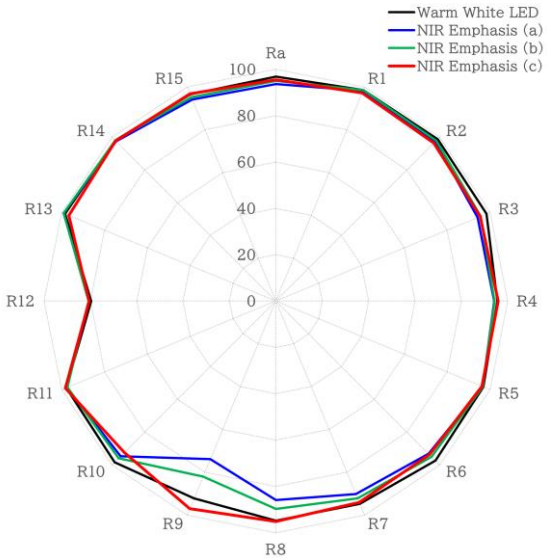

Figure 11: Color Rendering Index of LEDs for Vehicle Paint Inspection and Stage Lighting

Unlike the LEDs for replacement of halogen lamps mentioned above, light used for lighting also needs to have the same color rendering index as well as chromaticity (color

temperature, deviation), because illuminated objects are seen by human eyes.

The developed LEDs are adjusted to almost the same chromaticity (color temperature, deviation) as the warm white LEDs, and have almost the same color rendering index except for R9. (Table 6, Figure 11) R9 is an index for red, which is affected by the intensity of NIR (far-red) light. With comparing the 4 LEDs, although there are small differences in R9, there are clear differences between 4 LEDs in the intensity of NIR (far-red) light, as shown in Figure 12.

The values of spectral luminous efficiency function above 700nm are almost 0, but the spectrum multiplied 50 times shows that brightness can be sensed up to around 750nm. Therefore, objects illuminated by the developed LEDs are expected to be shown the same with those illuminated by sunlight.

For the poor visual sensitivity of NIR, the luminous efficiency of the developed LEDs was decreased by about half, while their *WPE* was decreased by about 30%. Since there is a trade-off relationship between these efficiencies and the intensity of the NIR light, it is preferable to adjust the intensity of the NIR light as necessary.

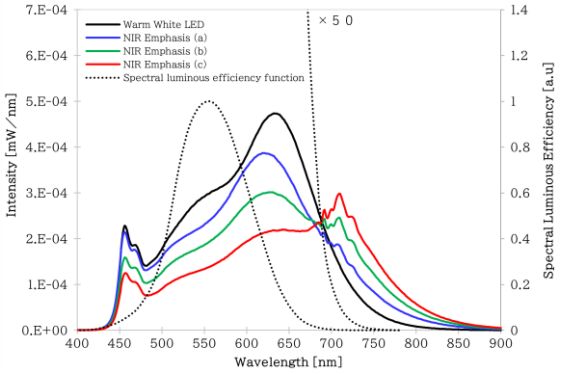

Figure 12: Emission Spectra of LEDs for Vehicle Paint Inspection and Stage Lighting

In this study, NIR light was emphasized by targeting the warm white light, but it can be applied to daylight white and other color temperatures as well. For this reason we have high expectations for LEDs for vehicle paint inspection and stage lighting.

Table 6: Characteristics of LEDs for Vehicle Paint Inspection and Stage Lighting

	Luminous Efficiency		Light Output $\sum_{380\text{-}1042}$		WPE	x	y	Color Temperature [K]	Deviation [duv]
	[lm/W]	Ratio	[mW]	Ratio					
Warm White LED	127	109%	82.3	100%.	45%	0.439	0.411	3022	0.002
NIR Emphasis (a)	108	93%	75.1	91%	41%	0.435	0.402	3006	-0.001
NIR Emphasis (b)	86	74%	68.3	83%	38%	0.437	0.405	3012	0.001
NIR Emphasis (c)	62	53%	60.5	74%	33%	0.434	0.400	3010	-0.001

5. Conclusion

Using NIR emitting phosphors, we have developed special LEDs for plant growth, spectroscopic analysis, vehicle paint inspection, and stage lighting. They have a unique emission spectrum from the NIR phosphors, and changes in their emission peak can be kept small. Since their luminous efficiency is at a practical step, we would like to move to demonstration experiment of each LEDs to confirm their usefulness.

We thank Dr. Yasushi Nanai of the National Defense Academy for his cooperation in measuring the emission and excitation spectra of NIR phosphors.

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Development of Intelligent Power Device SIP1 Series

Hiroaki Kawaguchi*

Abstract Automobiles are undergoing a period of major change, including electrification, automated driving, and connectedness, and with these changes, the E/E architecture of automobiles is undergoing a rapid shift from a functionally distributed architecture to domain-type and zone-type architectures.

In the zoned E/E architecture, it is expected that the conventional power distribution system using mechanical relays and fuses will be replaced by a power distribution system using semiconductors such as IPDs. We report on the development of the next-generation automotive IPD "SIP1 Series," which incorporates the functions required for next-generation zoned power distribution systems.

In the next-generation zoned power distribution system, the number of IPD channels in each body domain controller unit will increase, leading to an increase in the pin resources of the control MCU and an increase in the computing resources required to protect and monitor each IPD. That will in turn increase the work required for development, and increase the BOM cost due to the higher functionality of MCUs. To solve these problems, the following functions have been added:

(1) Built-in hardware wiring harness smoke emission protection function as a fuse substitute function

(2) IPD status monitoring via SPI communication and various function settings and holding functions

(3) Realization of on-resistance series lineup by changing MOS chip size

1. Introduction

In recent years, various attempts have been made to incorporate new technologies in automobiles, including electrification, automated driving, communications, and AI. In particular, a change in E/E architecture is being sought to realize automated driving. E/E architecture is a system structure that connects various components such as ECUs, sensors, and actuators installed in automobiles. E/E stands for Electrical/Electronics, and architecture means system configuration and design concept.

The transformation of E/E architecture has evolved the form of functional aggregation from functionally-distributed to domain-based. Furthermore, the transition to a zoned system is a turning point toward a system in which the onboard computer is assumed to operate the car in place of the driver, in anticipation of automated driving. Conventional power distribution systems use mechanical relays and fuses, but the high failure rate of the contact points, current consumption during operation, and ECU placement restrictions, etc., pose challenges. Therefore, it is expected that a large number of semiconductor switch devices such as IPDs will be used instead of mechanical relays and fuses in zoned E/E architectures.

IPD stands for Intelligent Power Device, which is a semiconductor switch device with built-in additional functions, such as various protection functions. The next-generation automotive IPD developed this time is equipped with a hardware-based smoking protection function for harnesses, and provides semiconductor switching functions for various loads by adjusting parameters for each wire diameter and wire type. This feature enables the product to control a large number of IPD channels while reducing the pins and computing resources of the control MCU, thereby increasing its applicability to next-generation zoned E/E architectures.

2. Product Overview

This product is a high-side switch IC (IPD) that utilizes our ZeroMOS and BCD processes to achieve low on-resistance, high robustness, and advanced control functions. The package is the HSSOP24, a small, high heat-dissipation surface-mount package, which contains two chips, an output element and a control element, in one package.

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A functional block diagram of the product is shown in Figure 1. A standard connection circuit diagram is shown in Figure 2.

The output element has multiple on-resistance lineups, allowing the selection of an on-resistance product to match the load. In addition, a temperature detection element is built in, enabling detection of overheating conditions at a point close to the heat source.

The control elements include a high-precision current detection circuit, an A/D converter, a CMOS logic control circuit, and a serial communication port. In addition, a harness smoking protection function is provided, which estimates the harness temperature from the load current and shuts off the output before smoke emission develops. Harness parameters can be flexibly set according to smoke emission characteristics, and various setting information can be retained in the internal non-volatile memory (EEPROM).

The product also has intelligent protection functions required for automotive applications, such as overvoltage/ low-voltage protection, overcurrent protection, overheat protection, reverse connection protection, and SPI communication breakdown protection (Limp Home). The operation settings and status of these protection functions can be checked via serial communication.

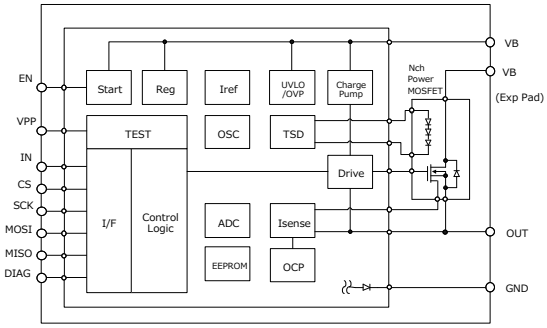

Figure 1: Functional Block Diagram

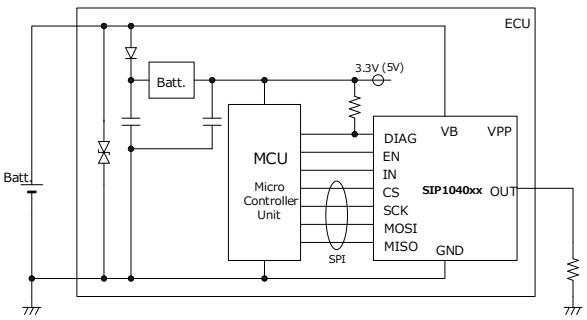

Figure 2: Standard Connection Circuit Diagram

3. Features

3.1. Wiring Harness Protection Function

As a differentiating feature, this product incorporates a harness protection smoke emission function based on hardware harness temperature estimation. This function uses a high-precision arithmetic circuit in the digital circuit to estimate the temperature of the harness from the load current and harness information as appropriate, and performs its protection operation when the preset protective temperature is reached.

Harness information and protective actions can be configured by the customer. Since these settings can be stored in EEPROM, they can be set once and the protection functions can be easily utilized. For harness information, parameters can be set according to the physical characteristics of each harness, in order to accommodate various types of harness. The main parameters that can be set for protective actions are listed below.

INEN: ON/OFF control switching via SPI communication

SR: Output slew rate setting

LHAct: SPI communication breakdown protection (Limp Home) operation setting

3.2. EEPROM (non-volatile memory)

EEPROM is mounted in the product to hold various setting information. The EEPROM can be written and read by the user via SPI communication. The various setting information written in advance is automatically read from EEPROM after power-on, eliminating the need for initial setting of various information via SPI communication. This is expected to shorten the overall system setup time and reduce the load on the ECU.

A humming code is added as an ECC (Error-Correction Code) to the data written to the EEPROM. This code enables error detection and one-bit data correction of transmitted and received data, and is expected to improve the robustness of the entire system.

3.3. Evaluation Environment for Operation Verification

A standard evaluation environment was established to support the characterization of the SIP1 Series.

(1) Evaluation board with 3 channels for our IPD
(2) Microcontroller board program for communication and IC control
(3) GUI program for controlling and monitoring ICs

Figure 3 shows the SIP1 Series evaluation board. Combining this evaluation board with a microcontroller board and connecting it to a PC via USB makes it possible to set parameters and monitor the operation of the IPD.

After setting various parameters of the wiring harness and various operation options in the GUI, the output can be controlled by pressing the On/Off button. The IPD successively calculates the estimated harness temperature from the load current and harness parameters, and can monitor the load current, estimated harness temperature, and IPD status information via SPI communication. Figure 4 shows an example of a GUI monitor waveform.

Figure 3: SIP1 Series Evaluation Board

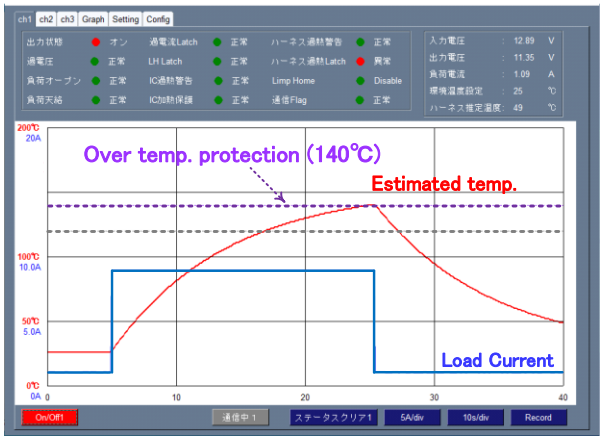

Figure 4: Example GUI Monitor Waveform

4. Design

4.1. Monolithic IC Chip

Figure 5 shows a photographic view of the chip surface of a monolithic IC. The process applied is our 8th-generation monolithic IC process, which is a BCD process combining 180nm fine CMOS and 100V voltage tolerance high-voltage DMOS. The BCD process is a process that can integrate bipolar transistors, CMOS, and low on-resistance DMOS FETs on a single chip.

CMOS logic control circuits are designed efficiently using language design (Verilog-HDL). In addition, the failure detection rate of CMOS logic control circuits must be improved to ensure high quality and reliability in automotive applications. This product achieves a high failure detection rate by introducing ATPG (Automatic Test Pattern Generator) and IDDQ testing to chip testing.

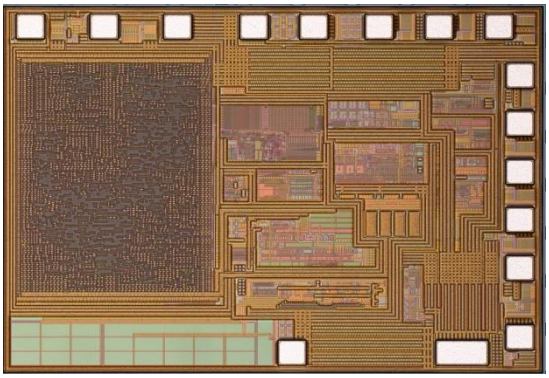

Figure 5: Photographic View of Monolithic IC Chip Surface

4.2. MOS FET

Figure 6 shows a photographic view of a MOS FET surface. The MOS FETs use our Zero MOS process with 40V voltage tolerance. The Zero MOS process has industry-leading FOM (Figure of Merit) performance, resulting in smaller size and lower on-resistance.

In addition, although reducing the wafer thickness of MOS FETs is effective in reducing the on-resistance, this entails risks in transit and risk of damage due to warpage. As a countermeasure, when grinding wafers, a process is employed in which the outermost rim of the wafer is left intact and only the inner periphery is ground to make the wafer thinner.

Figure 6: Photographic View of MOS FET Surface

4.3. Package

Figure 7 shows the internal structure of the SIP1 Series. An outline drawing is shown in Figure 8.

This product has a structure in which two chips are mounted on a metal frame that serves as a heat dissipation fin. The following on-resistance series lineups are planned, to be produced by changing the MOS FET chip size.

9.5mΩ, 7.5mΩ, 5.0mΩ, 4.0mΩ, 3.0mΩ, 2.0mΩ,
1.6mΩ, 1.3mΩ, 1.0mΩ

DAF (Die Attach Film) tape is used to connect the monolithic IC chip to the metal frame to ensure insulation, and sintered silver is used to connect the MOS FET chip to the metal frame to ensure high thermal conductivity and reliability. The connection between the chip and the external pins is made by wire bonding.

5. Conclusion

As the next-generation IPD for automotive applications, we have developed the SIP1 Series, a next-generation IPD with the following functions, in accordance with the zoned E/E architecture.

(i) Built-in hardware wiring harness smoke emission protection function as a fuse replacement function
(ii) IPD status monitoring and various function settings and holding functions via SPI communication
(iii) Realization of on-resistance series lineup by changing MOS chip size

In the future, we intend to expand the on-resistance lineup, consider further functional enhancements, and develop products that meet user needs.

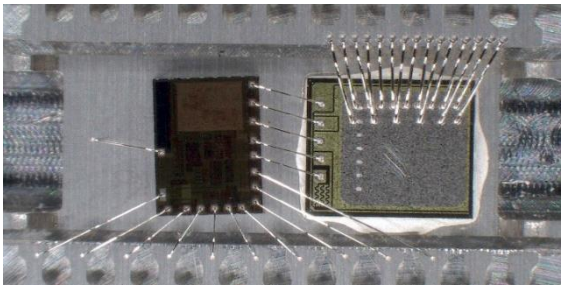

Figure 7 Internal Structure Diagram

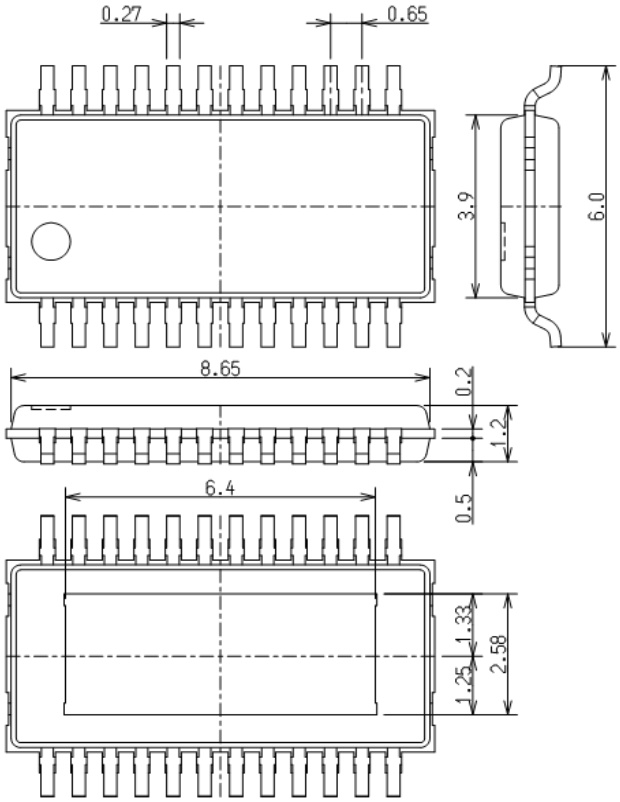

Figure 8: Outline Drawing

Development of Highly Efficient Controller of Synchronous Rectification for High-voltage Full-bridge LLC Power Supply

Kim Jungyul[*] **Koichi Ito**[*] **Kang Hanju**[**]

Abstract In the recent development of LLC power supplies for large TVs and the high-voltage battery chargers of EVs, there has been demand for smaller transformers and the elimination, or at least the size and weight reduction, of heat sinks for power devices, to make the power supplies slimmer. As a solution to this requirement, the secondary side of the power supply is configured as a full bridge to achieve high output voltage and low current. Additionally, synchronous rectification has been used in order to further reduce the temperatures of power devices, and a new synchronous rectification controller IC has been developed for efficient switching control. In this paper, we report on the proprietary high-efficiency system that we have established.

1. Introduction

In recent years, TV screens have become larger and higher resolution, and in addition, the trend toward thinner screens has progressed dramatically, compared to a few years ago. For that reason, TV manufacturers are focusing on the development of slimmer technology for power supply boards.

The biggest obstacle in slimming down the power supply board is the thickness of the transformer and heat sink. To solve this obstacle, a full-bridge configuration of the secondary side of the LLC power supply was considered, to achieve higher output voltage and lower current. The windings on the secondary side of the transformer can be reduced and the transformer can be made smaller by using a high-voltage rectifier with a full-bridge configuration on the secondary side. In addition, synchronous rectification of the high-voltage rectifier and efficient switching control can lower the heat generation temperature of the power devices and eliminate the need for a heat sink. This paper reports on the development of a new synchronous rectification controller IC for efficient switching control.

2. Product Overview

This synchronous rectification IC, developed to slim down the power supply board, is intended for the full-bridge configuration of the secondary side of the LLC power supply, as shown in Figure 1.

The full-bridge configuration reduces the transformer secondary winding to half (one winding compared to two) at the same output power, compared to the center-tapped structure shown in Figure 2.

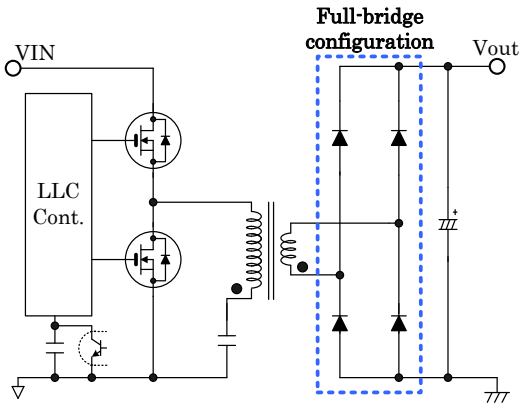

Figure 1: LLC Power Supply (Secondary Side Full-bridge Configuration)

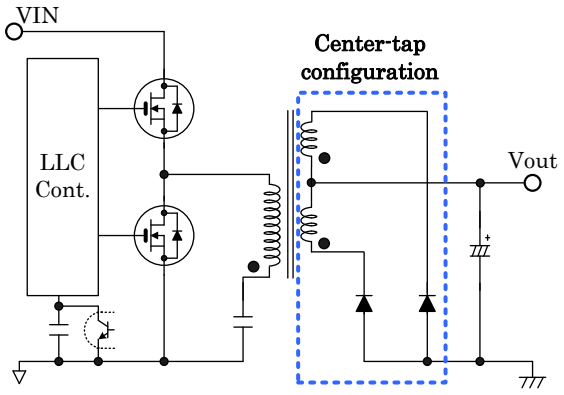

Figure 2: LLC Power Supply (Secondary Side Center-tapped Configuration)

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In addition, because there is no leakage inductance between the secondary windings and surge voltage generation is low, the voltage rating of the diodes can be less than half rectifier with a center-tap configuration. Therefore, there is no need to provide a voltage tolerance margin for the power device, compared to the center-tap configuration.

3. Secondary Side Synchronous Rectification Operation

To achieve synchronous rectification of the secondary side, the rectifier diode portion of the full bridge configuration on the secondary side in Figure 1 must be replaced with four power MOSFETs (hereinafter referred to as FETs) as shown in Figure 3, and the FETs must be driven with the timing shown in Figure 4. Q3 and Q4 on the low side shown in Figure 3 are main switches, while Q1 and Q2 on the high side are sub-switches. Efficient switching control of these four FETs reduces conduction losses and lowers the heat generation temperatures of the FETs.

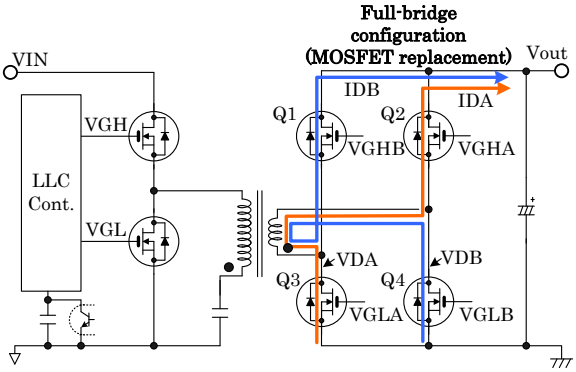

Figure 3: LLC Power Supply (Secondary side MOSFET Replacement)

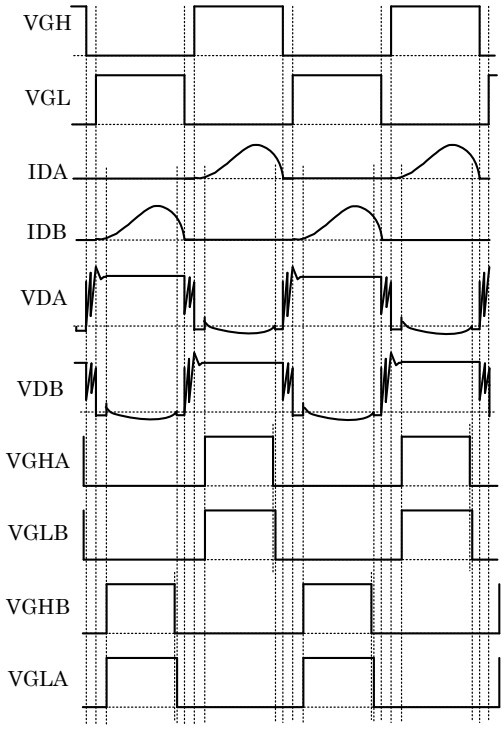

Figure 4: LLC Synchronous Rectification Operation Timing Chart

4. Control System

4.1. Block Structure of This Synchronous Rectification IC

Figure 5 shows a block diagram of this synchronous rectification IC. The voltage between the drain and source of Q3 and Q4 in Figure 3 is detected by VDA and VSA, and by VDB and VSB, as shown in Figure 6. This optimally controls the output timing of gate drive signals VGLA and VGLB for Q3 and Q4. Gate drive signals VGHA and VGHB for Q1 and Q2 are output in conjunction with VGLA and VGLB. A clock of several tens of MHz is used for internal control of the IC, and bit operations are performed at high speed based on information from one cycle earlier to control timing.

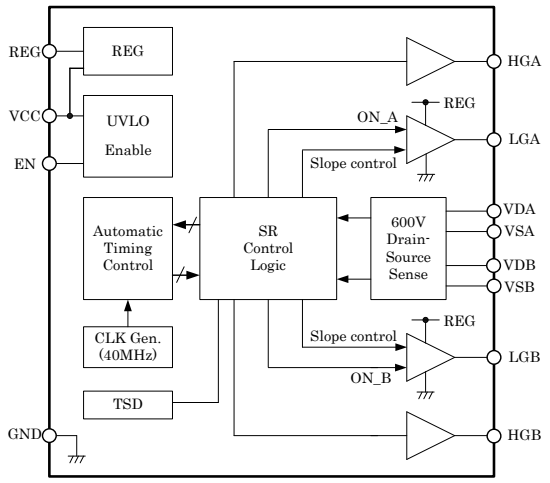

Figure 5: Block Diagram of This IC

4.2. Gate Drive Control of the Main Switches

The main switches, Q3 and Q4, perform digital drive control at the rising edge of the first half of the gate drive signal and slope control at the falling edge in the second half, as shown in Figure 6. In this IC, we have established and adopted a new driving method that combines both control types.

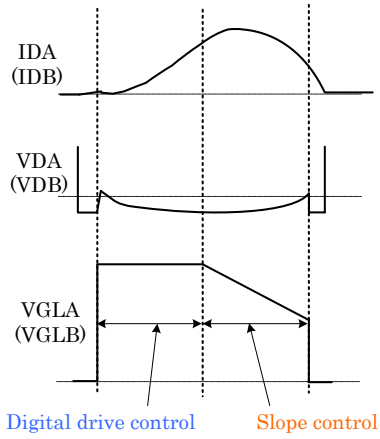

Figure 6 Gate Drive Waveform of This IC

In the case of digital drive control only, the switching speed of the gate drive signal can be increased and switching losses can be reduced. However, a large reverse voltage VL (hereinafter referred to as VL) is generated by the parasitic inductance of the FET leads shown in Figure 7 due to the sudden increase in the current change in I_{DA} (I_{DB}) just before turn-off time. This VL causes V_{DA} (or V_{DB}) to reach the off threshold early and the gate drive signal to turn off before I_{DA} at turn-off reaches 0A, as shown in Figure 8. This shortens the conduction period of the FET, which increases the conduction loss by the body diode and deteriorates efficiency.

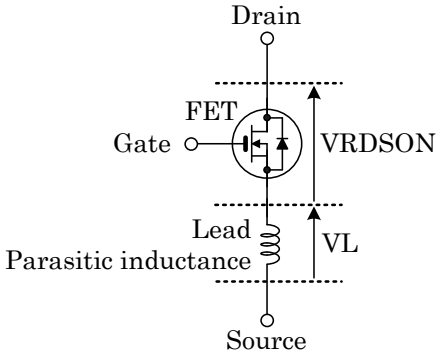

Figure 7: The Actual MOSFET

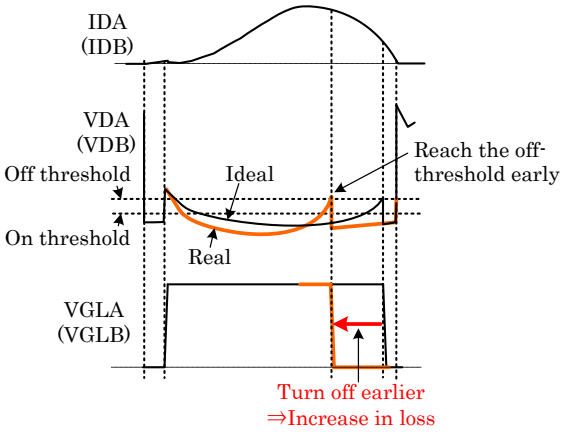

Figure 8: Ideal and Real Waveforms

To solve this problem, slope control was employed to control the on-resistance (R_{DSON}) by changing the slope of the gate drive signal during turn-off. Slope control detects the turn-off state of the gate drive signal one cycle earlier to determine the operation for the next cycle. When the gate drive signal is turned off early, the slope is controlled to be larger, and when it is turned off late, the slope is controlled to be smaller. Applying slope control to the gate drive signal prevents early turn-off by offsetting V_{RDSON}, ON voltage of FETs, and V_L induced by the parasitic inductor, shown in Figure 9. This can maximize performance as synchronous rectification.

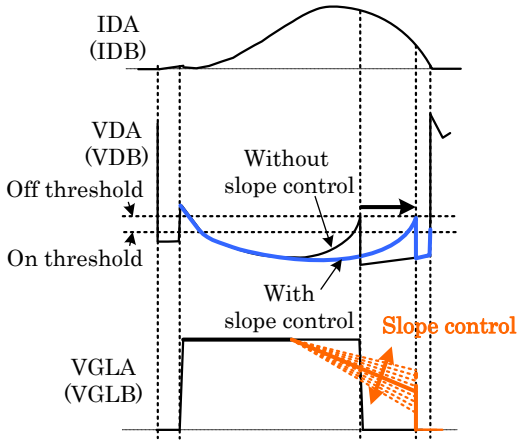

Figure 9: Effects of Slope Control

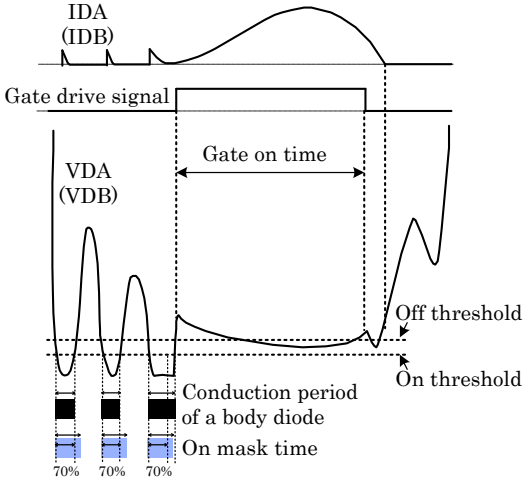

Figure 10: On-mask

4.3. On-mask Auto-adjustment Control

Ringing voltage is generated in the voltage waveform of the secondary winding when the channel of the conducting power device is switched. When the rectifier diode is replaced by an FET in synchronous rectification, the synchronous rectification IC detects that the voltage between the drain and source of the FET has reached the on threshold, and turns on the gate drive signal. For that reason, it is important to ensure that the IC controls the FETs not to malfunction due to ringing voltage.

In our previously developed synchronous rectification ICs, time setting to mask ringing voltage was done by an external pin. However, this has the disadvantage that the masking time is always the same even when the load changes, making it difficult to set the component constants [(1)]. In contrast, this IC determines the optimum on-mask time by counting the instances where the conduction time of the body diode immediately before gate turn-on, as shown in Figure 10, exceeds 70% of the on-mask time.

If the count is two or more times, the mask time for the next cycle is widened; if the count is less than two times, the mask time is narrowed. The gate drive signal turns on when the body diode conduction time is longer than the on-mask time.

This allows automatic adjustment of the mask time to obtain a gate drive signal with a wide conduction angle, thereby increasing efficiency.

5. Prototype Evaluation Results

5.1. Synchronous Rectification Operation

Figure 11 shows the operating waveforms of this synchronous rectification IC. During the period when the secondary winding current flows, the gate drive signal is optimally output by IC control.

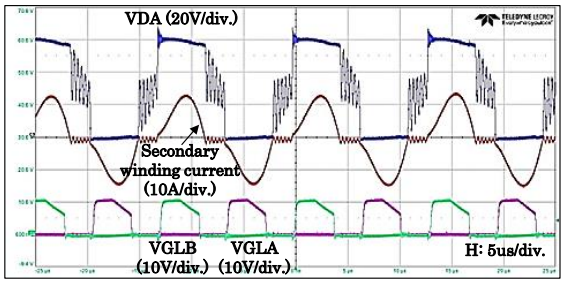

Figure 11: Synchronous Rectification Waveforms when at AC220V, Vo=60V, Io=6A Load

5.2. Characterization Results

Comparison of temperature and efficiency was made between center-tap diode rectification and synchronous rectification, using this IC in a full-bridge configuration at the same output power. The evaluation conditions are shown in Table 1.

Table 1: Evaluation Conditions

Configuration Control	Center tap Diode rectification	Full-bridge Synchronous rectification
Device	Diode	Power MOSFET
	200V/20A TO-220 10pcs (2ch/pc)	100V/8.6mΩ TO-220 4pcs
Heat-sink	120 × 50 × 7.5mm	None

Test model: 75-inch TV model board
Output power: 360W (VO=60V, IO=6A)
Aging: 2 hours

The evaluation results are shown in Table 2. In the case of diode rectification, 5 diodes (2 channel/pc) were used for each of Ach and Bch, and in the case of synchronous rectification, 2 FETs were used per channel (ch) (1 for H/S and 1 for L/S). The result is as follows, the synchronous rectification temperature averaged 54.6°C without a heat sink, demonstrating the favorable properties of synchronous rectification, on a par with diode rectification, which averaged 54.4°C with a heat sink. Good characteristics were also obtained in the efficiency and loss comparison in Figure 12.

Table 2: Evaluation Results

Configuration Control	Center tap Diode rectification			Full-bridge Synchronous rectification		
Transformer	72.0°C			70.2°C		
Heat-sink	120 × 50 × 7.5mm			None		
Device	Ach	#1	54.6°C	Ach	#1H/S	54.6°C
	Ach	#2	55.9°C		#2 L/S	55.6°C
	Ach/Bch	#3	54.0°C	Bch	#3 H/S	55.6°C
	Bch	#4	54.4°C		#4 L/S	54.6°C
	Bch	#5	53.2°C	-	-	-
	Average		54.4°C	Average		54.6°C

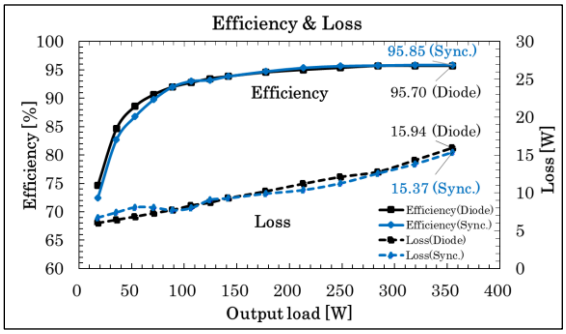

Figure 12: Efficiency and Loss Comparison

6. Conclusion

This IC was developed as a synchronous rectification IC for the secondary side of a high-voltage full-bridge LLC power supply. First, the voltage tolerance of the detection pins VDA and VDB is made high, which enables the output voltage to be high. Digital drive control and slope control were established as new gate drive controls. Prototype evaluation showed that even without a heat sink, the temperature was equivalent to that of a conventional diode configuration, and results showed that the area of the power supply board could be reduced. As a result of the above, the TV can be slimmed down by downsizing the transformer and eliminating the heat sink on the power supply board.

7. References

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Development of a Design Support Tool for Switching Power Supplies

Yuji Fukaishi*

Abstract The design calculation of switching power supplies requires knowledge of the IC used, transformer design, circuit design, and so on, and facilitating the design of power supplies is expected to have the effect of expanding opportunities for the adoption of such power supply ICs.

To increase such opportunities, we have developed “Sanken STR Pro”, a design support tool for power supply design using our ICs. Flyback converter power supply ICs, which are sold in large numbers, were selected as the target products for the tool, which is capable of automatic calculation, including peripheral circuits.

1. Introduction

In selecting a power supply IC, there are many details that need to be understood, such as the IC's supported power, pin functions, internal operation, and peripheral circuit configuration and constants. When designers who do not specialize in power supplies select a power supply IC from among power supply ICs made by multiple manufacturers, other factors besides QCD, such as the ease of prototyping and study, including the availability of adequate support, can also be considered.

Our lineup of power supply ICs includes those for LLC and PFC applications, which are used by a wide range of customers. We have developed an AC/DC converter design tool "Sanken STR Pro" using our power supply ICs for flyback converters, with the aim of expanding opportunities for the adoption of our power supply ICs.

2. Tool Philosophy

The number of configurable parameters has been minimized so that users can easily obtain calculation results. Figure 1 shows the Sanken STR Pro input screen.

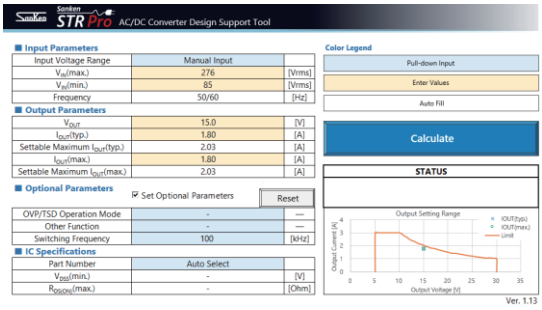

Figure 1: Sanken STR Pro Input Screen

Design results are obtained by selecting input/output specifications in the yellow cells and the desired power supply IC in the light blue cells on the input screen.

As a result of the design, the circuit diagram, bill of materials, and transformer specifications necessary for board design are output so that the fabrication of the actual machine can start immediately.

3. Internal Calculation Procedure

Design calculations within the tool are performed in the following order:

1: Transformer Calculation

2: IC Selection

3: Calculation of Peripheral Constants

In order to obtain practical results from the above calculations, knowledge gained from experience is required in addition to theoretical values, and that has conventionally been calculated and provided manually by FAEs. In addition to theoretical formulas, this tool incorporates the FAEs' accumulated knowledge and is automated using Excel and VBA, allowing users to obtain realistic results with simple operations.

The core of switching power supply design is the transformer design, and the first step is to calculate a transformer that meets the requirements based on the input/output specifications. The calculations are based on the following requirements:

- Can compatible power supply ICs be used? (IC temperature rise must be less than 50°C)

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Power Device Development Division, Engineering Development Headquarters

- Make the transformer as small as possible (calculated sequentially from EI16)
- NI margin (magnetic flux saturation must not occur)
- Winding thickness (can it actually be wound?)

The flowchart is as shown in Figure 2.

There are also multiple variable elements, and the computation of the transformer specification is complex. Therefore, for the flyback voltage and assumed efficiency, a table was prepared for the input/output conditions, and the parameters are selected.

For transformer calculations, assume the number of secondary-side windings N_s and primary-side windings Np, and the required wire diameter according to the output specifications. Under these conditions, the gap L_g shall be gradually increased from 0mm and repeated until all judgments are satisfied.

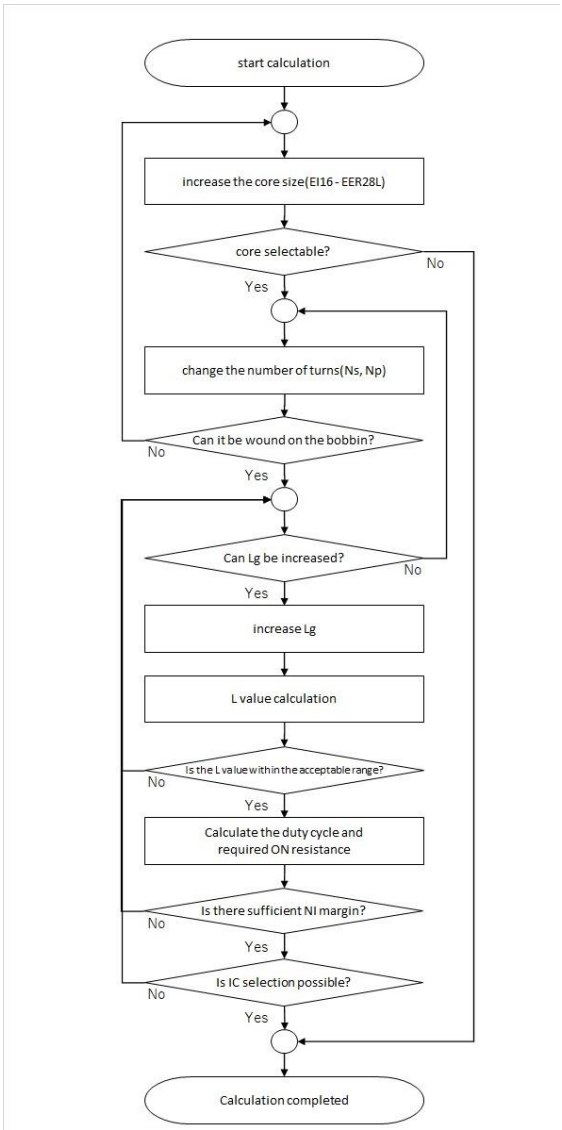

Figure 2: Transformer Calculation Decision Flowchart

The relationship between L_g, transformer inductance L, and NI margin (allowable primary side current) is shown in Figure 3. When L_g is small, the inductance L of the transformer is large, and the NI margin (allowable primary side current in Figure 3) is small. The calculation is completed if the inductance is greater than the criterion judgment value because the maximum inductance is reached under the calculation conditions at L_g, where the NI margin becomes the required value.

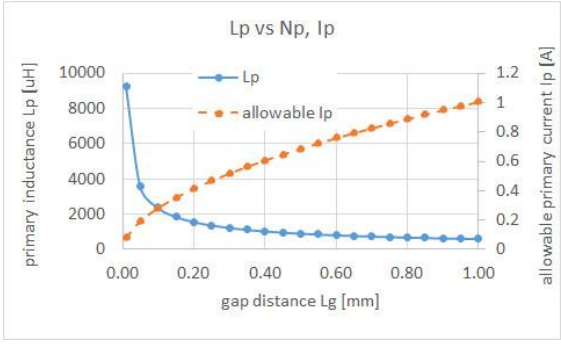

Figure 3: Relationship Between L_g and Inductance (e.g. EI16, N_p=100T)

For prototyping and mass production of transformers, it is necessary to consider the availability of components such as cores and bobbins. For that reason, this time we have received information on cores and bobbins that can be supplied via Sanshin Electric[(1)], and calculations have been made based on these drawings. Since the design is based on the bobbins that can be supplied, feasible design results can be obtained, and transformer prototype requests can be made based on the results.

Manual calculation methods require a certain amount of guesswork and may require too many calculation work-hours to adjust to the optimum value. The calculations in this tool are performed on a brute force basis for combinations of N_s and L_g, the number of secondary-side windings, to determine whether a smaller core will satisfy the required inductance. Therefore, it is possible to obtain results that are optimal within specified conditions, which would be too time-consuming and difficult to achieve with manual calculations.

In AC-DC power supply design, AC line noise suppression is also a difficult item to design for. The tool uses accumulated noise data from actual equipment to select a noise filter that matches the power specifications of the power supply. This enables the selection of appropriate noise filters, and is expected to reduce the working hours required by the user for noise countermeasures.

In addition, our power supply IC for flyback converters has a "green mode" that reduces the oscillation frequency according to the load. As shown in Figure 4, the oscillation frequency varies depending on the "green mode," making the calculation more complicated than for a fixed-frequency PWM. The tool finds the oscillation frequency corresponding to the load region to be calculated, and selects a more suitable IC.

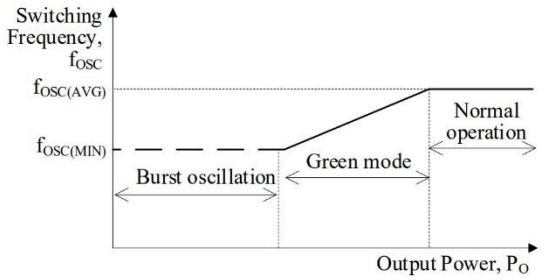

Figure 4: Green Mode Schematic

4. Results Obtained

The following can be obtained from the calculations:

1. Transformer Specifications (Figure 5)
2. Circuit Diagram (Figure 6)
3. Bill of Materials (Figure 7)

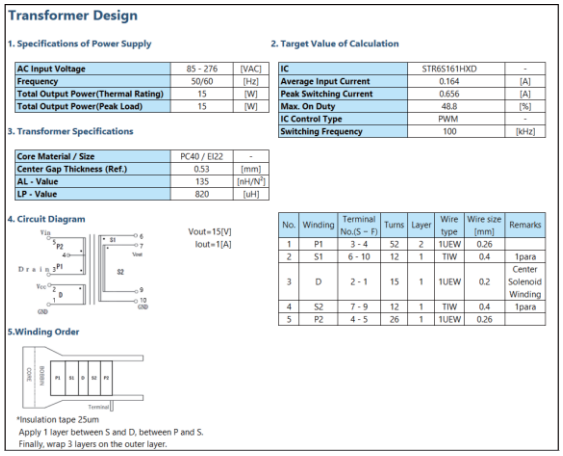

Figure 5: Transformer Specifications

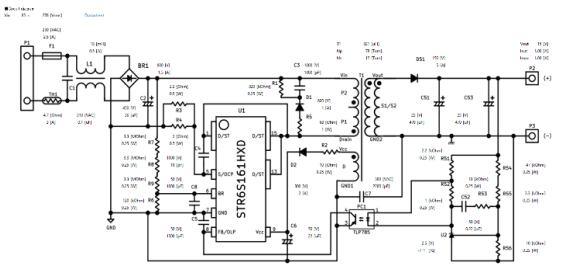

Figure 6: Circuit Diagram

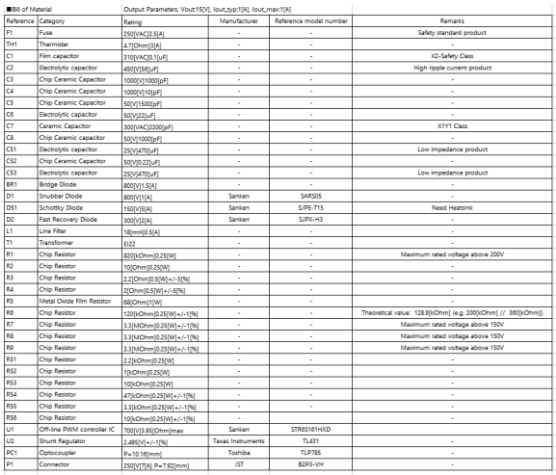

Figure 7: Bill of Materials

- The transformer specification results, which cover all parameters necessary for transformer prototyping, can be output to be submitted directly to the transformer manufacturer for prompt prototyping.
- The circuit diagram conforms to our evaluation board, making it easy to fabricate a board.
- The bill of materials includes ratings to support parts selection.

5. Validity of Results

As an AC/DC converter design tool, it is important to obtain results that can be applied to actual equipment. If the results are not practical, the main objective of improving design efficiency cannot be achieved.

As a verification of this tool, a prototype board (DE0023 [(2)(3)]) with an output of 15V/1.61A using STR 6 A153MVD was fabricated based on the output results. The results of the evaluation are shown below. (Figures 8 through 11, Table 1)

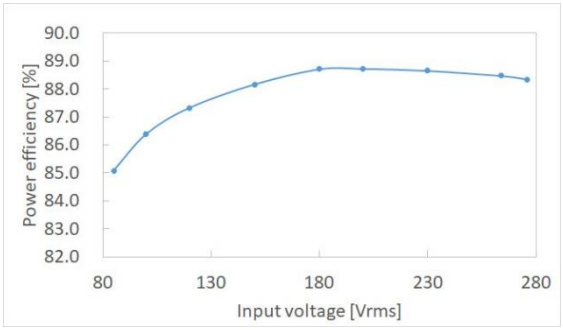

Figure 8: Input Voltage vs. Efficiency

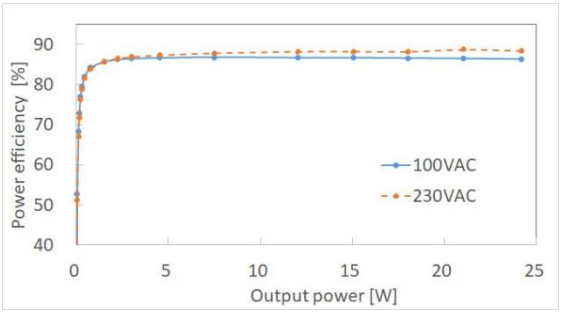

Figure 9: Output Power vs. Efficiency

The efficiency characteristics shown in Figures 8 and 9 confirm that the efficiency at rated load is at least 85%, which is sufficient performance.

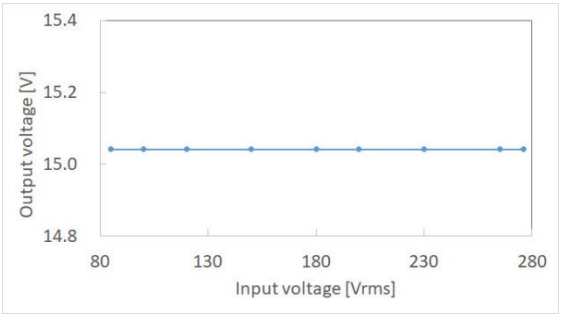

Figure 10: Line Regulation

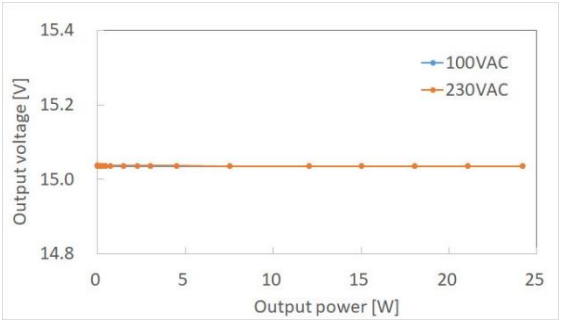

Figure 11: Load Regulation

The regulation characteristics shown in Figures 10 and 11 were also confirmed to be acceptable, with small changes in output voltage relative to input voltage and output load.

Table 1 shows the results for component temperature rise. The temperature rise of ICs and transformers was also confirmed to not exceed 100°C component temperature, compared to an ambient temperature of 50°C.

The above results confirm that the characteristics are not a problem in practical use.

Table 1: Component Temperatures

Ambient Temperature [°C]	Input Voltage [VAC]	Steady-state case temperature [°C]		
		PWM Controller IC (U1)	Secondary Rectifier Diode (D51)	Transformer (T1)
25	85	70.5	72	52.7
	276	59.8	72.4	52.7
50*	85	95.5	97	77.7
	276	84.8	97.4	77.7

*Case temperature converted from 25°C ambient temperature

6. Future Prospects

The Sanken STR Pro tool developed this time is freely available for download on our website, and has been downloaded by a wide range of people in Japan and abroad.

The current tool is for single output, but flyback converters are often used with multiple outputs, and we have received requests from users to support multiple outputs. Another point of concern for users is the temperature rise in the transformer.

Therefore, the addition of multiple outputs and transformer temperature estimation functions is under consideration for the next version.

7. Conclusion

We have developed an AC/DC converter design tool "Sanken STR Pro" that uses our STR Series of flyback converter power supply ICs. This success in simplifying the design of AC-DC power supplies required experience.

We will continue to add and update functions to make the tool even more useful.

Finally, we would like to thank everyone who helped us in the creation of the tool.

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Development of the AI-fact Image Inspection System

Soshi Oketani*

Abstract Dramatic advances in digital technology have made it pervasive in our daily lives today, and the digital literacy of each and every one of us has improved significantly. As a result, high levels of convenience are expected from the services companies provide, and they must create new value in order to meet the discerning level of demand. In addition, today, labor shortages are becoming the norm due to the declining birthrate and aging population, and we are moving from "an era in which a company chooses its employees" of long ago to "an era in which people choose their companies."

In order to cope with the drastic changes in the business environment, we are also working on the imaging (automation of functional inspection) to make our production plants into smart factories, as one of our measures to promote DX (Digital Transformation). This report describes our development of an in-house image inspection system called "AI-fact" to meet these requirements.

1.Introduction

As the use of imaging for visual inspection, a smart factory initiative, expands, there are increasing demands for image inspection systems to further improve productivity, increase the accuracy of image inspection, strengthen quality control, and reduce costs.

It has become difficult for the general-purpose image inspection systems (hereinafter referred to as "general-purpose systems") that have been introduced to date to meet these requirements. [(1)]

Sanken developed its own in-house image inspection system, AI-fact, based on the concept of responding flexibly to these requirements.

2. The Development of AI-fact

2.1. The AI-fact Development Concept

The name AI-fact was derived from the concept of replacing visual inspection with image inspection and incorporating the philosophy of smart factory. Based on the keywords "AI" (artificial intelligence), "eye", "factory", and "fact", this means that AI will play the role of eye in image inspection and realize quality control based on "fact," which is the goal of smart factory.

We set the following concepts for developing AI-fact.

(i) Enhanced traceability: By storing all images at each image inspection machine, the system can provide feedback for defect analysis, process improvement, and problem investigation [(2)].

(ii) Easy-to-use user interface: Developed for simplicity and ease of understanding in the production process

(iii) Cost reduction: Low-cost systems can be provided. Aim to reduce costs by approximately 40% from existing systems.

(iv) Reduction of over-detection rate: Aiming to reduce the over-detection rate by improving the accuracy of image inspection with functions not available in general-purpose systems.

(v) Promoting transition to SPP: Image inspection algorithm by Sanken Power-electronics Platform, user interface developed for ease of use.

(vi) Evolution: A highly scalable system that can adapt to our own ideas.

2.2. Enhanced Traceability

Imaging projects for large product size varieties are increasing, and high-resolution cameras of 20 MPixel (20 megapixel) or more are the mainstream. However, the use of a high-resolution camera increases the size of the image file and makes the saving process take longer. In addition,

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general-purpose systems could not store all images because their storage speed could not keep up with the required tact.

Therefore, we adopted parallel processing and high-speed storage for AI-fact, as shown in Figure 1. Parallel processing divides image processing into three tasks: imaging/inspection/storage, all of which are processed in parallel to reduce overall processing time.

With the introduction of high-speed storage, the change from conventional HDD to SSD has significantly reduced storage time.

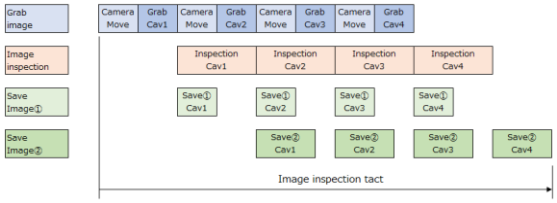

Figure 1: AI-fact Parallel Processing

Furthermore, AI-fact classifies images to be saved according to their purpose, such as for tuning or for history, and allows users to set individual file formats and destination paths for images. This allows for greater flexibility in image storage, and the ability to choose the storage method best suited to the purpose and requirements of each image.

Conventionally, images were stored on USB-HDD for each manufacturing process. As shown in Figure 2, AI-fact can transfer images stored by the image processing PCs for each process to the large storage capacity of the image server using a high-speed 10Gbps line. Images stored on the image server can be viewed within the Sanken Group network.

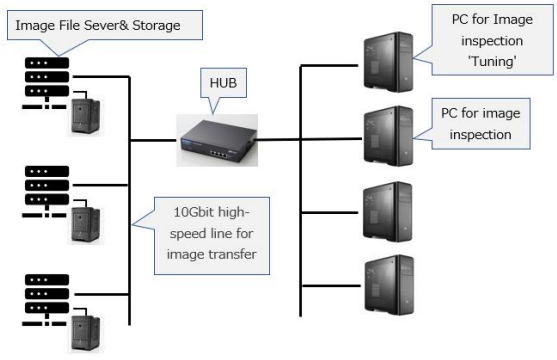

Figure 2: Imaging Device Network Configuration

2.3. User Interface

Figures 3 through 5 show the AI-fact user interface. We designed and created the Operation Screen, Area Edit Screen, and Debug Screen as the main function screens.

The Operation Screen displays the product image, lot, number of feeds, and inspection judgment.

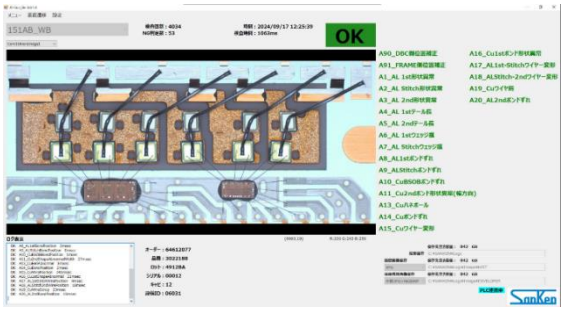

Figure 3: User Interface - Operation Screen

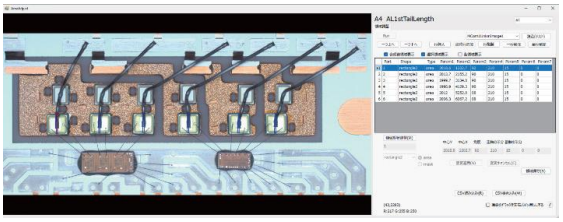

Figure 4: User Interface - Area Edit Screen

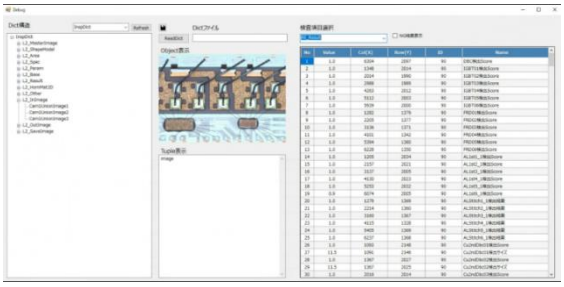

Figure 5: User Interface - Debug Screen

This screen displays flow information, such as results and number of defect judgments. The Area Edit Screen has functions for setting the inspection area, adjusting parameters, and setting threshold values. The Debug Screen can display all parameters used for image inspection, including processed images, inspection results, and detection values. Each item is classified hierarchically in a tree structure, making it easy to identify what is contained where. Each interface is simple and easy to understand, with only the necessary functions implemented.

2.4. Cost Reduction

AI-fact uses commercially available high-performance image processing software (hereinafter referred to as "high-performance image software") to achieve high-speed and high-precision image analysis.

On the software side, sophisticated image processing algorithms within the newly adopted high-performance image software have significantly reduced the processing time

required for image inspection. On the hardware side, we have had to select from a limited lineup of general-purpose systems. However, with AI-fact, a system can be constructed by combining a wide variety of inexpensive commercially available PCs and peripherals. Since image processing internally consists mainly of repetitive arithmetic operations, processing time is highly dependent on CPU performance. Since AI-fact allows users to select a commercially available PC (CPU) with specifications that meet their requirements, it can both significantly shorten processing time and reduce costs.

This improvement in processing time has other significant effects. Where two cameras were needed to cover the number of areas to be inspected and meet tact requirements, that can now be reduced to one camera. The conventional manufacturing process, in which multiple image inspection machines were used for inspection, could be consolidated into a single machine through this improvement. This has achieved significant cost savings, reduced installation space, and saved design/start-up resources. Figure 6 shows the system and equipment configuration of AI-fact.

Furthermore, the development of AI-fact has made it possible to use equipment from various manufacturers, whereas with conventional general-purpose system it was necessary to purchase an assortment of cameras and lenses from the same manufacturer. This has improved the advantages in a wide range of aspects, such as specifications, cost, and delivery time.

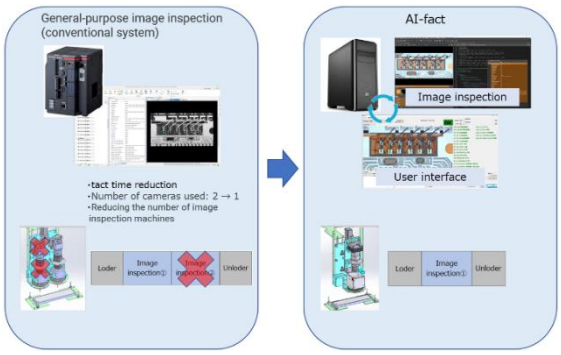

Figure 6: AI-fact System Configuration and Equipment Configuration

2.5. Over-detection Reduction

Over-detection refers to the erroneous detection of a product that has no problem as defective in image inspection. The technical challenge is to consider "missing" as a counterpart to over-detection, and to set up a balance between the two conflicting aspects.

In AI-fact, the introduction of high-performance image software enabled more advanced image processing and various shape filtering, and was effective in reducing over-detection. In addition, the simulation environment has been improved when adjusting for over-detection. In the past, the operator had to visit the production process, retrieve the USB HDD on which the images were stored, and copy the image files to a PC for the person in charge of the images to perform over-detection adjustment. This workload has been improved by AI-fact.

As shown in Figure 2, a PC for image tuning was prepared and an infrastructure was built to enable image transfer and simulation over the network. This has reduced physical losses.

When adjusting for over-detection, it is necessary to quickly identify the location of the occurrence and the trend, and make the adjustment without any backtracking. For this reason, as shown in Figure 7, we created a program to consolidate information such as enlarged images of defective locations, defect details, and image numbers corresponding to product serial numbers, into a single composite image for use in identifying the location of defects and analyzing trends. The increased efficiency of the adjustment process has reduced the resources required for over-detection reduction.

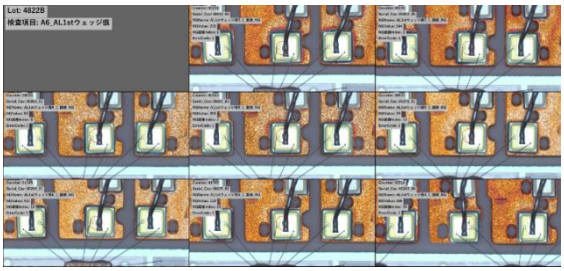

Figure 7: Composite Image of Defect Capture

2.6. Transition to SPP

The high-performance image software used in AI-fact's image processing writes program code to create inspection algorithms. AI-fact incorporates the concept of SPP and consists of an inspection program in procedure file format created for each inspection item. SPP is an initiative to review development methods and to reform design and operations based on common concepts.

As shown in Figure 8, the procedure is given a defined input and output, and the code for the parts related to this is prepared in a standardized format. Standard formats were also created for edge detection and other processes frequently used in image processing. These systems were established so that the same results can be reproduced by anyone at any time.

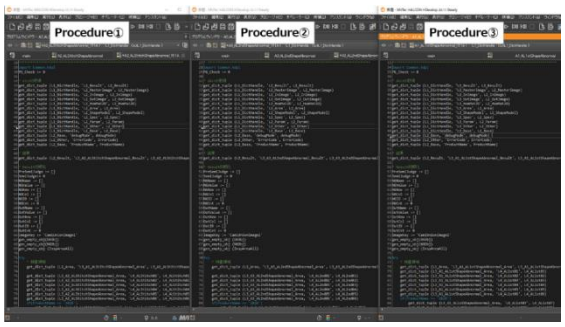

Figure 8: Program Code

2.7. Evolution

Future prospects for AI-fact include the introduction of AI (artificial intelligence) and the use of 3D images. This system can solve issues that are currently problematic with 2D images.

High-performance image software is equipped with various AI functions such as classification, segmentation, and OCR, using deep learning. By utilizing these, advanced image judgment by AI will be possible even for items that could not be identified from conventional rule-based 2D images. AI-fact is a highly scalable system that can easily incorporate these advanced technologies.

2.8. Summary of the Development of AI-fact

AI-fact development was based on six concepts. It solved issues that could not be solved with a general-purpose system, and achieved the improvements shown in Figure 9.

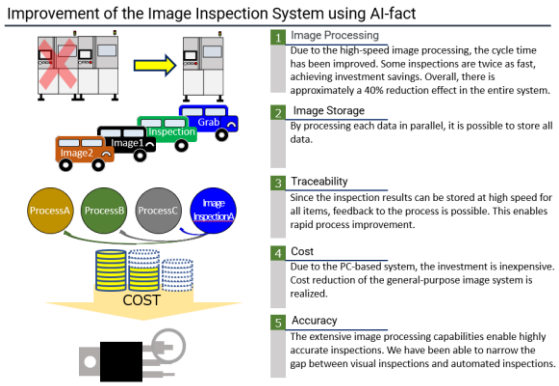

Figure 9: Improvement of Image Inspection Systems by AI-fact

3. AI-fact Deployment Record

AI-fact equipped image inspection systems machines were installed on the production lines of two of our production factories.

- Ishikawa Sanken Horimatsu Factory, Building B, SIM2 - WB Imaging Equipment (Photo 1)
- Ishikawa Sanken Horimatsu Factory, Building B, SIM2 - Exterior Imaging Equipment
- Niigata Sanken Semiconductor module processes, various imaging devices

Photo 1: Example of AI-fact Installation

4. Conclusion

The introduction of AI-fact, which was developed in line with our concept, into our factories has resulted in improved production efficiency and quality control effects which are actually beginning to be seen.

We will continue to further evolve and enhance AI-fact's functions to solve problems in production processes, and to play a role as an image inspection system in each step of activities toward the final form of the smart factory.

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(2) Niijima, Sanken Technical Report Vol.55, p46-50

Development of Equipment Manipulation System for Smart Factory Promotion

Hiroyuki Tanaka*

Abstract One of the most important items in our efforts to promote DX (Digital Transformation) in order to maintain, acquire, and strengthen corporate competitiveness in the rapidly-changing business environment of recent years has been the shift to smart factories in production factories. In order to realize automatic flow in smart factory promotion, it is essential to collect equipment parameter data, operating data, quality data, etc., automatically post them to a check sheet, and then determine whether the equipment can be operated, based on the results of the check sheet. However, for equipment that does not support IoT data collection and for some data types, these data cannot be collected due to equipment specifications. This report paper describes the construction of a production system infrastructure capable of automatic flow as an original system that can handle these requirements.

1. Introduction

In recent years, various companies have been promoting DX (Digital Transformation) to develop sustainable business by reforming their operations and corporate culture, through the use of vast amounts of data and digital technology. In order to respond to the drastic changes in the business environment, we too are promoting DX to transform our business, operations, and corporate culture through the use of data and digital technology.

As a manufacturer, the most important item in the promotion of DX is the conversion of production plants into smart factories.

We have traditionally implemented quality and productivity improvements through initiatives such as production line automation and process improvements. By utilizing new IoT (Internet of Things) technology and linking information with various systems, we will optimize processes and production in a flexible manner. This will not only further improve quality and productivity, but will also contribute to reducing in-process inventories, shortening delivery times, and improving the efficiency of indirect operations, etc., thereby increasing our market competitiveness.

2. Package Roadmap

Figure 1 shows a roadmap of packages currently being deployed or planned to be deployed until 2029.

High power density power modules are in mass production at DSK (Dalian Sanken) and NSK (Niigata Sanken), and compact high heat dissipation substrate modules are in mass production at ISK's (Ishikawa Sanken) Horimatsu Factory Building B. All of the production plants (manufacturing lines) are in the process of converting to smart factories.

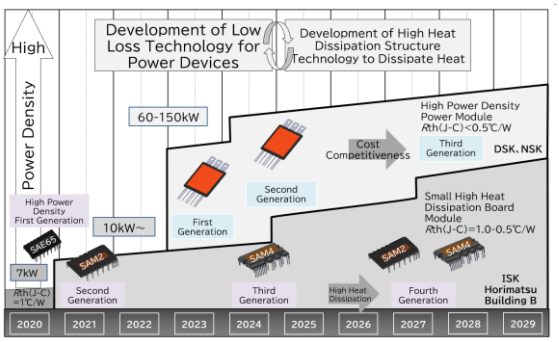

Figure 1: High Power Density Package Development Roadmap

3. Smart Factory Overview

I will give an overview of the smart factories that we are working on.

As shown in Figure 2, our smart factories are intended to reform business processes through the utilization of digital

* Smart Factory Promotion Section, Production Innovation Department Manufacturing Development Center, Manufacturing Headquarters

technology, including IT infrastructure and various types of data.

Our two main approaches are (1) production line reform and (2) business process reform. The former is aimed at quality improvement, productivity improvement, and cost reduction, through automation, imaging, and IT of production lines, which are mainly direct operations. For the latter, we will use IT data mainly for indirect operations to obtain necessary data immediately, which will lead into a PDCA cycle for indirect operations and speed up decision making.

In direct operations, various data are collected while we implement production line reforms. By utilizing the collected data in indirect operations, we are implementing drastic operational improvements. The goal is to finally achieve unprecedented production reforms through mutual cooperation.

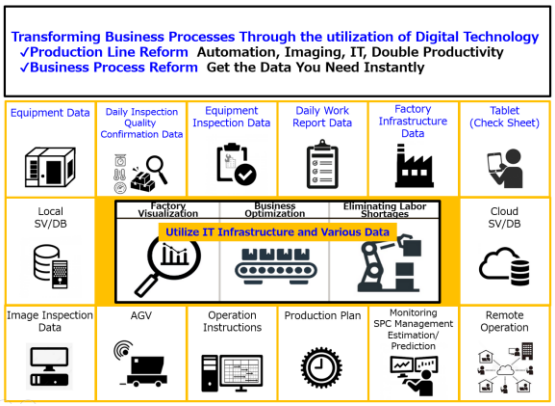

Figure 2: Smart Factory Overview

4. Smart Factory Roadmap

In promoting production plants as smart factories, we are working on the basis of smart factory 9-step activities, as shown in Table 1. The major categories are data collection, storage, and utilization.

The initial step starts with systems that can operate as stand-alone systems, and each successive step combines the systems completed in the previous step to achieve a production line that does not rely on human operators.

Smart factories will enable automatic flow, remote operation, and more efficient design using process data. For this purpose, it is essential to automatically collect various data necessary for automatic control of production lines under stable product quality, and with improved productivity.

Table 1: Smart Factory Roadmap

Deployment	Definition	Initiative Details
Step9	Big Data Deployment	Deploying Process Big Data to Other Systems (IoT) Production Line Reform, Process Reform, DX, Remote Control
Step8	Automatic Flow	LOT Abolished, Individual Piece Management Flow
Step7	Process Control	Line Control and Operation Instructions
Step6	Estimation/Prediction	Preventing Product Defects and Equipment Failures Predictive Scheduling and Feedback
Step5	Production System Collaboration	Mutual Use of Data such as Data Input/Output Processing
Step4	Automation	Automation of Parts and Product Transportation (AGV) Automation of Sensory Testing (Image)
Step3	Data Analysis Utilization	Visualization, Traceability Management, Process Improvement Visualization, New Product/Line Design, Quality Improvement
Step2	Equipment Data Collection	Database of Equipment Data Collection of SG Data Using Cube-Type Database
Step1	Paperless	Abolition of Paper Document, Database Creation, Digitization

5. Background to the Development of This System (Step8 Automatic Flow Issues)

As mentioned in the previous section, an essential item in fulfilling our objective in promoting smart factories is the automatic collection of various data necessary for automatic control of production lines.

Step 8 The desired state of automatic flow is as shown in Figure 3. It shows the flow of data from five perspectives: production facilities, quality checks, data accumulation, BI tools, and people. It is essential to automatically collect equipment parameter data, operating data, quality data, etc., automatically post them to a check sheet, determine whether the equipment can be used based on the results, and automatically control the production line.

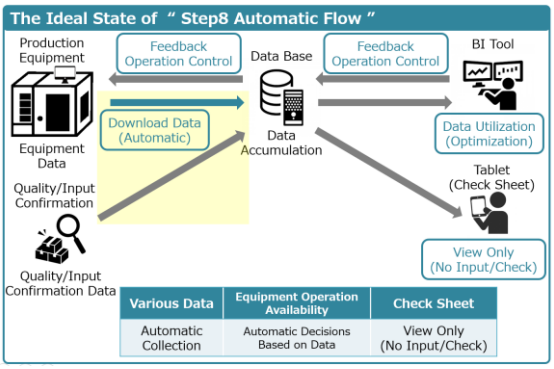

Figure 3: Step 8 Desired State of Automatic Flow

However, in its current state, as shown in Figure 4, there are production facilities and data that are not compatible with data collection (IoT). The data collection process is manual, with human intervention to check the relevant data ⇒ manual input into electronic media ⇒ check the input contents ⇒ transfer the data.

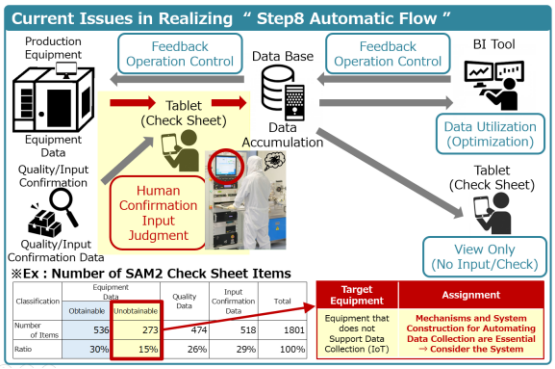

Figure 4: Step 8 Current Issues in Realizing Automatic Flow

Since automatic collection of these data is not possible due to the specifications of the production facilities, it is essential to establish a mechanism or system to enable automatic collection of data. Based on the above background, we developed our own data collection system.

6. Consideration of This System

The following is a description of our consideration of this system.

6.1. Consideration of Changing Equipment Specifications

As shown in Table 2, a study was conducted to see if it would be possible to extract data by changing the specifications of the equipment itself.

In conclusion, we concluded that this method was not feasible due to the limitations on the equipment side, which made it too difficult to modify the equipment. We decided to consider another plan that is feasible without modifying the equipment.

Table 2: Consideration with changing equipment specifications

Consideration Proposal		Equipment Renovation	Overall Judgement
Equipment Specification Changes	Add Data Extraction Functionality to the Equipment itself	× Cannot be Renovated	×
	Scraping the Equipment Monitor Screen *1	× Cannot Add Software	×
	Take a Screenshot of the Equipment Monitor Screen +OCR Processing *2	× Cannot Add Software	×

*1 : Screen Scraping ⇒ Extracting on-screen text from a running application.
*2 : OCR ⇒ Abbreviation for Optical Character Reader.
Recognizing the text part of image data and extracting it as character data.

6.2. Consideration of a Camera Imaging Method

Next, a study was conducted using the camera imaging method, as shown in Figure 5.

The flow of this method is that the Equipment Monitor screen is captured by an external camera, image correction and OCR processing are applied to the captured image data, and text data is extracted. The installation of an external camera on the front of the equipment monitor may reduce the workability as well as the appearance of the equipment.

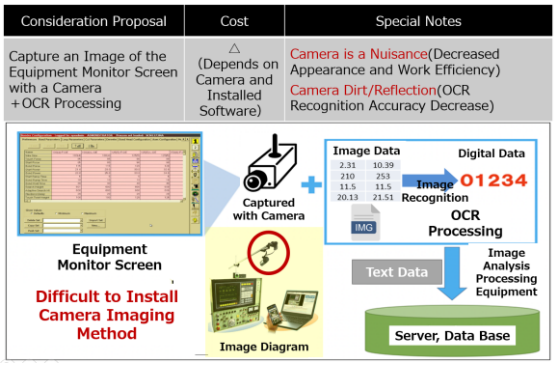

Figure 5: Consideration of a Camera Imaging Method

There is also a concern that dirt on the camera and reflections could degrade the accuracy of OCR recognition. We decided to consider another proposal.

6.3. Consideration of the Monitor Distribution + Screen Capture Method

This proposal was inspired by a hint from casual daily life during the search for another proposal.

Photo 1 shows live game streaming using a popular video content distribution platform.

The same image projected on the game monitor screen is projected to a PC for streaming, and streamed to the streaming platform via streaming software for viewing by the viewer.

Photo 1: Live Game Streaming
(Created with Microsoft Copilot, a Generative AI Engine)

Applying this method, we devised the following system: The system flow is as follows: the Equipment Monitor screen is projected to a PC for streaming, the projected screen is converted to image data, image correction and OCR processing are performed, and text data is extracted. We assumed that this method could solve the problem, so we conducted a more in-depth study.

Figure 6 shows an overview of the video content streaming method, and Figure 7 shows the results of examining the system configuration with reference to the video content streaming method.

First, the Equipment Monitor screen is streamed via a monitor distributor. Next, screen capture is performed on the image analysis processor via the capture board and streaming software. The projected screen is converted to image data, image correction and OCR processing are performed, and text data is extracted.

The advantages of this proposal include a sleek appearance due to the camera-less design, and stable OCR recognition accuracy that is unaffected by dirt and reflections. In addition, by utilizing general-purpose systems and in-house software, we were able to achieve lower costs, and we proceeded to realize the study plan.

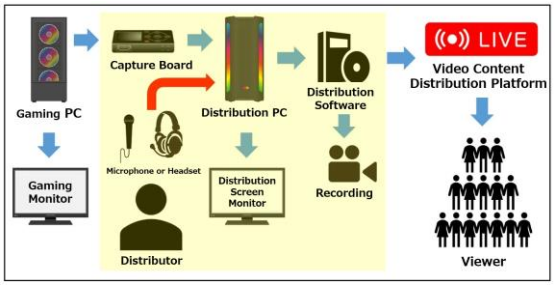

Figure 6: Overview of Video Content Streaming Methods

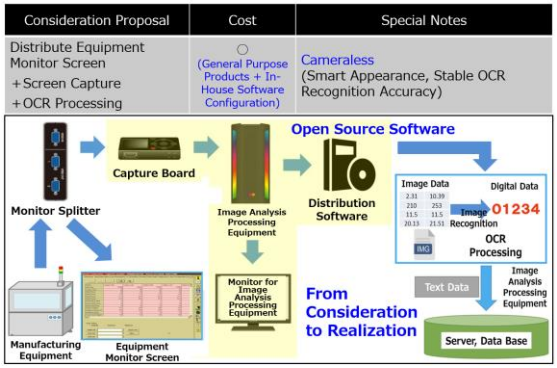

Figure 7: Consideration of Monitor Streaming + Screen Capture Method

7. System Overview

The following is an overview of this system as embodied.

7.1. System Configuration and Operation Flow

The system consists of data extraction and character recognition by an OCR engine, as shown in Figure 8.

The data extraction is for equipment that cannot extract data and cannot be modified by the user due to limitations on the equipment side. Capture equipment monitor screens by applying the video content streaming methods used in popular video content distribution platforms. Using the most suitable general-purpose OCR engine and applying the most suitable image correction to the screen image data obtained improves character recognition accuracy, and data can be extracted as digital data.

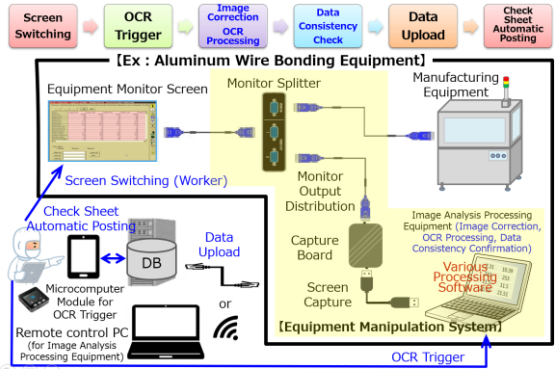

Figure 8: System Configuration and Operation Flow

7.2. Selection of an OCR Engine

There are several important points to consider when selecting an OCR engine, the first and most important being recognition accuracy. It is important to check how accurately the engine can recognize characters in a particular character set and format. Support for the target language is also important, especially when specialized support is needed for Japanese or other non-alphabetic characters.

Processing speed is also important, and the ability to quickly process large amounts of data is an important factor, especially in situations where real-time processing is required. The engine's support for the target document format should also be checked when selecting the engine.

As for the construction environment, whether the engine can be easily integrated with other systems and applications, whether an API (Application Programming Interface) or SDK (Software Development Kit) is provided, whether it is easy to configure and customize, and whether a network environment is required, are also important points.

Regarding the type of license and cost, it is also necessary to comprehensively consider not only the initial cost but also the ongoing support cost, and the operating cost based on the amount of use.

We needed to evaluate these points comprehensively to select the most appropriate OCR engine, and several OCR engines were selected as candidates.

As a result of the selection, we decided to introduce "Company G's OCR engine" into this system, as shown in Table 3.

Table 3: OCR Engine Selection

OCR Engine	Character Recognition Accuracy	Cost	Processing Speed	Built Environment	Overall Judgement
①Company A OCR Engine	○	Paid (WebApp)	△	× Requires NetWork Environment	×
②Company B OCR Engine	○	Paid (WebApp)	△	× Requires NetWork Environment	×
③Company C OCR Engine	○	Free (WebApp)	×	× Requires NetWork Environment	×
④Company D OCR Engine	○	Free (Lib)	×	△ Easy to Set Up	△
⑤Company E OCR Engine	△	Free (OSS)	△	△ Complicated Environment Settings	△
⑥Company F OCR Engine	○	Free (OSS)	△	△ Complicated Environment Settings	△
⑦Company G OCR Engine	○	Free (API)	○	○ Easy to Set Up	○

7.3. Captured Image Optimization

The expected performance cannot be achieved if the quality of images input to the OCR engine is poor. As shown in Figure 9, the recognition accuracy of the general-purpose OCR engine is greatly improved by correcting and optimizing captured images in the preliminary stage of input to the OCR engine.

✓ Image size setting
Adjusting the size of the image appropriately means text can be displayed more clearly and easily recognized.

✓ Image resolution setting
Adjusting the resolution of the image appropriately means text can be displayed more clearly and easily recognized.

✓ Binarization
Converting a color or grayscale image to a binarized (black and white) image clarifies the outlines of characters and makes them easier to recognize.

✓ Mask processing
Excluding areas that contain noise or unnecessary information makes characters easier to recognize.

✓ Distortion correction
Since the OCR engine has difficulty recognizing distorted characters, correcting the distortion makes the characters easier to recognize.

✓ Contrast correction
Emphasizing the contrast between the text and the background makes the text easier to recognize.

✓ Noise removal
Removing unnecessary noise in the image makes character parts clearer and easier to recognize.

✓ Margin removal
Excluding areas that contain noise or unnecessary information makes characters easier to recognize.

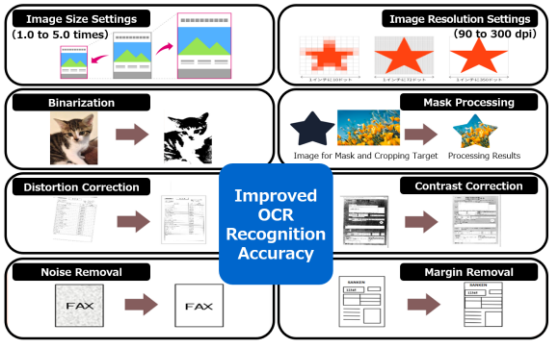

Figure 9: Captured Image Optimization

7.4. Verification on Actual Equipment

Photo 2 shows verification on an actual machine. Verification was conducted using actual production equipment to check the accuracy of the extracted text, and to adjust the position and size of the mask as necessary. We also observed the processing speed for large data sets and evaluated the degree of error for noise and misrecognition. The algorithm and mask settings were fine-tuned based on feedback as needed, and additional adaptive thresholding and other processing techniques were introduced to accommodate variations in image quality.

After the above verification using actual equipment, the versatility, various restrictions, and introduction and operation costs were scrutinized, and the system was officially introduced.

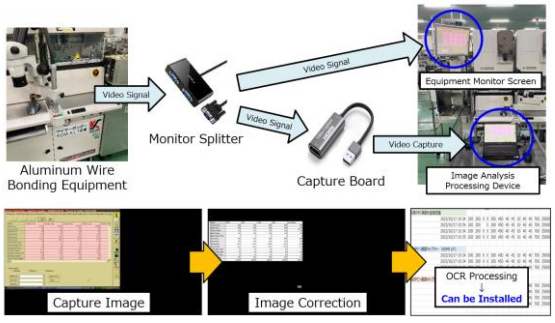

Photo 2: Verification on Actual Equipment

8. Conclusion

In this paper, we outline the equipment manipulation system in our Smart Factory promotion activities at our production factories.

The title "equipment manipulation system" is derived from "automating the operation of equipment by humans" such as extraction of equipment data and input confirmation work.

The development of this system is on track to greatly automate the data entry and data checking tasks that have been performed by workers in the past.

Furthermore, since this system is a data extraction method that can be easily introduced into existing facilities at low cost, it is expected to be deployed in conventional manufacturing equipment. This has established the basic technology for the development of smart factories that can be deployed horizontally.

Now that the path to automatic collection of all equipment data is clear, the only data input remaining is the operator's work verification check.

To address that, we will first review the items in question in cooperation with Ishikawa Sanken, which introduced this system earlier, and work to significantly reduce the number of items.

In addition, a demonstration experiment for "Step 8: Automatic Flow" of the 9-Step Smart Factory Promotion Activity has already started in some of the processes of Ishikawa Sanken's Horimatsu Factory Building B, and we will further accelerate and work toward the realization of this activity in the future.