Generalized Performance Board Design for Docking Interfaces

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Abstract

Our company handles power semiconductors such as Intelligent Power Modules (IPMs) and power management ICs. In wafer testing, which is one of the front-end processes in semiconductor manufacturing, continuous improvement in quality and throughput is required. To enhance throughput, we utilize the multi-site measurement function of Automated Test Equipment (ATE) and probers, which enables testing of multiple chips at once. As the number of chips tested in multi-site configurations increases, components such as performance boards and probe cards tend to become larger. Manufacturing these large components for each product individually leads to increased costs. To suppress these costs, we designed generalized components. This paper reports on the design case of such generalized performance boards.

1. Introduction

Our company develops and manufactures power semiconductors such as IPMs and power management ICs, and conducts wafer testing to evaluate the electrical characteristics and functions of the semiconductor chips used in these products.

Wafer testing involves two main pieces of equipment: ATE, which inputs test conditions and decides pass/fail results based on output data, and probers, which handle wafer transport and positioning. However, these two devices alone are not sufficient for wafer testing. Two additional components—performance boards (PBs) and probe cards—play critical roles in determining test quality and operational costs at manufacturing sites.

PBs are interface boards equipped with electronic components necessary for testing the target chips. They receive electrical signals from the ATE and transmit them to the probe card. Probe cards, in turn, are interface boards equipped with probes (needles) that deliver the signals to the chip.

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In wafer testing, two connection methods between these interface boards and the equipment are commonly used: cable connection and docking connection.

The cable connection method, as the name suggests, connects the ATE and PB via cables, with the ATE installed several meters away from the device. In contrast, the docking connection method directly attaches the PB to the ATE (Figure 1). Compared to cable connections, the wiring distance to the device is reduced to several tens of centimeters, minimizing parasitic capacitance and its impact on measurements. Additionally, this method uses fewer connectors, reducing the risk of connection

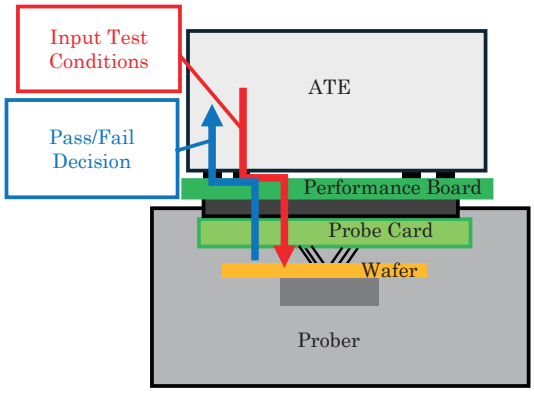

Figure 1. Interconnection of system components

failures and disconnections due to repeated plugging and unplugging.

Despite its advantages, the docking connection method presents challenges. PBs and probe cards become larger, increasing the cost per board. Traditionally, our company designed and manufactured PBs for each product group with different functions, resulting in higher costs.

In addition, the structure between the ATE and the device is extremely compact, leaving no space to freely place oscilloscope probes. As a result, waveform observation is difficult, and the efficiency of characteristic evaluation tends to be lower compared to the cable connection method.

2. Generalized PB Design

Previously, our company designed and manufactured PBs for each product group with different functions. However, due to the large size of the boards, production costs tended to increase. To address this, we aimed to design a single PB capable of testing various semiconductor chips used in our products.

2.1. Generalization Strategy

To improve productivity, it is essential to achieve both generalization and increased throughput. Generalizing PBs means appropriately allocating ATE resources (power supplies, measurement instruments, signal lines, etc.) to the terminals of semiconductor chips so that multiple types of chips can be tested using a single PB.

To enhance throughput, it is necessary to utilize the multi-site measurement function and maximize the number of chips tested at once. Efficient use of ATE resources is crucial to achieving this.

Therefore, the key to balancing generalization and throughput lies in the optimal allocation of resources. We examined methods to achieve this.

Typically, electrical characteristic testing of semiconductor chips consists of multiple test items executed in a sequence. Considering the entire sequence, resources must be connected to all terminals. Furthermore, multi-site testing increases the required number of resources.

However, ATE resources are limited. Connecting resources to all terminals at all times makes it difficult to scale up multi-site testing, especially for chips with many terminals.

On the other hand, not all terminals require constant resource connections during individual tests. Focusing on this point, we optimized resource allocation. The critical factor here is the test conditions for each terminal.

We analyzed the terminal configurations and test conditions of recently developed semiconductor chips. Based on the results, we identified the resources required for each test and designed circuits that efficiently allocate resources to terminals using branching circuits. This enabled us to achieve both generalization and increased throughput.

2.2. Support for High-Voltage Products

Many of our products are high-voltage power semiconductors exceeding 600V, requiring specialized board designs.

When forming high-voltage wiring patterns on the board, it is necessary to consider creepage distance to prevent dielectric breakdown. Ensuring sufficient creepage distance limits the freedom of wiring patterns and component placement, hindering generalization.

To address this, we used high-voltage wires instead of wiring patterns for high-voltage connections. This reduced the number of areas requiring creepage distance considerations and increased the flexibility of wiring and component placement.

2.3. Effects of Generalization

Based on the above design, we produced a generalized PB. As a result, most of our semiconductor chips can now be tested using a single PB.

Generalization eliminated the need to store multiple PBs, reducing management workload and storage space. It also shortened the time required to prepare for testing by reducing the design workload for each product group.

However, some products require specialized circuits. For such cases, we designed PBs with dedicated circuits, which are discussed in the next chapter.

3. Sub-PB Design

The generalized PB described so far is referred to as the “main PB,” while PBs with product-specific circuits are called “sub-PBs” (Figure 2).

3.1. Sub-PB

Sub-PBs are used in combination with the main PB. Previously, all test circuits for each DUT (Device Under Test) were implemented on a single PB. In contrast, sub-PBs separate part of the test circuits for each DUT.

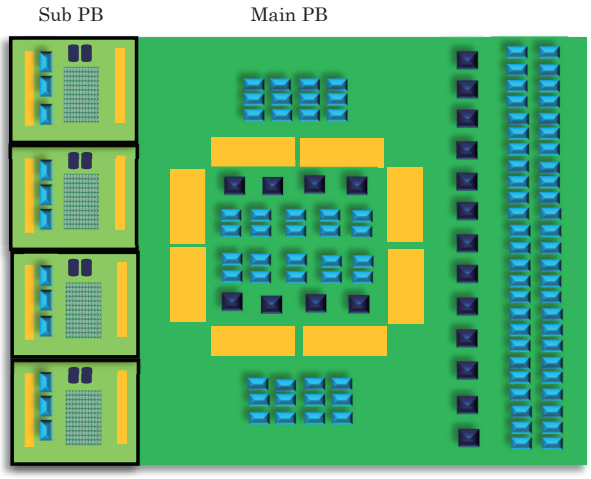

Figure 2. Top view of the PB layout

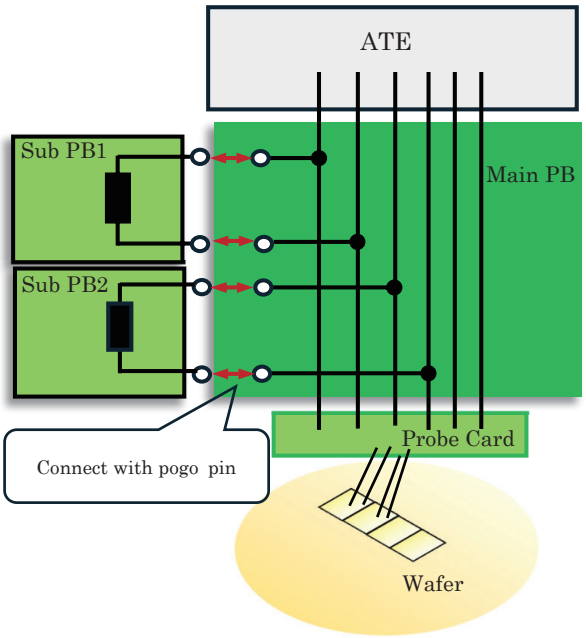

Figure 3. SubPBs and MainPB wiring connection

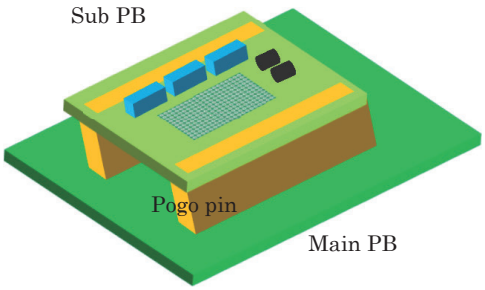

Figure 4. 3D layout of PB connections

During characteristic evaluation, PB circuit modifications are sometimes necessary. Using sub-PBs allows evaluation to proceed without waiting for modifications to all DUT circuits.

Sub-PB design only requires circuits for a single DUT, making it easy to produce using printed circuit boards and to prepare spare boards.

Sub-PBs also offer advantages during mass production. If a sub-PB fails, it can be quickly replaced with a spare, enabling rapid recovery of production.

3.2. Connection Between Main PB and Sub-PB

There are two key points in connecting sub-PBs to the main PB.

First, the main PB is designed to allow retrofitting of sub-PB circuits. Pre-arranged wiring patterns on the main PB enables connection to sub-PBs without modifying the main PB circuits (**Figure 3**). The wiring length between the main and sub-PBs is kept within a range that does not affect electrical characteristics.

Second, connection reliability is improved. Since sub-PBs are expected to be frequently replaced for different product groups, using connectors with short mechanical lifespans increases failure risk. Therefore, we selected pogo pins, which have longer contact lifespans (**Figure 4**).

3.3. Ease of Replacement

In wafer testing, it is common to replace components when switching the test target from product group A to product group B. Our company also replaced PBs and probe cards for each product group.

However, replacing large PBs is inefficient due to their weight. Sub-PBs are approximately one-twentieth the size of main PBs, making them compact and lightweight. Replacing sub-PBs significantly improves work efficiency.

This retrofit structure of sub-PBs enables flexible response to product-specific test requirements.

4. Monitor PB

In docking connection methods, the short distance between the ATE and semiconductor chips minimizes cable effects. However, as mentioned in Chapter 1, structural constraints make waveform observation using external instruments such as oscilloscopes difficult, reducing evaluation efficiency.

To address this issue, we developed a monitor PB dedicated to waveform observation.

The monitor PB is attached to the PB only during characteristic evaluation and is easily detachable. As a result, evaluation efficiency has dramatically improved.

5. Future Challenges

We have designed a generalized performance board (main PB), sub-PBs, and a monitor PB.

However, another important component remains a challenge: the generalization of probe cards.

Generalizing probe cards is more complex than PBs, primarily due to the need to test high-voltage products. High-voltage testing requires sufficient creepage distance on the board, but probe cards have smaller dimensions and limited mounting area compared to PBs.

Additionally, the diverse arrangements of high-voltage terminals on semiconductor chips further complicate generalization.

Like PBs, generalizing probe cards is important for reducing production costs and shortening development lead time. Although complex, we will continue to explore designs that enhance generalization.

6. Conclusion

This paper reported on the generalized design of performance boards, which are critical components in wafer testing.

The new design eliminates the need to replace or produce multiple large main PBs, improving work efficiency and reducing costs.

Moving forward, we aim to generalize probe cards as well, further lowering costs and delivering products that satisfy our customers.