High-Speed Driving and Short-Circuit-Free Protection Technology for Smart SiC-IC

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Abstract

SiC-MOSFETs offer high breakdown voltage and compact size, enabling high-current and high-speed switching in high-voltage circuits. In particular, using a gate-source terminal that does not carry main current allows for low-inductance gate control, achieving fast switching.

However, when a short circuit occurs during high-voltage switching, SiC-MOSFETs experience extremely fast short-circuit currents of several thousand A/μs, leading to device failure in less than 1μs. When applying conventional 3-terminal (3P) driving, as used in Si-IGBTs, to SiC-MOSFETs, switching speed significantly decreases, but short-circuit current is limited, extending the short-circuit withstand time by several times.

This study developed a driving method that combines the fast switching of 4-terminal (4P) driving with the short-circuit protection of 3P driving.

1. Introduction

SiC has approximately ten times the breakdown electric field of Si, and when applied to high-voltage devices, it offers the potential to reduce device size to a fraction of conventional designs. However, simply replacing Si devices in circuits optimized for Si does not allow SiC to fully demonstrate its performance. Therefore, SiC devices must be properly designed and driven.

As shown in Figure 1, the National Institute of Advanced Industrial Science and Technology (AIST) has been developing SiC-MOSFETs with built-in SiC-CMOS gate drivers that enable ultra-fast switching. These chips minimize parasitic inductance in gate wiring by integrating CMOS gate drivers within the SiC-MOSFET chip. This technology has successfully achieved switching of 1200V in just a few nanoseconds [(1), (2), (3), (4)].

On the other hand, when such high-speed devices are used in high-voltage circuits, various surge phenomena become problematic. Among them, surge current during short-circuit events is particularly critical. Due to the rapid switching, short-circuit current peaks in a very short time, potentially causing device destruction [(5), (6), (7)].

To address this issue, AIST and our company have been jointly developing gate driving technologies that can

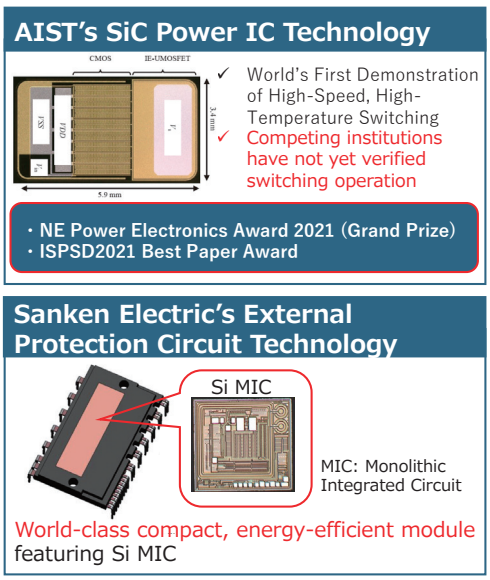

Figure 1. Overview of Joint Development with AIST

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safely protect against short circuits, aiming to realize "SiC-MOSFETs that enable ultra-fast switching with simple operation."

2. Relationship Between High-Speed Switching and Short-Circuit Withstand Capability

Figure 2 shows the circuit used for short-circuit evaluation of SiC-MOSFETs. The DUT (Device Under Test) includes a sense source (SS) terminal that does not carry source current, allowing switching between the SS and standard source (S) terminals for evaluation.

Figure 3 presents typical short-circuit current waveforms of SiC-MOSFETs with gate resistances Rg = 470Ω and Rg = 10Ω, respectively. The gate is driven via the S terminal using 3P driving. The SiC-MOSFET used has a rating of 1200V and 40mΩ, and the test simulates a short-circuit condition at Vd = 600V.

When switching with Rg = 470Ω, the current peaks around 3μs and then decreases due to self-heating, potentially leading to device failure in low withstand devices. In contrast, with Rg = 10Ω, switching speed increases, causing the short-circuit current to peak at around 2μs with a higher amplitude. The current then rapidly decreases due to temperature rise.

Short-circuit failure is caused by the energy consumed, which is the product of short-circuit current, voltage, and duration. As shown in Figure 3, reducing Rg increases switching speed, but also raises the risk of failure due to faster current peaking.

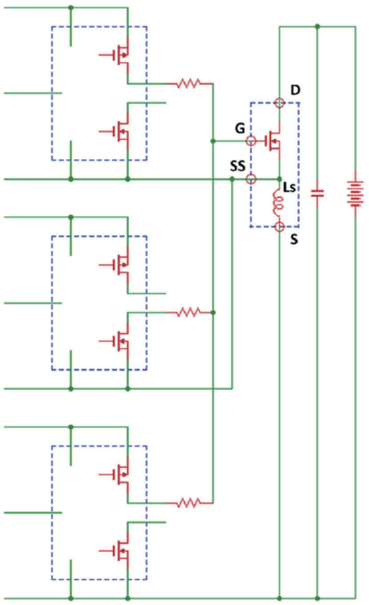


Figure 2. Short-Circuit Evaluation Circuit for SiC-MOSFET

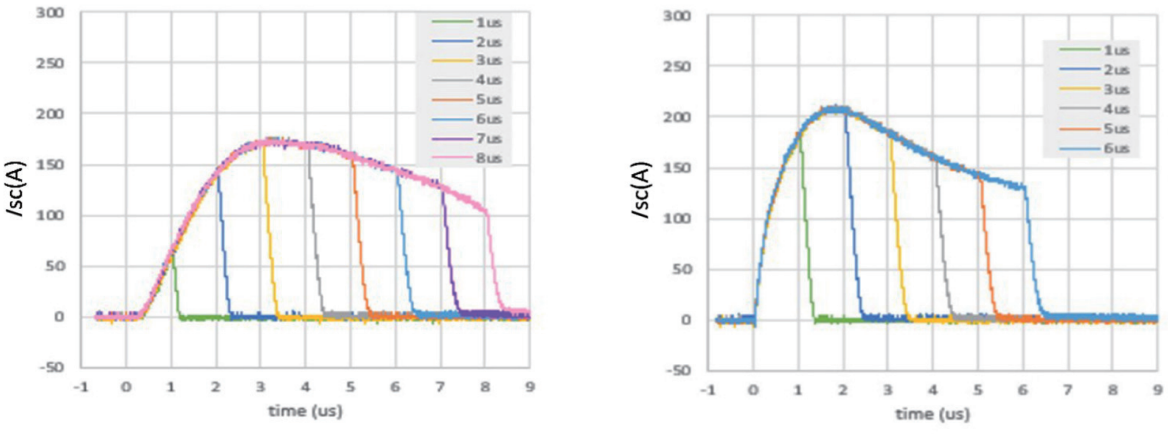
3. Comparison of 4P and 3P Driving

In compound semiconductors such as SiC, 4-terminal packages with a gate-source terminal (SS) that does not carry source current are commonly used to enable high-speed switching (see Figure 2).

4P driving minimizes parasitic inductance and enables fast switching, but short-circuit withstand time is reduced, increasing the risk of failure. On the other hand, 3P driving suppresses current changes due to voltage generated by parasitic inductance, offering better short-circuit tolerance but slower switching.

To address the issue of extremely short short-circuit withstand time caused by high-speed switching, we developed a technique that switches between 4P and 3P source terminal connections.

During switching, the gate driver is connected to the



(a) Rg = 470 Ω (b) Rg = 10 Ω

Figure 3. Typical Short-Circuit Current Waveforms of SiC-MOSFETs

SS terminal for 4P driving to achieve high-speed switching. Afterward, during steady-state operation, the connection is switched to the S terminal for 3P driving, which is expected to improve short-circuit tolerance.

By optimizing this switching method, we aim to achieve both the fastest possible switching and significantly extended short-circuit withstand time in SiC-MOSFETs.

4. Introduction of New Monolithic IC (MIC)

Figure 4 shows the evaluation board for SiC-MOSFETs using a MIC with 4P/3P switching capability. The MIC includes three channels for 4P driving and one channel for 3P driving.

The three 4P driving channels directly drive the gates of P-channel MOSFETs, N-channel MOSFETs, and power SiC-MOSFETs equipped with AIST's CMOS drivers, connected to SS terminals for 4P operation.

The remaining channel also directly drives the gate of a power SiC-MOSFET, but is connected to the S terminal for 3P operation.

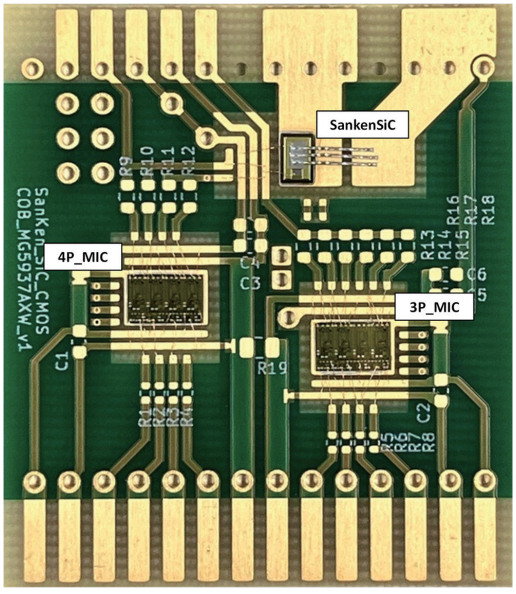


Figure 4. Photograph of SiC-MOSFET Short-Circuit Evaluation Board

This MIC is designed to detect short-circuit events by sensing the induced voltage (V_{Ls}) generated by the parasitic inductance between SS and S terminals due to rapid *di*/*dt* of short-circuit current.

The MIC's output delay is approximately 300ns, and including the detection circuit delay (within 500ns), short-circuit protection can be achieved within 1µs.

Furthermore, when multiple SiC-MOSFETs are driven in parallel, the MIC can detect short-circuit via V_{Ls} in any device and synchronously shut down all devices.

Although the MIC is capable of driving AIST's CMOS-equipped SiC-MOSFETs with a single chip, the evaluation board uses two MIC chips for 4P and 3P driving respectively, to facilitate separate evaluation of high-speed switching and short-circuit protection.

Each channel's output allows independent Source and Sink control, enabling multi-stage switching of gate resistance (*Rg*) during both ON and OFF states for optimized switching performance.

5. Experimental Results

5.1. Short-Circuit Waveform in 4P Driving

Figure 5 shows the short-circuit current waveform when a short occurs in a high-speed switching circuit using 4P driving. The short-circuit current (*I*sc) peaks at approximately 200ns, reaching around 600A. Subsequently, the current rapidly decreases due to device heating, and failure occurs within 1µs after the short-circuit event.

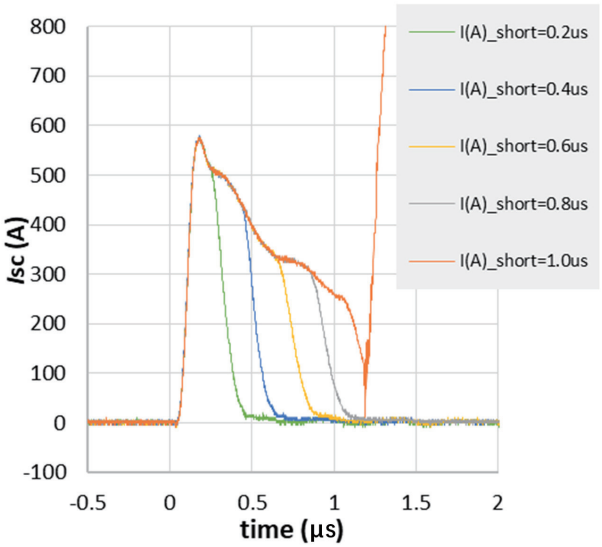


Figure 5. Short-Circuit Current Waveforms under 4P Configuration

5.2. Short-Circuit Protection and Issues in 4P/3P Switching

Figure 6 shows the short-circuit waveform during 4P/3P switching. In this method, both 4P and 3P are driven simultaneously, and 4P driving is turned off after 100ns, switching to 3P driving for protection.

During ON-state simultaneous driving, the large *di*/*dt* causes delayed gate voltage (*Vg*) rise. As a result, *Vg*

remains at 13V at 100ns, indicating that the gate voltage rise is suppressed due to the 3P driving effect under high *di*/*dt* conditions.

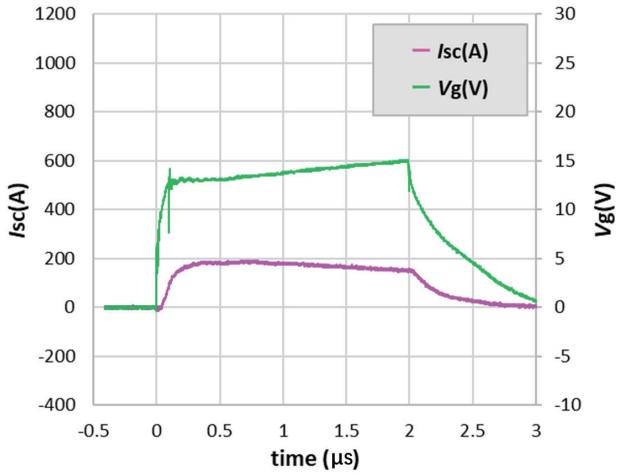


Figure 6. Short-Circuit Waveforms during 4P/3P Switching Operation

5.3. Improved Short-Circuit Protection in 4P/3P Switching

To improve the previous method, the initial state was set to 4P driving only, and 3P driving was activated after 4P driving was turned off.

Figure 7 shows the switching waveform under improved 4P/3P switching conditions. The steady-state driving current (*I*ds) was set to 10A, and switching was performed on the low side of a half-bridge circuit.

Figure 8 shows the short-circuit waveform under the same driving conditions. During the short-circuit event, a negative voltage is induced in the source inductance (Ls) due to the instantaneous large current. By switching to 3P driving before the gate voltage rises sufficiently, the gate voltage (*V*g) during the short-circuit is suppressed, reducing the short-circuit current (*I*sc).

As a result, short-circuit withstand capability was significantly improved compared to 4P driving alone.

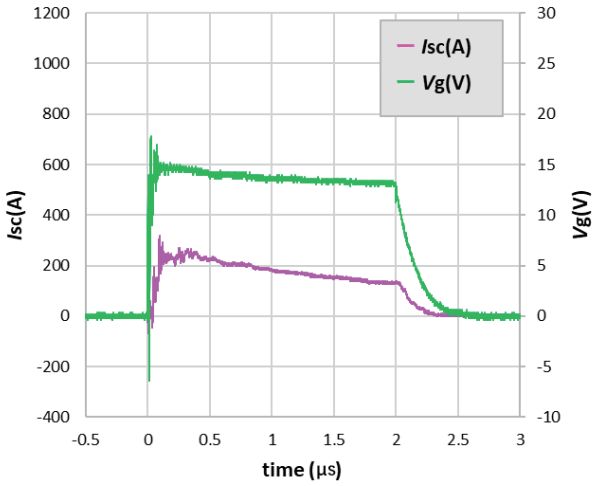


Figure 8. Short-Circuit Waveform Measurements under Improved 4P/3P Switching Conditions

6. Conclusion

This study examined the challenge of maintaining high-speed switching performance in SiC-MOSFETs while improving short-circuit tolerance, and demonstrated the effectiveness of 4P/3P switching.

As a result, the short-circuit withstand time of devices previously limited to 1µs under 4P driving was extended

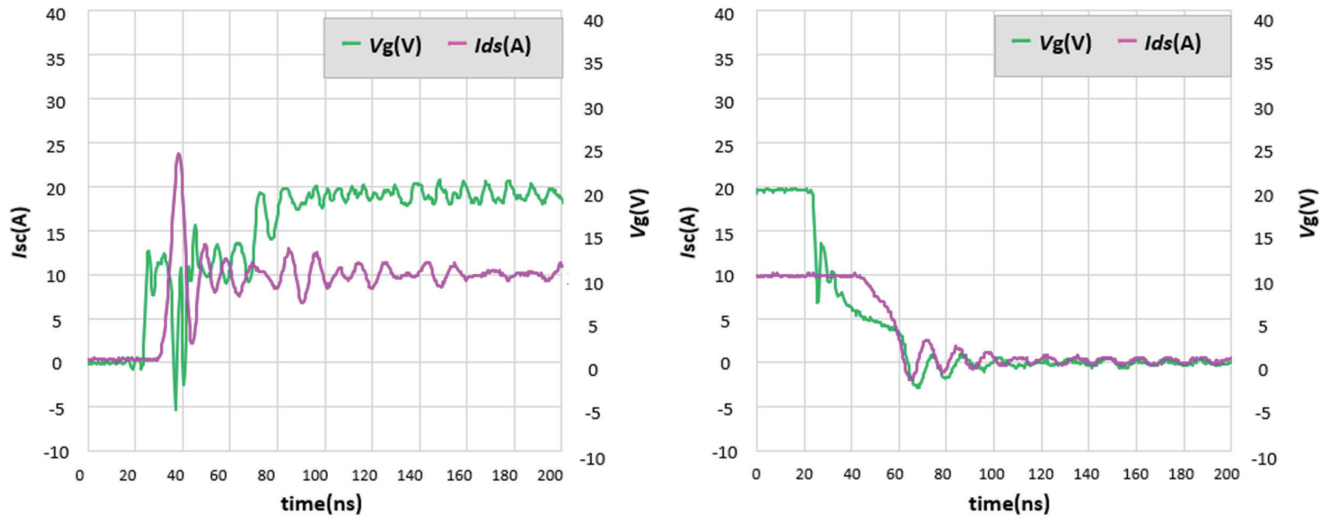


Figure 7. Switching Waveform Measurements under Improved 4P/3P Switching Conditions

to over 2μs using the 4P/3P switching method.

Based on these results, we will continue to pursue the realization of "SiC-MOSFETs that enable ultra-fast switching with simple operation."

7. Acknowledgments

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