

Development of PSJGaN HEMT

Hironori Ito*

Abstract

A prototype device development was conducted with utilizing polarization super junction (PSJ) technology originally developed by Powdec Co., Ltd.

PSJGaN is expected to increase breakdown voltage and suppress current collapse because the simultaneous presence of positive and negative polarization charges confined in respective double heterojunction interfaces leads to a uniform distribution of the electric field.

To verify these effects, prototype fabrication and device evaluation were conducted. Comparative analysis with conventional GaN HEMTs (High Electron Mobility Transistors) revealed superior performance of breakdown voltage and current collapse characteristics. Furthermore, in cascode configuration, PSJGaN demonstrated better switching performance than SJMOS. Based on these results, development toward commercialization of integrated devices of PSJGaN, MOSFET, and control IC will be continued.

1. Introduction

Gallium nitride (GaN) has excellent material characteristics such as a wide bandgap, high electron mobility, and high breakdown electric field as shown in **Table 1**. These characteristics offer significant improvements in power density and switching performance over conventional silicon (Si) devices.

In recent years, as the demand for higher efficiency and miniaturization of power conversion systems has increased, GaN HEMTs have gained significant traction as power semiconductor devices.

Nevertheless, achieving both high breakdown voltage

and low on-resistance, which are inherently conflicting characteristics, is still a major challenge. Therefore, innovation of device structure is required. As a new approach to address this challenge, we have been developing PSJGaN, a GaN HEMT utilizing PSJ structure—an original technology of Powdec Co., Ltd. now merged with Sanken Electric Co., Ltd.

PSJGaN utilizes the polarization properties unique to group III-V materials and leads to a uniform distribution of the electric field like the concept of super junction in Si devices, thereby it enables both low on-resistance and high breakdown voltage. Additionally, by using sapphire as the supporting substrate, it allows for the use of thin epitaxial layers and offers superior cost performance compared to GaN on Si. Moreover, higher breakdown voltage devices exceeding 1200V, which are difficult to achieve with GaN on Si, can be realized. On the other hand, because sapphire is an insulating substrate, there is concern that PSJGaN may suffer from current collapse.

Herein, the device performance and application prospects of the PSJGaN are studied through device design, processing, fabrication, and evaluation and its effectiveness for practical use.

* Engineering Development Headquarters, Process Engineering Division, GaN Device Development Department, GaN Device Development Section

2. Structure and Features of PSJGaN

As shown in Fig.1, when the PSJ structure, a GaN/AlGaN/GaN double heterostructure, is formed, a piezoelectric field is generated within the AlGaN layer due to piezoelectric polarization. This can lead to the formation of the high density, high mobility of electrons (2DEG) and holes (2DHG) at respective heterointerfaces⁽¹⁾.

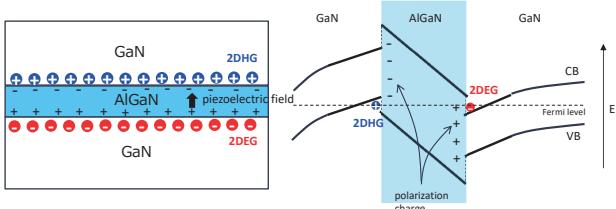


Figure 1. GaN/AlGaN/GaN Double Heterostructure and Energy Band Diagram

2DEG exhibits high charge density and high mobility, enabling the realization of devices with low specific on-resistance. Furthermore, by utilizing PSJ structure, high breakdown voltage devices can be achieved.

Fig.2 shows the device structures of PSJGaN and conventional GaN HEMTs during turn-off, respectively.

When a negative bias is applied to the gate of PSJGaN, 2DHG is depleted from the upper GaN region as shown in Fig.2(a). As a result, both 2DEG and 2DHG are depleted through respective terminals by charge balance.

This leads to a uniform distribution of the electric field at the PSJ structure, which enables the device to withstand high voltages.

However, a positive gate voltage is required to turn on the device because controlling 2DHG is necessitated for gate drive.

On the other hand, conventional GaN HEMTs use Si substrate (GaN on Si) and rely on field plate (FP) structures

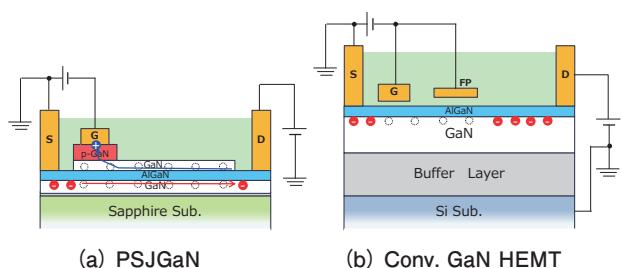


Figure 2. Device Structures and Carrier Distribution in the Off-State

to prevent breakdown voltage degradation caused by electric field concentration at the gate edge as shown in Fig.2(b).

However, considering the electric field between the drain electrode and the Si substrate, breakdown voltage is currently limited to below 800 V.

Additionally, conventional GaN HEMTs sometimes suffer from current collapse—a phenomenon where current flow is suppressed during switching operation, resulting in increased on-resistance. This phenomenon is caused by electrons trapped in the GaN layer or the interface between AlGaN and interlayer due to electric field concentration at the gate edge or the drain edge during turn-off, forming a virtual gate. As a countermeasure, FP structures are utilized to mitigate such electric field concentration.

Because PSJGaN can lead to a uniform distribution of the electric field, it is expected to suppress current collapse more effectively than conventional GaN HEMTs.

3. Evaluation Results of Prototype Devices

3.1 Breakdown Voltage Characteristics

Breakdown voltage characteristics were evaluated for the various length of the PSJ structure (L_{psj}) shown in Fig.3. A trend of increasing breakdown voltage with longer L_{psj} was obtained and the dependence of breakdown voltage on gate-drain distance (L_{gd}) is shown in Fig.4.

PSJGaN exhibited higher breakdown voltage at the same L_{gd} compared to the conventional GaN HEMTs, which suggests superior performance of PSJGaN.

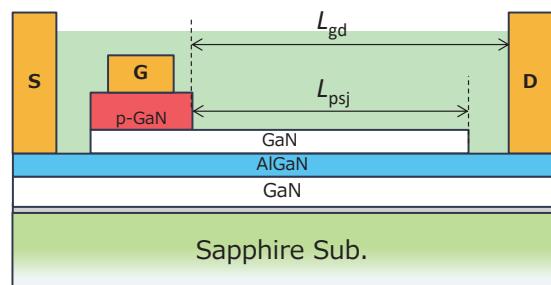


Figure 3. Cross-sectional View of PSJGaN

3.2 Current Collapse Characteristics

Current collapse characteristics were quantitatively evaluated using a pulse IV measurement method. A two-level(on/off) pulse signal was applied to the gate. The pulse width was 25 μ s and drain current and voltage were measured 20 μ s after turn-on.

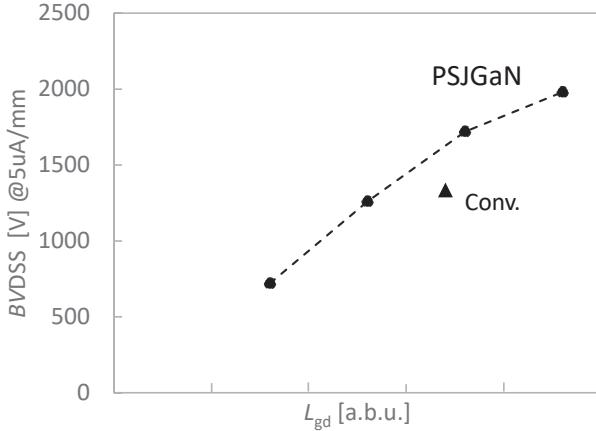


Figure 4. Breakdown Voltage Characteristics of PSJGaN with Varying L_{psj}

The relative change of on-resistance during switching operation (R_{on} dynamic) compared to the initial on-resistance (R_0) was defined as the collapse ratio to evaluate current collapse quantitatively. If the value is close to 1, the impact of current collapse becomes almost negligible.

$$\{\text{collapse ratio}\} = R_{on} \text{ (dynamic)} / R_0$$

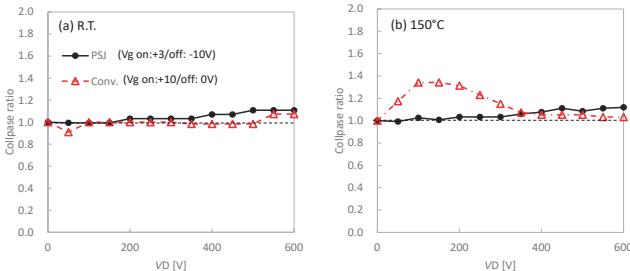


Figure 5. Current Collapse Characteristics of PSJGaN

Fig.5 shows the current collapse characteristics of PSJGaN and conventional GaN HEMTs, respectively.

PSJGaN achieved equal or better current collapse characteristics than conventional GaN HEMTs despite using a sapphire substrate. Therefore, it is confirmed that the PSJ structure is also effective for suppressing current collapse.

3.3 Dynamic Characteristics of Cascode Configuration

By applying a cascode configuration, a normally-on GaN HEMT is connected in series with a MOSFET, and the gate of the GaN HEMT is grounded. This allows the device to operate as a normally-off device, as shown in Fig. 6.

The transfer characteristics and output I-V characteristics for the case where a normally-on PSJGaN is applied

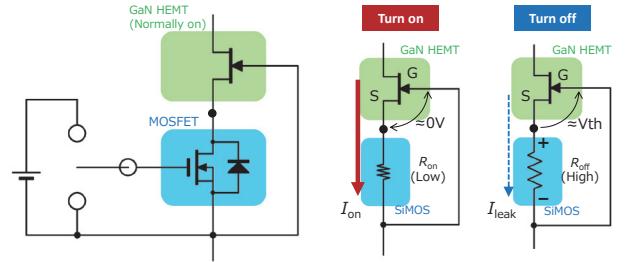


Figure 6. Cascode Connection of Normally-On GaN HEMT

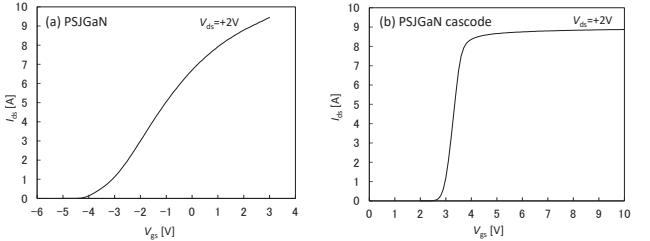


Figure 7. Transfer Characteristics

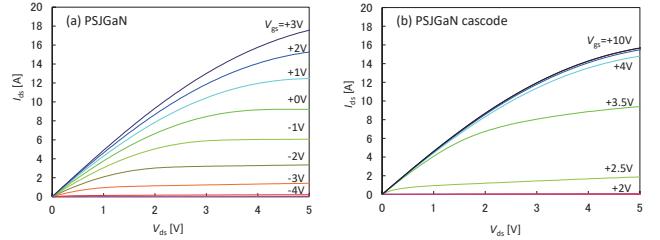


Figure 8. I-V Characteristics

in a cascode configuration (PSJGaN cascode) are shown in Fig. 7 and Fig. 8, respectively.

Because it is necessary to control not only the gate but also PSJ structure during the gate drive, the gate charge (Q_g) is larger than that of conventional GaN HEMTs. However, because the PSJGaN gate is grounded and the MOSFET gate is driven in a cascode configuration, it is expected to mitigate the impact on capacitance characteristics and switching speed.

Fig.9 shows the capacitance characteristics of PSJGaN cascode and Super Junction MOSFET (SJMOS), respectively. PSJGaN cascode showed lower C_{oss} and C_{rss} compared to SJMOS.

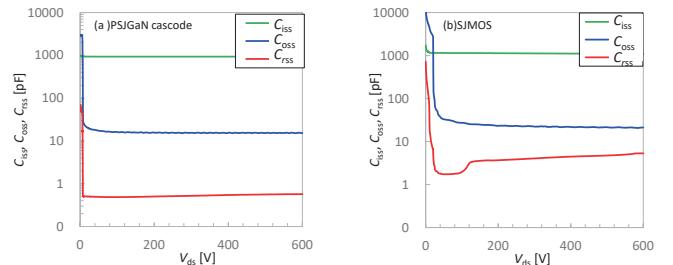


Figure 9. Capacitance Characteristics

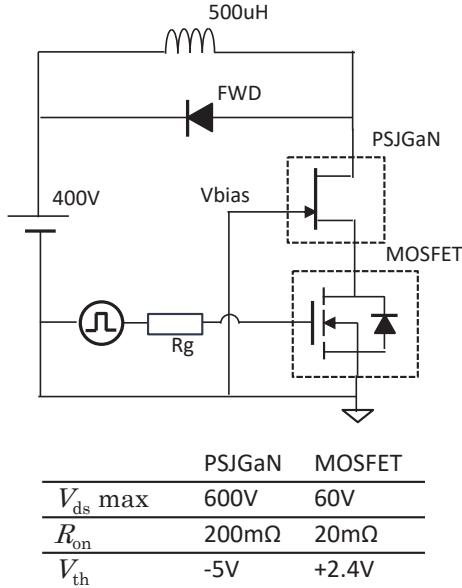


Figure 10. Switching Evaluation Circuit of the PSJGaN Cascode

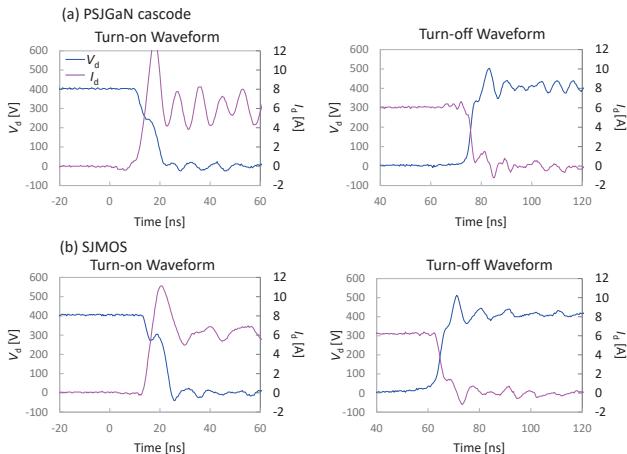


Figure 11. Switching Waveforms of (a) PSJGaN Cascode and (b) SJMOS

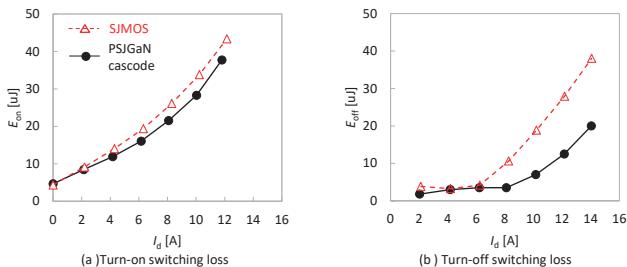


Figure 12. Switching Energy Loss of (a) PSJGaN Cascode and (b) SJMOS

Switching performance was also evaluated under hard switching conditions with an inductive load (Fig.10). Fig.11 shows the switching waveforms at 400V/6A operation.

Based on the results, the switching energy losses during turn-on and turn-off were extracted, as shown in Fig.12.

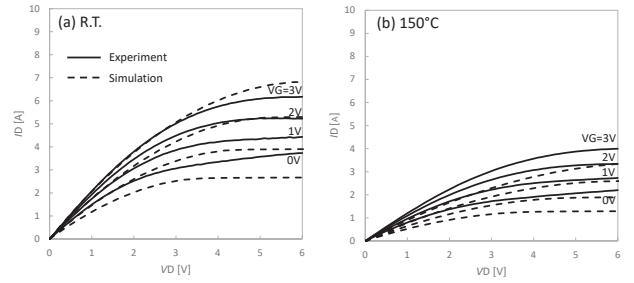
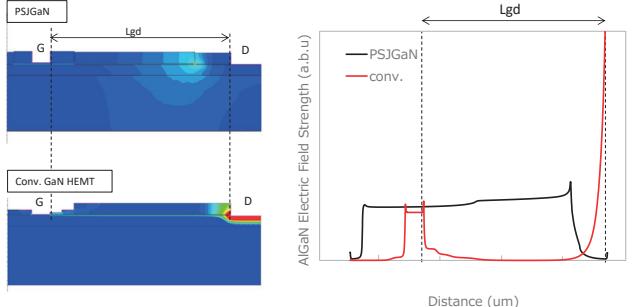
Figure 13. $I-V$ Characteristics of PSJGaN

Figure 14. Simulation Results of Electric Field Strength Distribution under High Voltage in the Off-State

From these results, it is confirmed that PSJGaN cascode exhibited lower switching energy losses than SJMOS.

4. Challenges in Device Simulation

Device simulation of PSJGaN using TCAD is currently undertaken.

For output $I-V$ characteristics, relatively good reproducibility was achieved at room temperature, but discrepancies remain at high temperatures as shown in Fig.13.

Moreover, simulation results of the distribution of electric field during turn-off are shown in Fig.14 for PSJGaN and conventional GaN HEMTs, respectively.

The results show that PSJGaN exhibits a more uniform distribution of electric field compared to conventional GaN HEMTs with FP structures.

This tool will support device design after validating the physical models and improving simulation accuracy.

5. Conclusion

This report introduced PSJGaN, a GaN-based device capable of achieving low power conversion loss and high efficiency.

Evaluation of prototype devices demonstrated that PSJGaN offers superior breakdown voltage and current collapse characteristics compared to conventional GaN

HEMTs. Additionally, PSJGaN cascode showed superior capacitance characteristics and switching performance compared to SJMOS.

The drive ICs which can control PSJGaN under optimal conditions will be also developed in conjunction with improvements in PSJGaN performance.

TCAD device simulation of PSJGaN is also undertaken

and this tool will be useful for device design and accelerate the commercialization of such integrated devices.

References

1. Sato et al., "Toyota Gosei Technical Report," Vol. 63, pp. 41-45 (2021)

RISC-V Microcontroller MD6605 for Power Electronics Control

Takanaga Yamazaki *

Hitomi Shishido * *

Abstract

Sanken Electric has developed the microcontroller MD6605 for advanced power electronics control systems such as power supplies and motors. MD6605 is built on a cutting-edge 22nm ultra-low-leakage process and incorporates a RISC-V CPU core along with non-volatile ReRAM memory. In addition to the RISC-V CPU core, MD6605 features a heterogeneous multi-core architecture consisting of a DSP for digital filter computation and an EPU (Event Processing Unit) capable of high-speed task switching, enabling high efficiency and functionality in power electronics control systems. Sanken Electric plans to actively deploy products utilizing MD6605 for various power electronics control applications.

1. Introduction

In recent years, the promotion of GX (Green Transformation) initiatives aimed at achieving a decarbonized society has driven increasingly stringent requirements for energy-saving performance in electronic devices. In particular, data centers, which are expanding due to the proliferation of generative AI, consume large amounts of electricity and demand significant improvements in power delivery efficiency.

Moreover, power supply systems used in widely adopted consumer electronics and industrial equipment are also subject to ongoing efficiency improvements. Recent AI processors and high-performance SoCs (System on a Chip), which utilize ultra-fine process technologies and operate at higher clock frequencies, require low-voltage and high-current power supplies under demanding conditions, necessitating high-precision power control.

To address these challenges, Sanken Electric has long pursued digital control methods for power supplies

and has developed the advanced microcontroller MD6605 to meet increasingly stringent requirements. MD6605 is not only suitable for power supply control but also for brushless DC (BLDC) motor control used in home appliances and industrial equipment. It contributes to improved efficiency and offers automatic parameter adjustment functions to simplify development.

2. Digital Power Control and Its Advantages

Traditionally, power supplies have been controlled using analog methods, as shown in **Figure 1**. These methods are well-established and can be implemented with relatively simple hardware. However, analog control using resistors and capacitors for linear phase compensation has limitations in parameter adjustment range, resulting in fixed converter topologies. Efficiency improvements through optimal control require complex hardware, and noise countermeasures rely solely on hardware, necessitating many additional components. Communication with external systems and implementation of intelligent functions are also difficult. In high-output power supplies, reducing losses across the full load range is challenging, often requiring large heat sinks and increasing system costs.

* Engineering Development Headquarters, Power Device Development Division, System Development Department

** Engineering Development Headquarters, Power Device Development Division, System Development Department, Digital Development Section

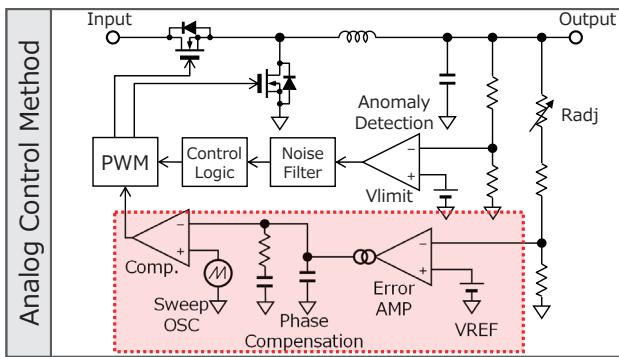


Figure 1. Example of Analog Control Method for a Power Supply (Buck Converter)

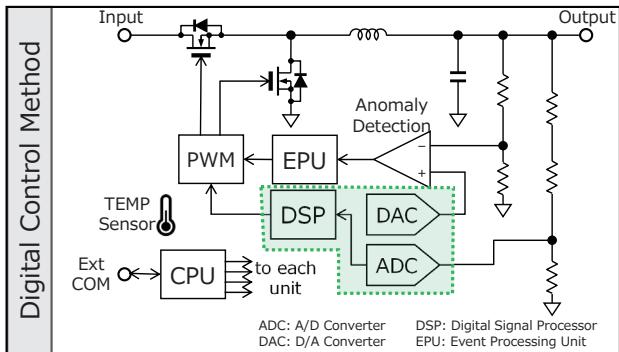


Figure 2. Example of Digital Control Method for a Power Supply (Buck Converter)

Figure 2 illustrates a digitally controlled power supply. Digital control enables flexible linear and nonlinear control through numerical computation, which is not possible with analog methods. Although digital control requires more hardware, such as DSPs (Digital Signal Processors), it offers numerous advantages:

- Capable of supporting any power converter topologies
- High-precision and fast response through advanced control algorithms
- High efficiency through optimized control tailored to load conditions and other operating factors
- Flexible noise countermeasures via software
- Implementation of communication and intelligent functions
- Reduction of heat sinks and noise countermeasure components due to improved efficiency
- Lower system costs, especially in high-output, high-precision power supplies

As a result, digital control is widely adopted in high-output power supplies for server centers, high-end AV equipment, and low-voltage, high-current power supplies for high-performance AI processors.

The following sections detail specific advantages of digital control.

(1) Compatibility with Various Converter Topologies

Digital control is primarily software-based, enabling adaptation to various converter topologies, such as the buck converter in Figure 2 and other types shown in Figure 3, without requiring any changes to the controller hardware.

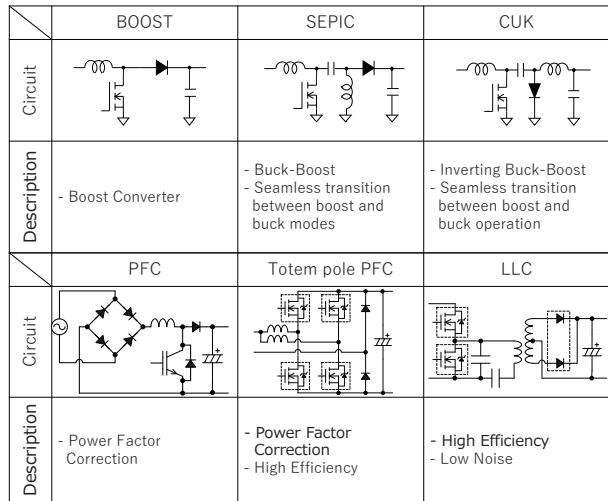


Figure 3. Various Power Converter Topologies Supported by Digital Power Supplies

(2) High-Precision Output Voltage

By detecting ambient temperature in real time using temperature sensors and applying compensation, power supplies with minimal temperature variation characteristics, as shown in Figure 4, can be achieved.

(3) Efficiency Improvement Across Full Load Range

Power supplies typically exhibit reduced efficiency under light-load conditions. Digital control enables fine-tuned optimal control based on load conditions, improving efficiency across the entire load range. For example, the switching frequency can be reduced under light loads. Figure 5 shows an example of efficiency in a digitally controlled high-efficiency DC-DC intermediate bus converter.

(4) Implementation of Advanced Modern Control

Figure 6 shows a block diagram of PID control (classical control), commonly used in analog systems. It performs feedback control to match the output voltage with the target value. However, in high-power systems with large load fluctuations and high precision requirements, this method struggles to meet targets.

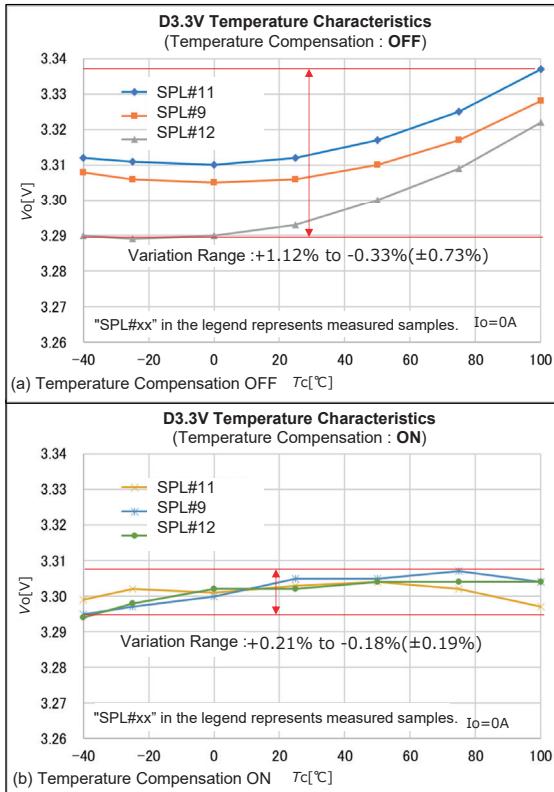


Figure 4. Effect of Temperature Compensation by Digital Control

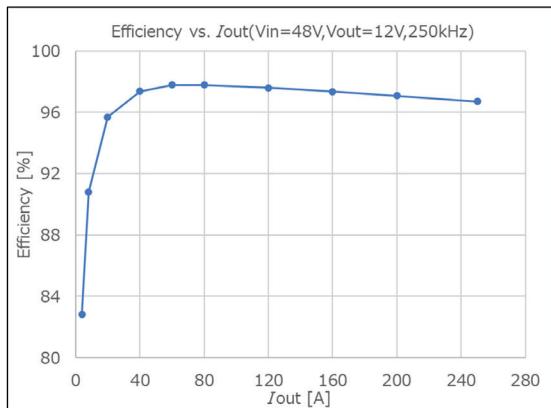


Figure 5. Efficiency of a High-Performance DC-DC Power Supply with Digital Control

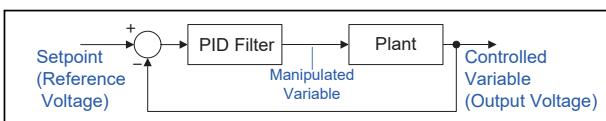


Figure 6. Typical PID Control (Classical Control)

Figure 7 presents an approximate two-degree-of-freedom control (modern control) method that adds a disturbance estimate to the target value to cancel out disturbances. This method requires numerical computation and can only be implemented through digital control.

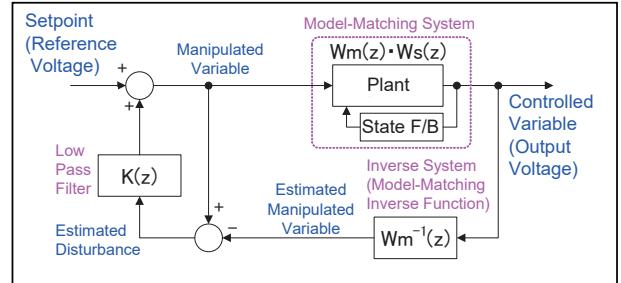


Figure 7. Approximate Two-Degree-of-Freedom Control (Modern Control)

Figure 8 demonstrates the effectiveness of two-degree-of-freedom control, showing simultaneous improvement in target response and disturbance rejection. This method is effective for controlling power supplies for large-scale AI processors requiring low voltage (0.5V–0.9V), high precision (±20mV), and high current (100A or more).

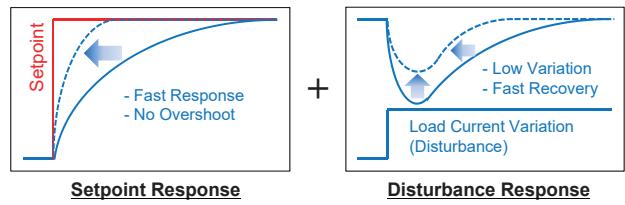


Figure 8. Effectiveness of Approximate Two-Degree-of-Freedom Control

(5) Fault Detection and Prediction

Digital control enables early detection of signs of power supply abnormalities.

- FFT Processing: Output voltage waveforms sampled via A/D converters are analyzed using FFT to detect changes in frequency components indicating potential faults.
- Edge AI: Real-time duty cycle command patterns are analyzed by edge AI using learned data to detect signs of abnormalities (Figure 9).

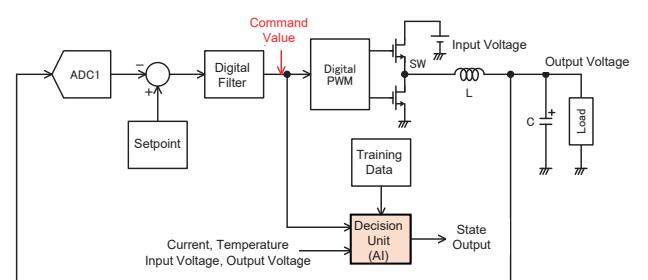


Figure 9. Fault Prediction Using Edge AI

(6) Realization of Intelligent Power Supplies

Digital control using microcontrollers (CPUs) allows complex system processing.

- Multi-output power sequencing: Arbitrary configuration of power-up and power-down sequences for multiple output rails
- Communication control: External communication enables voltage adjustment, ON/OFF control, current limit changes, and monitoring of power operation status (PMBUS, AVSBUS)
- Operation log management: Logging of power operation and fault detection status in non-volatile memory
- Self-diagnosis: Self-diagnosis of the microcontroller chip and the entire power system, with automatic shutdown or external reporting in case of abnormalities

3. Required Functions for Power Control Microcontrollers

To flexibly implement the digital control described above, a dedicated microcontroller is essential (Figure 10). Power control involves fast-responding electrical circuits, requiring much shorter control cycles than motor control. Therefore, high-speed DSPs and A/D converters are indispensable.

Additionally, higher PWM carrier frequencies require high-resolution PWM timers. Power systems also require rapid response to events such as overvoltage/overcurrent, zero-crossing of voltage/current, and fault detection. While simple operations can be handled by hardware, complex cases requiring flexibility cannot be efficiently managed through CPU interrupt processing due to latency. Thus, a specialized high-speed response processor is needed.

Consequently, power control microcontrollers must

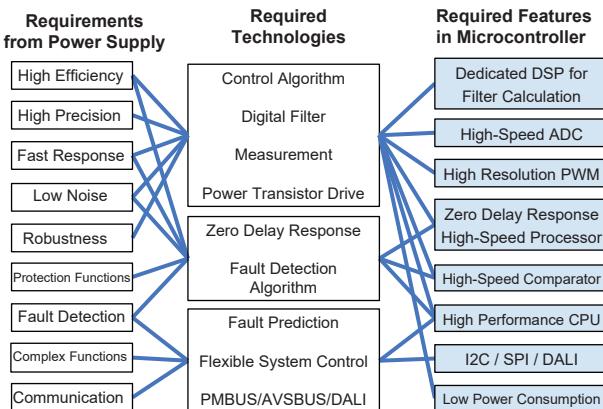


Figure 10. Required Functions for Power Control Microcontrollers

adopt a heterogeneous multi-core system comprising not only a CPU core but also DSP cores and high-speed response processors.

4. MD6605 Microcontroller for Power Electronics Control

Sanken Electric has developed MD6605 as the next-generation microcontroller for power supply control. Considering applications that require simultaneous control of motors and power supplies, MD6605 is equipped with functions necessary for motor control and is designed as a comprehensive microcontroller for power electronics control.

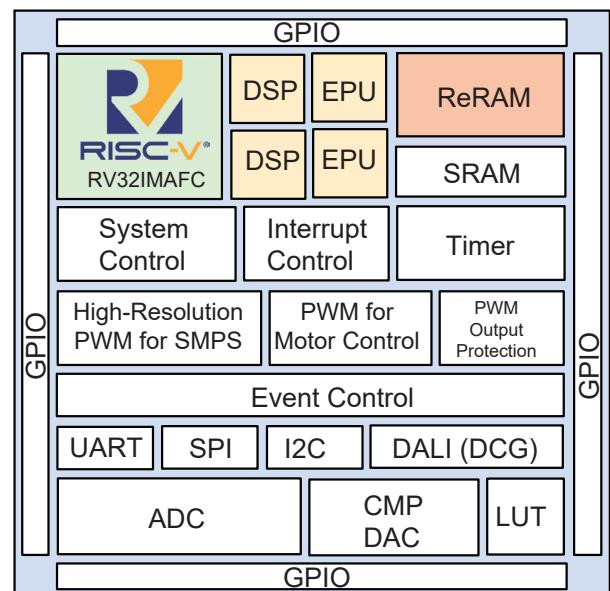


Figure 11. Block Diagram of MD6605

Table 1. Summary of MD6605 Specifications

Item	Specification
RISC-V CPU	ISA=RV32IMAFc, Debugger I/F=cJTAG
DSP	x2units Floating Point Operations
EPU	x2units Zero-Delay Task Switching
ROM	ReRAM (Resistive Memory) 128KB+ECC
RAM	8KB+ECC
Interrupt	x64inputs x16priorities Dedicated Timer
System Control	OSC PLL Low-Power Functional-Safety
Timer	16bit Timer, Low Power Timer, WDT etc.
HPWM (SMPS)	High-Resolution PWM x8 outputs
MPWM (Motor)	Complementary PWM x6 outputs
Event Control	Event Network Switches & Event Handling
Serial COMM	UARTx3ch SPIx1ch I2Cx1ch DALI (DCG)
ADC	x3units 12bits 3MSPS x8inputs/unit
Comparator	x6units with 10bit DAC, Logical Operations
GPIO	Any Functions can be assigned in each Pin.
Operating Cond.	66.6MHz, VDD=3.3V (Single Voltage)
Process	TSMC 22nm ULL Process integrating ReRAM

Figure 11 shows the block diagram of MD6605, and Table 1 summarizes its specifications. The following sections describe the key features of MD6605.

5. Heterogeneous Multi-Core Architecture

As previously mentioned, MD6605 adopts a heterogeneous multi-core architecture that enables parallel processing using three types of cores with distinct characteristics to achieve high-efficiency and high-precision power electronics control.

(1) CPU (Central Processing Unit)

Responsible for system-wide control tasks such as communication, operation logging, fault diagnosis, and control during non-steady states. Due to increasing program complexity, a high-performance 32-bit CPU is required. For digital filter processing and motor vector control, floating-point arithmetic is preferred over fixed-point to avoid issues such as limited dynamic range, overflow, and underflow. Therefore, the CPU must support floating-point instructions.

(2) DSP (Digital Signal Processor)

Handles digital filter computations for power electronics control. As control sampling frequency increases, high-speed arithmetic processing becomes essential. The DSP must be capable of executing multiply-accumulate operations in a single cycle using both integer and floating-point arithmetic.

(3) EPU (Event Processing Unit)

Handles rapid responses to various events such as comparator inversion at zero-crossing of current or voltage, completion of A/D conversion, and timing events from PWM timers. These operations require high-speed responsiveness, which cannot be achieved with conventional CPU interrupt handling due to latency from register saving and restoring. Therefore, a dedicated processor capable of zero-latency task switching is necessary.

Figure 12 illustrates the heterogeneous multi-core configuration of MD6605. Since DSP and EPU frequently interact with A/D converters and PWM timers, they are connected via dedicated buses. With two DSP units and two EPU units, MD6605 performs parallel processing using a total of five cores including the CPU. This parallelism enhances system performance without increasing

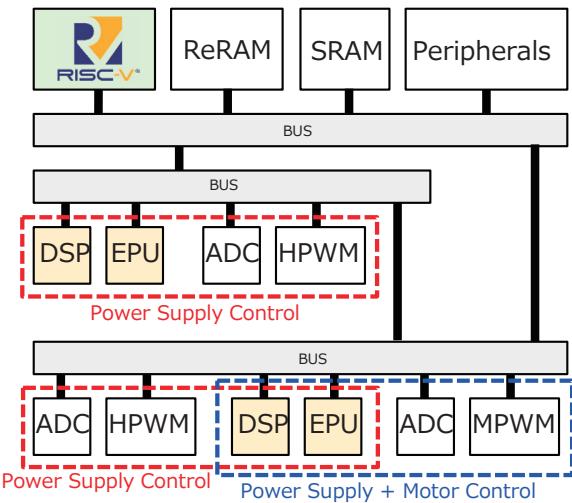


Figure 12. Configuration of MD6605 Heterogeneous Multi-Core Architecture

operating frequency.

MD6605 operates at 66.6 MHz, but its heterogeneous architecture delivers floating-point performance of 400 MFLOPS and integer performance of 600 MOPS.

6. Integration of 32-bit RISC-V CPU Core

MD6605 employs the latest RISC-V*** architecture as its main CPU. RISC-V is an open instruction set architecture that allows anyone to design freely. Although commercial IP cores are available, Sanken Electric has developed its own implementation.

RISC-V features a simple instruction set, high processing performance, and efficient code density. Its surrounding ecosystem, including development environments, is rapidly maturing, and widespread adoption is anticipated.

Table 2 presents the specifications of the RISC-V CPU core integrated in MD6605.

Table 2. Specifications of the RISC-V CPU Core Integrated in MD6605

Item	Specification
Instruction Set Architecture	RV32IMAFPC (Multiplication, Floating Point)
Pipeline	Integer:3 to 5 stages Floating:5 to 6 stages
Integer MUL	1cyc
Floating Point	Add/Sub/Mul/Mul&Add : 1cyc
Debugger	2-wire JTAG x4 Hardware Breakpoints
Interrupt	x3 RISC-V standard x64 Expanded Inputs (x16 priorities)
Dhrystone 2.1	1.6 DMIPS/MHz
Coremark 1.0	3.30 Coremark/MHz
Development Environment	<ul style="list-style-type: none"> MD Studio (based on Eclipse) 3rd Party IDE (planning)

*** RISC-V is a registered trademark of RISC-V International and Mr. Krste Asanović.

7. Enhanced DSP and EPU Cores

MD6605 includes two units each of proprietary DSP and EPU cores. **Table 3** summarizes their specifications.

Table 3. Specifications of DSP and EPU

Item	DSP	EPU
Purpose	High-speed computation independent of CPU	High-speed response to power control events
Number of cores	2 cores	2 cores
Number of threads	1 thread	2 threads
Instruction set	Fixed 16-bit	
Pipeline	3-5 stages	
Event response	Event wait, timer wait, event output (real-time application capability)	
Thread control	None	Zero-time thread switching
32-bit fixed-point arithmetic	Add/Sub/Mul/Mul/Add : 1cyc Div : 8 cyc (Newton-Raphson)	
32-bit floating-point arithmetic	Add/Sub/Mul/Mul/Add : 1cyc Div : 8 cyc (Newton-Raphson)	None
Debugger	Step execution / PC break / Data break / Software break	

The DSP is a processor equipped with 32-bit floating-point and fixed-point arithmetic units. **Figure 13** shows its block diagram. The DSP can perform arithmetic, logic operations, and data transfers in response to events without CPU intervention. It supports single-cycle execution of addition, subtraction, multiplication, and multiply-accumulate operations for both floating-point and fixed-point data, enabling high-precision control such as phase compensation and vector control. Division using the Newton-Raphson method can be completed in eight cycles.

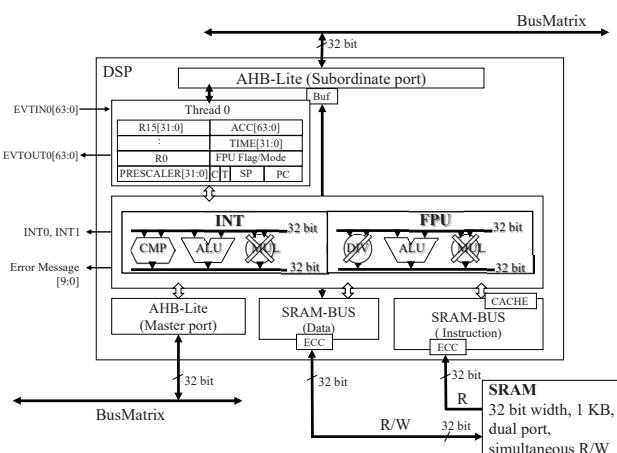


Figure 13. Block Diagram of DSP

The EPU differs from the DSP in terms of floating-point support and thread count. Each EPU has two threads and one fixed-point arithmetic unit. Each Thread has its own general-purpose registers, timer, and program counter. The EPU executes tasks assigned to threads sequentially based on priority.

In power electronics control, rapid response to numerous events is essential. Upon receiving an event signal, the EPU immediately executes the corresponding task.

During task switching, thread-specific resources such as registers are retained, eliminating the need for data saving and restoring. Unlike CPU interrupt handling, the EPU enables zero-latency task switching.

Figure 14 illustrates an example of zero-latency task switching using fixed priority (Thread 0 > Thread 1). When Thread 0 is inactive or waiting for an event, Thread 1 executes instructions. Upon receiving an event, Thread 0 immediately takes over execution.

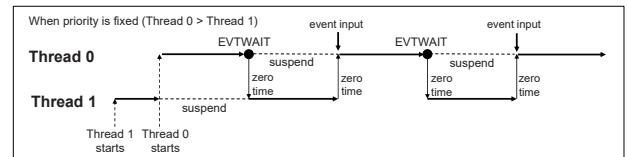


Figure 14. Zero-Latency Task Switching

A key feature of the EPU is its ability to control event input/output via instructions. MD6605 also supports internal event routing. In power electronics control, synchronized operation among modules is required, which is achieved through event signals exchanged between modules.

As shown in **Figure 15**, MD6605 handles various internal event signals such as A/D conversion completion and comparator inversion. Event routing is configurable via the Event Controller (EVC), enabling synchronized operation across modules.

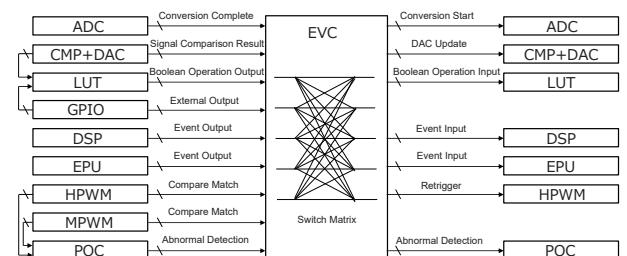


Figure 15. Event Connections in MD6605

8. Peripheral Functions and Their Features

This section describes the main peripheral functions integrated in MD6605.

(1) HPWM: High-Resolution PWM

HPWM is a high-resolution PWM designed for power supply control. Since power control requires short control

cycles and high PWM carrier frequencies, high resolution is essential. The HPWM in MD6605 offers sub-nanosecond resolution, enabling fine adjustment of duty cycles. It features a 16-bit counter that determines the PWM period and duty cycle by comparing counter and reference values. Both up-count and up-down count modes are supported.

Additionally, HPWM includes a retrigger function that enables real-time changes to counter behavior in response to events such as overvoltage, overcurrent, or zero-crossing of voltage/current. This allows immediate execution of operations such as PWM stop, duty cut, or cycle skip operations.

(2) MPWM: PWM for Motor Control

MPWM is a PWM module for motor control. It features a 32-bit up-down counter and can generate six PWM signals (three complementary pairs). As shown in Figure 16, MPWM adopts a center-aligned mode, which offers high noise immunity and precise control for motor applications. The duty cycle is adjustable from 0% to 100%, and a dead-time function prevents simultaneous switching of paired transistors.

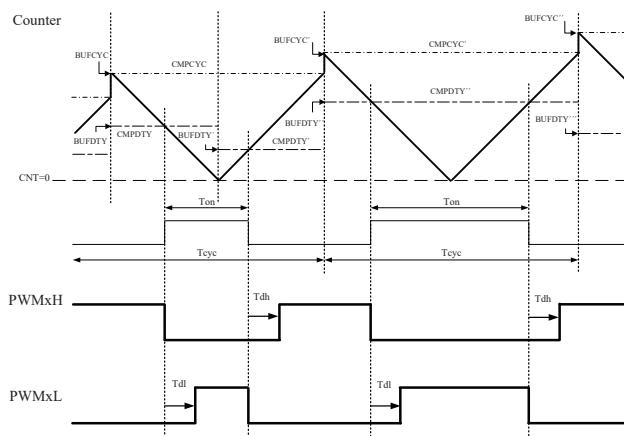


Figure 16. MPWM Counter and Output Waveforms

(3) POC (PWM Output Controller)

POC controls the output state of PWM terminals based on changes in comparator or LUT outputs, or events from the EVC. In abnormal power conditions, POC can override PWM control and immediately fix the output state, enabling rapid protection. MD6605 includes two POC units: POC0 for HPWM and POC1 for MPWM.

(4) A/D Converters

MD6605 integrates three 12-bit successive approximation A/D converters. In power control, they enable simultaneous control of three converters; in motor control, they allow concurrent sampling of three-phase currents. These converters are compact, fast, and energy-efficient. At a 66 MHz clock, the maximum conversion rate is 3 MSPS.

(5) LPTMR: Low-Power Timer

LPTMR is used to wake the microcontroller from low-power modes. In power electronics control, the system may enter low-power mode under specific conditions, such as idle states. MD6605 supports the following low-power modes and wake-up sources:

- Sleep Mode: Wake-up via interrupt
- Standby Mode: Wake-up via GPIO interrupt, comparator level interrupt, LPTMR, or DCG (DALI Control Gear)
 - Normal Standby: GPIO, comparator
 - LPTMR Standby: GPIO, comparator, LPTMR
 - DCG Standby: GPIO, comparator, DCG

LPTMR is suitable for periodic wake-up from low-power modes to execute scheduled tasks.

9. Adoption of TSMC 22nm Process and ReRAM

MD6605 is manufactured by TSMC using a cutting-edge 22nm ULL (Ultra Low Leak) process and incorporates ReRAM (Resistive RAM) as non-volatile memory.

The 22nm process was selected for the following reasons:

1. Reduced chip size and lower cost
2. Lower power consumption using ULL process and HVT (High V_t) transistors
3. As the final generation of planar processes, it ensures long-term supply stability

For non-volatile memory, ReRAM was chosen over FLASH due to implementation challenges in 22nm nodes. ReRAM has a simpler structure, built in the interconnect layers, and offers the following advantages:

- Fewer additional masks, resulting in lower cost
- Column-level overwrite without block erasure, improving usability
- Reliability (data retention) equal to or better than FLASH

Although MRAM (Magnetoresistive RAM) is another option for fine-process non-volatile memory, ReRAM is increasingly adopted in automotive and other applications due to its cost advantages.

10. Deployment in AC-DC Power IC Products

MD6605 is offered as an integrated one-package solution designed to enhance system integration. By combining high-voltage gate drivers and other key components, it significantly improves usability and efficiency. It will not be released as a standalone microcontroller.

Figure 17 shows the MD67xx product series for AC-DC power supply units (PSUs). MD67xx integrates MD6605 and supports simultaneous control of a totem-pole PFC and two-channel LLC resonant converters.

Key benefits of MD67xx in PSU applications include:

1. High efficiency (>98%) across all load ranges enabled by bridgeless totem-pole PFC, zero-cross switching, and load-adaptive control
2. Low THD achieved through high-speed optimal control of PFC
3. Fast transient response enabled by advanced current-mode control of LLC
4. Compact heat sinks and platforms made possible by the use of GaN/SiC devices
5. Enhanced functionality, including communication control, operation logging, and fault diagnosis

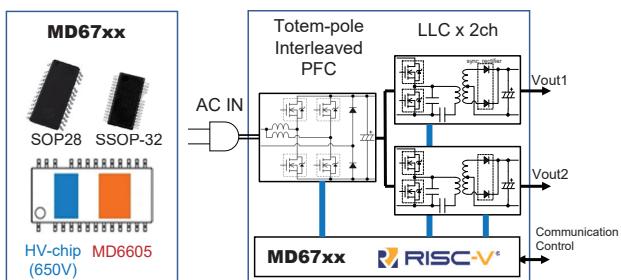


Figure 17. Application Example of MD6605 in PSUs

11. Deployment in DC-DC Power IC Products

Figure 18 shows the MD77xx product series designed for intermediate bus converters (IBC) in DC-DC power systems. MD770x integrates MD6605 and controls multiple high-efficiency hybrid converters in parallel.

Key benefits of MD77xx in IBC applications include:

1. High efficiency (>98%) even at large step-down ratios enabled by advanced hybrid converters
2. Output current exceeding 200A achieved through parallel multi-phase operation and precise current balancing

3. Flexible control of multiple converter types with a single MD770x (e.g., dual IBC or one IBC plus six POL channels)

4. Power management via PMBUS/AVB/US communication

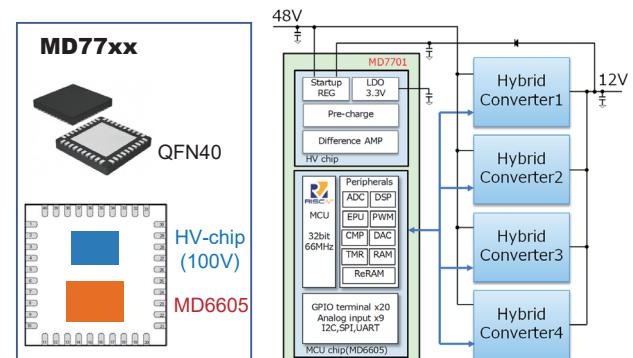


Figure 18. Application Example of MD6605 in IBCs

12. Deployment in Motor Control Products

Figure 19 illustrates the application of MD6605 in BLDC motor control for industrial and home appliance sectors. While conventional IPMs (Intelligent Power Modules) integrate power devices and gate drivers, the digital IPM with MD6605 adds advanced motor control capabilities such as speed and torque regulation.

Thanks to its high processing performance, MD6605 enables simultaneous motor and power control (e.g., PFC control).

Key features of the digital IPM with MD6605 include:

1. Sensorless vector control and auto self-alignment function for automatic motor parameter extraction and optimal control
2. Adjustable dv/dt of gate-drive waveforms for noise reduction
3. Reduced component count and PCB size through integrated motor and power control

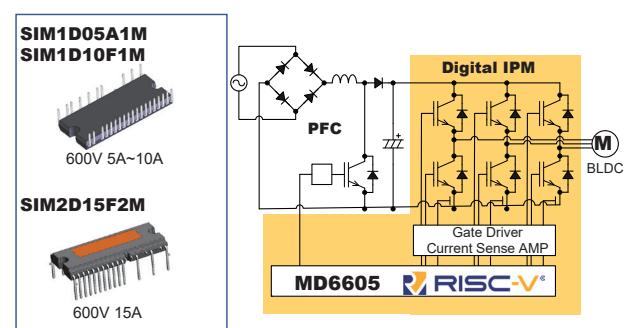


Figure 19. Application Example of MD6605 in Motor Control

4. GUI-based application for automatic motor parameter tuning, improving development efficiency
5. Intelligent features, including communication, fault detection, and fault prediction

13. Conclusion

Sanken Electric has developed the MD6605 microcontroller for advanced power electronics control systems, featuring a RISC-V CPU core and ReRAM non-volatile memory technology built on a 22nm ultra-low-leakage process. Its heterogeneous multi-core architecture, comprising CPU, DSP, and EPU cores, delivers exceptional processing performance.

Looking ahead, Sanken will continue to expand its lineup of high-efficiency IC products based on MD6605, contributing to GX (Green Transformation) initiatives aimed at achieving a decarbonized society.

References

1. *The RISC-V Instruction Set Manual Volume I: Unprivileged Architecture*, May 2025, RISC-V International.
2. *The RISC-V Instruction Set Manual Volume II: Privileged Architecture*, May 2025, RISC-V International.

Development of MOSFET Module SAM4L10M30Z1 for 48V Automotive

Seiji Suzuki*

Abstract

In recent years, the electrification of automobiles has led to the development of various powertrains. Among them, 48V mild hybrid electric vehicles (48V MHEVs), which are in high demand particularly in Europe, have attracted attention. Sanken Electric (hereinafter referred to as “the Company”) has developed a 100V low-voltage three-phase MOSFET module, SAM-4L10M30Z1, designed for use in electric compressors installed in 48V MHEVs. To achieve both the required performance and compact packaging, it is essential to reduce the on-resistance of the MOSFET and optimize the module’s package structure. This paper introduces the performance and development status of this product, which is currently under development.

1. Introduction

As automotive electrification progresses, long-term forecasts suggest a continued shift toward electric vehicles (EVs). In the short term, however, while environmental awareness has led to resistance against internal combustion engine vehicles (ICEs), concerns over the high cost and limited driving range of battery electric vehicles (BEVs) have caused some users to hesitate in purchasing them. As a result, demand for hybrid electric vehicles (HEVs) has been increasing to meet these needs. Among them, 48V mild hybrid electric vehicles (48V MHEVs), which use a 48V power supply, are particularly popular in Europe.

Globally, voltages above DC60V are considered hazardous to the human body and are subject to strict safety standards, which in turn increase costs. Therefore, 48V MHEVs were developed under the concept of reducing CO₂ emissions while keeping costs low. To enter this MHEV market, which can also accommodate future fluctuations in BEV demand, the Company has developed the 100V low-voltage three-phase MOSFET module SAM4L10M30Z1.

In developing this product, customers have requested a compact module package. To meet this requirement, it is necessary to reduce the on-resistance of the MOSFET to support high current while minimizing chip size, and to adopt a package structure with excellent heat dissipation.

This paper discusses the background of the low on-resistance MOSFET and high heat dissipation package design, as well as the product’s performance, features, and development status.

2. Market Background

As of 2025, the production ratio of powertrains in the automotive market (see Figure 1) shows that ICEs account for approximately 60% of total vehicle production. In contrast, the combined share of BEVs, range extender EVs (REEV), and fuel cell electric vehicles (FCEVs) is slightly less than 20%. The remaining slightly more than 20% is occupied by other powertrain types, indicating that ICEs still dominate production.

Future projections suggest a gradual shift toward electrification through 2033, and the market for MHEVs, which are the target of this product, is expected to grow steadily. Furthermore, by around 2027, the share of electrified vehicles is forecasted to surpass that of ICEs.

* Engineering Development Headquarters, Power Module Development Division, Intelligent Power Module Development Department, Development Section 2

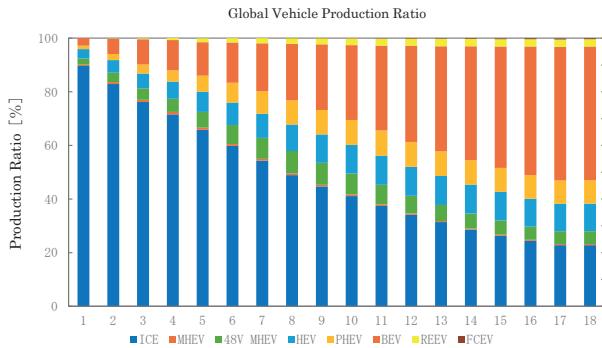


Figure 1. Forecast of Global Vehicle Production Ratio by Powertrain (2023-2033)

Source: Data prepared by MarkLines, "Forecast of Powertrain Composition Ratios in Global Light Vehicle Sales" (Accessed October 2025) ⁽¹⁾

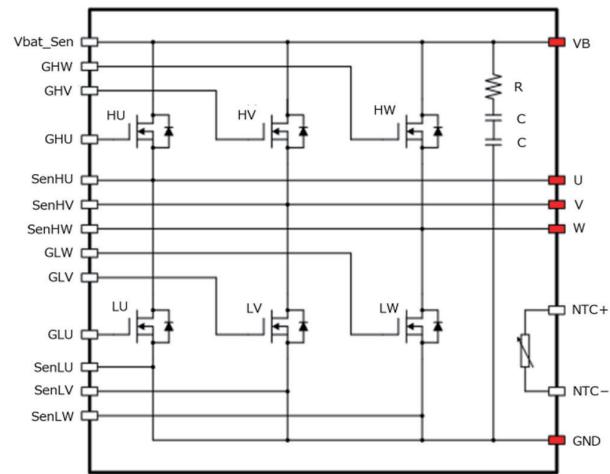


Figure 3. Internal Block Diagram

3. Product Overview

The development concept of this product is to expand the Company's portfolio for automotive applications using 48V power systems, while also addressing potential fluctuations in future BEV demand. The target application is 48V automotive compressors, and the product is a low-voltage three-phase MOSFET module incorporating six low-voltage power MOSFET elements. The specifications of this product are shown in Tables 1, 2, and 3, and Figures 2 and 3.

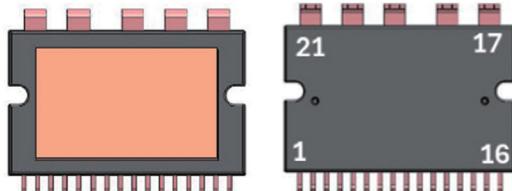


Figure 2. External Appearance Illustration

Table 1. Absolute Maximum Ratings

symbol	Parameter	Condition	SAM4L10M30Z1			unit
			Min	Typ	Max	
V_{DS}	Drain-to-Source Voltage	$I_D = 1\text{mA}, V_{GS} = 0\text{V}$	(100)	—	—	V
V_{GS}	Gate-to-Source Voltage	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	—	—	(5)	μA
E_{AS}	Single Pulse Avalanche Energy ($I_{AS} = 50\text{A}$)		T.B.D.			mJ
$T_j(\text{max})$	Maximum Operating Junction Temperature		175			°C
T_{STG}	Storage Temperature		-45 to 175			°C
$V_{\text{ISO}}(\text{RMS})$	Isolation Voltage		2500			V

Table 2. Electrical Characteristics

symbol	Parameter	Condition	SAM4L10M30Z1			unit
			Min	Typ	Max	
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 1\text{mA}, V_{GS} = 0\text{V}$	(100)	—	—	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	—	—	(5)	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}$	—	—	(± 100)	nA
V_{GSOH}	Gate Threshold Voltage	$V_{DS} = 10\text{V}, I_D = 1\text{mA}$	(2.0)	(3.0)	(4.0)	V
$R_{\text{DS(ON)}} \text{ HV}$	Drain-Source On-Resistance (High-Side V Phase)	$I_D = 150\text{A}, V_{GS} = 10\text{V}$	—	(2.05)	(2.75)	$\text{m}\Omega$
V_{DS}	Drain-Source Diode Forward Voltage Drop	$V_{GS} = 0\text{V}, I_S = 100\text{A}$	—	(0.85)	(1.3)	V
$R\theta_{\text{JC}}$	Junction-to-Case Thermal Resistance		—	(0.26)	(0.36)	°C/W

Table 3. Pin Assignment

Pin Number	Pin Name	Function
1	NTC+	NTC Thermistor Pin 1
2	NTC-	NTC Thermistor Pin 2
3	SenLW	Low-Side W-Phase Sense Pin
4	GHW	High-Side W-Phase Gate Pin
5	SenHW	High-Side W-Phase Sense Pin
6	GLW	Low-Side W-Phase Gate Pin
7	SenLV	Low-Side V-Phase Sense Pin
8	GHV	High-Side V-Phase Gate Pin
9	SenHV	High-Side V-Phase Sense Pin
10	GLV	Low-Side V-Phase Gate Pin
11	GLU	Low-Side U-Phase Gate Pin
12	SenLU	Low-Side U-Phase Sense Pin
13	SenHU	High-Side U-Phase Sense Pin
14	GHU	High-Side U-Phase Gate Pin
15	Vbat Sen	Vbat Sense Pin
16	Vbat Sen	Vbat Sense Pin (Shared: 15, 16)
17	VB	Battery Voltage Pin
18	GND	Ground Pin
19	U	U-Phase Output Pin
20	V	V-Phase Output Pin
21	W	W-Phase Output Pin

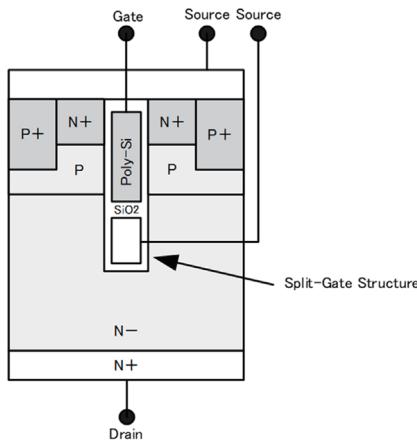


Figure 4. Cell Structure Diagram of ZeroMos

In addition to the VFP structure, optimization of cell pitch and implementation of wafer thinning technology further reduce on-resistance compared to conventional MOSFET structures. These improvements contribute to the miniaturization of the MOSFET chip and, consequently, the module package.

4.2 Built-in RC Filter Circuit

The product incorporates an RC filter circuit between VB and GND, composed of resistors and capacitors (see Figure 3). This filter effectively suppresses surge voltage, switching noise, and ringing. By integrating the filter circuit within the package, the need for external filtering on the customer side is reduced, contributing to cost savings.

4.3 Built-in Thermistor Function

The product includes a thermistor function between terminals 1 and 2. Customers require temperature monitoring close to the chip, and by integrating the thermistor within the package, early detection of abnormal heating and prevention of thermal damage to the system are made possible.

4.4 Adoption of High Heat Dissipation DBC Structure

The package employs a Direct Bonding Copper (DBC) structure with excellent heat dissipation properties, achieving low thermal resistance (see Table 2).

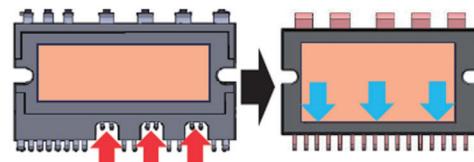
4.5 Package Design Changes from Previous Products

This product is based on the package design of the Company's previous automotive high-voltage three-phase brushless motor driver series, SAM470xx (DIP27). However, the DIP27 package could not accommodate the larger ZeroMos chip size.

To address this, the new package design retains the compact form factor of DIP27 while implementing the following changes:

- First, the staggered layout used to secure creepage distance for high-voltage applications was eliminated, as it is unnecessary for this low-voltage product (see Figure 5).
- Second, the internal stage for mounting a control chip (MIC), which was present in previous products, was removed since this product does not include a control chip.

These changes allowed for an expanded DBC substrate area, enabling the integration of the ZeroMos chip.



(a) Conventional Product Package (b) Newly Developed Product Package

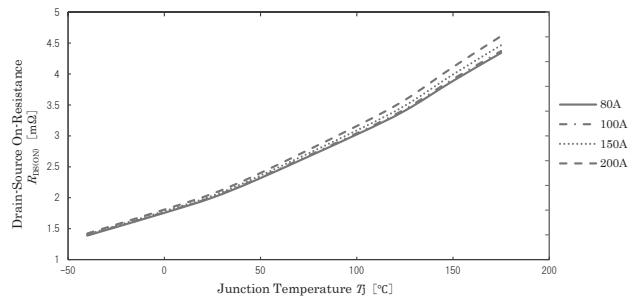
Figure 5. Diagram of Changes from SAM470xx Package

5. Evaluation Results

This section presents selected evaluation results for the product currently under development.

5.1 Temperature Characteristics of $R_{DS(ON)}$

To verify the performance of the low on-resistance ZeroMos described in Section 4.1, temperature characteristics of $R_{DS(ON)}$ were measured and plotted (see Figure 6). The results confirmed that the $R_{DS(ON)}$ value at 25°C meets the specified requirements (see Table 2).



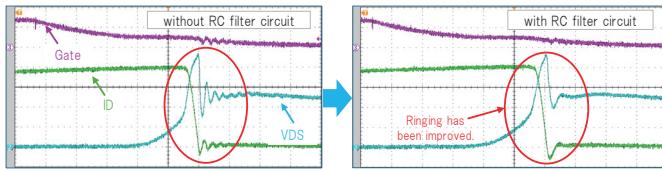
Conditions : Measurement Phase = Hi-Side V Phase, $V_{GS} = 10V$, $I_D = 80A$ to $200A$, $T_J = -40^{\circ}C$ to $175^{\circ}C$

Figure 6 Temperature Characteristics of $R_{DS(ON)}$

5.2 Effectiveness of RC Filter

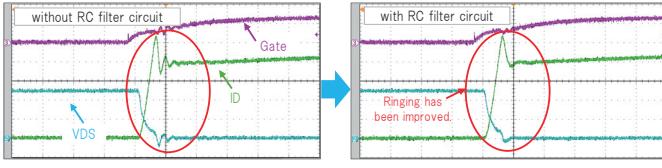
To evaluate the effectiveness of the built-in RC filter described in Section 4.2, switching characteristics were compared with and without the filter. The results are shown in **Figures 7 and 8**.

The results showed improved ringing during both turn-off and turn-on operations, confirming the effectiveness of the RC filter.



Conditions : Verification Phase = Low-Side V Phase, $V_B = 48V$, $V_{GS} = 15V$, $L_p = 14\mu F$, $T_a = 25^\circ C$, Filter Constants = $2.20 + 0.047\mu F + 0.047\mu F$ (with and without)

Figure 7. Switching Waveform at Turn-Off

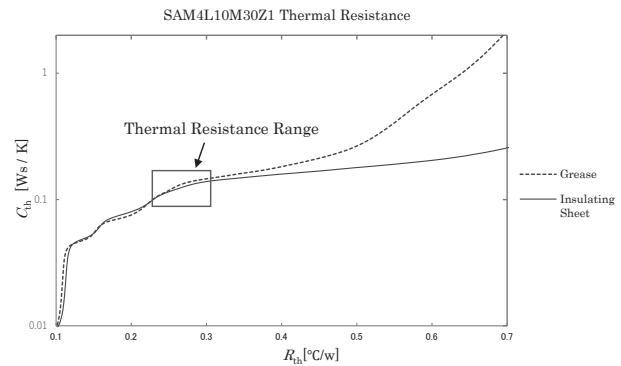


Conditions : Verification Phase = Low-Side V Phase, $V_B = 48V$, $V_{GS} = 15V$, $L_p = 14\mu F$, $T_a = 25^\circ C$, Filter Constants = $2.20 + 0.047\mu F + 0.047\mu F$ (with and without)

Figure 8. Switching Waveform at Turn-On

5.3 Thermal Resistance Evaluation

To verify the performance of the high heat dissipation DBC substrate described in Sections 4.4 and 4.5, thermal resistance evaluation was conducted. The results are shown in **Figure 9**. Post-evaluation structural function analysis confirmed that the boundaries of grease and insulation sheet were clearly identified within the graph, indicating compliance with the specifications (see **Table 2**).



Conditions : Measurement Phase = Hi-Side W Phase,
Sample Mounting = Two Conditions : with Grease and with Insulating Sheet

Figure 9. Structure Function Graph

6. Conclusion

This paper introduced the product SAM4L10M30Z1, currently under development, and presented its evaluation results. The evaluation confirmed that the product meets its specifications. Reliability tests such as AQG324 and AEC101 are planned for future development.

The results of the current and upcoming evaluations will be reflected in product development to deliver higher-quality products to customers.

References

- (1) MarkLines, "Forecast of Powertrain Composition Ratios in Global Light Vehicle Sales," MarkLines Official Website, https://www.marklines.com/portal_top_ja.html
- (2) Kondo, Tanaka: Sanken Technical Report, vol. 53, p.47, (November 2021)

Development of Power Devices for Automotive 1200V IPM Series

Takaaki Ishii*

Hayato Yamada*

Abstract

We have developed the SAM2 series of intelligent power modules (IPMs), which integrate power devices, control ICs equipped with drive and protection functions, and temperature-sensing thermistors within a transfer-molded package. These modules contribute to the miniaturization and improved energy efficiency of inverter units used for motor control in automotive and industrial air-conditioning systems. To address increasingly diverse market requirements, we are expanding our product lineup to include devices rated at 1200 V. This paper presents newly developed 1200V power devices intended for automotive applications and the corresponding SAM2 modules that incorporate these devices, designed specifically for electric water-pump driver systems.

1. Introduction

Power devices are semiconductor switching components used to control, convert, and distribute electrical power. As environmental concerns continue to intensify, the importance of power devices in power electronics — technologies that facilitate the efficient utilization of energy resources — has grown significantly.

We have focused on developing power device processes centered around the 600V class, and has produced products incorporating in-house IGBTs and FRDs. These products have been commercialized across a wide range of applications, from consumer electronics such as air conditioners and IH heaters to industrial equipment like inverters and UPS systems, as well as automotive applications.

Leveraging the technologies and experience cultivated through the development of IPMs for consumer air conditioners, we have commercialized the SAM2 series — transfer-molded IPMs equipped with high-voltage, high-current power devices, control ICs, and thermistors — for industrial and automotive air conditioning systems⁽¹⁾.

To meet the growing demand for product diversity and expanded applications, we have also developed 1200V-class power devices and associated packaging technologies, and have launched 1200V-rated SAM2 products for industrial equipment⁽²⁾.

Table 1 shows the SAM2 series products, and **Figure 1** illustrates the development trends for automotive SAM2 series.

In recent xEVs (electric vehicles), systems that circulate coolant using electric water pumps have emerged. To add SAM2 power modules for controlling these systems to our lineup, we are developing 1200V IGBTs and FRDs with rated currents of 15A or less. For water pump cooling system applications, low-loss characteristics and high-response drive performance are required.

Table 1. SAM2 series products

Product name	Specification	Application	Status
SAM265M30AA1	650V/30A	Automotive	In Mass Production
SAM265M50AA1	650V/50A	Automotive	In Mass Production
SAM265M50BS3	650V/50A	Industrial	In Mass Production
SAM265M50AS3	650V/50A	Automotive	In Mass Production
SAM212M05BF1	1200V/5A	Industrial	In Mass Production
SAM212M10BF1	1200V/10A	Industrial	In Mass Production
SAM212M15BF1	1200V/15A	Industrial	In Mass Production
SAM212M05AF1	1200V/5A	Automotive	Under Development
SAM212M10AF1	1200V/10A	Automotive	Under Development
SAM212M15AF1	1200V/15A	Automotive	In Mass Production
SAM212M25AF1	1200V/25A	Automotive	Under Development

* Engineering Development Headquarters, Process Engineering Division, Advanced Power Device Development Department, Product Development Section

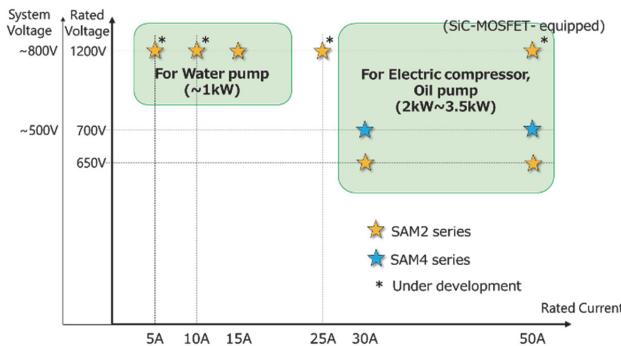


Figure 1. Development trends for automotive SAM2 series

2. Product Overview

The SAM2 products are three-phase inverter IPMs with a transfer-molded structure, incorporating IGBTs and FRDs as output switching elements, pre-driver ICs, bootstrap diodes with limiting resistors, and temperature-sensing thermistors. Figure 2 shows the appearance of SAM2 series products. The package design ensures sufficient insulation distance to support the 1200V rating.

Key features common to the SAM2 series include:

- Maximum control voltage rating: 25V
- Insulation withstand voltage: 2500V (1 minute)
- Built-in thermistor
- Various protection functions
- Adjustable overcurrent protection hold time
- Guaranteed operating temperature for IGBT and FRD: $T_j = 175^\circ\text{C}$

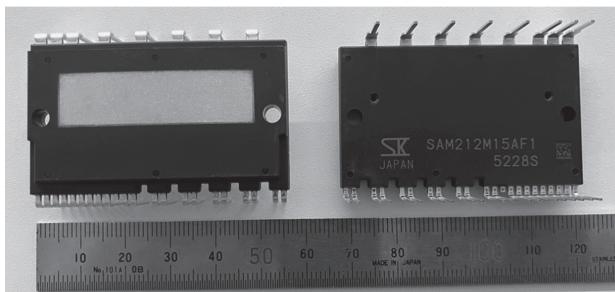


Figure 2. Appearance of SAM2 Series Products

Figure 3 shows a typical application circuit using a single shunt resistor for the automotive 1200V/15A-rated product SAM212M15AF1. The IGBTs are driven by signals from the controller on the left side of the diagram, enabling control of high voltage and high current. This allows the conduction state and current direction of the motor output terminals U, V, and W to be changed, enabling motor drive tailored to the customer's usage conditions.

The product also includes system-supporting features such as overcurrent protection and temperature monitoring via the built-in thermistor. These features enable feedback to the controller, which is a key characteristic of the product.

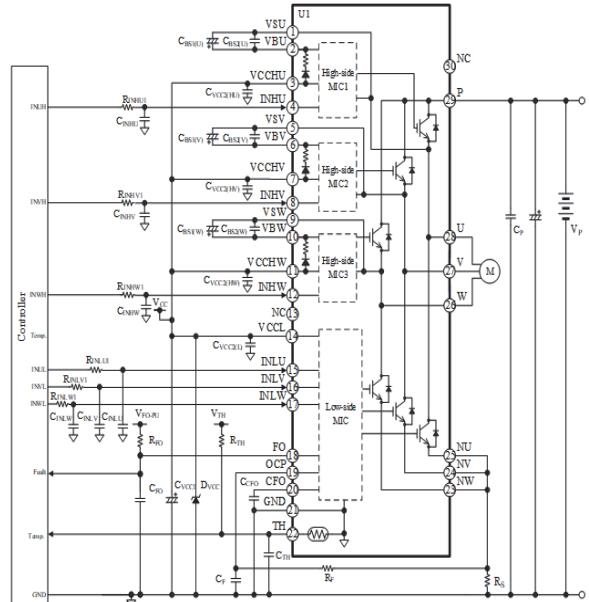


Figure 3. Typical Application Circuit using a Single Shunt Resistor

3. Development of 1200V Power Devices

3.1 1200V FS-IGBT Chip Technology

For the 1200V-rated IGBT, we adopted a Field Stop (FS) structure by thinning the wafer, established a stable thinning process, refined and optimized the trench gate structure, and improved the backside structure⁽³⁾. These efforts enabled both high withstand voltage and low loss characteristics. As a result, we have begun mass production of current-rated SAM2 products for industrial applications. The features of the 1200V FS-IGBT for automotive use are described in the following section.

3.2 Features of Automotive 1200V FS-IGBT

(A) Rated Voltage Guarantee at Low Temperatures

In automotive applications, products must operate reliably under harsh conditions, including low temperatures down to -40°C . At low temperatures, lattice vibrations in the silicon crystal decrease, increasing the probability of impact ionization due to collisions between electrons and atoms. This result leads to a reduction in device withstand voltage. To address this, we optimized the thickness of the N drift layer in the IGBT structure to maintain withstand voltage even at low temperatures.

(B) High-Temperature Operation Guarantee**($T_{j\max} = 175^\circ\text{C}$)**

To ensure stable operation under high-temperature conditions, the junction temperature (T_j) of the IGBT is guaranteed up to 175°C . **Figure 4** shows relationship between the junction temperature (T_j) and the collector-to-emitter leakage current (I_{CES}) of a single IGBT chip at rated voltage 1200 V. Since excessive leakage current at high voltage can lead to thermal runaway, it is a critical indicator for ensuring the quality and reliability of power devices. In the development of 1200V SAM2 products, we optimized the chip structure to suppress leakage current even when T_j exceeds 175°C . As shown in **Figure 4**, the leakage current of the IGBT chip at 190°C is approximately 3mA, confirming that thermal runaway does not occur.

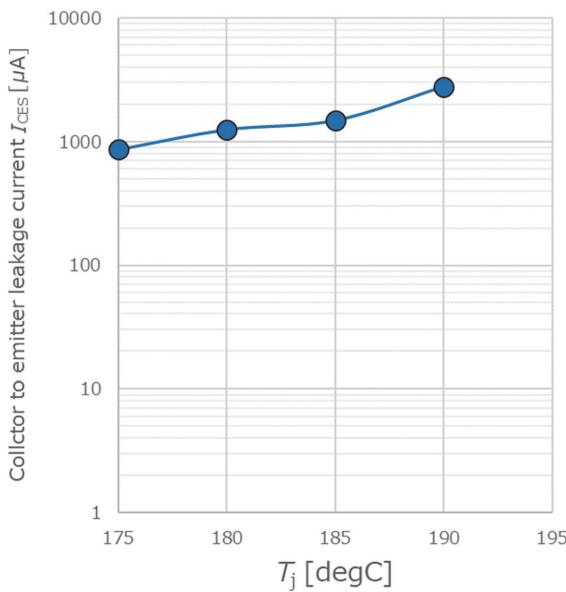


Figure 4. Collector-to-Emitter Leakage Current (I_{CES}) vs. Junction Temperature (T_j) at Rated Voltage 1200V for Single IGBT Chip

(C) Safe Operating Area Guarantee During Short-Circuit Conditions

IGBTs handle large amounts of power, so while reducing on-state voltage and turn-off switching losses, it is also necessary to ensure sufficient ruggedness. In cases of short circuits or failure of other components, the IGBT must withstand the current until the gate voltage is shut off by the protection circuit. By utilizing the current saturation characteristics of the IGBT, adjusting the channel region corresponding to the surface N-emitter layer, and optimizing the MOS structure, we suppressed the saturation current and ensured the required ruggedness.

(D) Approach to Automotive Quality Assurance

For automotive products, we conduct risk analysis on critical characteristics related to quality and safety, as well as customer requirements. Technical elements related to high-impact items are reflected in product design and specifications. In manufacturing, we manage key process parameters using Statistical Process Control (SPC). This approach enables not only the early detection and prevention of anomalies but also daily monitoring of process variation and control of process capability, thereby contributing to stable product quality.

3.3 1200V FRD Chip Technology

For the 1200V-rated FRD, a low-concentration anode structure was adopted, based on the active region structure of our 600V low-noise FRD⁽⁴⁾. By implementing lifetime control techniques, both low loss and soft recovery characteristics were achieved. The features of the 1200V FRD for automotive applications are described in the next section.

3.4 Features of Automotive 1200V FRD**(A) Soft Recovery Characteristics**

Figure 5 shows the active region structure of the 1200V automotive FRD. To suppress switching noise in the product, the bottom of the drift layer was designed with a gentle concentration gradient in the N layer, which moderates abrupt carrier disappearance and enables soft-recovery behavior. The low-concentration anode structure suppresses hole injection, and optimization of lifetime control through particle irradiation contributes to reduced losses.

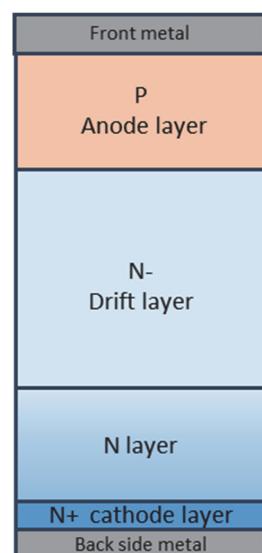


Figure 5. Active region structure of 1200V automotive FRD

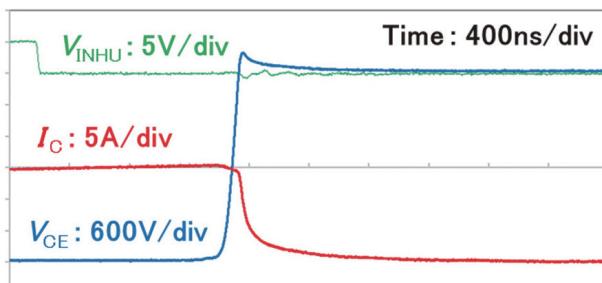
(B) Rated Voltage Guarantee at Low Temperatures and Suppression of Forward Recovery Voltage

To maintain rated voltage at -40°C , the N drift layer must be thickened. However, this increases the forward recovery voltage⁽²⁾. When IGBT is turned off, carriers are injected into the high-resistance N drift layer of the FRD, and conductivity modulation gradually lowers the resistance. Immediately after turn-off, the resistance remains high, causing the forward recovery voltage to rise. This voltage can be applied as a negative potential to the high-side driver IC, potentially causing malfunction. Therefore, the thickness and carrier concentration of the N layer were optimized to balance low-temperature withstand voltage retention with suppression of the forward recovery voltage.

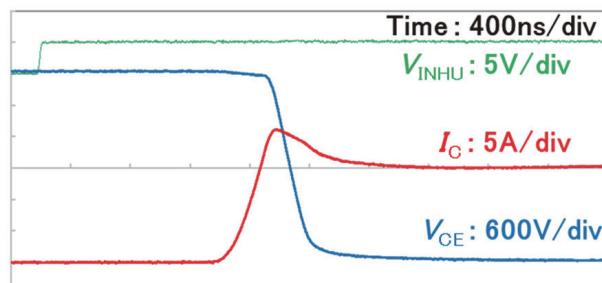
4. Product Evaluation Results

4.1 Switching and Electrical Characteristics

Switching tests were conducted on the automotive-grade SAM2 product, SAM212M15AF1, rated at 1200V/15A. The test waveforms are shown in Figure 6. Stable high-temperature operation was confirmed at a junction temperature of $T_j = 175^{\circ}\text{C}$. The switching losses and soft recovery characteristics met the product targets. Detailed electrical characteristics are summarized in Table 2.



(a) High-side switching turn-off waveform



(b) High-side switching turn-on waveform

Vertical axis : V_{INHU} , V_{CE} , I_{C} , Horizontal axis : Time
Conditions : $V_{\text{P}} = 600\text{V}$, $V_{\text{CC}} = 15\text{V}$, $I_{\text{C}} = 15\text{A}$, $T_j = 175^{\circ}\text{C}$

Figure 6. Switching waveforms

4.2 Conducted Noise Characteristics

The influence of current and voltage generated by inverter switching operations was evaluated across various frequency bands. The conducted noise characteristics are shown in Figure 7. The product complies with the CISPR22 Class B standard, confirming that the balance between switching losses and noise performance has been appropriately optimized.

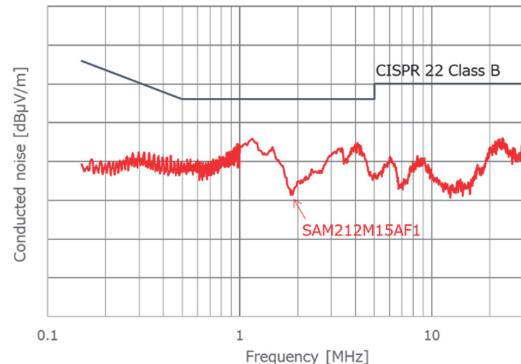
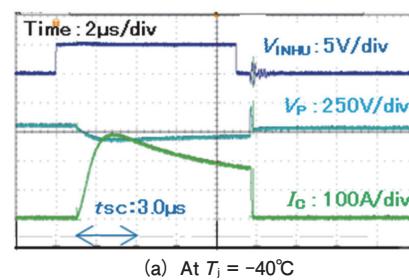


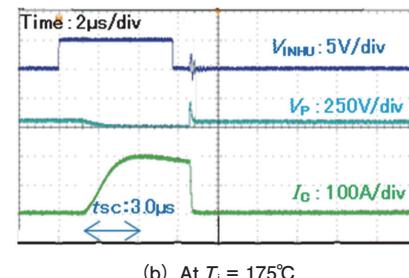
Figure 7. Conducted noise characteristics

4.3 Short-Circuit Testing

Figure 8 shows the waveforms from short-circuit testing. Under both low-temperature (-40°C) and high-temperature (175°C) conditions, the product withstood short-circuit current without damage during the short-circuit current duration of $t_{\text{sc}} = 3.0\mu\text{s}$, which is the target value. This confirms that sufficient short-circuit ruggedness is ensured across the full temperature range.



(a) At $T_j = -40^{\circ}\text{C}$



(b) At $T_j = 175^{\circ}\text{C}$

Vertical axis : V_{INHU} , V_{P} , I_{C} , Horizontal axis : Time
Conditions : $V_{\text{P}} = 800\text{V}$, $V_{\text{CC}} = 16.5\text{V}$

Figure 8. Short-circuit waveforms

Table2. Transistor characteristics of SAM12M15AF1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	$V_{CE} = 1200 \text{ V}, T_j = 25 \text{ }^\circ\text{C}$	—	—	0.1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(\text{SAT})}$	$I_C = 15 \text{ A}, T_j = 25 \text{ }^\circ\text{C}$	—	1.7	2.2	V
		$I_C = 15 \text{ A}, T_j = 125 \text{ }^\circ\text{C}$	—	2.1	2.7	V
Diode Forward Voltage Drop	V_F	$I_F = 15 \text{ A}, T_j = 25 \text{ }^\circ\text{C}$	—	2.1	2.6	V
High-side Switching Characteristics						
Diode Reverse Recovery Time	t_{rr}	$V_{P(\text{DC})} = 600 \text{ V}, I_C = 15 \text{ A}, V_{IN} = 0 \leftrightarrow 5 \text{ V}, T_j = 25 \text{ }^\circ\text{C}$, Inductive load	—	0.50	—	μs
Turn-on Time	t_{ON}		—	1.25	—	μs
Turn-on Switching Time	$t_{C(ON)}$		—	0.45	—	μs
Turn-off Time	t_{OFF}		—	1.30	—	μs
Turn-off Switching Time	$t_{C(OFF)}$		—	0.30	—	μs
Low-side Switching Characteristics						
Diode Reverse Recovery Time	t_{rr}	$V_{P(\text{DC})} = 600 \text{ V}, I_C = 15 \text{ A}, V_{IN} = 0 \leftrightarrow 5 \text{ V}, T_j = 25 \text{ }^\circ\text{C}$, Inductive load	—	0.45	—	μs
Turn-on Time	t_{ON}		—	0.90	—	μs
Turn-on Switching Time	$t_{C(ON)}$		—	0.45	—	μs
Turn-off Time	t_{OFF}		—	0.90	—	μs
Turn-off Switching Time	$t_{C(OFF)}$		—	0.30	—	μs

4.4 Reliability Evaluation

The SAM212M15AF1 automotive-grade SAM2 product, rated at 1200V/15A, underwent comprehensive reliability evaluations conducted in accordance with the guidelines of IEC, JEITA, and AQG324. The results confirmed that the product meets all required standards without any issues.

5. Conclusion

To support the integration of IPM motor driver products for automotive applications, we developed new 1200V power devices — IGBTs and FRDs. As a result, we commercialized the SAM2 product SAM212M15AF1, rated at 1200V/15A, thereby expanding the SAM2 series lineup.

Moving forward, we plan to sequentially mass-produce products with current ratings comparable to those for industrial equipment. In addition, we will continue to develop power devices and packaging technologies to further expand the lineup of 1200V-rated IPM products for high-current applications.

References

- (1) Takayama, Asami, Ono: Sanken Technical Report, Vol. 53, pp. 21–24, Nov. 2021
Development of SAM265M30AA1 and SAM265M50AA1
- (2) Cho, Kuga: Sanken Technical Report, Vol. 54, pp. 9–12, Nov. 2022
Development of Industrial Motor Driver IPM SAM212M10BF1
- (3) Ishii: Sanken Technical Report, Vol. 52, pp. 17–20, Nov. 2020
Development of 1200V FS-IGBT
- (4) Minamino: Sanken Technical Report, Vol. 50, pp. 39–42, Nov. 2018
Development of Low-Noise FRD FMXR-1206S

High-Speed Driving and Short-Circuit-Free Protection Technology for Smart SiC-IC

Kaito Yokoi*

Osamu Machida**

Abstract

SiC-MOSFETs offer high breakdown voltage and compact size, enabling high-current and high-speed switching in high-voltage circuits. In particular, using a gate-source terminal that does not carry main current allows for low-inductance gate control, achieving fast switching.

However, when a short circuit occurs during high-voltage switching, SiC-MOSFETs experience extremely fast short-circuit currents of several thousand A/μs, leading to device failure in less than 1μs. When applying conventional 3-terminal (3P) driving, as used in Si-IGBTs, to SiC-MOSFETs, switching speed significantly decreases, but short-circuit current is limited, extending the short-circuit withstand time by several times.

This study developed a driving method that combines the fast switching of 4-terminal (4P) driving with the short-circuit protection of 3P driving.

1. Introduction

SiC has approximately ten times the breakdown electric field of Si, and when applied to high-voltage devices, it offers the potential to reduce device size to a fraction of conventional designs. However, simply replacing Si devices in circuits optimized for Si does not allow SiC to fully demonstrate its performance. Therefore, SiC devices must be properly designed and driven.

As shown in Figure 1, the National Institute of Advanced Industrial Science and Technology (AIST) has been developing SiC-MOSFETs with built-in SiC-CMOS gate drivers that enable ultra-fast switching. These chips minimize parasitic inductance in gate wiring by integrating CMOS gate drivers within the SiC-MOSFET chip. This technology has successfully achieved switching of 1200V in just a few nanoseconds^{(1), (2), (3), (4)}.

On the other hand, when such high-speed devices

are used in high-voltage circuits, various surge phenomena become problematic. Among them, surge current during short-circuit events is particularly critical. Due to the rapid switching, short-circuit current peaks in a very short time, potentially causing device destruction^{(5), (6), (7)}.

To address this issue, AIST and our company have been jointly developing gate driving technologies that can

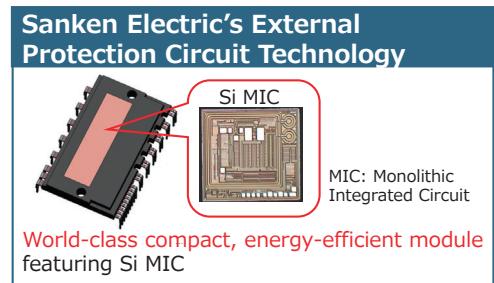


Figure 1. Overview of Joint Development with AIST

* Engineering Development Headquarters, Process Engineering Division

** Engineering Development Headquarters, Process Engineering Division, GaN Device Development Department, GaN Device Development Section

safely protect against short circuits, aiming to realize “SiC-MOSFETs that enable ultra-fast switching with simple operation.”

2. Relationship Between High-Speed Switching and Short-Circuit Withstand Capability

Figure 2 shows the circuit used for short-circuit evaluation of SiC-MOSFETs. The DUT (Device Under Test) includes a sense source (SS) terminal that does not carry source current, allowing switching between the SS and standard source (S) terminals for evaluation.

Figure 3 presents typical short-circuit current waveforms of SiC-MOSFETs with gate resistances $R_g = 470\Omega$ and $R_g = 10\Omega$, respectively. The gate is driven via the S

terminal using 3P driving. The SiC-MOSFET used has a rating of 1200V and 40mΩ, and the test simulates a short-circuit condition at $V_d = 600V$.

When switching with $R_g = 470\Omega$, the current peaks around $3\mu\text{s}$ and then decreases due to self-heating, potentially leading to device failure in low withstand devices. In contrast, with $R_g = 10\Omega$, switching speed increases, causing the short-circuit current to peak at around $2\mu\text{s}$ with a higher amplitude. The current then rapidly decreases due to temperature rise.

Short-circuit failure is caused by the energy consumed, which is the product of short-circuit current, voltage, and duration. As shown in **Figure 3**, reducing R_g increases switching speed, but also raises the risk of failure due to faster current peaking.

3. Comparison of 4P and 3P Driving

In compound semiconductors such as SiC, 4-terminal packages with a gate-source terminal (SS) that does not carry source current are commonly used to enable high-speed switching (see **Figure 2**).

4P driving minimizes parasitic inductance and enables fast switching, but short-circuit withstand time is reduced, increasing the risk of failure. On the other hand, 3P driving suppresses current changes due to voltage generated by parasitic inductance, offering better short-circuit tolerance but slower switching.

To address the issue of extremely short short-circuit withstand time caused by high-speed switching, we developed a technique that switches between 4P and 3P source terminal connections.

During switching, the gate driver is connected to the

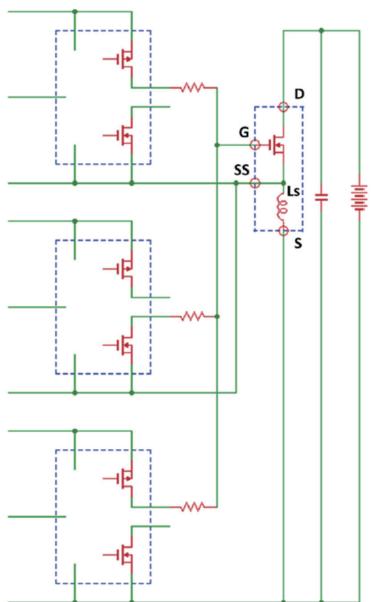
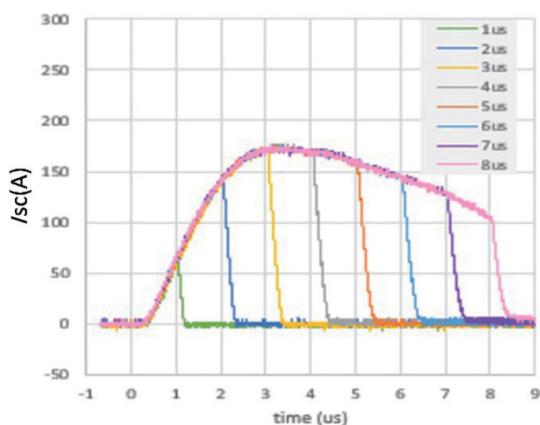


Figure 2. Short-Circuit Evaluation Circuit for SiC-MOSFET



(a) $R_g = 470 \Omega$

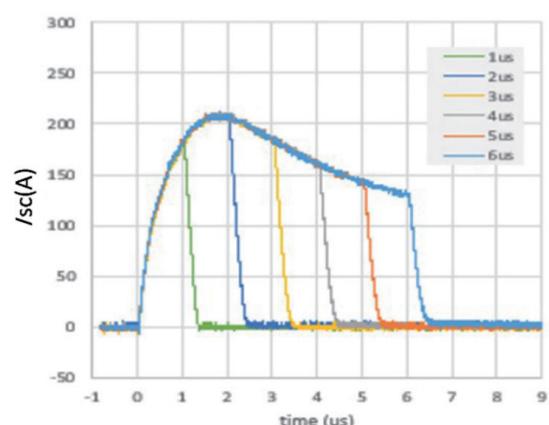


Figure 3. Typical Short-Circuit Current Waveforms of SiC-MOSFETs

SS terminal for 4P driving to achieve high-speed switching. Afterward, during steady-state operation, the connection is switched to the S terminal for 3P driving, which is expected to improve short-circuit tolerance.

By optimizing this switching method, we aim to achieve both the fastest possible switching and significantly extended short-circuit withstand time in SiC-MOSFETs.

4. Introduction of New Monolithic IC (MIC)

Figure 4 shows the evaluation board for SiC-MOSFETs using a MIC with 4P/3P switching capability. The MIC includes three channels for 4P driving and one channel for 3P driving.

The three 4P driving channels directly drive the gates of P-channel MOSFETs, N-channel MOSFETs, and power SiC-MOSFETs equipped with AIST's CMOS drivers, connected to SS terminals for 4P operation.

The remaining channel also directly drives the gate of a power SiC-MOSFET, but is connected to the S terminal for 3P operation.

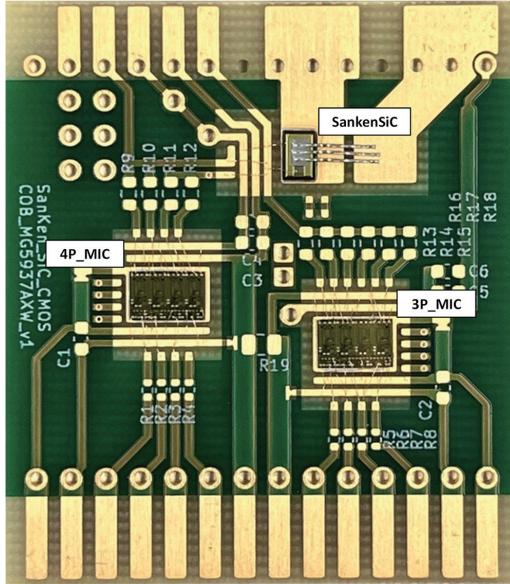


Figure 4. Photograph of SiC-MOSFET Short-Circuit Evaluation Board

This MIC is designed to detect short-circuit events by sensing the induced voltage (V_{ls}) generated by the parasitic inductance between SS and S terminals due to rapid di/dt of short-circuit current.

The MIC's output delay is approximately 300ns, and including the detection circuit delay (within 500ns), short-circuit protection can be achieved within 1 μ s.

Furthermore, when multiple SiC-MOSFETs are

driven in parallel, the MIC can detect short-circuit via V_{ls} in any device and synchronously shut down all devices.

Although the MIC is capable of driving AIST's CMOS-equipped SiC-MOSFETs with a single chip, the evaluation board uses two MIC chips for 4P and 3P driving respectively, to facilitate separate evaluation of high-speed switching and short-circuit protection.

Each channel's output allows independent Source and Sink control, enabling multi-stage switching of gate resistance (R_g) during both ON and OFF states for optimized switching performance.

5. Experimental Results

5.1. Short-Circuit Waveform in 4P Driving

Figure 5 shows the short-circuit current waveform when a short occurs in a high-speed switching circuit using 4P driving. The short-circuit current (I_{sc}) peaks at approximately 200ns, reaching around 600A. Subsequently, the current rapidly decreases due to device heating, and failure occurs within 1 μ s after the short-circuit event.

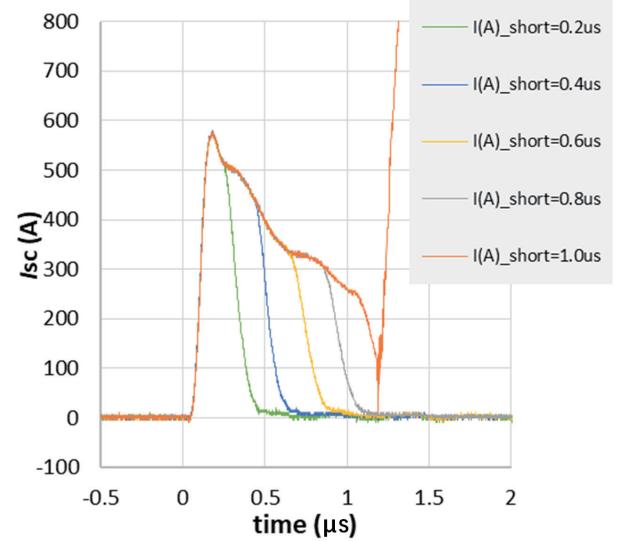


Figure 5. Short-Circuit Current Waveforms under 4P Configuration

5.2. Short-Circuit Protection and Issues in 4P/3P Switching

Figure 6 shows the short-circuit waveform during 4P/3P switching. In this method, both 4P and 3P are driven simultaneously, and 4P driving is turned off after 100ns, switching to 3P driving for protection.

During ON-state simultaneous driving, the large di/dt causes delayed gate voltage (V_g) rise. As a result, V_g

remains at 13V at 100ns, indicating that the gate voltage rise is suppressed due to the 3P driving effect under high di/dt conditions.

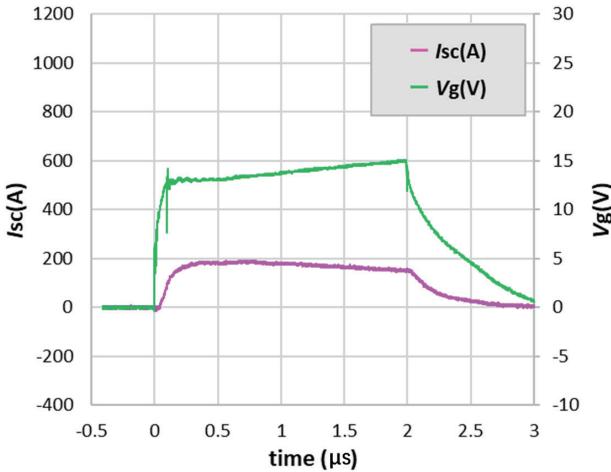


Figure 6. Short-Circuit Waveforms during 4P/3P Switching Operation

5.3. Improved Short-Circuit Protection in 4P/3P Switching

To improve the previous method, the initial state was set to 4P driving only, and 3P driving was activated after 4P driving was turned off.

Figure 7 shows the switching waveform under improved 4P/3P switching conditions. The steady-state driving current (I_{ds}) was set to 10A, and switching was performed on the low side of a half-bridge circuit.

Figure 8 shows the short-circuit waveform under the same driving conditions. During the short-circuit event, a negative voltage is induced in the source inductance (L_s)

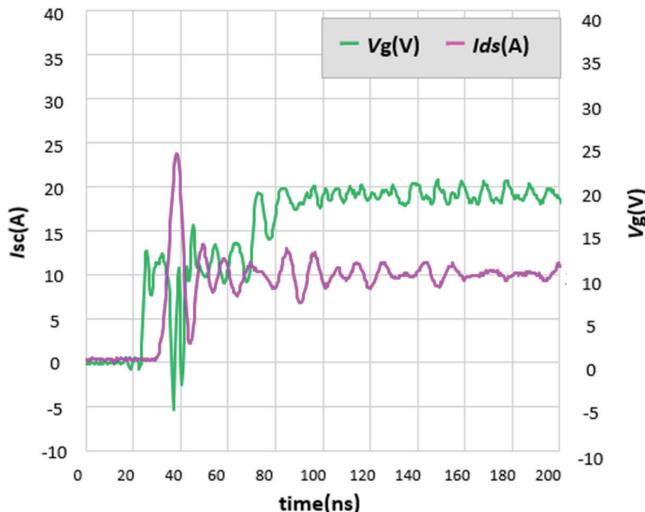


Figure 7. Switching Waveform Measurements under Improved 4P/3P Switching Conditions

due to the instantaneous large current. By switching to 3P driving before the gate voltage rises sufficiently, the gate voltage (V_g) during the short-circuit is suppressed, reducing the short-circuit current (I_{sc}).

As a result, short-circuit withstand capability was significantly improved compared to 4P driving alone.

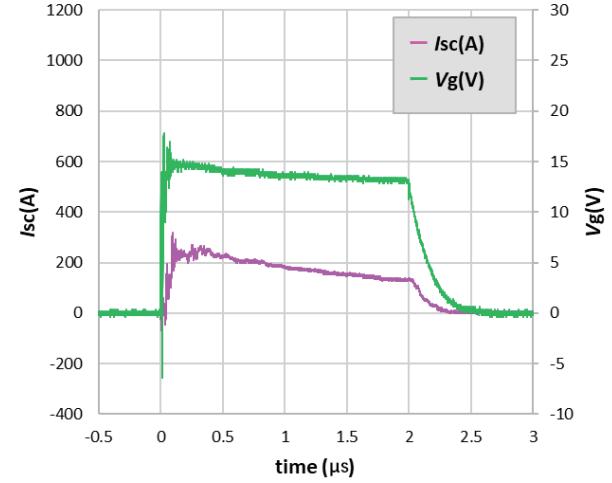
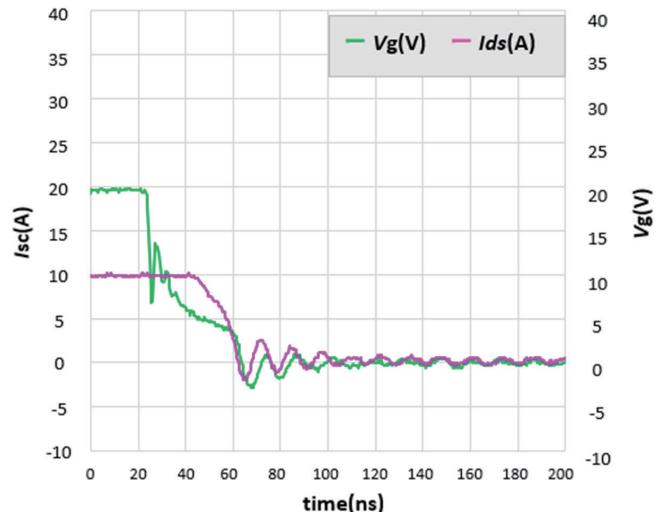


Figure 8. Short-Circuit Waveform Measurements under Improved 4P/3P Switching Conditions

6. Conclusion

This study examined the challenge of maintaining high-speed switching performance in SiC-MOSFETs while improving short-circuit tolerance, and demonstrated the effectiveness of 4P/3P switching.

As a result, the short-circuit withstand time of devices previously limited to 1μs under 4P driving was extended



to over 2μs using the 4P/3P switching method.

Based on these results, we will continue to pursue the realization of “SiC-MOSFETs that enable ultra-fast switching with simple operation.”

7. Acknowledgments

Part of this research was conducted under the commissioned project (Project No. JPNP14004) of the New Energy and Industrial Technology Development Organization (NEDO).

References

- (1) Atsushi Yao, “High-speed switching operation for a SiC CMOS and power module,” *IEICE Electronics Express*, Vol. 18, No. 14, pp. 1–5, 2021.
- (2) Atsushi Yao, “High-speed and high-temperature switching operations of a SiC power MOSFET using a SiC CMOS gate driver installed inside a power module,” *Solid State Phenomena*, Vol. 360, pp. 81–87, September 2024.
- (3) Mitsuo Okamoto, “First Demonstration of a Monolithic SiC Power IC Integrating a Vertical MOSFET with a CMOS Gate Buffer,” *Proceedings of the 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 71–74, 2021.
- (4) Atsushi Yao, “High-Speed and High-Temperature Switching Operations of a SiC Power MOSFET Using a SiC CMOS Gate Driver Installed inside a Power Module,” *Solid State Phenomena*, Vol. 360, pp. 81–87, 2024.
- (5) Anas El Boubkari, “CMOS Gate Driver with Integrated Ultra-Accurate and Fast Gate Charge Sensor for Robust and Ultra-Fast Short Circuit Detection of SiC Power Modules,” *Proceedings of the 2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Vol. 2023–May, pp. 68–71, IEEE, May 2023.
- (6) Zhiqiang Wang, “Design and Performance Evaluation of Overcurrent Protection Schemes for Silicon Carbide (SiC) Power MOSFETs,” *IEEE Transactions on Industrial Electronics*, Vol. 61, No. 10, pp. 5570–5581, October 2014.
- (7) Yuxiang Shi, “Switching Characterization and Short-Circuit Protection of 1200 V SiC MOSFET T-Type Module in PV Inverter Application,” *IEEE Transactions on Industrial Electronics*, Vol. 64, No. 11, pp. 9135–9143, 2017.

Development of Infrared Chip LED with Backside Light Leakage Suppression

Kosaku Noda*

Abstract

Due to the recent trend toward miniaturization of electronic devices, backside light leakage from infrared chip LEDs has become a significant issue. In this development, we successfully suppressed backside light leakage by changing the substrate material of the infrared chip LED to one with lower infrared transmittance. The newly developed infrared chip LED maintains compatibility with existing products in terms of external dimensions and mounting land patterns, eliminating the need for circuit board design changes on the user side. This paper reports on the characteristics and features of the developed LED.

1. Introduction

Our company offers a lineup of infrared LEDs for applications ranging from remote controls to proximity sensors. In recent years, demands for product miniaturization, circuit board downsizing, and power saving have led to reduced spacing between components. As a result, when LEDs and photodetectors are placed in close proximity, light leakage from areas other than the intended receiving section can no longer be ignored as optical noise.

Typically, optical noise is reduced by installing light-shielding covers on both the photodetector and LED sides. However, when the components are closely positioned, the circuit board itself can act as a light guide, making it difficult to achieve sufficient shielding.

In this development, we focused on light leakage from the LED to the circuit board and developed an infrared LED that prevents the circuit board from functioning as a light guide. This paper outlines the development.

2. Infrared LED with Backside Light Leakage Suppression

2.1 Development Concept

The goal of this development was to suppress light leakage without compromising the usability of existing LEDs. Specifically, we aimed to enable users to replace existing LEDs without modifying the circuit board's mounting pattern or resist layout.

2.2 Structure of Existing Infrared Chip LED

The basic structure of the existing infrared chip LED (hereafter referred to as the "existing LED") is shown in **Figure 1** and consists of a BT substrate, LED chip, wire, die attach, and encapsulating resin. The encapsulating

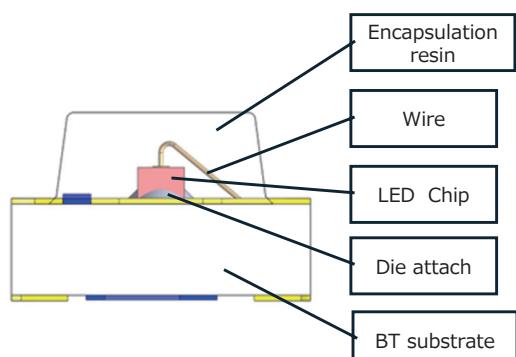


Figure 1. Structure of Existing Infrared Chip LED

* Engineering Development Headquarters, Power Device Development Division, Opto Engineering Department, LED Development Section

resin, which controls light distribution, is a colorless transparent epoxy resin with high transmittance.

The BT substrate is a white board composed of layered glass fibers impregnated with reflective material and BT (bismaleimide-triazine) resin. The BT substrate exhibits a high reflectance of over 90% in the visible to infrared light range. The remaining 10% is absorbed by the substrate, which contributes to backside light leakage.

2.3 Issues with Existing LED

When using the existing LED to detect a target object with a photodetector placed nearby on the same circuit board, the configuration is as shown in **Figure 2**. In this setup, part of the light emitted from the LED is transmitted as a signal and reflected by the target object, which is then received by the photodetector.

Simultaneously, light that undergoes multiple reflections within the encapsulating resin penetrates the BT substrate and propagates through the circuit board, appearing as optical noise on the photodetector side. While strong reflected light can mask this optical noise, weak reflected light makes the optical noise more prominent.

Therefore, it is necessary to suppress backside light leakage to a level where it can be ignored.

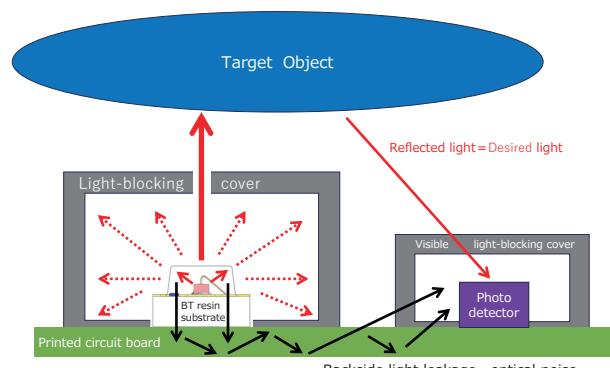


Figure 2. Conceptual Illustration of Backside Light Leakage

2.4 Consideration of Infrared Chip LED with Leakage Suppression

To suppress light leakage to the circuit board, we considered changing the substrate material of the infrared chip LED to one with lower infrared transmittance than the existing BT substrate.

Table 1 shows the evaluation levels. To verify the optical transmittance of each substrate, we used infrared light ($\lambda_p = 850$ nm) and measured the integrated spectral

value of light passing through a 2 mm diameter hole, as shown in **Figure 3**. The condition without any substrate was used as the reference spectrum.

As shown in **Table 1** and **Figure 4**, neither the existing BT substrate nor the Level 1 black substrate achieved a zero reference spectral ratio. Only the Level 2 black substrate, equivalent to FR5, achieved a zero ratio.

Table 1. Substrate Evaluation Levels

	Material	Color	Thickness	Reference spectral ratio
Current model	BT	White	0.5 mm	0.01%
Level 1	BT	Black	0.5 mm	0.15%
Level 2	Equivalent to FR-5 grade	Black	0.5 mm	0.00%

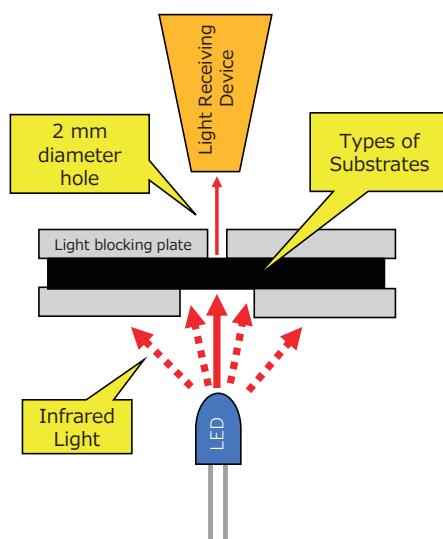


Figure 3. Method of Spectral Transmission Measurement

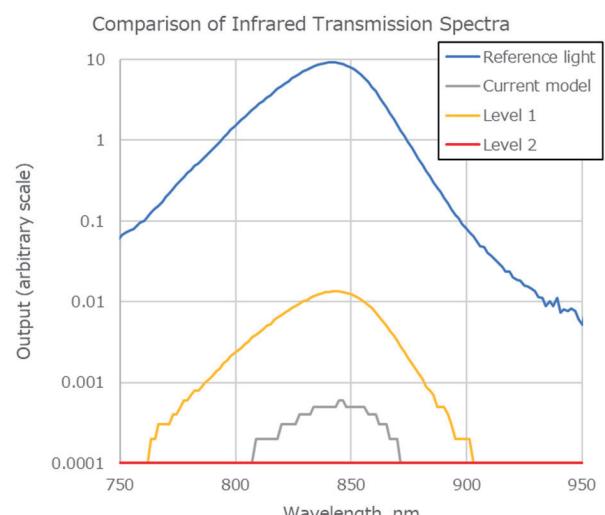


Figure 4. Transmission Spectrum

Although both Level 1 and Level 2 substrates are black, their infrared transmittance differs. The Level 2 substrate is specifically designed to absorb light in the 650 to 1300 nm spectral range.

Based on these results, we adopted the Level 2 substrate for the design of the infrared chip LED.

2.5 Appearance and Emission Characteristics of Infrared Chip LED

Figure 5 shows the appearance of the newly developed chip LED (hereafter referred to as the “developed LED”) on the left and the existing LED on the right. Due to the black substrate material of the developed LED, the contours of the gold-plated pad pattern are clearly visible.

Figure 6 compares the emission states. Light emitted from the top surface of each chip LED undergoes diffusion and multiple reflections within the transparent encapsulating resin, with some light spreading toward the substrate.

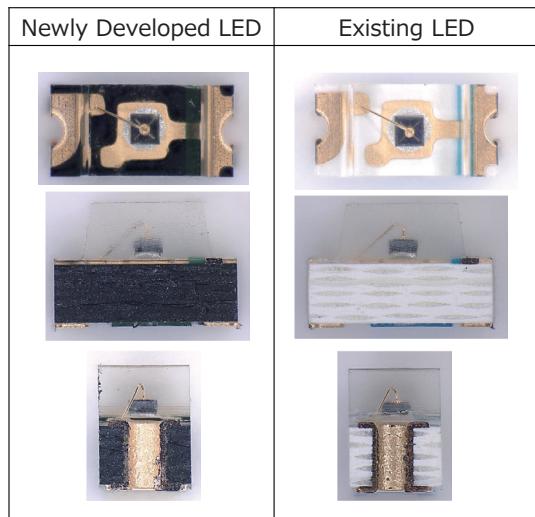


Figure 5. External Appearance Comparison of Chip LEDs

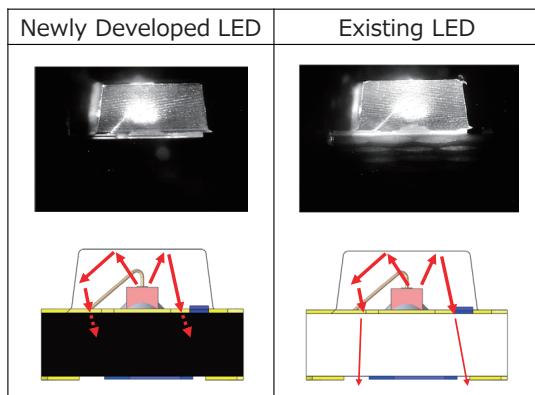


Figure 6. Comparison of Light Emission States of Chip LEDs

In the existing LED, the diffused infrared light penetrates the substrate, and part of it leaks from the substrate side, making the layered structure of glass fibers and BT resin observable.

In contrast, the developed LED shows no visible layered structure of glass fibers and black resin, indicating that the substrate absorbs the infrared light.

2.6 Light Leakage Characteristics of Chip LED

We investigated backside light leakage from each chip LED. The measurement method, shown in **Figure 7**, involved comparing the light output from the top and bottom sides of five samples each. During backside measurements, only light passing through a 0.4 mm diameter hole was measured to prevent reflection and wraparound from the top side.

The results are shown in **Table 2**. For the Level 2 substrate, the backside output was below the measurement limit and effectively zero, more than two orders of magnitude lower than the existing LED. This confirms that backside light leakage to the circuit board can be suppressed.

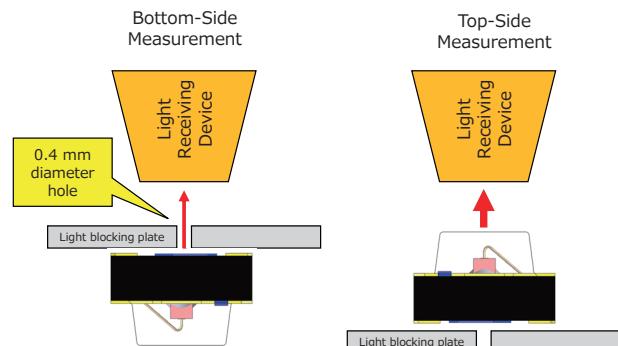


Figure 7. Optical Output Measurement of Chip LEDs

Table 2. Optical Output Comparison of Chip LEDs

	No	Top-Side Light Output mW	Bottom-Side Light Output mW	Top-to-Bottom Light Output Ratio
Existing LED	1	59.7	0.009	0.02%
	2	65.7	0.01	0.02%
	3	60.3	0.007	0.01%
	4	75.1	0.011	0.01%
	5	50.4	0.012	0.02%
	AVG	62.2	0.01	0.02%
Newly Developed LED	1	47.5	0	0.00%
	2	42.2	0	0.00%
	3	40	0	0.00%
	4	48.1	0	0.00%
	5	43.6	0	0.00%
	AVG	43.6	0	0.00%

However, a trade-off of the Level 2 substrate is that it absorbs infrared light, resulting in a reduction of top-side output to approximately 70%.

3. Conclusion

We developed an infrared chip LED with backside light leakage suppression by using an infrared-absorbing

substrate. Standard reliability tests have been completed, and the product is expected to be a viable replacement for existing LEDs.

Future work will focus on exploring structures and materials that prevent reduction in top-side output, as well as proposing modules that combine the LED with photodetectors.

Development of RGB-LEDs Using RGB Phosphors

Yousuke Umetsu*

Abstract

RGB-LEDs are widely used for indirect lighting in vehicle interiors. However, conventional methods that directly utilize the emission from RGB chips suffer from significant color variation in both primary and mixed colors. In this study, we addressed this issue by applying phosphors corresponding to each RGB color to suppress color variation. Additionally, we improved temperature characteristics and brightness degradation under high current conditions, enabling the development of high-power RGB-LEDs. This paper introduces the details of the development.

1. Introduction

Light Emitting Diodes (LEDs) have become widely used in various applications such as lighting and displays, and it is now rare to go a day without encountering LED light in daily life. In recent years, RGB-LEDs have been increasingly adopted for automotive interior lighting. While primarily used for ambient lighting, the need for RGB-LEDs is expected to grow in both interior and exterior applications as autonomous driving technology advances. **Figure 1** shows an example of RGB lighting using a light guide.

White LEDs typically emit white light by combining a blue InGaN chip with yellow and red phosphors. In contrast, conventional RGB-LEDs mainly use a red AlGaInP chip and blue and green InGaN chips, a method referred to as the “chip method.” Although amber and red LEDs

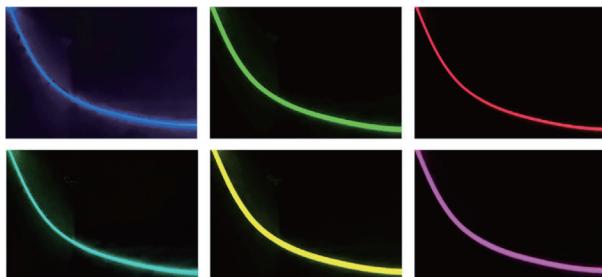


Figure 1. Example of RGB Lighting Using a Light Guide

* Engineering Development Headquarters, Power Device Development Division, Opto Engineering Department, LED Development Section

using phosphor conversion (PC) have already been commercialized⁽¹⁾⁽²⁾, there are no examples of LEDs that emit RGB light using only phosphor emissions within a single package.

In this study, we developed an RGB-LED design that uses phosphors for all RGB colors (referred to as the phosphor method) and addressed the following three challenges:

1. Significant color variation in RGB chips, which currently requires fine software-based adjustments.
2. Large color shifts due to temperature changes, also corrected via software.
3. Increasing demand for high brightness that is visible even during daytime.

2. Wavelength Variation in Chips and Phosphors

LED chips are fabricated through wafer processes, but variations in elemental composition ratios and film thickness lead to inconsistencies in electrical characteristics, light output, and emission wavelength. Therefore, each diced chip is individually measured and categorized into wavelength ranks.

Figure 2(a) illustrates a conceptual diagram of wavelength variation among chips across the wafer, categorized into wavelength ranks.

Example distributions of wavelength variation in blue chips are shown in **Figure 3(a)**. Typical blue LEDs exhibit a wavelength variation exceeding 10 nm and are ranked in 2.5 nm increments.

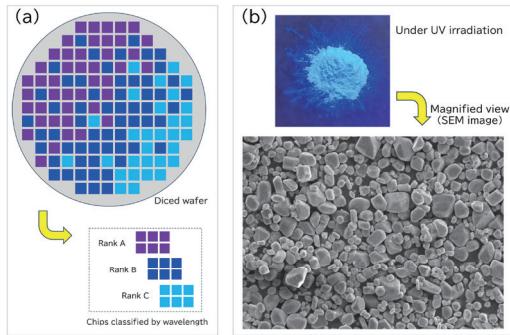


Figure 2. (a) Conceptual Diagram of Wavelength Ranking for Chips and (b) Photograph and SEM image of Phosphors

In contrast, as shown in Figure 2(b), phosphors consist of powders with particle sizes ranging from 5 to 20 μm . Several hundred grams of raw material are placed in crucibles and fired. After firing, the phosphors are processed through crushing, washing, adjusting particle size, and mixing to produce the final product. The mixing process helps to homogenize powders with slightly different properties, resulting in minimal wavelength variation across the entire batch.

As an example, Figure 3(b) shows the wavelength distribution of the blue phosphor $\text{BaMgAl}_{10}\text{O}_{17}:\text{Eu}^{2+}$, which was used in cold cathode fluorescent lamps (CCFL) for LCD backlights. Compared to blue LED chips, which typically have a wavelength variation exceeding 10 nm and are ranked in 2.5 nm increments, the phosphor's distribution is confined to a narrow 0.5 nm range (467.0 to 467.5 nm), demonstrating its superior consistency.

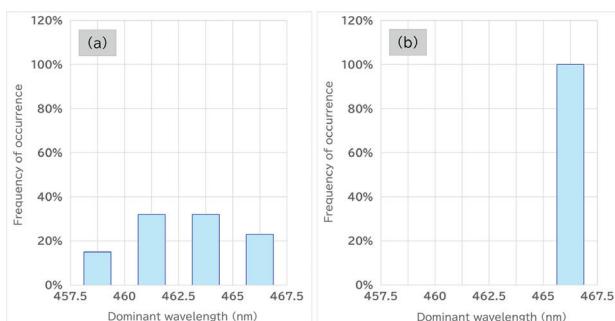


Figure 3. (a) Wavelength Variation in Blue Chips and (b) Wavelength Variation in Blue Phosphors

3. Reduction of Chromaticity Variation in Primary Colors

In the chip method, phosphors are not required, and chips are simply encapsulated with silicone resin. In contrast, the phosphor method requires three phosphors for RGB color. While the chip method cannot adjust chroma-

ticity variation through encapsulation, the phosphor method allows control of chromaticity by adjusting the amount of phosphor.

The following sections describe the chromaticity variation reduction for each RGB color using the phosphor method.

3.1 Red (PC-Red) LED

A blue chip was combined with a phosphor resin made by mixing silicone resin and red phosphor ($\text{Sr,CaAlSi}_3\text{:Eu}^{2+}$). Figure 4 shows the emission spectra when varying the amount of phosphor.

The following phenomena were observed:

1. Increasing the phosphor amount decreases blue emission.
2. The phosphor absorbs blue light and converts it to red, increasing red emission.
3. Beyond a certain threshold, red emission decreases due to concentration quenching.
4. Excess phosphor leads to reabsorption and re-emission at longer wavelengths, shifting the emission spectrum (This process is known as the reabsorption-and-excitation process).

These effects cause the chromaticity to shift from blue toward red on the CIE chromaticity diagram. As the chromaticity approaches the boundary of the reproducible color range, it moves along the edge (Figure 5(a)). By

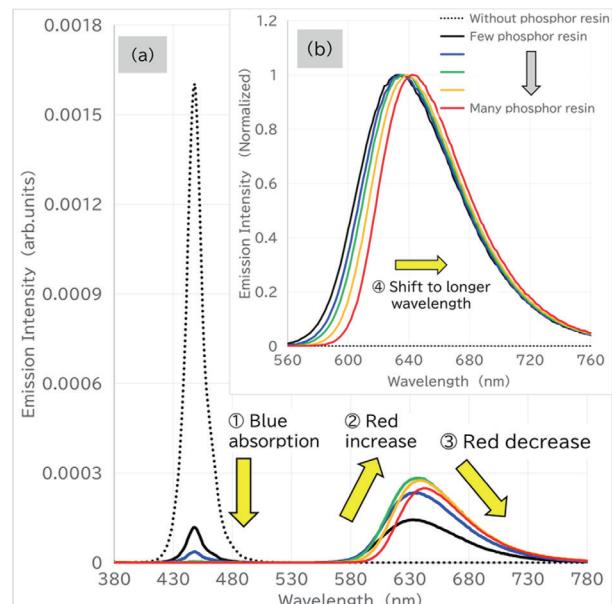


Figure 4. (a) Emission Spectrum of a Blue Chip Combined with Red Phosphor and (b) Emission Spectrum Normalized to the Red Emission Peak

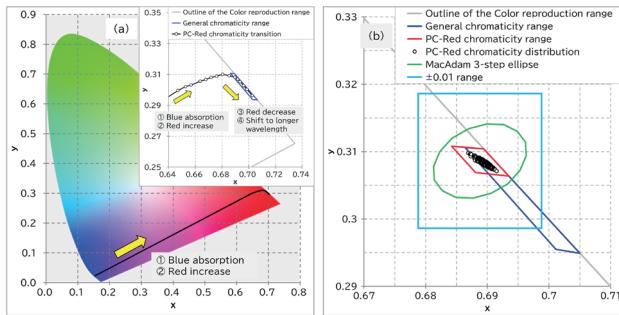


Figure 5. (a) Chromaticity Shift of PC-Red with Varying Phosphor Amount and (b) Chromaticity Distribution

maintaining a uniform phosphor amount, chromaticity variation can be suppressed.

Figure 5(b) shows the target chromaticity range of ± 0.01 , the MacAdam 3-step ellipse, and the chromaticity distribution of PC-Red LEDs. The distribution falls within the MacAdam ellipse, confirming the effectiveness of this method.

The chromaticity range (red line) was defined accordingly. Compared to the conventional 9 nm wavelength range of red LEDs, PC-Red achieves a narrower 3 nm range, reducing variation to one-third.

3.2 Green (PC-Green) LED

A blue chip was combined with a phosphor resin made by mixing silicone resin and green phosphor

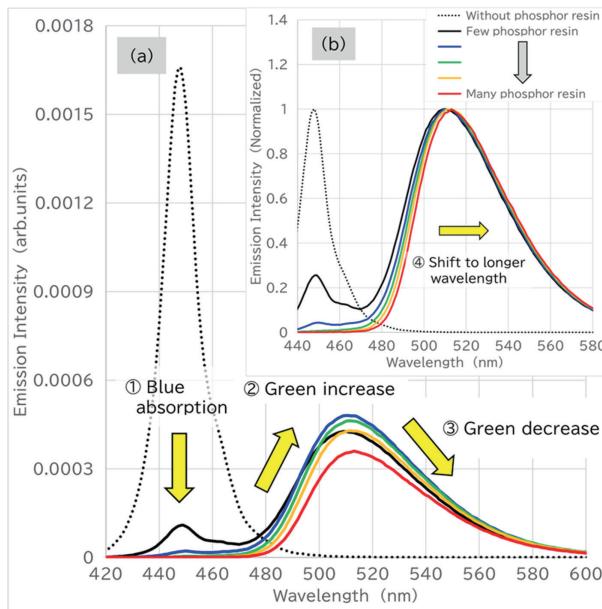


Figure 6. (a) Emission Spectrum of a Blue Chip Combined with Green Phosphor and (b) Emission Spectrum Normalized to the Green Emission Peak Intensity

$\text{Ca}_8\text{Mg}(\text{SiO}_4)_4\text{Cl}_2\text{Eu}^{2+}$, and the resulting emission spectrum is shown in Figure 6.

Similar phenomena to PC-Red were observed:

1. Increasing the phosphor amount decreases blue emission.
2. The phosphor absorbs blue light and converts it to green, increasing green emission.
3. Beyond a certain threshold, green emission decreases due to concentration quenching.
4. Excess phosphor leads to reabsorption and re-emission at longer wavelengths, shifting the emission spectrum.

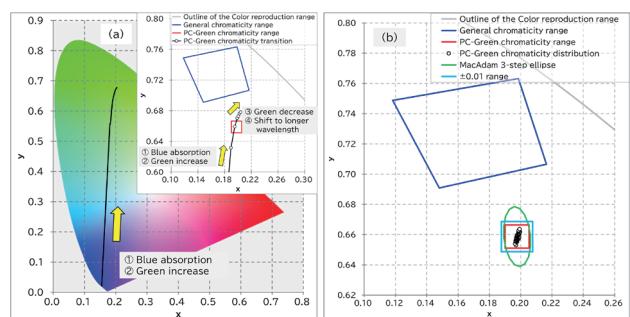


Figure 7. (a) Chromaticity Shift of PC-Green with Varying Phosphor Amount and (b) Chromaticity Distribution

As shown in Figure 7(a), chromaticity shifts from blue toward green. The green phosphor used has a broad emission bandwidth, so the chromaticity does not reach the outer edge of the reproducible color range. Increasing the phosphor amount decreases chromaticity shifts, and uniform phosphor application suppresses variation (Figure 7(b)).

The chromaticity distribution of PC-Green also falls within the ± 0.01 range and the MacAdam 3-step ellipse. The chromaticity range (red line) was defined accordingly. Compared to the conventional 15 nm wavelength range of green LEDs, PC-Green achieves a narrower 3 nm range, reducing variation to one-fifth.

3.3 Blue (PC-Blue) LED

Examples of combining blue chips with blue phosphors are rare due to the perception that chromaticity variation in blue chips is difficult to control. However, techniques using blue phosphors to suppress such variation are known⁽³⁾.

A blue chip was combined with a phosphor resin made by mixing silicone resin and blue phosphor $\text{Sr}_3\text{MgSi}_2\text{O}_8\text{Eu}^{2+}$, and the resulting emission spectrum is shown in Figure 8.

Although the emission spectra of the chip and phosphor overlap, the following phenomena were observed:

1. Increasing the phosphor amount decreases chip-originated blue emission.
2. Increasing the phosphor amount increases blue emission from phosphor.
3. Excess phosphor causes a decrease in blue emission from phosphor.
4. Excess phosphor leads to reabsorption and re-emission at longer wavelengths, shifting the emission spectrum.

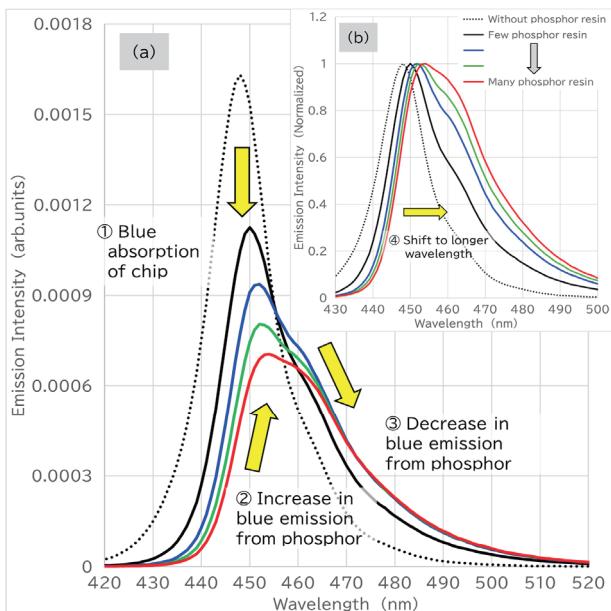


Figure 8. (a) Emission Spectrum of a Blue Chip Combined with Blue Phosphor and (b) Emission Spectrum Normalized to the Blue Emission Peak Intensity

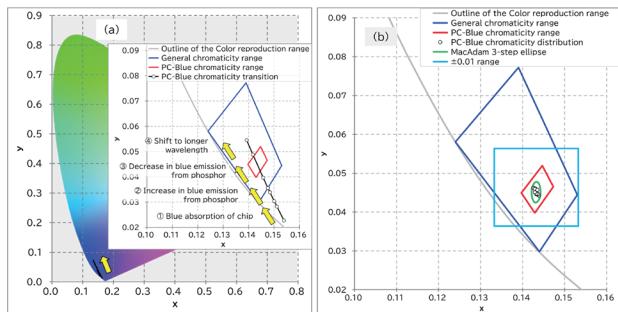


Figure 9. (a) Chromaticity Shift of PC-Blue with Varying Phosphor Amount and (b) Chromaticity Distribution

Table 1. Chromaticity Width of PC RGB-LEDs within MacAdam Ellipse (3-Step)

Region	x	y
Red Region	0.015	0.011
Green Region	0.017	0.04
Blue Region	0.002	0.005

As shown in Figure 9(a), chromaticity moves linearly within the blue region. Uniform phosphor application suppresses chromaticity variation.

The chromaticity distribution of PC-Blue falls within the ± 0.01 range and the MacAdam ellipse (3-step), but the blue region's ellipse is smaller than those for red and green (Table 1). Therefore, the chromaticity range (red line) for PC-Blue was set slightly larger than the ellipse. Compared to the conventional 10 nm range of blue LEDs, PC-Blue achieves a 2 nm range, reducing variation to one-fifth.

4. Expansion of Color Reproduction Range

To suppress chromaticity variation in RGB LEDs, conventional methods generate the reference color points within the emission distribution of the chips⁽⁴⁾.

Specifically, the triangle formed by the upper and lower chromaticity limits of RGB colors is used as the color reproduction range, with its vertices serving as reference points. For example, green is reproduced by weakly emitting blue and red LEDs.

In chip methods, RGB chips are ranked in 4 to 5 nm increments, requiring different emission ratios for each rank combination. This necessitates software-based adjustments for each rank, posing a challenge.

In contrast, the phosphor method achieves chromaticity distributions within the ± 0.01 range and the MacAdam 3-step ellipse for each RGB color. Therefore, each color can be used as a single rank reference point.

The area of the resulting triangle was compared with the NTSC standard commonly used in displays. The chip method achieved 83.4% of NTSC, while the phosphor method reached 95.1%, demonstrating a wider color reproduction range (Figure 10).

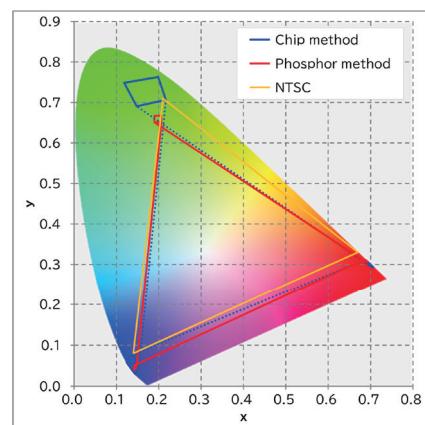


Figure 10. Comparison of Color Reproduction Range

5. Reduction of Chromaticity Variation in White Light

RGB-LEDs can produce mixed colors such as white, cyan, yellow, and amber by adjusting the emission intensity of each RGB component. In conventional chip methods, if chromaticity variation in RGB chips is not corrected via software, the output ratio of RGB remains fixed, resulting in noticeable variation in mixed colors.

Figure 11 presents a simulation of how chromaticity variation in RGB primary colors affects the chromaticity of white light when output ratios are fixed.

Figure 11(a) shows the chip method, where 64 chromaticity coordinates are generated from combinations of four points within the chromaticity ranges of RGB chips (blue lines in Figures 5(b), 7(b), and 9(b)).

Figure 11(b) shows the phosphor method, where 64 chromaticity coordinates are generated similarly using the chromaticity ranges of phosphor-based RGB LEDs (red lines in Figures 5(b), 7(b), and 9(b)).

The phosphor method clearly demonstrates smaller chromaticity variation in white light, with all coordinates falling within the ± 0.01 target range. Although some combinations slightly exceed the MacAdam 3-step ellipse, this is attributed to the PC-Blue chromaticity range (red line in Figure 9(b)) being set slightly larger than the MacAdam 3-step ellipse. If the PC-Blue range is adjusted to fit within the MacAdam 3-step ellipse, mixed color variation can also be suppressed accordingly.

To reduce the PC-Blue chromaticity range, improvements are needed in both material design (e.g., phosphor composition and particle size distribution) and manufacturing techniques (e.g., uniform application of phosphor resin). Both areas offer sufficient room for enhancement.

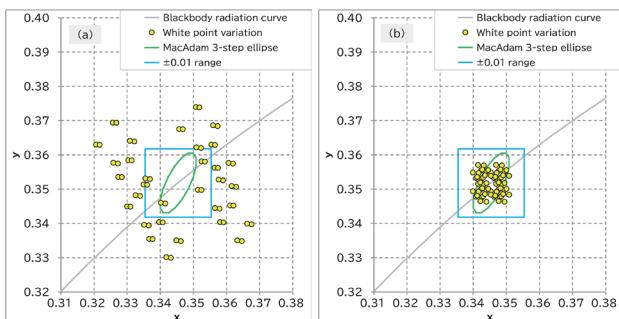


Figure 11. Chromaticity Variation in White Light:
(a) Chip Method and (b) Phosphor Method

6. Chromaticity Shift Due to Temperature Change

The temperature characteristics of LED chips are largely determined by their material composition. Red chips, in particular, exhibit poor temperature stability, with emission intensity decreasing as temperature rises. Additionally, the emission wavelength shifts toward longer wavelengths, resulting in deeper red light with lower visual brightness⁵.

In contrast, PC-Red uses a blue chip with good temperature characteristics and a red phosphor, resulting in less brightness degradation compared to red chips (Figure 12).

Phosphor temperature characteristics can be improved by reducing the concentration of activators⁶. However, this also reduces blue light absorption, making it difficult to achieve high color purity in PC-Green and PC-Red emissions. Therefore, sharing the blue light absorption function with pigments or color filters (e.g., color resist materials) may offer a solution for improving temperature stability.

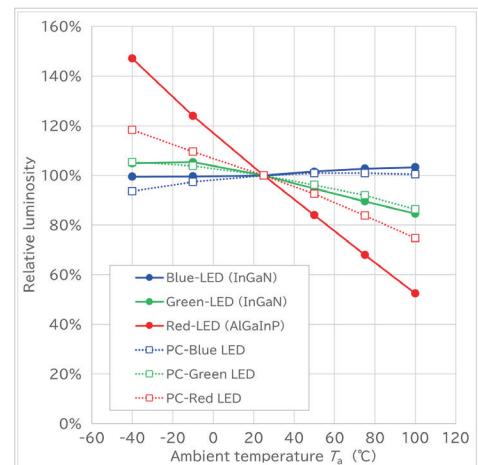


Figure 12. Temperature Characteristics of Chip Method and Phosphor Method

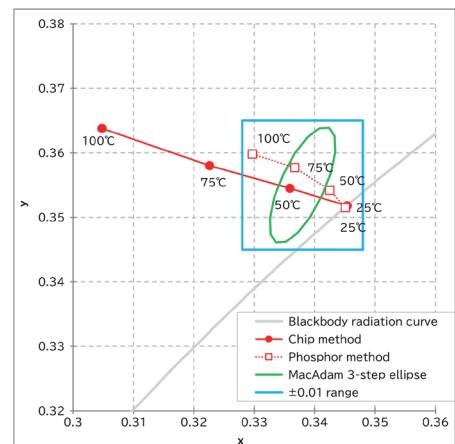


Figure 13. Chromaticity Shift Due to Temperature Increase

Figure 13 shows the chromaticity shift of white light due to temperature changes in both chip methods and phosphor methods. The phosphor method maintains chromaticity within the ± 0.01 range even when the temperature increases from 25°C to 100°C . In contrast, the chip method exhibits more than twice the chromaticity shift, which is visually noticeable (Figure 14).

Ambient Temperature T_a	25°C	50°C	75°C	100°C
Chip method				
Phosphor method				

Figure 14. Appearance of RGB-LED Emission Color Change with Temperature Increase (Photographed Through a Diffuser Plate)

7. Adaptation to High-Power Operation

While indirect lighting in vehicle interiors provides attractive effects at night, visibility during daytime is limited. In Europe, daytime running lights (DRLs) are mandatory to improve vehicle visibility. Although not yet required in Japan, visibility will become increasingly important with the spread of autonomous driving.

Therefore, high-power RGB-LEDs are expected to be necessary in the future, and this study examined their feasibility.

The simplest approach to high-power LED design is to increase chip size to accommodate higher current. Figure 15 shows the change in brightness with increasing current.

Blue chips tend to shift their emission toward shorter wavelengths under high current, resulting in darker blue light due to lower visual sensitivity. However, the RGB phosphors used in this study exhibit increased emission intensity when excited by shorter wavelengths.

As a result, PC-Blue and PC-Green show less brightness degradation compared to blue chips, making them suitable for high-power applications.

PC-Red, while less bright than red chips at 25°C , maintains brightness better at elevated temperatures. At 100°C , PC-Red is brighter than the red chip (Table 2). Since high-power LEDs generate significant heat and must operate at high temperatures, the phosphor method offers advantages in maintaining brightness under such conditions.

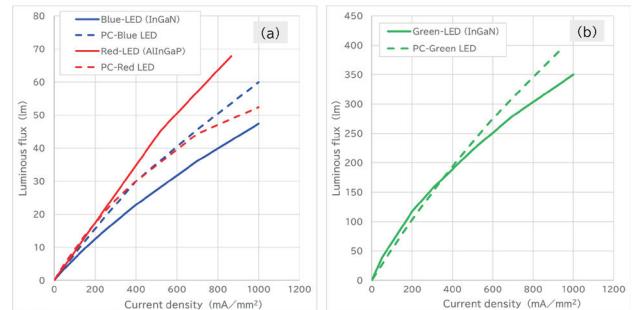


Figure 15. Relationship Between Current Density and Luminous Flux: (a) Blue and Red, (b) Green
(Current Application Time: 10 ms to Suppress Heat Effects)

Table 2. Brightness of Red LED with Temperature Increase
(Current Application Time: 10 ms)

Ambient Temperature (T_a)	25°C	100°C
Red LED (AlGaInP)	64 lm	33 lm
PC-Red LED	47 lm	35 lm

8. Product Concept

The phosphor method requires separate phosphor resin layers for each RGB color. To prevent unintended emission from non-target phosphors (e.g., PC-Green or PC-Blue when PC-Red is activated), shielding between phosphor layers is necessary.

Two LED packaging types are considered:

- Surface Mount Device (SMD) type, with three compartments in a single package
- Chip on Board (COB) type, where chips are mounted directly on the substrate (Figure 16)

To realize high-power RGB-LEDs, the COB type is preferable due to its superior heat dissipation. COB also allows adjustment of chip quantity based on required brightness and supports integration of electrical circuits for modularization.

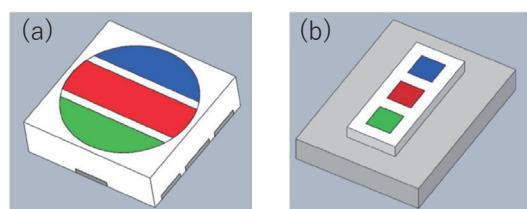


Figure 16. (a) SMD Type and (b) COB Type

9. Conclusion

We developed RGB-LEDs using phosphors for each RGB color. Compared to the conventional chip method,

chromaticity variation in primary colors was significantly reduced, and mixed color variation such as white was also suppressed.

Temperature-induced chromaticity shifts were minimized, eliminating the need for software-based color correction. These features make the phosphor-based RGB-LEDs highly promising for practical applications.

Although this report focused on specific phosphors, changing the phosphor type allows customization of chromaticity variation, temperature characteristics, and emission wavelength, enabling tailored RGB-LEDs to meet customer requirements.

Furthermore, the phosphor method is well-suited for high-power applications, maintaining brightness under high current and high temperature conditions. Combined

with COB customization, this approach aligns with our commitment to delivering products for niche markets, addressing detailed customer needs.

References

- (1) Japan Patent Application No. 2023-145094
- (2) Japan Patent Application No. 2024-056800
- (3) Japan Patent Application No. 2017-152522
- (4) Sugiura et al., Toyoda Gosei Technical Report, Vol. 61, pp. 37–39 (2019)
- (5) Umetsu, Sanken Technical Report, Vol. 56, pp. 4-01–4-06 (2024)
- (6) Y. Umetsu, S. Okamoto, and H. Yamamoto, J. Electrochem. Soc., Vol. 155 (2008), J193

Development of Non-Isolated Converter Power Supply IC STR5M400 Series

Koichi Ito*

Koichi Shiotsu**

Akira Hayakawa***

Abstract

In recent years, power supply ICs used in small home appliances such as ceiling fans, coffee makers, dehumidifiers/humidifiers, and vacuum cleaners have required surface-mount miniaturization, elimination of photocouplers through non-isolation, reduction of external components, and high efficiency across the entire load range. To meet these demands, we have developed the STR5M400 series, which is reported in this paper.

1. Introduction

For small-capacity power supplies of 5W or less used in small home appliances such as lighting equipment, ceiling fans, coffee makers, dehumidifiers/humidifiers, and vacuum cleaners, non-isolated buck converters are commonly used. These converters eliminate the need for isolation transformers and photocouplers, enabling compact, low-cost, and high-efficiency designs.

Market trends in this load range for power supply ICs include surface mounting for labor-saving, reduction of PCB area for miniaturization, and component selection tailored to load capacity for cost reduction.

In response to these trends, the STR5M400 series achieves both a reduction in component count and high efficiency across the full load range. Furthermore, to support a wide variety of applications, the series offers a rich lineup with variations in output voltage, operating frequency, and output power capacity.

2. Product Overview

The STR5M400 series is a power supply IC that integrates a control chip and a high-voltage 700V power MOSFET in a surface-mount SOIC8 package. Compared to the existing mass-produced STR5A464S⁽¹⁾, the number of external components has been reduced by five.

In the power supply circuit diagram of STR5A464S shown in **Figure 1**, the feedback (FB) detection resistor (output voltage setting resistor) in section (a) and the diode and electrolytic capacitor in section (b) were required. In the STR5M400 series, these components are eliminated by combining the VCC and FB terminals into a single shared terminal, enabling a simplified power supply circuit diagram as shown in **Figure 2**.

For the capacitor in section (c) of **Figure 2**, we con-

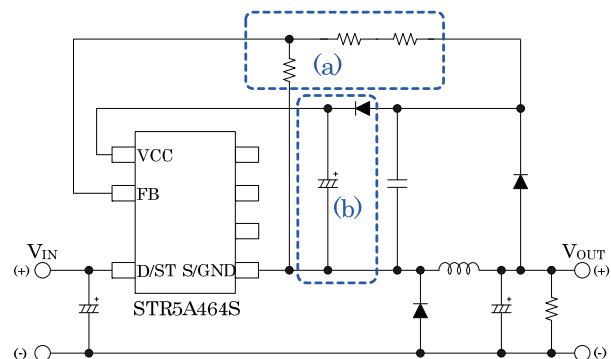


Figure 1. Power Supply Circuit Diagram of the Existing STR5A464S Mass-Produced Product

* Sanken Electric Korea Co., Ltd.

** Engineering Development Headquarters, Power Device Development Division, Power Management IC Development Department, Development Section 1

*** Engineering Development Headquarters, Power Device Development Division, Power Management IC Development Department, Power Control Development Section

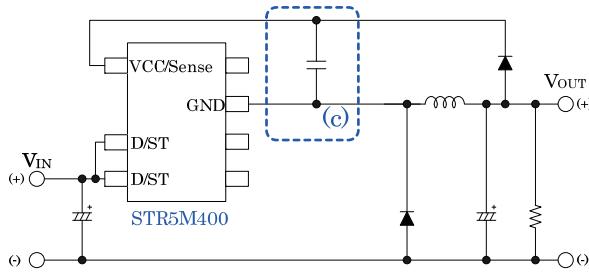


Figure 2. Power Supply Circuit Diagram of the STR5M400 Series

sidered applying it to the shared VCC/Sense terminal. In the existing STR5A464S, a capacitor of $10\mu\text{F}$ or more was used to ensure OLP (Overload Protection) delay time, but this resulted in degraded response performance, posing a challenge for low-capacitance designs.

To address this issue, we reviewed the internal circuitry and successfully ensured accurate delay time even with low-capacitance components, achieving both responsiveness and protection.

The STR5M400 series lineup, shown in **Table 1**, offers various combinations of output voltage, switching frequency, on-resistance, output current, and Green Mode support to accommodate diverse application needs.

Table 1. STR5M400 series lineup

製品名	V_{OUT} [V]	f_s [kHz]	$R_{\text{DS(ON)}}$ Max. [Ω]	I_{o} [A]	GM
STR5M467H4	14.2	100	16	0.10	—
STR5M467H3	13.0	100	16	0.10	—
STR5M467M5	15.0	60	16	0.25	✓
STR5M422M5	15.0	60	3	0.40	✓
STR5M422M2	12.0	60	3	0.40	✓

Notes:

1. Including conceptual products

2. GM refers to Green Mode, a function that reduces the oscillation frequency under light-load conditions.

3. Product Features

Figure 3 shows the block diagram of the IC. The key features of this product are the integration of the following four functions:

- (1) Feedback resistor
- (2) Current sensing resistor
- (3) Phase compensation circuit
- (4) Overload protection (OLP) timer

3.1 Feedback Resistor

The feedback resistor corresponds to section (1) in

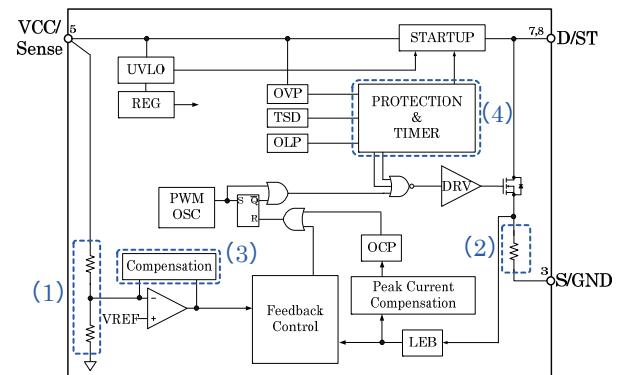


Figure 3. Block diagram

Figure 3. By integrating the resistor into the IC, external components can be reduced, and users are relieved from the task of individually setting resistor values.

3.2 Current Sensing Resistor

The current sensing resistor corresponds to section (2) in **Figure 3** and, as shown in **Figure 4**, utilizes interconnect resistance on the control chip. This wiring resistance is formed using aluminum alloy and typically exhibits a temperature characteristic of over 30% increase at a 100°C rise. Our proprietary technology compensates for this temperature characteristic.

The IC adopts a current-mode control method, detecting current information via the sensing resistor. Overcurrent conditions are also detected using this resistor. As with the feedback resistor, integrating this component reduces external parts and eliminates the need for user-side constant setting.

Notably, this IC is the first product to use our latest high-voltage process⁽²⁾, which has been cost-optimized compared to our existing high-voltage process.

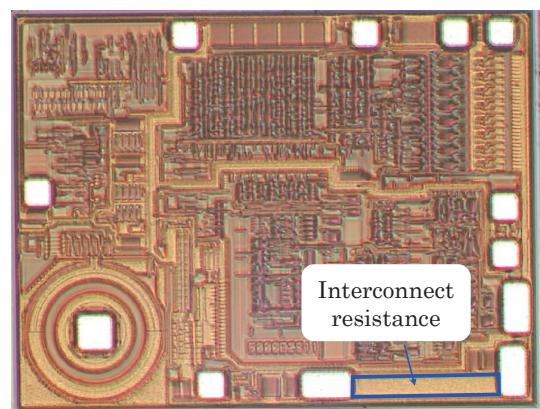


Figure 4. Photograph of the Control Chip

3.3 Phase Compensation

The IC includes a phase compensation circuit within the error amplifier section. This circuit supports output capacitors ranging from low to high capacitance (approximately $10\mu\text{F}$ to $470\mu\text{F}$), including low-ESR ceramic capacitors. It also eliminates the need for users to set compensation constants individually.

3.4 OLP Timer

Figure 5 shows the timing waveform of VCC and the gate signal DRV of the Power MOSFET during OLP operation. The OLP time 1 and OLP time 2 are both controlled by internal timers, allowing the IC to maintain switching stop time without being affected by the VCC capacitor value, unlike the STR5A464S.

This ensures reliable suppression of IC temperature rise during abnormal conditions.

As shown in Figure 5, when VCC drops to VCC (Bias) during OLP time 1 or 2, the startup circuit activates bias assist to maintain VCC voltage. After OLP time 2 ends, bias assist stops, and when VCC falls below VCC (OFF), bias assist reactivates to raise VCC. This cycle results in intermittent switching operation.

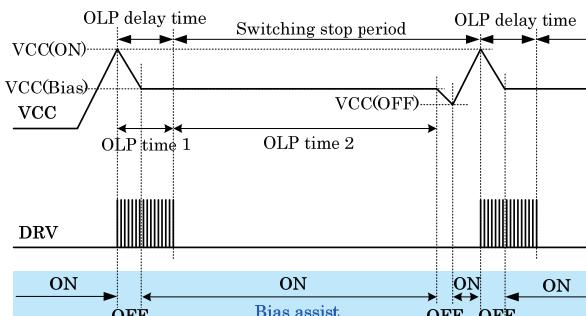


Figure 5. Timing waveform during OLP operation

Figure 6 shows the operating waveform under heavy-load conditions during OLP at AC 200 V. Due to this intermittent operation, the temperature during OLP at AC 265 V is maintained at 92.4°C , satisfying the requirement of being below 100°C (assuming $\text{Ta} = 60^\circ\text{C}$).

3.5 Oscillation Control

To improve power conversion efficiency under medium to light loads, the IC adopts Green Mode, as shown in Figure 7. The oscillation frequency is automatically controlled according to the load, minimizing unnecessary power

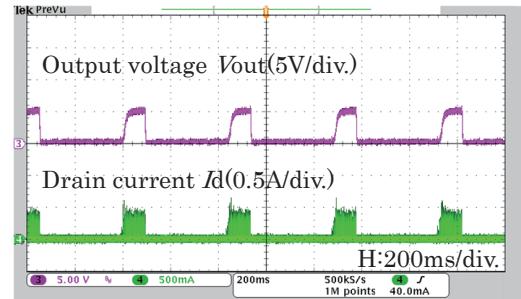


Figure 6. OLP operation

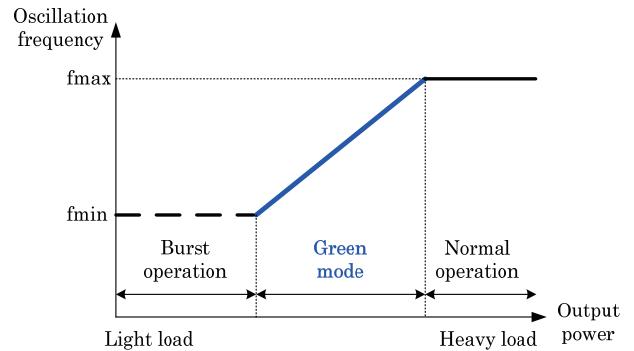


Figure 7. Operating Area of Green Mode

consumption and enabling high-efficiency power supply design across the full load range.

Additionally, the IC incorporates a random switching function that superimposes frequency variation on the average PWM oscillation frequency. This design ensures compliance with CISPR J14 standards for conducted emissions, even without noise suppression components such as input line filters, as shown in Figure 8.

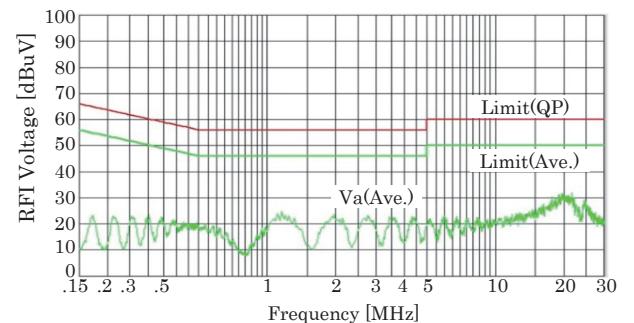


Figure 8. Conducted Emission Test (AC200V, in accordance with CISPR J14 Standard)

Under conditions of AC200V and $V_{\text{OUT}} = 15\text{V}$, the burst oscillation waveform at $I_{\text{OUT}} = 3\text{mA}$, Green Mode

waveform at $I_{OUT} = 25\text{mA}$, and normal operation waveform at $I_{OUT} = 200\text{mA}$ are shown in **Figures 9, 10, and 11**, respectively.

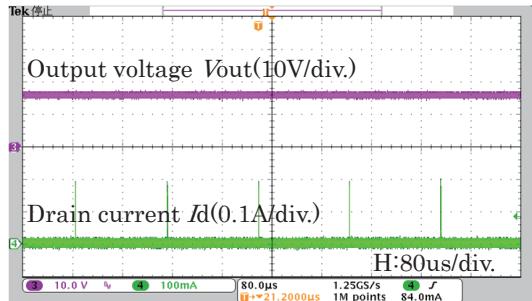


Figure 9. Burst Oscillation Mode

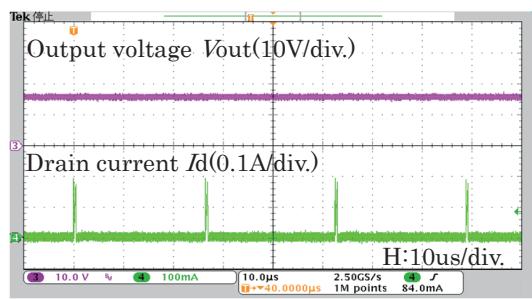


Figure 10. Green Mode

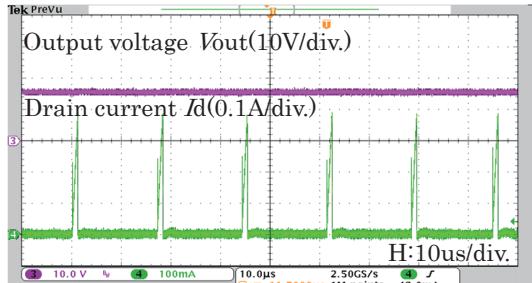


Figure 11. Normal Operation

4. Prototype Evaluation Results

Figure 12 shows the schematic of the power supply evaluation board using this IC, and **Figure 13** shows the implementation photo. **Table 2** shows the list of mounted components, demonstrating a 42% reduction in component count compared to the conventional product.

This section reports the results of power supply evaluation conducted using the evaluation board.

4.1 Power Supply Characteristics

Figure 14 shows the efficiency characteristics, and

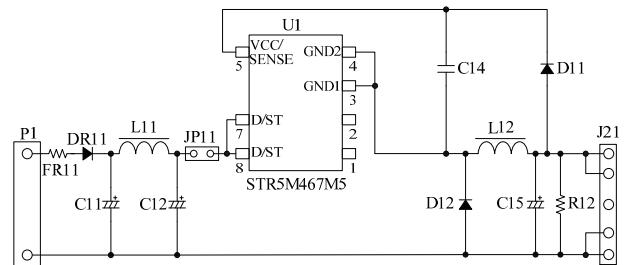
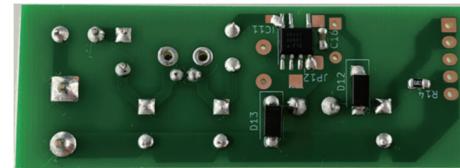


Figure 12. Power Board Schematic



(a) Front



(b) Back

Figure 13. Power Evaluation Board

Table 2. List of Mounted Components

Symbol	Part name	Rating	Proposed product	Conventional product
C12	Electrolytic capacitor	105 °C, 400 V, 8.2 μF	✓	✓
C14	Ceramic capacitor	50 V, 0.47 μF	✓	✓
C15	Electrolytic capacitor	105 °C, 25 V (220 μF)	✓	✓ (470 μF)
C16	Electrolytic capacitor	105 °C, 50 V, 10 μF	—	✓
D11	Fast recovery diode	500 V, 1 A (SJPD-D5)	✓	✓
D12	Fast recovery diode	500 V, 1 A (SJPD-D5)	✓	✓
D13	Schottky Barrier Diode	60 V/1 A (SJPD-D6)	—	✓
L12	Inductor	470 μH , 0.6 A	✓	✓
R1	Chip resistor	6.8 k Ω , 1/8 W, 1608	—	✓
R2	Chip resistor	33 k Ω , 1/8 W, 1608	—	✓
R3	Chip resistor	1.3 k Ω , 1/8 W, 1608	—	✓
R12	Chip resistor	6.8 k Ω , 1/8 W, 1608	✓	✓
U1	PWM offline converter IC	STR 5M467	STR 5A464S	

Figure 15 shows the load regulation characteristics. The evaluation confirmed that high efficiency is maintained across a wide output current range under input conditions of AC100V and AC230V.

5. Conclusion

We have developed the STR5M400 series as the first

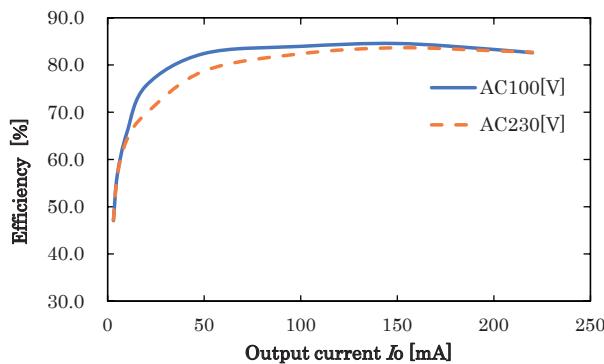


Figure 14. Efficiency Characteristics

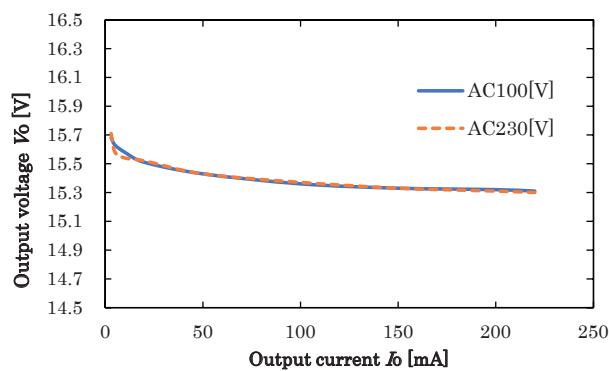


Figure 15. Load Regulation Characteristics

product using our latest high-voltage process for power supply ICs.

By adopting Green Mode, the IC achieves high efficiency under light load conditions. Additionally, it is the first in our lineup to use chip wiring resistance as a current sensing resistor, and by integrating the FB detection resistor into the IC, we have realized both miniaturization and cost reduction of the power supply.

Looking ahead, we plan to expand into new markets by developing products with higher capacity and efficiency, including GaN-based power MOSFETs and dual-output configurations.

References

1. Tadamasa, Terasawa, Kawamata: Sanken Technical Report, vol.46, p29–32 (Nov. 2014)
2. Aoki: Sanken Technical Report, vol.55, p22–25 (Nov. 2023)

Development of Non-Isolated Flyback Power Supply IC STR5A300 Series

Tetsuya Tabata*

Koichi Shiotsu*

Akira Hayakawa* **

Abstract

This report describes the development of a power supply IC designed for low-capacity power sources used in white goods such as air conditioners, washing machines, and air purifiers, as well as smart meters. For these applications, cost reduction and space-saving in the power system are critical requirements, and further miniaturization is expected in the future. The newly developed IC integrates a high-voltage (900V) power MOSFET and an internal error amplifier, targeting non-isolated power supply applications. This report outlines the key features of the IC, compares circuit topologies, and presents the characteristics of a power board equipped with the IC.

1. Introduction

In recent years, energy conservation has become increasingly important to reduce the consumption of energy resources. It is also expected to contribute to the reduction of CO₂ emissions, a major factor in global warming. In Japan, energy efficiency standards based on the Top Runner Program have been introduced for designated equipment such as household appliances and automobiles. Manufacturers are required to produce and supply products that comply with these standards. For residential air conditioners, new standards will be applied starting in fiscal year 2027, requiring compliance with even stricter regulations⁽¹⁾.

Under these circumstances, semiconductor products such as power supply ICs are expected to play a significant role in energy conservation. For low-capacity power supplies, the flyback topology is widely used due to its ease of design. In isolated types, feedback signals from the output side are typically controlled via a voltage detection circuit and a photocoupler⁽²⁾. However, in white goods

such as air conditioners, where the enclosure is already insulated, the power system may not require isolation, allowing for a non-isolated configuration. In non-isolated systems, the omission of the photocoupler—a component with limited lifespan—offers advantages such as improved reliability and quality.

In this development, a non-isolated power supply IC was created featuring a high-voltage (900V) power MOSFET and a flyback topology optimized for high efficiency under light load conditions.

2. Product Overview

Figures 1 and 2 show the external appearance and application circuit examples of the STR5A300 series. Tables 1 and 2 present the product lineup and pin functions.

This series is characterized by high efficiency across the full load range and low power consumption of 25mW or less under no-load conditions. The power MOSFET lineup includes high-voltage 900V models, designed to ensure robustness even in regions with unstable power supply conditions.

The package options include DIP (Dual In-line Package) for through-hole mounting and SMD (Surface Mount Device) for surface mounting, both commonly used in flyback power supply ICs.

* Engineering Development Headquarters, Power Device Development Division, Power Management IC Development Department, Development Section 1

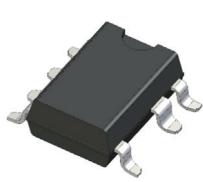
** Engineering Development Headquarters, Power Device Development Division, Power Management IC Development Department, Power Control Development Section

Table 1. Product Lineup

Line up	$f_{OSC(AVG)}$ typ.	V_{DSS} min.	$R_{DS(ON)}$ max.	P_{OUT} (230V/Wide)
STR5A361	100kHz /130kHz	700V	3.95Ω	35W/23.5W
STR5A369			6.0Ω	30W/19.5W
STR5A342		900V	3.0Ω	37.5W/26W
STR5A349			6.5Ω	30W/19.5W



DIP type



SMD type

Figure 1. External Appearance

Table 2. Pin Functions

Pin Number	Pin Name	Description
1	S/OCP	Power MOSFET source / Overcurrent protection (OCP) signal input
2	BR	Input voltage sensing input
3	GND	Ground
4	FB	Feedback input for constant voltage control
5	VCC	Logic power supply input / overvoltage protection (OVP) signal input
6	—	(Pin removed)
7	D/ST	Power MOSFET drain / Startup current input
8		

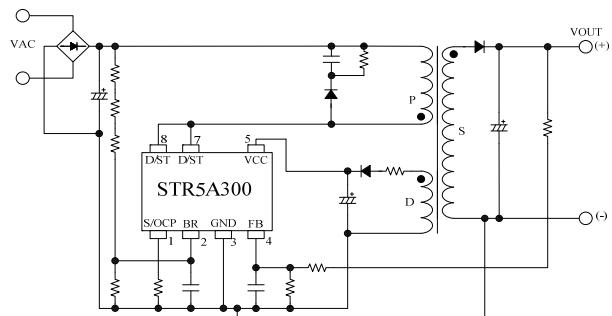


Figure 2. Application Circuit Example

3. Power Supply Configuration for Isolation

Figure 3 illustrates the feedback configuration of conventional isolated products, while Figure 4 shows the feedback configuration of the newly developed non-isolated STR5A300 series.

In conventional isolated types, feedback signals from the output side are transmitted to the internal control circuit of the IC via a voltage detection circuit and a photocoupler.

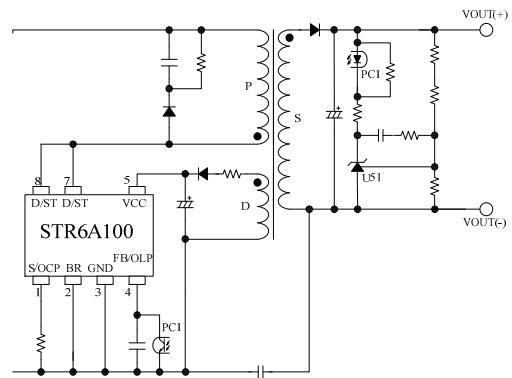


Figure 3. Isolated Type (Conventional Product)

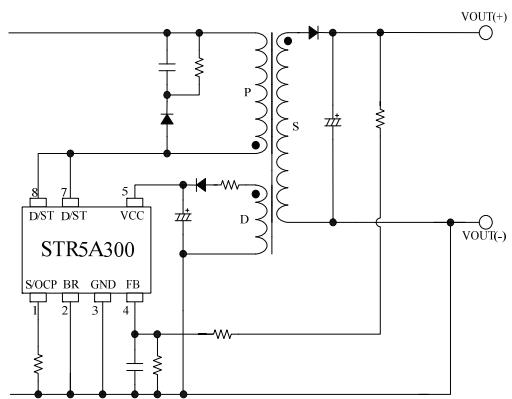


Figure 4. Non-Isolated Type (Developed Product)

In contrast, the newly developed non-isolated type integrates an error amplifier within the IC's internal control circuit, eliminating the need for peripheral components such as shunt regulators and photocouplers that were previously required.

This results in a reduction of five components, enabling miniaturization and cost reduction of the power system in applications where non-isolated configurations are feasible.

4. Functions and Features

4.1 Step Drive Control

Figure 5 illustrates the operation of step drive control, and Figures 6 and 7 show waveforms during startup with and without step drive control.

When the power MOSFET turns on, a surge voltage is generated across the secondary-side rectifier diode D51 due to recovery current and inductive components.

The rectifier diode must be selected with a voltage rating that accounts for this surge voltage.

Using Sanken's proprietary step drive control technology, the gate rise time of the built-in power MOSFET

is optimally controlled within the IC according to load conditions.

This suppresses the slope of the recovery current during turn-on and reduces surge voltage.

As shown in **Table 3**, step drive control allows the VRM voltage rating of the rectifier diode to be set lower than conventional values, enabling cost reduction and improved circuit efficiency through lower forward voltage (VF).

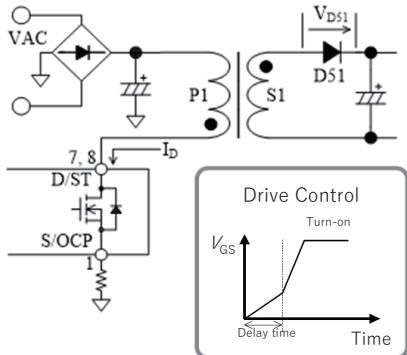


Figure 5. Operation of Step Drive Control

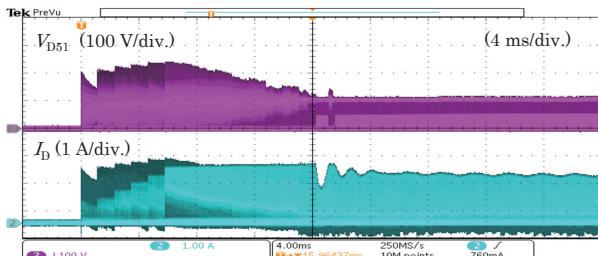


Figure 6 Startup Waveforms without Step Drive Control
($V_{OUT} = 24V$)

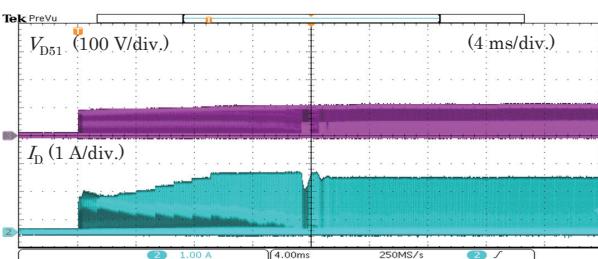


Figure 7. Startup Waveforms with Step Drive Control
($V_{OUT} = 24V$)

Table 3. VRM Voltage Rating of Rectifier Diodes
(Reference Values)

Output Voltage	without Step Drive Control	with Step Drive Control
5V	100V	60V
12V	200V	120V
15V	200V	120V
24V	400V	200V

Step drive control is effective under transient conditions and disabled during steady-state operation. The drive speed is switched between transient and steady-state conditions to optimize switching speed. As a result, power loss in the power MOSFET is reduced and high efficiency of the power supply is achieved across the entire operating range.

4.2 Input Voltage Sensing Function

The input voltage sensing function is designed to ensure safe operation even in regions with unstable power supply conditions. It includes an AC input overvoltage protection function (HVP) that activates when the input voltage is high, and a brown-in/brown-out function (BR_IN/BR_OUT) that activates under abnormal low input voltage conditions. Both functions are configured on the same pin.

By continuously monitoring the input voltage, the IC can instantly suppress damage to the power MOSFET caused by overvoltage and prevent overheating due to prolonged low input voltage.

Figure 8 shows the relationship between the BR pin voltage and switching current. The input voltage sensing function detects the input voltage via the BR pin and controls switching operation based on the BR pin voltage to transition to appropriate protection modes.

If the input voltage sensing function is not used, it can be disabled by connecting the BR pin to GND to fix the potential.

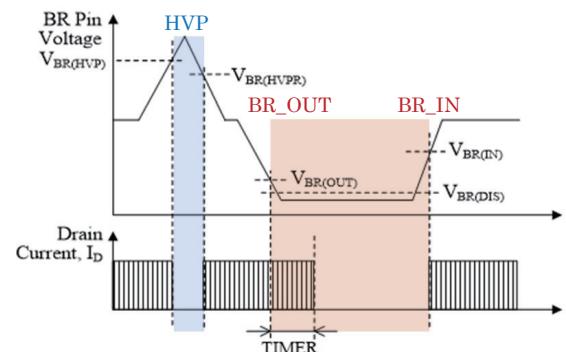


Figure 8. BR Pin Voltage and Switching Current

4.3 Low Power Consumption and High Efficiency Across Full Load

Measured values for the STR5A361 model (oscillation frequency: 100kHz) are reported. **Figure 9** shows the

evaluation board used for efficiency measurement.

The no-load power consumption is 25mW (AC230V), equivalent to that of conventional isolated products, achieving low power consumption.

Although the non-isolated STR5A300 series integrates an error amplifier into the control IC, resulting in increased circuit scale, a review of the circuit configuration has enabled the control chip size to remain equivalent to that of conventional products.

As shown in Figures 10, 11, and 12, the IC automatically switches its operating mode according to the load current: Burst Oscillation Mode, Green Mode (25kHz–100kHz), and Normal Operation (100kHz).

When the load decreases to standby conditions, the IC transitions from Green Mode to Burst Oscillation Mode. In Green Mode, switching frequency is reduced, and in Burst Oscillation Mode, switching operation is temporarily halted, both contributing to reduced switching losses and improved conversion efficiency.

Figure 13 shows the output power and load regulation characteristics, confirming favorable load regulation.

Figure 14 presents the efficiency characteristics under full load. Through optimized oscillation frequency control and drive circuitry, high efficiency of approximately 88–89% was achieved in the output power range of 5W to 23W.

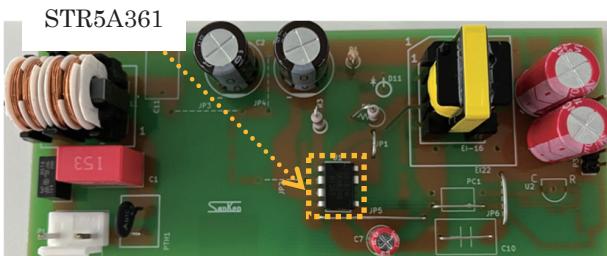


Figure 9. External View of Evaluation Board

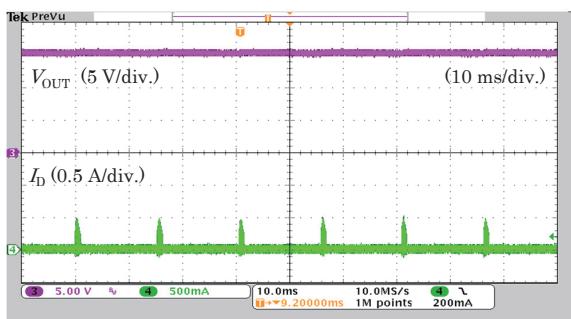


Figure 10. Burst oscillation mode

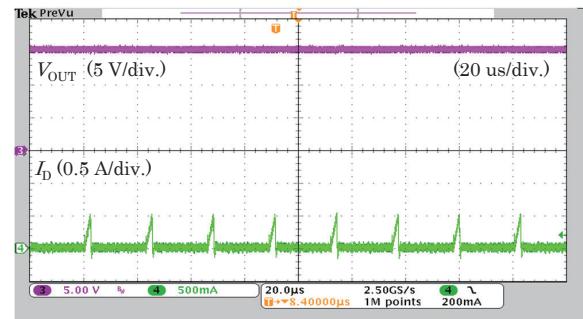


Figure 11. Green Mode

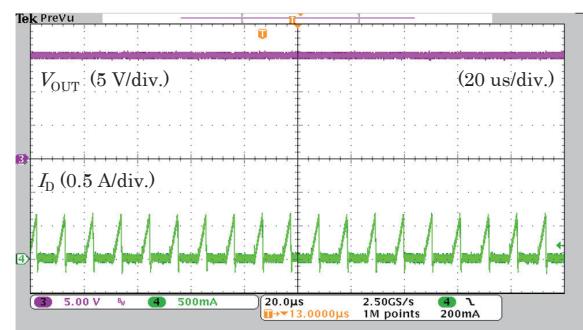


Figure 12. Normal Operation

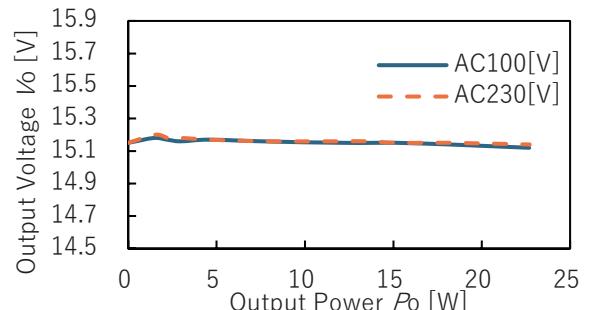


Figure 13. Load Regulation Characteristics

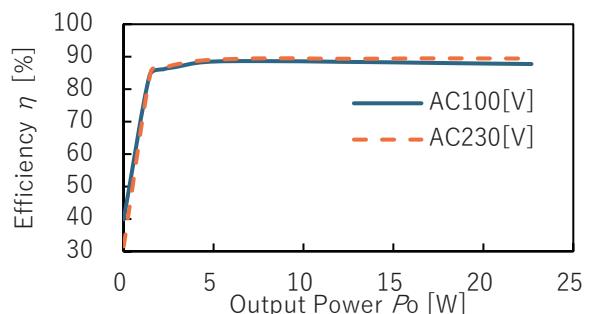


Figure 14. Efficiency Characteristics

5. Conclusion

A non-isolated flyback power supply IC, the STR5A300 series, has been developed for use in non-isolated power supply systems.

By integrating an error amplifier, five peripheral components were eliminated, enabling miniaturization and cost reduction of the power system.

Step drive control and oscillation frequency control have achieved low power consumption and high efficiency across the full load range.

Additionally, the incorporation of high-voltage power MOSFETs and input voltage sensing functions ensures safe operation even in regions with unstable power supply conditions.

Future product development will continue to address diverse power supply requirements and contribute to energy conservation.

References

- (1) Agency for Natural Resources and Energy, "New Energy Efficiency Standards for Residential Air Conditioners Established," Ministry of Economy, Trade and Industry, 2022. URL: <https://www.meti.go.jp/press/2022/05/20220531003.html> (Accessed: September 18, 2025)
- (2) Hayakawa, A. and Tabata, T.: "Sanken Technical Report," 2014, Vol. 46, pp. 33–36.

Generalized Performance Board Design for Docking Interfaces

Shougo Kimura*

Asami Sanao*

Abstract

Our company handles power semiconductors such as Intelligent Power Modules (IPMs) and power management ICs. In wafer testing, which is one of the front-end processes in semiconductor manufacturing, continuous improvement in quality and throughput is required. To enhance throughput, we utilize the multi-site measurement function of Automated Test Equipment (ATE) and probers, which enables testing of multiple chips at once. As the number of chips tested in multi-site configurations increases, components such as performance boards and probe cards tend to become larger. Manufacturing these large components for each product individually leads to increased costs. To suppress these costs, we designed generalized components. This paper reports on the design case of such generalized performance boards.

1. Introduction

Our company develops and manufactures power semiconductors such as IPMs and power management ICs, and conducts wafer testing to evaluate the electrical characteristics and functions of the semiconductor chips used in these products.

Wafer testing involves two main pieces of equipment: ATE, which inputs test conditions and decides pass/fail results based on output data, and probers, which handle wafer transport and positioning. However, these two devices alone are not sufficient for wafer testing. Two additional components—performance boards (PBs) and probe cards—play critical roles in determining test quality and operational costs at manufacturing sites.

PBs are interface boards equipped with electronic components necessary for testing the target chips. They receive electrical signals from the ATE and transmit them to the probe card. Probe cards, in turn, are interface boards equipped with probes (needles) that deliver the signals to the chip.

In wafer testing, two connection methods between these interface boards and the equipment are commonly used: cable connection and docking connection.

The cable connection method, as the name suggests, connects the ATE and PB via cables, with the ATE installed several meters away from the device. In contrast, the docking connection method directly attaches the PB to the ATE (Figure 1). Compared to cable connections, the wiring distance to the device is reduced to several tens of centimeters, minimizing parasitic capacitance and its impact on measurements. Additionally, this method uses fewer connectors, reducing the risk of connection

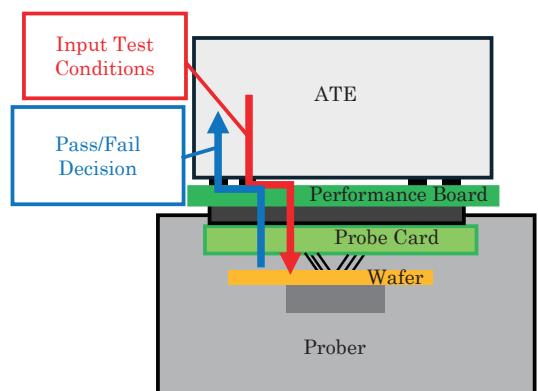


Figure 1. Interconnection of system components

* Engineering Development Headquarters, Process Engineering Division, IC Device Department, Test Section

failures and disconnections due to repeated plugging and unplugging.

Despite its advantages, the docking connection method presents challenges. PBs and probe cards become larger, increasing the cost per board. Traditionally, our company designed and manufactured PBs for each product group with different functions, resulting in higher costs.

In addition, the structure between the ATE and the device is extremely compact, leaving no space to freely place oscilloscope probes. As a result, waveform observation is difficult, and the efficiency of characteristic evaluation tends to be lower compared to the cable connection method.

2. Generalized PB Design

Previously, our company designed and manufactured PBs for each product group with different functions. However, due to the large size of the boards, production costs tended to increase. To address this, we aimed to design a single PB capable of testing various semiconductor chips used in our products.

2.1. Generalization Strategy

To improve productivity, it is essential to achieve both generalization and increased throughput. Generalizing PBs means appropriately allocating ATE resources (power supplies, measurement instruments, signal lines, etc.) to the terminals of semiconductor chips so that multiple types of chips can be tested using a single PB.

To enhance throughput, it is necessary to utilize the multi-site measurement function and maximize the number of chips tested at once. Efficient use of ATE resources is crucial to achieving this.

Therefore, the key to balancing generalization and throughput lies in the optimal allocation of resources. We examined methods to achieve this.

Typically, electrical characteristic testing of semiconductor chips consists of multiple test items executed in a sequence. Considering the entire sequence, resources must be connected to all terminals. Furthermore, multi-site testing increases the required number of resources.

However, ATE resources are limited. Connecting resources to all terminals at all times makes it difficult to scale up multi-site testing, especially for chips with many terminals.

On the other hand, not all terminals require constant resource connections during individual tests. Focusing on

this point, we optimized resource allocation. The critical factor here is the test conditions for each terminal.

We analyzed the terminal configurations and test conditions of recently developed semiconductor chips. Based on the results, we identified the resources required for each test and designed circuits that efficiently allocate resources to terminals using branching circuits. This enabled us to achieve both generalization and increased throughput.

2.2. Support for High-Voltage Products

Many of our products are high-voltage power semiconductors exceeding 600V, requiring specialized board designs.

When forming high-voltage wiring patterns on the board, it is necessary to consider creepage distance to prevent dielectric breakdown. Ensuring sufficient creepage distance limits the freedom of wiring patterns and component placement, hindering generalization.

To address this, we used high-voltage wires instead of wiring patterns for high-voltage connections. This reduced the number of areas requiring creepage distance considerations and increased the flexibility of wiring and component placement.

2.3. Effects of Generalization

Based on the above design, we produced a generalized PB. As a result, most of our semiconductor chips can now be tested using a single PB.

Generalization eliminated the need to store multiple PBs, reducing management workload and storage space. It also shortened the time required to prepare for testing by reducing the design workload for each product group.

However, some products require specialized circuits. For such cases, we designed PBs with dedicated circuits, which are discussed in the next chapter.

3. Sub-PB Design

The generalized PB described so far is referred to as the “main PB,” while PBs with product-specific circuits are called “sub-PBs” (Figure 2).

3.1. Sub-PB

Sub-PBs are used in combination with the main PB. Previously, all test circuits for each DUT (Device Under Test) were implemented on a single PB. In contrast, sub-PBs separate part of the test circuits for each DUT.

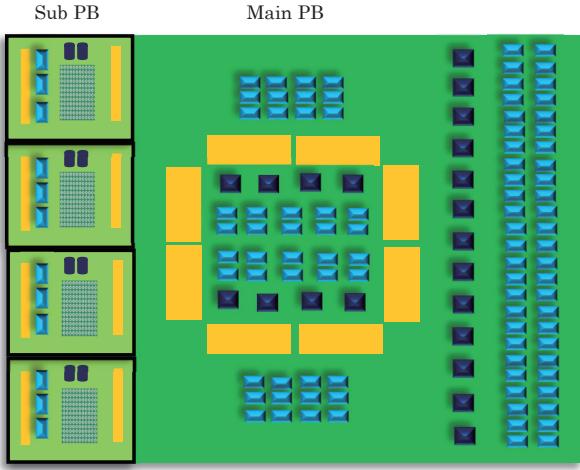


Figure 2. Top view of the PB layout

During characteristic evaluation, PB circuit modifications are sometimes necessary. Using sub-PBs allows evaluation to proceed without waiting for modifications to all DUT circuits.

Sub-PB design only requires circuits for a single DUT, making it easy to produce using printed circuit boards and to prepare spare boards.

Sub-PBs also offer advantages during mass production. If a sub-PB fails, it can be quickly replaced with a spare, enabling rapid recovery of production.

3.2. Connection Between Main PB and Sub-PB

There are two key points in connecting sub-PBs to the main PB.

First, the main PB is designed to allow retrofitting of sub-PB circuits. Pre-arranged wiring patterns on the main PB enables connection to sub-PBs without modifying the main PB circuits (Figure 3). The wiring length between the main and sub-PBs is kept within a range that does not affect electrical characteristics.

Second, connection reliability is improved. Since sub-PBs are expected to be frequently replaced for different product groups, using connectors with short mechanical lifespans increases failure risk. Therefore, we selected pogo pins, which have longer contact lifespans (Figure 4).

3.3. Ease of Replacement

In wafer testing, it is common to replace components when switching the test target from product group A to product group B. Our company also replaced PBs and probe cards for each product group.

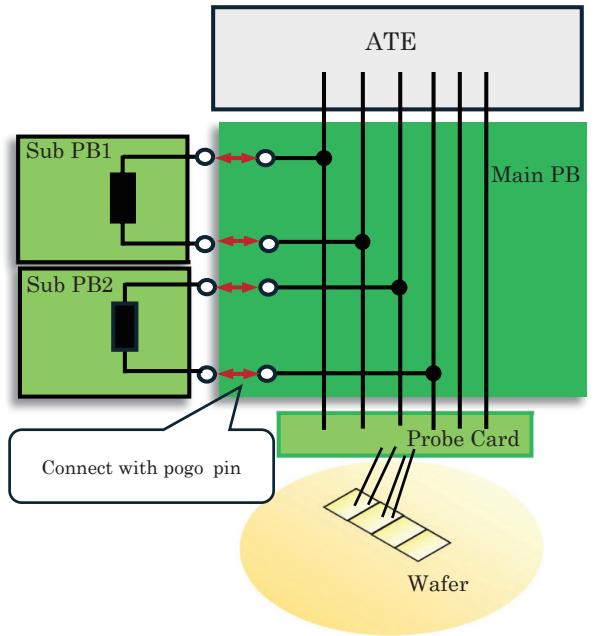


Figure 3. SubPBs and MainPB wiring connection

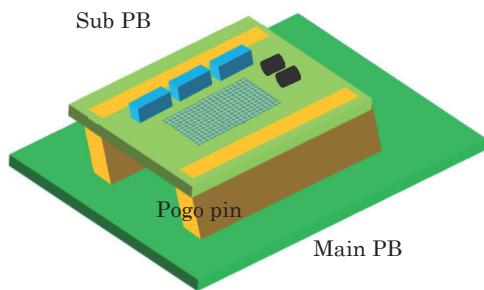


Figure 4. 3D layout of PB connections

However, replacing large PBs is inefficient due to their weight. Sub-PBs are approximately one-twentieth the size of main PBs, making them compact and lightweight. Replacing sub-PBs significantly improves work efficiency.

This retrofit structure of sub-PBs enables flexible response to product-specific test requirements.

4. Monitor PB

In docking connection methods, the short distance between the ATE and semiconductor chips minimizes cable effects. However, as mentioned in Chapter 1, structural constraints make waveform observation using external instruments such as oscilloscopes difficult, reducing evaluation efficiency.

To address this issue, we developed a monitor PB dedicated to waveform observation.

The monitor PB is attached to the PB only during characteristic evaluation and is easily detachable. As a result, evaluation efficiency has dramatically improved.

5. Future Challenges

We have designed a generalized performance board (main PB), sub-PBs, and a monitor PB.

However, another important component remains a challenge: the generalization of probe cards.

Generalizing probe cards is more complex than PBs, primarily due to the need to test high-voltage products. High-voltage testing requires sufficient creepage distance on the board, but probe cards have smaller dimensions and limited mounting area compared to PBs.

Additionally, the diverse arrangements of high-voltage terminals on semiconductor chips further complicate generalization.

Like PBs, generalizing probe cards is important for reducing production costs and shortening development lead time. Although complex, we will continue to explore designs that enhance generalization.

6. Conclusion

This paper reported on the generalized design of performance boards, which are critical components in wafer testing.

The new design eliminates the need to replace or produce multiple large main PBs, improving work efficiency and reducing costs.

Moving forward, we aim to generalize probe cards as well, further lowering costs and delivering products that satisfy our customers.