LC5550LD Series PWM and Quasi-Resonant Off-Line Switching Regulator ICs

General Description

LC5550LD series is a PWM and quasi-resonant topology non-isolated buck LED driver IC. It incorporates separate controller and power MOSFET chips, and is designed for input capacitorless applications. The controller adapts the average current control method for realizing high power factors. The rich set of protection features helps to realize low component counts, and high performance-to-cost power supply.

Figure 1. The LC5550LD series package is a fully molded DIP8, with pin 7 removed for greater isolation. (Image not to scale.)

Features and Benefits

- PWM and quasi-resonant topology
- Integrated on-time control circuit (it realizes high power factor by average current control)
- Integrated soft-start circuit (reduces power stress during start-up on the incorporated power MOSFET and output rectifier)
- Integrated bias assist circuit (improves startup performance, suppresses V_{CC} voltage droop during operation, and allows use of low-rated ceramic capacitor on VCC pin)
- Integrated Leading Edge Blanking (LEB) circuit
- Integrated maximum on-time limit circuit
- Protection features:
  - Overcurrent protection (OCP): pulse-by-pulse
  - Overvoltage protection (OVP): latched shutdown
  - Overload protection (OLP): latched shutdown
  - Thermal shutdown (TSD): latched shutdown

Applications

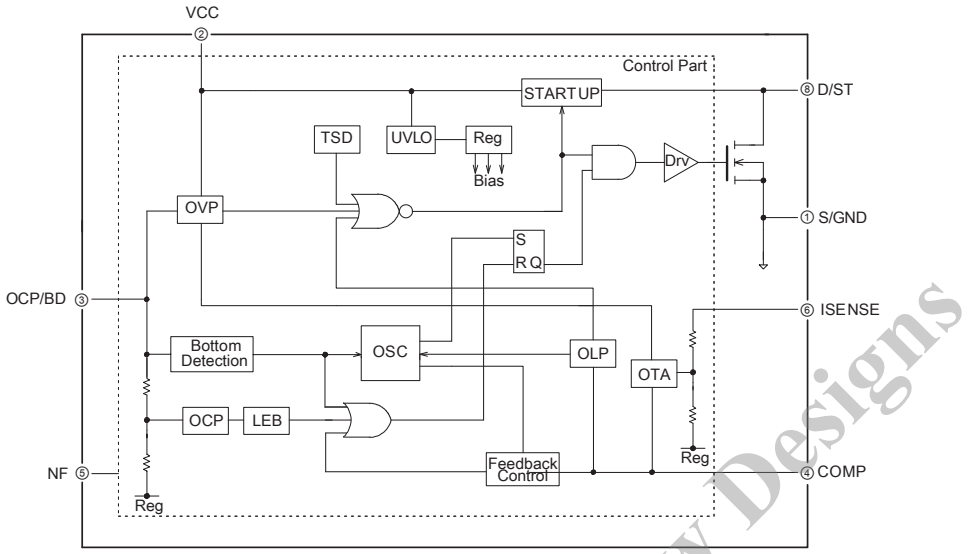
- LED lighting fixtures
- LED light bulbs

The product lineup for the LC5550LD series provides the following options:

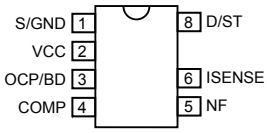
Part Number	MOSFET V_{DSS}(min) (V)	$R_{DS(on)}$ (max) (Ω)	PWM Operation Frequency, f_{OSC}(typ) (kHz)	On-Time $t_{ON(MAX)}$(typ) (µs)	P_{OUT}* (W)	
					230 VAC	Universal
LC5555LD	650	3.95	72	9.3	13	10
LC5556LD	650	1.9	60	11.2	20	16

*Based on the thermal rating; the allowable maximum output power can be up to 120% to 140% of this value. However, maximum output power may be limited in such an application with low output voltage or short duty cycle.

Functional Block Diagram



Pin-out Diagram

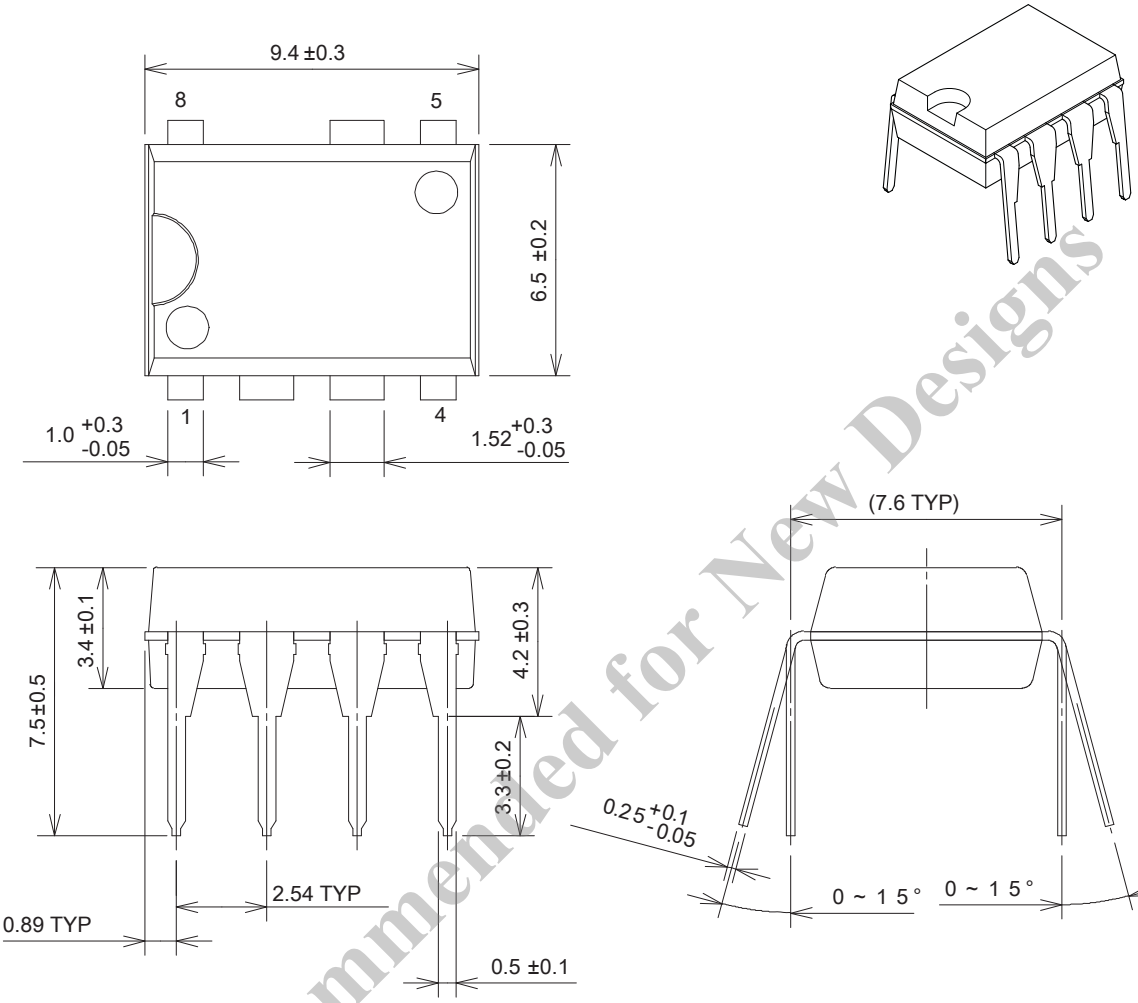


Pin List Table

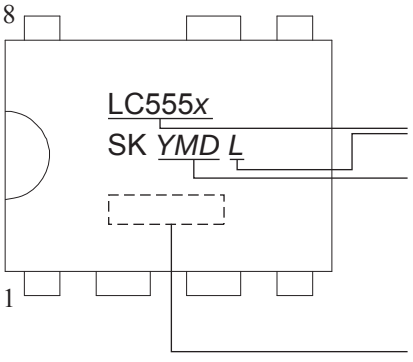
Number	Name	Function
1	S/GND	MOSFET source and GND pin for the Control Part
2	VCC	Supply voltage input and Overvoltage Protection (OVP) signal input
3	OCP/BD	Overcurrent Protection (OCP), quasi-resonant signal input, and Overvoltage Protection (OVP) signal input
4	COMP	Feedback phase-compensation input
5	NF	No function; must be externally connected to S/GND pin with as short a trace as possible, for stable operation of the IC
6	ISENSE	Output current sensing voltage input
7	–	Pin removed
8	D/ST	MOSFET drain pin and input of the startup current

Table of Contents

Package Diagram
DIP8 package



Unit: mm



Part Number

Lot Number
Y is the last digit of the year (0 to 9)
M is the month (1 to 9, O, N, or D)
D is a period of days (1 to 3):
1 – 1st to 10th
2 – 11th to 20th
3 – 21st to 31st

Sanken Control Number

Pb-free. Device composition compliant with the RoHS directive.

Electrical Characteristics

• This section provides electrical characteristic data for each product.

• The polarity value for current specifies a sink as "+ ," and a source as "−," referencing the IC.

• Please refer to the datasheet of each product for additional details.

Absolute Maximum Ratings Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Notes		Pins	Rating	Unit
Drain Current	I_{DPEAK}	LC5555LD	Single pulse	8 – 1	2.5	A
		LC5556LD	Single pulse	8 – 1	4.0	A
Single Pulse Avalanche Energy	E_{AS}	LC5555LD	I_{LPEAK} = 2.0A, V_{DD} = 99 V, L = 20 mH	8 – 1	47	mJ
		LC5556LD	I_{LPEAK} = 2.7A, V_{DD} = 99 V, L = 20 mH	8 – 1	86	mJ
Input Voltage for Control Part (MIC)	V_{CC}			2 – 1	35	V
OCP/BD Pin Voltage	V_{OCP}			3 – 1	−2.0 to 5.0	V
COMP Pin Voltage	V_{COMP}			4 – 1	−0.3 to 7.0	V
ISENSE Pin Voltage	V_{SEN}			6 – 1	−0.3 to 5.0	V
Allowable Power Dissipation of MOSFET	P_{D1}	Mounted on a 15 mm × 15 mm PCB		8 – 1	0.97	W
Operating Ambient Temperature	T_{OP}			—	−55 to 125	°C
Storage Temperature	T_{stg}			—	−55 to 125	°C
Channel Temperature	T_{ch}			—	150	°C

LC5550LD Electrical Characteristics of MOSFET Unless specifically noted, T_A is 25°C

Characteristic	Symbol		Test Conditions	Pins	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V_{DSS}			8 – 1	650	—	—	V
Drain Leakage Current	I_{DSS}			8 – 1	—	—	300	μA
On-Resistance	$R_{DS(on)}$	LC5555LD		8 – 1	—	—	3.95	Ω
		LC5556LD			—	—	1.9	Ω
Switching Time	t_f	LC5555LD		8 – 1	—	—	250	ns
		LC5556LD			—	—	400	ns
Thermal Resistance*	$R_{\theta ch-c}$	LC5555LD		—	—	—	42	°C/W
		LC5556LD			—	—	35.5	°C/W

*The thermal resistance between the channels of the MOSFET and the case. T_C measured at the center of the case top surface.

Electrical Characteristics of Control Part (MIC) Unless specifically noted, T_A is 25°C, V_{CC} is 20 V

Characteristic	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Unit
Power Supply Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		2 – 1	13.8	15.1	17.3	V
Operation Stop Voltage*	$V_{CC(OFF)}$		2 – 1	8.4	9.4	10.7	V
Circuit Current in Operation	$I_{CC(ON)}$		2 – 1	–	–	4.7	mA
Startup Circuit Operation Voltage	$V_{STARTUP}$		8 – 1	18	21	24	V
Startup Current	$I_{CC(STARTUP)}$	V_{CC} = 13 V	2 – 1	−8.5	−4.0	−1.5	mA
Startup Current Threshold Biasing Voltage*	$V_{CC(BIAS)}$		2 – 1	9.5	11.0	12.5	V
Normal Operation							
PWM Operation Frequency	f_{OSC}	LC5555LD	8 – 1	60	72	84	kHz
		LC5556LD		50	60	70	kHz
Maximum On-Time	$t_{ON(MAX)}$	LC5555LD	8 – 1	8.0	9.3	11.2	µs
		LC5556LD		9.0	11.2	13.4	µs
COMP Pin Control Minimum Voltage	$V_{COMP(MIN)}$		4 – 1	0.30	0.55	0.80	V
Error Amplifier Reference Voltage	$V_{SEN(TH)}$		6 – 1	–0.21	–0.2	–0.19	V
Error Amplifier Source Current	$I_{SEN(SOURCE)}$		4 – 1	−36	−24	−12	µA
Error Amplifier Sink Current	$I_{SEN(SINK)}$		4 – 1	12	24	36	µA
Leading Edge Blanking Time	$t_{ON(LEB)}$		3 – 1	–	600	–	ns
Quasi-Resonant Operation Threshold Voltage-1	$V_{BD(TH1)}$		3 – 1	0.14	0.24	0.34	V
Quasi-Resonant Operation Threshold Voltage-2	$V_{BD(TH2)}$		3 – 1	0.11	0.16	0.21	V
Protected Operation							
OCP/BD Pin Overcurrent Protection (OCP) Threshold Voltage	$V_{OCP(TH)}$		3 – 1	−0.92	−0.8	−0.68	V
OCP/BD Pin Source Current	I_{OCP}		3 – 1	−120	−40	−10	µA
OCP/BD Pin Overvoltage Protection (OVP) Operation Voltage	$V_{BD(OVP)}$		3 – 1	2.2	2.6	3.0	V
Overload Protection (OLP) Threshold Voltage	$V_{COMP(OLP)}$		4 – 1	4.1	4.5	4.9	V
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 1	28.5	31.5	34.0	V
Thermal Shutdown Activating Temperature	$T_{J(TSD)}$		–	135	–	–	°C

*$V_{CC(BIAS)}$ > $V_{CC(OFF)}$ always.

Typical Application Circuits

The LC5550LD series is a non-isolated buck LED driver IC which can be used with both PWM control and quasi-resonant control. Figure 1 shows a circuit example with PWM control. Details are described in the PWM Operation section.

Figure 2 shows a circuit example with quasi-resonant control. In a quasi-resonant circuit configuration, a delay circuit (D7, D8, R7, and C8 in the figure) is added to PWM circuit. When the output voltage rises, the OCP/BD pin voltage will also rise, and when the quasi-resonant signal of the positive voltage on the OCP/BD pin reaches $V_{BD(TH1)}$ = 0.24 V or more, the quasi-resonant operation will begin. Details are described in the Quasi-Resonant Operation section.

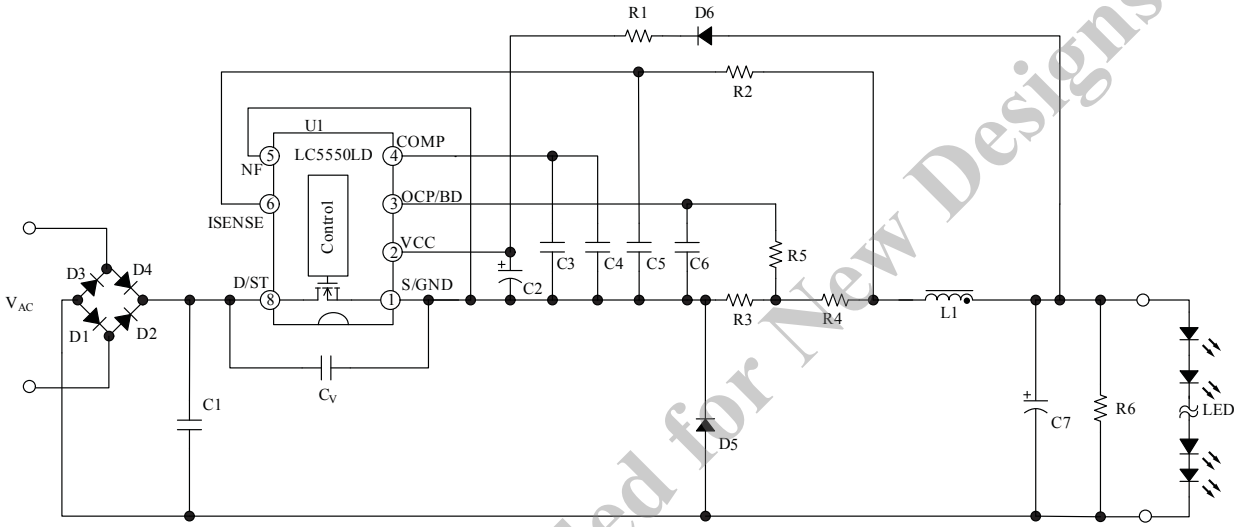


Figure 1. Typical application circuit 1, PWM control

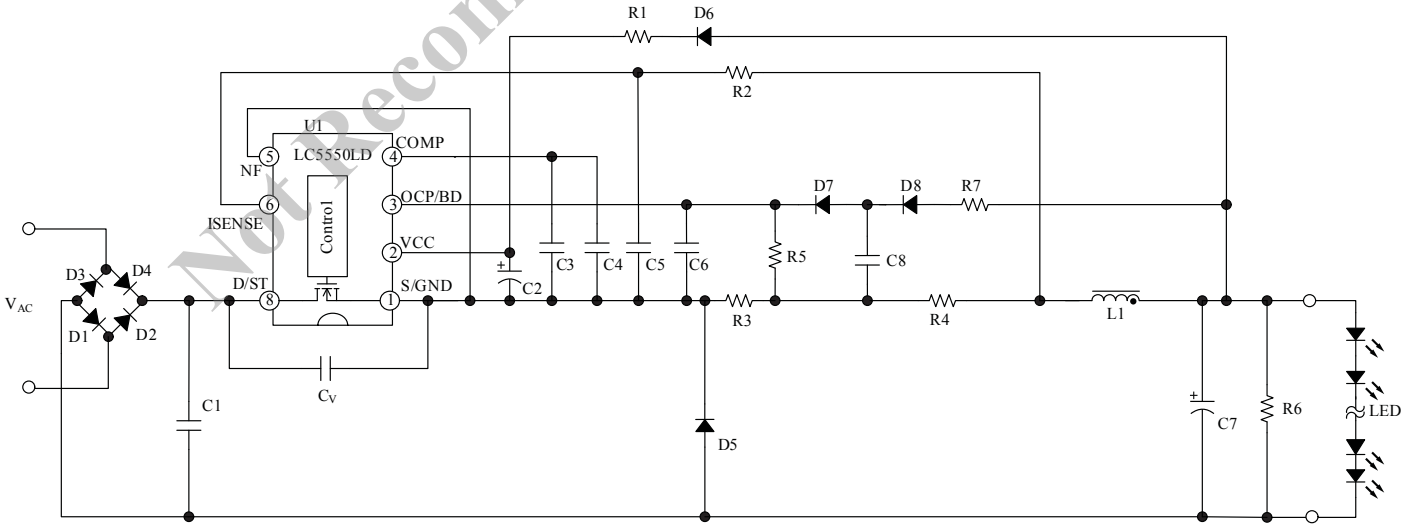


Figure 2. Typical application circuit 2, Quasi-resonant control

Functional Description

All of the parameter values used in these descriptions are typical values, according to the LC5555LD specification, unless they are specified as minimum or maximum.

With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

Startup Operation

Startup Period

Figure 3 shows the VCC pin peripheral circuit. The VCC pin voltage can be supplied from V_O in buck-converter configuration. The built-in startup circuit is connected to the D/ST pin, and it generates a constant current, $I_{CC(STARTUP)}$ = –4.0 mA to charge capacitor C2 connected to the VCC pin. During this process, when the VCC pin voltage reaches $V_{CC(ON)}$ = 15.1V, the Control Part (MIC) starts operation. After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

The startup time is determined by the C2 capacitance. A ceramic or film capacitor can be used for C2, and a value of 0.22 to 22 µF is generally recommended. The approximate value of the startup time can be calculated using the following formula:

$$t_{START} \approx C_2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{CC(STARTUP)}|} \quad (1)$$

where:

t_{START} is the startup time in s, and

$V_{CC(INT)}$ is the initial voltage of the VCC pin in V.

Undervoltage Lockout (UVLO) Circuit

Figure 4 shows the relation of the VCC pin voltage to the circuit current, I_{CC}. When the VCC pin voltage reaches the Operation Start Voltage, $V_{CC(ON)}$ = 15.1 V, the Control Part (MIC) starts operation and the circuit current increases. In operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the Control Part stops operation by UVLO circuit, and reverts to the state before startup.

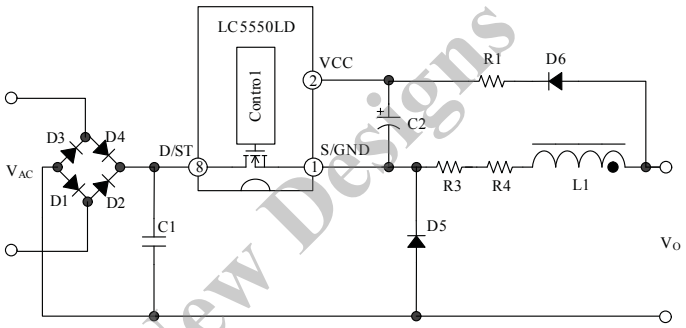


Figure 3. D/ST and VCC pin peripheral circuits

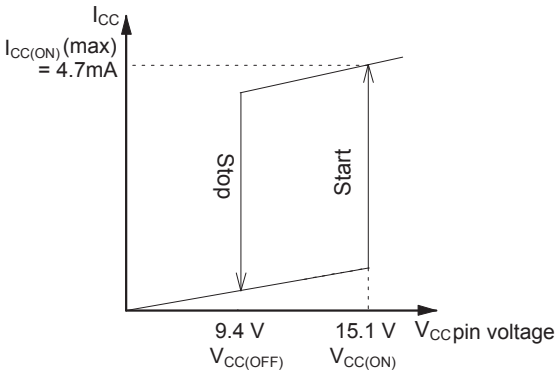


Figure 4. V_{CC} versus I_{CC}

The VCC pin voltage must be set within the specifications of the input voltage range and the output load range of the power supply, according to the following formula. The optimal value is around 20 V.

$$V_{CC(BIAS)}(\max) < V_{CC} < V_{CC(OVP)}(\min) \quad (2)$$
$$12.5\ (V) < V_{CC} < 28.5\ (V)$$

When the V_O is in the range shown in the above formula, within the specifications of the input voltage range, and the output load range of the power supply, the VCC pin voltage can be supplied from V_O (figure 3). In the case where V_{CC} is higher than $V_{CC(OVP)}(\min)$, the Zener diode D7 is inserted, to supply VCC pin voltage (figure 5).

When the increasing power consumption of the Zener diode is not negligible (V_{CC} is higher than $V_{CC(OVP)}(\min)$), or V_{CC} is lower than $V_{CC(BIAS)}(\max)$, the transformer (T1) is used to supply the VCC pin voltage (figure 6).

Bias Assist Function

Figure 7 shows the VCC pin voltage behavior during the startup period. If VCC pin voltage decreases enough to reach the Startup Current Threshold Biasing Voltage, $V_{CC(BIAS)}$ = 11.0 V, the Bias Assist function is activated before the voltage decreases to $V_{CC(OFF)}$ = 9.4 V. While the Bias Assist function is operating, any decrease of the VCC pin voltage is counteracted by a supplementary current from the Startup circuit, and thus V_{CC} is kept almost constant.

Because of the Bias Assist function, the use of a low-value capacitor for C2 (see figure 3) is allowed. Also, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function can also be shortened. It is necessary to check and adjust the startup process in the application, so that poor starting conditions may be avoided.

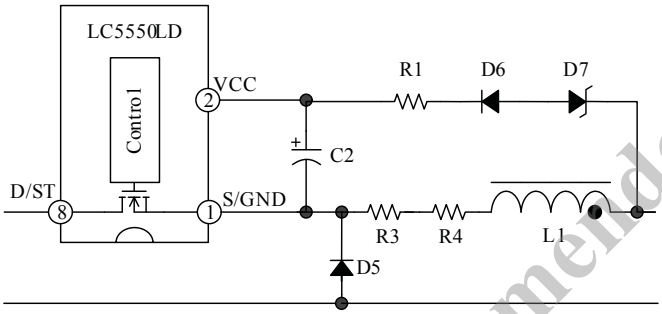


Figure 5. VCC pin peripheral circuits (V_{CC} > $V_{CC(OVP)}(\min)$)

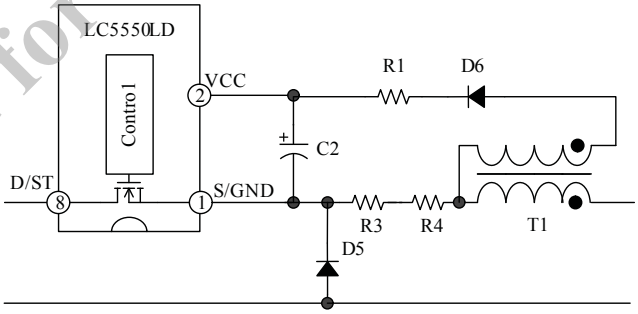


Figure 6. VCC pin peripheral circuits (V_{CC} > $V_{CC(OVP)}(\min)$)

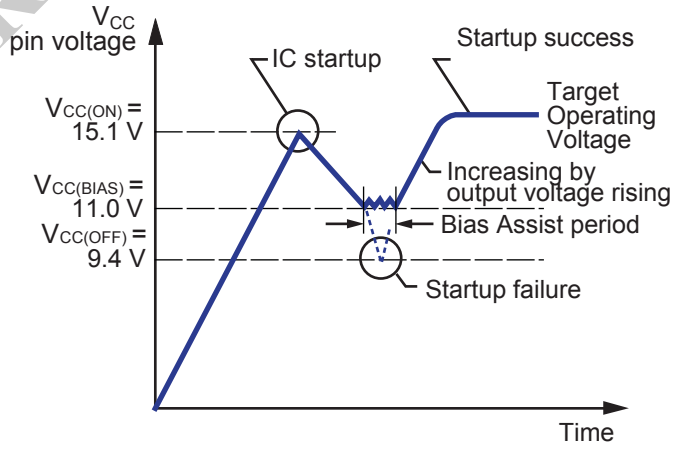


Figure 7. V_{CC} during startup period

Soft Start Function

Figure 8 shows the operation waveform at startup. The soft start operation begins when the COMP pin voltage reaches $V_{COMP(MIN)}$ = 0.55 V, and lasts until the output current becomes constant.

During this period, check the items below:

• Ensure the VCC pin voltage does not drop to the Operation Stop Voltage, $V_{CC(OFF)}$.

• Ensure the output current reaches the target value before the Overload Protection (OLP) function is activated by the COMP pin voltage reaching $V_{COMP(OLP)}$ = 4.5 V.

Operational Mode at Startup

Figure 8 shows the operation mode at startup. After the startup period, when the COMP pin voltage reaches $V_{COMP(MIN)}$= 0.55 V, the switching operation begins in PWM operation at an operation frequency of f_{OSC} = 72 kHz (for LC5555LD, 60 kHz for LC5556LD).

Then, when the output voltage rises, the auxiliary winding voltage will also rise, and when the quasi-resonant signal of the positive voltage on the OCP/BD pin reaches $V_{BD(TH1)}$ = 0.24 V or more, the quasi-resonant operation will begin.

Figure 9 shows the OCP/BD pin voltage waveform expanded time scale at point A of figure 8.

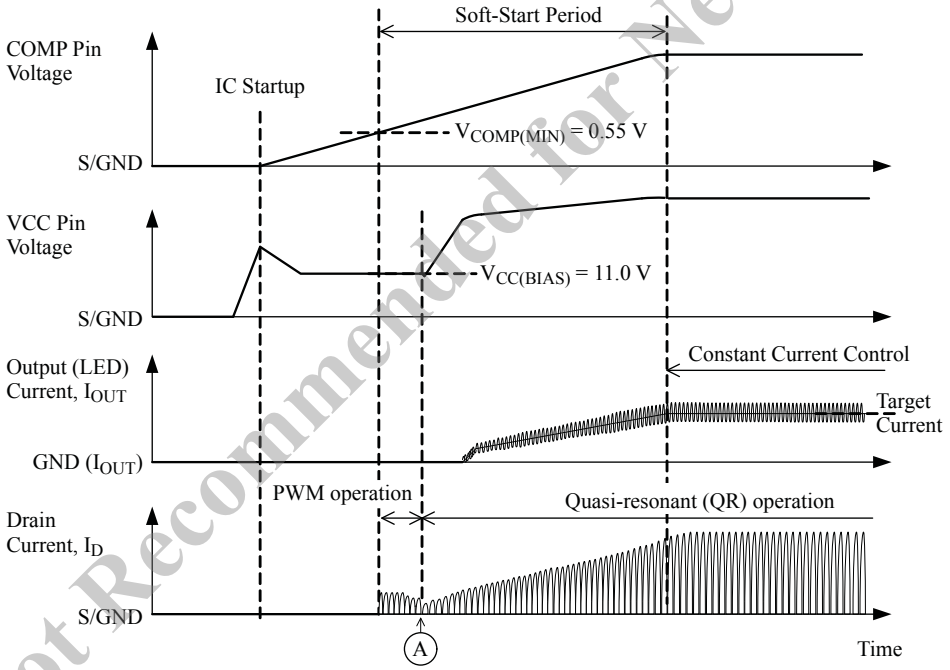


Figure 8. Soft-start operation waveforms at startup

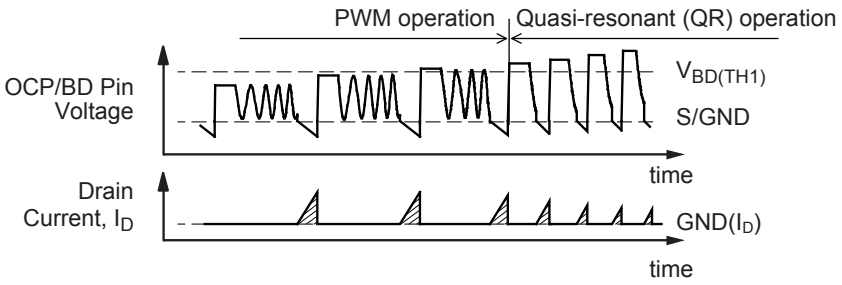


Figure 9. OCP/BD Pin Voltage (with time scale expanded at point A of figure 8)

Normal Operation

On-Time Control Operation

Figure 10 shows the peripheral circuit at the COMP pin, and figure 11 shows the on-time control. The output control is done by voltage mode control, which controls on-time depending on output load, and average current control.

As shown in figure 11, in the average current control operation, the internal error amplifier reference voltage $V_{SEN(TH)}$ = –0.2 V is compared with the voltage drop of secondary side constant current detection resistance in the OTA circuit, and is equalized with the COMP pin.

This averaged voltage at the COMP pin is compared with the internal oscillator (OSC) output by the internal FB comparator, and the on-time is controlled. Here, the internal OSC indicates the oscillator circuit, which controls the PWM operation frequency, quasi-resonant oscillation, and the maximum on-time limit. The recommended value of capacitor C4 linked to the COMP pin is approximately 1.0 to 4.7 µF. The value of R2 is 100 to 220 Ω.

R2 and C5 are the filter for ISENSE pin. In the case where R2 value is large, ISENSE current (–40 µA) affects the accuracy of the LED current. Thus R2 and C5 values are recommended to be approximately 220 Ω and approximately 0.1 µF, respectively.

The constant output current control of the output is done as below:

- When the output load current becomes less than the target value, the ISENSE pin voltage becomes low. This causes the averaged OTA circuit output voltage at the COMP pin to become high, and the on-time and the output current increase.
- When the output current becomes greater than the target value, the circuits operate in the opposite way. The averaged voltage at the COMP pin becomes low, and the on-time and the output current decrease.

Figure 12 shows the average input current waveform. The averaged COMP pin voltage becomes constant, and the duty cycle control becomes based on the E_{IN} voltage (C1 voltage in figure 3). It makes an averaged input current sine waveform which realizes a high power factor.

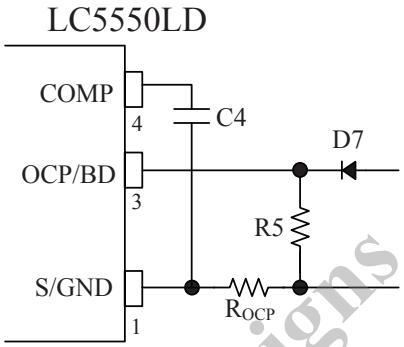


Figure 10. COMP pin peripheral circuit

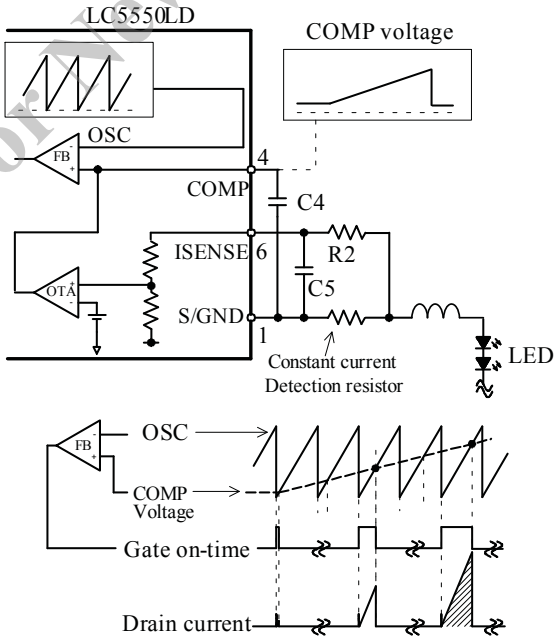


Figure 11. On-time control

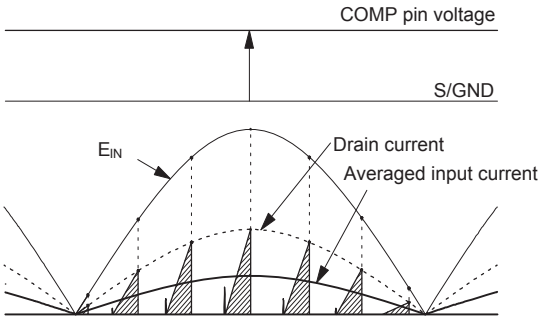


Figure 12. Averaged input current waveform

PWM Control

Figure 13 shows the waveforms and figure 14 shows the output current path in PWM operation, respectively. The basic current control of internal PWM is described in the following

PWM On-Time Period At startup, or during normal operation before the output current through the LED string reaches the target current level, the internal power MOSFET turns on and the output current flows through the I_{ON} path shown in figure 14.

Turing-Off Period The output current through the LED string is equivalent to the current through the detection resistors, R3 and R4. Thus the LED current is detected at the ISENSE pin as a voltage, V_{ISENSE}. As described in the On-Time Control Operation section, the on-time of the MOSFET is controlled using V_{ISENSE}. When V_{ISENSE} is equal to the internal PWM reference voltage, the internal power MOSFET turns off.

PWM Off-Time Period When the internal power MOSFET turns off, the current recirculation diode, D5, is forward biased by the back electromotive force (BEMF) in the inductor, L1, and D5 turns on. Then the energy stored in L1 during the PWM on-time flows through the recirculation path shown as I_{OFF} in figure 14.

Turning-On Period After the PWM operation cycle (T = 1 / f_{OSC}), the internal power MOSFET turns-on again, and the PWM on-time period repeats.

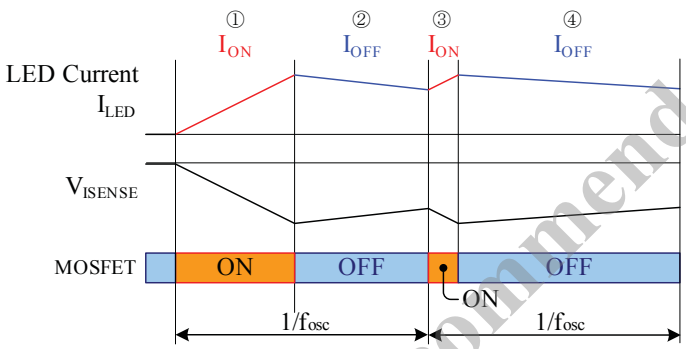


Figure 13. Constant current control operation in a buck configuration

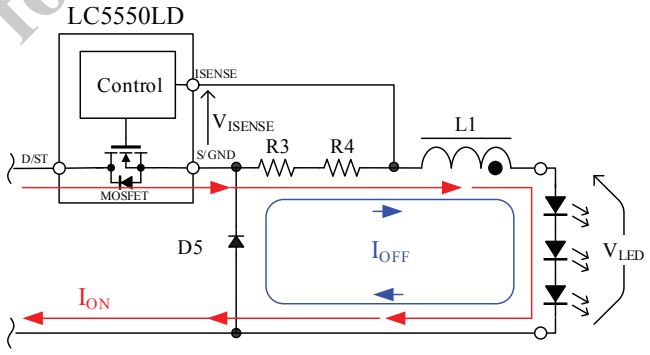
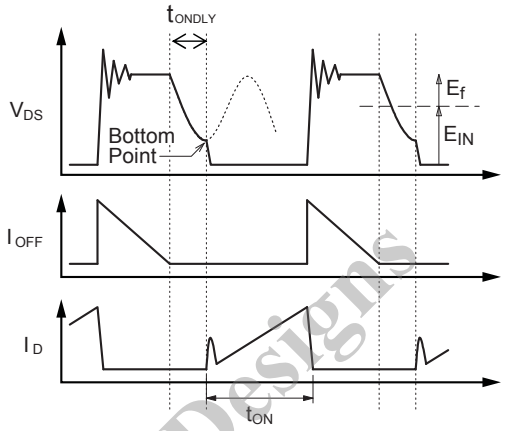


Figure 14. Output current flow in a buck configuration during PWM on-time and off-time periods

Quasi-Resonant Operation

Figure 15 shows the circuit of quasi-resonant topology. The buck converter is a system which transfers the energy stored in the choke coil, L1, to the output when the power MOSFET is turned off. The MOSFET drain node begins free oscillation based on the inductance, L, of the choke coil, L1, and C_V across the drain and source pins. The quasi-resonant operation is the V_{DS} bottom-on operation that turns-on the MOSFET at the bottom point of V_{DS} free oscillation.

Figure 16 shows an ideal V_{DS} waveform during bottom-on operation. Using bottom-on operation, switching loss and switching noise are reduced and it is possible to obtain converters with high efficiency and low noise.



Half cycle of free oscillation, $t_{ONDLY} \approx \pi\sqrt{L_P \times C_V}$

Figure 16. Ideal bottom-on operation waveform (MOSFET turn-on at a bottom point of a V_{DS} waveform)

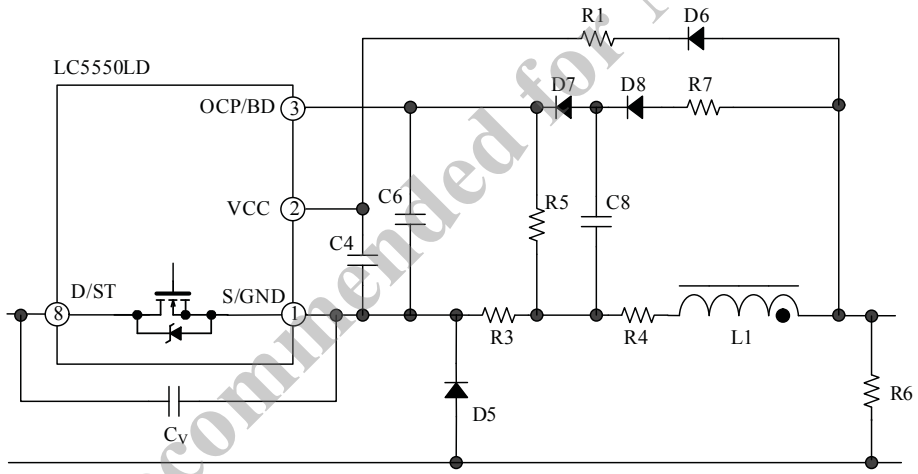


Figure 15. OCP/BD pin peripheral circuit

Bottom-On Timing

During the turning-off of the power MOSFET, the output voltage is fed through the delay circuit (D7, D8, R7, and C8 of figure 15) to the OCP/BD pin, and a positive voltage quasi-resonant signal is provided to the OCP/BD pin (the quasi-resonant signal is V_{BD}).

After the power MOSFET turns off, the quasi-resonant signal immediately goes up and it exceeds the Quasi-Resonant Operation Threshold Voltage 1, $V_{BD(TH1)}$ = 0.24 V. After this occurs, the power MOSFET remains off until the quasi-resonant signal comes down enough to cross the Quasi-Resonant Operation Threshold Voltage 2, $V_{BD(TH2)}$ = 0.16 V. Then the power MOSFET again turns on. In addition, at this point, the threshold voltage goes up to $V_{BD(TH1)}$ automatically, to prevent malfunction of the quasi-resonant operation from noise interference.

Figure 17 defines the pulse width of the quasi-resonant signal. For initiating quasi-resonant operation, the quasi-resonant signal pulse width between the two points $V_{BD(TH1)}$ and $V_{BD(TH2)}$, t_{QR}, must be equal to 1.2 µs or more. This pulse width must be ensured, while at the same time the OCP/BD pin peak voltage, $V_{BD(PK)}$, is recommended to be between 1.5 and 2.0 V. Both conditions should be satisfied throughout the power supply input and output ranges, and covering variations in R5 and R7 actual component values.

R5 and C6 Setup R5 is recommended to be between 100 and 330 Ω, and C6 to be between 100 and 470 pF.

R7 Setup R7 must set the range for the quasi-resonant signal: either greater than or equal to $V_{BD(TH1)}$ (under input and output conditions where V_{CC} becomes lowest), or less than the OCP/BD Pin Overvoltage Protection (OVP) Threshold Voltage, $V_{BD(OVP)}$ = 2.6 V (under conditions where V_{CC} becomes highest). The formula below is used to calculate R7, ignoring the value of R_{OCP} assuming R_{OCP} << R5:

$$R_7 = \frac{R_3 \times (V_{CC} - V_{BD(PK)} - 2 \times V_f)}{V_{BD(PK)}} \quad (2)$$

given R_5 = 220 Ω, $V_{BD(PK)}$ = 1.5 V, V_{CC} = 16 V, and the V_f of D7 and D8 = 0.8 V. R_7 is approximately 1.89 kΩ, and it is 1.8 kΩ in the E12 series.

If the pulse width is not satisfied, increase R5 or decrease R7, in order to raise $V_{BD(PK)}$. Alternatively, increasing the capacitance of resonant capacitor C_V is also effective because it widens the free oscillation period. However, it causes an additional switching loss increase; therefore, ensure the IC temperature rise is acceptable.

D7 and D8 Setup D7 and D8 are fast recovery and low coupling capacitance diodes.

C8 Setup The delay time, t_{ONDLY}, after which the power MOSFET turns on, is adjusted by the value of C8 , so that the power MOSFET turns on at the bottom-on of V_{DS}. To do so, observe the power MOSFET drain voltage, V_{DS}, the drain current, I_D, and the quasi-resonant signal, under the maximum input voltage and the maximum output power.

The following show how to adjust the turn-on point:

- If the turn-on point precedes the bottom of the V_{DS} signal, it causes higher switching losses. In that situation, after confirming the initial turn-on point, delay the turn-on point by increasing the C8 value gradually, so that the turn-on will match the bottom point of V_{DS}.
- In the converse situation, if the turn-on point lags behind the V_{DS} bottom point, it causes higher switching losses also. After confirming the initial turn-on point, advance the turn-on point by decreasing the C8 value gradually, so that the turn-on will match the bottom point of V_{DS} .

An initial reference value for C8 is about 1000 pF.

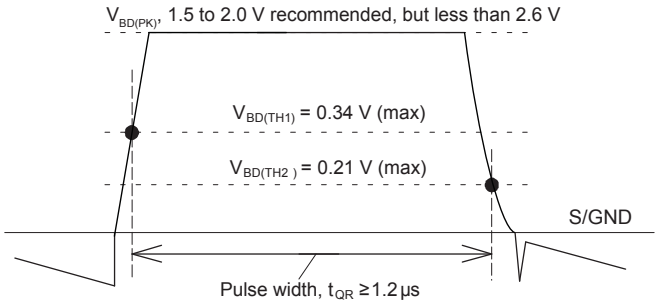


Figure 17. Definition of the pulse width of the quasi-resonant signal

Protection Functions

Overvoltage Protection (OVP)

The IC has two OVP activation methods: linked to the VCC pin and to the OCP/BD pin. Both methods are latched. After the switching operation stops, the VCC pin voltage will begin to decrease, and when it falls to $V_{CC(BIAS)}$ = 11.0 V, the Bias Assist Function will be activated. When the Bias Assist Function is activated, the startup current is supplied to the VCC pin in order to prevent the VCC pin voltage from decreasing to $V_{CC(OFF)}$ = 9.4 V, and thus the latched state is maintained. Releasing the latched state is done by turning off the input voltage and allowing the VCC pin voltage to drop below $V_{CC(OFF)}$.

VCC Pin Overvoltage Protection

Figure 18 shows the waveforms of the OVP function on the VCC pin. When the VCC pin voltage with reference to the S/GND pin reaches $V_{CC(OVP)}$ = 31.5 V or more, VCC pin OVP is activated and the IC stops switching operation, in latch mode. Because VCC pin voltage is proportional to the output voltage, it can be used to detect an output overvoltage event.

In the cases represented by the typical application circuit (figures 1 and 2), the output voltage $V_{OUT(OVP)}$ is approximately 31.5 V. When the output voltage is higher than the VCC operation range, Zener diode D9 is necessary, as shown in figure 19. The output voltage is approximately 31.5 V + V_{ZENER}, in this configuration.

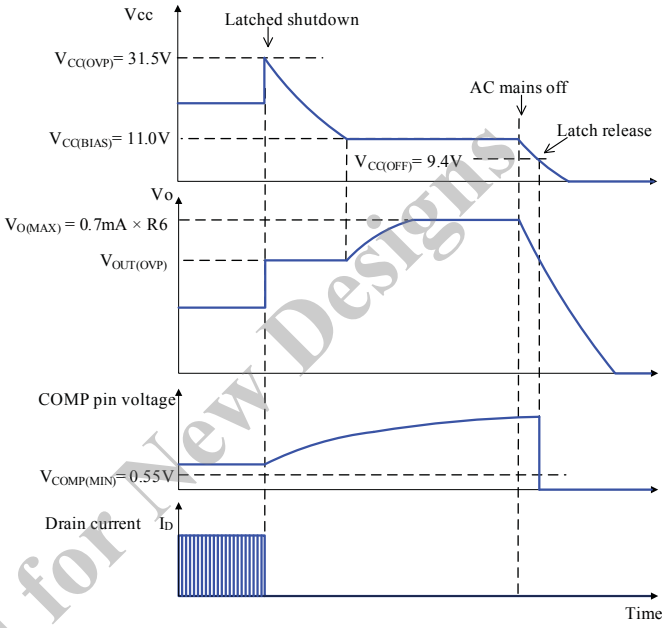


Figure 18. Waveforms when VCC pin OVP function is being activated

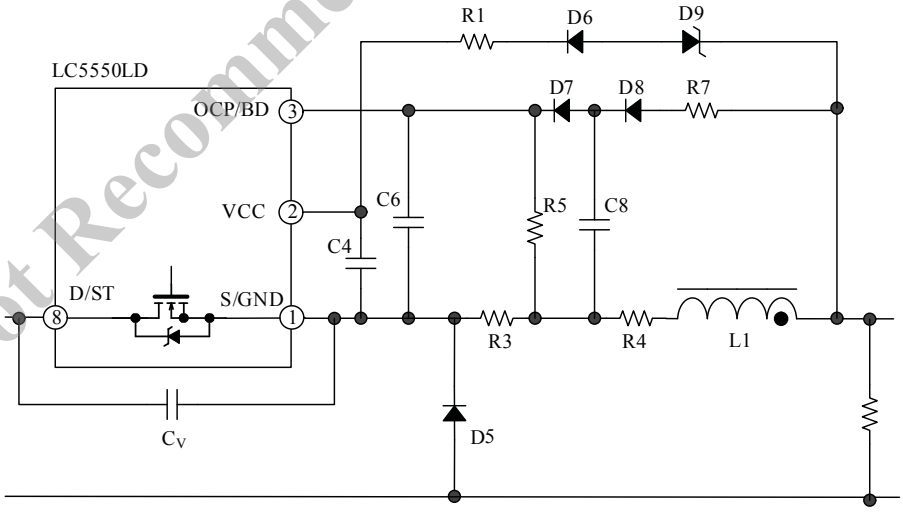


Figure 19. Circuit example in the case where the output voltage is higher than the VCC operation range

When the VCC pin OVP function is being activated, the VCC pin voltage is maintained by the current from the startup circuit of the IC. Thus the latch operation continues. The current charges the output capacitor. Thus the output voltage rises.

When the D/ST pin voltage with reference to the S/GND pin drops below the Startup Circuit Operation Voltage, $V_{STARTUP}$, the VCC pin voltage decreases and the latched is released.

In order to continue the latch operation, the D/ST pin voltage must be above $V_{STARTUP}$. The resistor (R6 in figures 1 and 2) is necessary, placed in parallel to the output capacitor. The maximum output voltage in latch operation is approximately $V_O(max) \approx 0.7\ mA \times R_6$.

The optimal value of R6 should be determined with consideration of the latch operation, the maximum output voltage, and the effect on LED current in normal operation. Releasing the latched state is done by turning off the input voltage and allowing the VCC pin voltage to drop below $V_{CC(OFF)}$.

OCP/BD Pin Overvoltage Protection

Figure 20 shows the OCP/BD pin OVP circuit. The OCP/BD pin OVP function is activated when diode D10 is added between OCP/BD pin and VCC pin in a quasi-resonant circuit configuration.

Figure 21 shows the waveform of the OCP/BD pin OVP function. When the OCP/BD pin voltage with reference to the S/GND pin reaches $V_{BD(OVP)}$ = 2.6 V or more, OCP/BD pin OVP is activated and the IC stops switching operation, in latch mode. This input voltage must be less than the absolute maximum rating, 5 V. Releasing the latched state is done by turning off the input voltage and allowing the VCC pin voltage to drop below $V_{CC(OFF)}$.

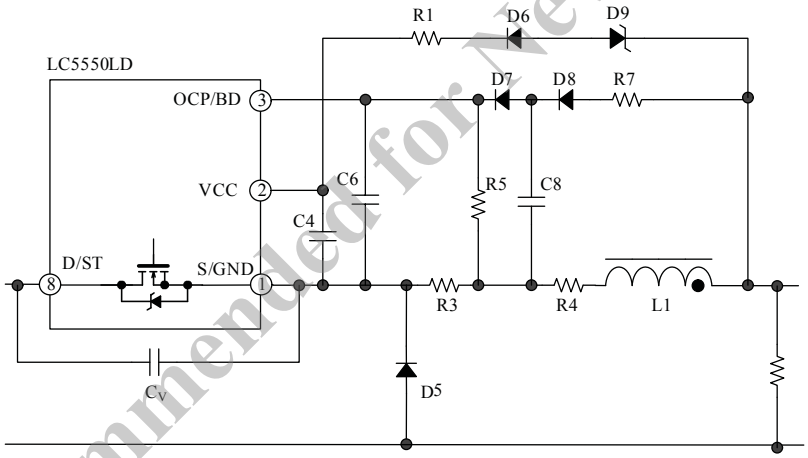


Figure 20. OCP/BD pin OVP circuit

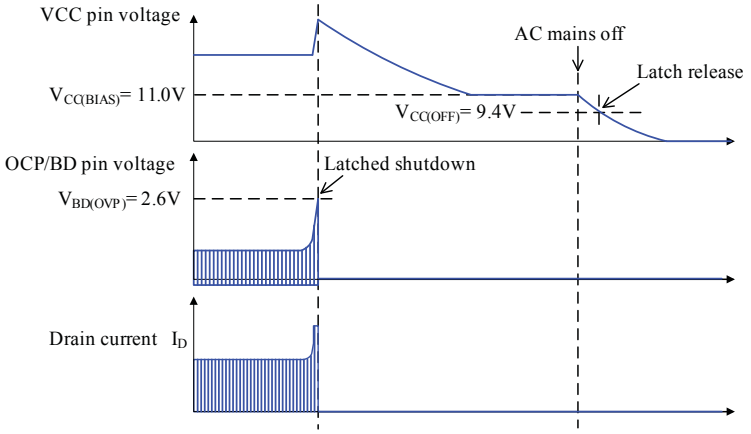


Figure 21. Waveforms when OCP/BD pin OVP function is being activated

Overload Protection (OLP)

In the overload protection (OLP) state, the peak drain current is limited by OCP operation under an overload condition. Figures 22 and 23 show the peripheral circuit of the COMP pin and waveforms when OLP function is being activated, respectively.

In an overload condition, the VCC pin voltage drops because the output voltage drops. When the VCC pin voltage reaches the Startup Current Threshold Biasing Voltage, $V_{CC(BIAS)}$ = 11.0 V, the Bias Assist Function is activated to avoid the VCC pin voltage from decreasing.

Simultaneously, the ISENSE pin voltage decreases. Because the OTA circuit output inside the IC will be lost if the ISENSE pin voltage falls to the error amplifier reference voltage, $V_{SEN(TH)}$ = –0.2 V, the C4 capacitor, connected to the COMP pin, is charged by the current generator inside the COMP pin.

When the COMP pin voltage reaches the OLP Threshold Voltage, $V_{COMP(OLP)}$ = 4.5 V, the overload protection circuit will operate and stop switching operation, in latch mode. Releasing the latched state is done by turning off the input voltage and allowing the VCC pin voltage to drop below $V_{CC(OFF)}$.

If the OLP function is activated at transient conditions such as startup, it may cause startup failure. In order to avoid this, a C4 value of 1 to 4.7 µF is generally recommended. Too determine the optimal value, it is necessary to check and adjust in the application

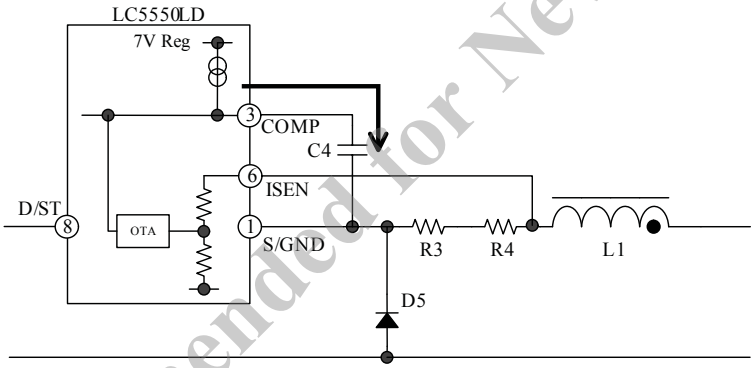


Figure 22. COMP pin peripheral circuit

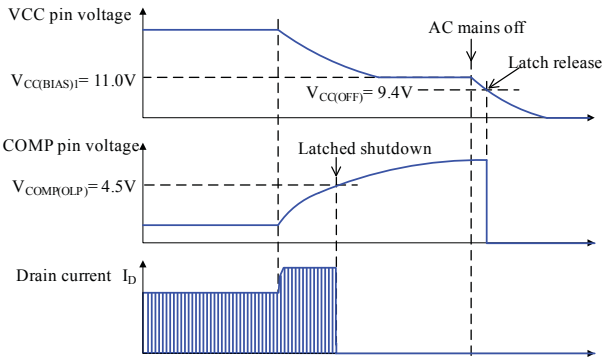


Figure 23. Waveforms when OLP function is being activated

Overcurrent Protection (OCP)

The Overcurrent Protection (OCP) feature monitors the power MOSFET drain current on a pulse-by-pulse basis, in order to limit output power. The drain current of the power MOSFET is detected by the current detection resistor, R3, placed between the OCP/BD pin and the S/GND pin, as shown in figure 24.

The voltage across R3, V_{R3} , is fed through R5 to the OCP/BD pin, to be detected by it. The turn-off point for the power MOSFET can be determined as that point where V_{R3} reaches the value of the following equation:

$$V_{R3} = -\left(|V_{OCP}| + R_5 \times |I_{OCP}| \right) \quad (3)$$

where

V_{OCP}: OCP threshold voltage (−0.8 V),

R_5: R5 resistance, and

I_{OCP}: OCP/BD pin source current (−40 μA).

A filter is inserted at the OCP/BD pin in order to prevent malfunction:

• R5 setup. In order to minimize effects of variation in the internal resistor, R5 is recommended to have a value from 100 to 330 Ω.

• C6 setup. C6 is recommended to have a value from 100 to 470 pF, with good temperature characteristics. Selecting larger capacitances for C6 would cause OCP response to become slow, and then it would result in an increase in the peak drain current at transient conditions, such as startup.

Because the OCP function detects a peak current, it can react to the surge voltage at the power MOSFET turn-on edge and thus the power MOSFET might turn off. In order to avoid this, the Leading Edge Blanking Time is built-in. The Leading Edge Blanking Time, $t_{ON(LEB)}$, is set to 600 ns.

The surge current pulse width must be less than $t_{ON(LEB)}$ as shown in figure 25. In case its width is longer than that, try these measures:

• adjust the turn-on point to the V_{DS} bottom point

• reduce the voltage resonant capacitor C_V capacitance

Thermal Shutdown Protection

Thermal Shutdown protection is activated when the temperature of the Control Part (MIC) in the IC reaches $T_{J(TSD)}$ = 135°C(min), and then the IC stops switching operation, in latch mode. Releasing the latched state is done by turning off the input voltage and allowing the VCC pin voltage to drop below $V_{CC(OFF)}$.

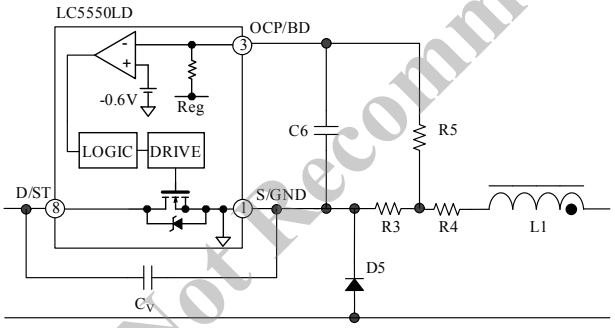


Figure 24. OCP/BD pin peripheral circuit

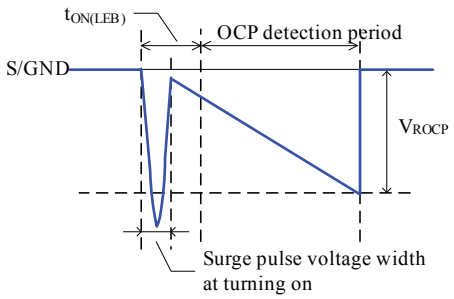


Figure 25. OCP/BD pin voltage (converted from MOSFET drain current by R3)

Maximum On-Time Limiting Function

The maximum on-time, set at $t_{ON(MAX)}$ = 9.3 µs (for the LC5555LD, 11.2 µs for LC5556LD), limits lower side operation frequency (see figure 26), at low AC input voltage on or off. Ensure that the actual on-time at the minimum AC input and the maximum load condition does not reach $t_{ON(MAX)}$.

Design Considerations

Output Load (LEDs) The relation between the LED ratings and the output current ratings of the IC should be considered. In buck configuration, the total forward voltage drop, V_{LED}, of the LEDs in series, should be less than the input voltage, V_{AC}, because the LEDs would be turned off if V_{LED} were more than V_{AC}. Normally, a V_{LED} of 9 to 60 V is assumed.

Free-Wheeling Diode (D5) This is a free-wheeling diode for recirculation of the output current. The energy stored during the PWM on-time period is provided to LEDs through this diode during the off-time period. The withstand voltage and recovery time, t_{rr}, should be considered. If a diode with a long recovery time, t_{rr}, is selected, surge current may flow through IC when the internal power MOSFET turns on. As a result, it would cause increased noise, potentially malfunction due to the noise, and decreased efficiency. Thus, it is recommended to select a diode which has a t_{rr} of approximately 30 ns, or a diode with a lower t_{rr}.

Current Detection Resistor (R3) Choose a low equivalent series inductance and high surge tolerant type for the current detection resistor. If a high inductance type is used, it may cause malfunctioning because of the high frequency current running through it.

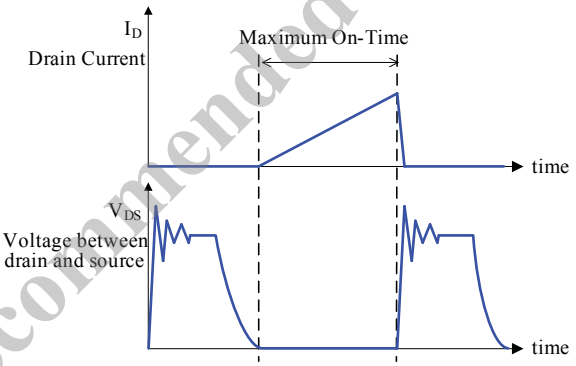


Figure 26. Confirmation of Maximum On-Time

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