650 V, 30 A
3-phase Motor Driver

SAE6530P0DA01

Data Sheet

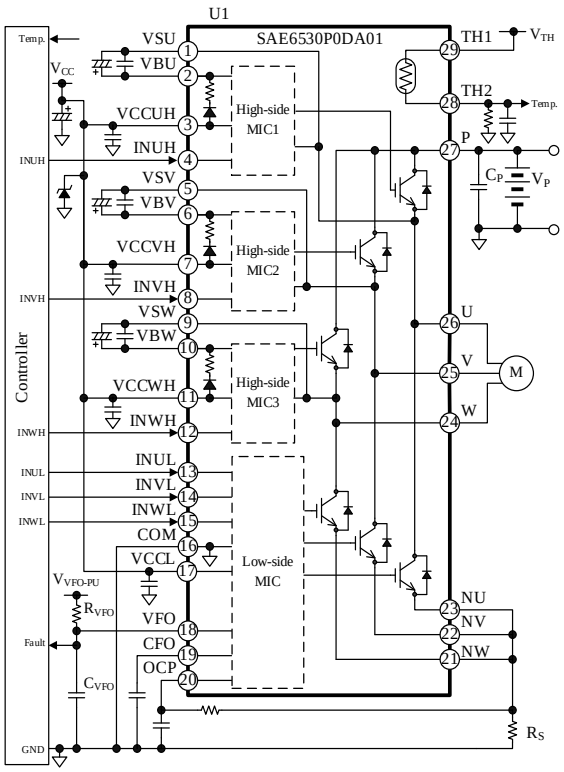
Description

The SAE6530P0DA01 is 3-phase motor driver in which output transistors, pre-driver ICs (MICs), bootstrap diodes with current-limiting resistors, and a temperature-sensing thermistor are highly integrated. The IC is suitable for driving 3-phase motor of an automotive high voltage auxiliary equipment system.

Features

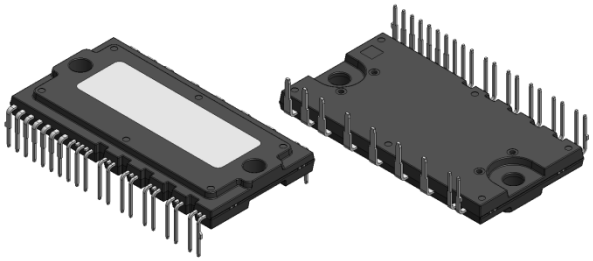
- AEC-Q100 Qualified
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Isolation Voltage: 2500 V (for 1 min)
- Built-in Thermistor
- Built-in Bootstrap Diodes
- CMOS-compatible Input (3.3 V or 5 V)
- Fault Signal Output at Protection Activation
- Shutdown Signal Input
- Adjustable OCP Hold Time
- Protections Include:
  Undervoltage Lockout for Power Supply
  VBx Pin (UVLO_VBx): Auto-restart
  VCCxH Pin (UVLO_VCCxH): Auto-restart
  VCCL Pin (UVLO_VCCL): Auto-restart
  Overcurrent Protection (OCP): Auto-restart

Typical Application



Package

DIP29
Pin Pitch: 2.54 mm
Mold Dimensions: 60 × 31 × 6.3 mm



Not to scale

Specifications

- Output Transistors: IGBT + Freewheeling Diode
- Output Transistor Breakdown Voltage: 650 V
- Rated Current: 30 A

Applications

For driving 3-phase motor of the following high voltage auxiliary equipment system such as hybrid electric vehicles (HEV) and electric vehicles (EV):

- Electric Compressor
- Electric Oil Pump

Contents

1. Introduction

For pin descriptions, this docment employs a notation system that denotes a pin name with the arbitrary letter “x”, depending on context. The U-, V-, and W-phase (3-phases) output pins are represented as the pin numbers U, V, and W, respectively. Thus, “the VBx pin” is used when referring to any or all of the VBU, VBV, and VBW pins. When different pin names are mentioned as a pair (e.g., “the VBx and VSx pins”), they are meant to be the pins in the same phase. Also, “the OUTx pin” is used when referring to any or all of the output pins (U, V, and W).

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

2. Absolute Maximum Ratings

Unless specifically noted, T_A = 25 °C.

Parameter	Symbol	Conditions	Ratings	Unit
Main Power Supply Operation				
Main Supply Voltage	V_P	In operation, P–COM	500	V
		In non-operation, P–COM	650	V
Output				
Collector-to-Emitter Voltage (Surge)	$V_{CE(SURGE)}$	In operation, P–OUTx, OUTx–Nx	550	V
Collector-to-Emitter Voltage	V_{CES}	In non-operation, P–OUTx, OUTx–Nx	650	V
Collector Current[(1)]	I_C	T_C = 25 °C	30	A
Collector Current (Peak)	I_{CP}	T_C = 25 °C, pulse width < 1 ms, duty cycle < 1%	60	A
Power Dissipation	P_C	T_C = 25 °C, 1 element operating (IGBT)	125	W
		T_C = 25 °C, 1 element operating (fleewheeling diodes)	62.5	W
Control				
Nx Pin Voltage	V_{Nx}	Nx–COM	−5 to 5	V
VCCxH Pin Voltage	V_{VCCxH}	VCCxH–COM	−0.5 to 20	V
VCCL Pin Voltage	V_{VCCL}	VCCL–COM	−0.5 to 20	V
VBx-VSx Voltage	$V_{VBx-VSx}$	VBx–VSx	−0.5 to 20	V
INxH Pin Voltage	V_{INxH}	INxH–COM	−0.5 to 5.5	V
INxL Pin Voltage	V_{INxL}	INxL–COM	−0.5 to 5.5	V
VFO Pin Voltage	V_{VFO}	VFO–COM	−0.5 to 5.5	V
VFO Pin Sink Current	I_{VFO}		1	mA
OCP Pin Voltage	V_{OCP}	OCP–COM	−0.5 to 5.5	V
Change Rate of VCC Supply Voltage Time	$\Delta V_{VCC}/\Delta t$		−1 to 1	V/µs
Bootstrap Circuit				
Bootstrap Diode Reverse Voltage	V_{R-BS}		650	V

[(1)] Should be derated depending on an actual case temperature. See Section 15.4.

Parameter	Symbol	Conditions	Ratings	Unit
Thermistor				
Operating Thermistor Temperature	T_{TH}		−40 to 150	°C
Thermistor Allowable Current	$I_{TH\text{-}MAX}$		10	mA
Thermistor Allowable Power	$P_{TH\text{-}MAX}$		300	mW
Common				
Junction Temperature[(2)]	T_J		−40 to 150	°C
Operating Case Temperature[(3)]	T_C	For measurement point, see Figure 2-1.	−40 to 125	°C
Storage Temperature	T_{STG}		−40 to 150	°C
Isolation Voltage[(4)]	$V_{ISO(RMS)}$	Between surface of heatsink side and each pin; AC, 60 Hz, 1 min	2500	V

(2) Refers to the junction temperature of each chip built in the IC, including the monolithic IC (MIC), IGBTs, and freewheeling diodes.
(3) Refers to a case temperature measured during IC operation.
(4) Refers to voltage conditions to be applied between the case and all pins. All pins have to be shorted.

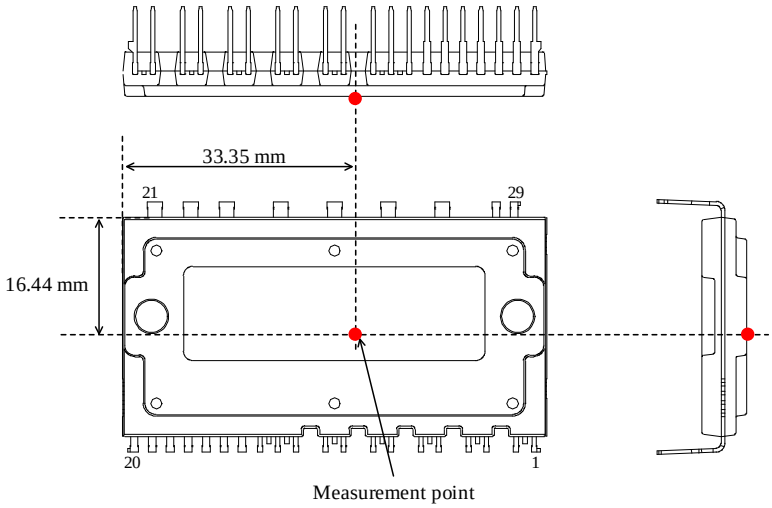


Figure 2-1. Operating Case Temperature Measurement Point

3. Recommended Operating Conditions

Unless specifically noted, T_C = −40 °C to 125 °C, V_P = 300 V, V_{VCCxH} = V_{VCCL} = 15 V, R_{VFO} = 10 kΩ, C_{VFO} = 0 µF, and V_{VFO-PU} = 5 V.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Main Supply Voltage	V_P	P–COM		150	300	450	V
Phase Current (Effective Value)[1]	$I_{C(RMS)}$	Sine wave, modulation index = 1, power factor = 0.8, −40°C ≤ T_C ≤ 100°C, −40°C ≤ T_J ≤ 150°C	f_{PWM} = 5 kHz	—	—	21	A
			f_{PWM} = 10 kHz	—	—	17	
			f_{PWM} = 15 kHz	—	—	14	
			f_{PWM} = 20 kHz	—	—	11	
VCCxH Pin Voltage	V_{VCCxH}	VCCxH–COM		13.5	15.0	16.5	V
VCCL Pin Voltage	V_{VCCL}	VCCL–COM		13.5	15.0	16.5	V
VBx-VSx Voltage	$V_{VBx-VSx}$	VBx–VSx		13.5	15.0	16.5	V
Dead Time of Input Signal	t_{DEAD}	INxH, INxL		2.0	2.5	—	µs
PWM Control Frequency	f_{PWM}			5	10	20	kHz
INxH Pin Input Pulse Width (On)	$t_{INXH(ON)}$			0.5	—	—	µs
INxH Pin Input Pulse Width (Off)	$t_{INXH(OFF)}$			0.5	—	—	µs
INxL Pin Input Pulse Width (On)	$t_{INXL(ON)}$			0.5	—	—	µs
INxL Pin Input Pulse Width (Off)	$t_{INXL(OFF)}$			0.5	—	—	µs
P Pin Capacitor	C_P			22	47	—	µF
VCCxH/VCCL Pin Capacitor 1	C_{VCC1}			22	47	—	µF
VCCxH/VCCL Pin Capacitor 2	C_{VCC2}	Ceramic capacitor		0.47	1.0	2.2	µF
Bootstrap Capacitor 1	C_{BS1}			4.7	10	22	µF
Bootstrap Capacitor 2	C_{BS2}	Ceramic capacitor		0.47	1.0	2.2	µF
External VCC Supply Output Current	I_{VCC}	f_{PWM} = 5 kHz		15	—	—	mA
		f_{PWM} = 10 kHz		18	—	—	
		f_{PWM} = 15 kHz		21	—	—	
		f_{PWM} = 20 kHz		24	—	—	
VCCxH/VCCL Pin Zener Diode Breakdown Voltage	V_{Z-DVCC}	I_Z = 1 mA		16.5	18.2	20.0	V
VFO Pin Pull-up Resistor	R_{VFO}			5.5	10	33	kΩ
VFO Pin Pull-up Voltage	V_{VFO_PU}			3.0	5.0	5.5	V
VFO Pin Capacitor	C_{VFO}			—	1000	3300	pF
CFO Pin Capacitor	C_{CFO}			0.01	0.1	1	µF
Shunt Resistor	R_S	OCP operating current: 30 A to 60 A		9.0	12.2	15.3	mΩ
OCP RC Filter Time Constant	t_{RFCF}	$t_{RFCF} = R_F \times C_F$		1.0	1.5	2.0	µs
Thermistor Operating Current	I_{TH}			—	—	0.3	mA

[1] The maximum value of the phase current varies depending on application conditions.

4. Electrical Characteristics

Unless specifically noted, T_C = −40 °C to 125 °C, V_P = 300 V, V_{VCCxH} = V_{VCCL} = 15 V, R_{VFO} = 10 kΩ, C_{VFO} = 0 µF, and V_{VFO-PU} = 5 V. The shipping test is performed at T_A = 25 °C and 125 °C for the electrical characteristics shown below (except for the parameters guaranteed by design).

4.1. Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
VCCxH Pin Operating Voltage	V_{VCCxH_H}		11.0	11.6	12.5	V	UVLO recovery voltage
VCCxH Pin Operating Stop Voltage	V_{VCCxH_L}		10.5	11.1	12.0	V	UVLO detection voltage
VCCxH Pin Hysteresis	V_{VCCxH_HYS}		—	0.5	—	V	
VCCL Pin Operating Voltage	V_{VCCL_H}		12.0	12.6	13.5	V	UVLO recovery voltage
VCCL Pin Operating Stop Voltage	V_{VCCL_L}		11.5	12.1	13.0	V	UVLO detection voltage
VCCL Pin Hysteresis	V_{VCCL_HYS}		—	0.5	—	V	
VBx−VSx Operating Voltage	$V_{VBx-VSx\_H}$		11.0	11.6	12.5	V	UVLO recovery voltage
VBx−VSx Operating Stop Voltage	$V_{VBx-VSx\_L}$		10.5	11.1	12.0	V	UVLO detection voltage
VBx−VSx Hysteresis	$V_{VBx-VSx\_HYS}$		—	0.5	—	V	
VCCxH Pin Input Current	I_{VCCXH}	V_{INxH} = 0 V, each pin	—	1.1	2.0	mA	
		V_{INxH} = 5 V, each pin	—	1.1	2.0		
VCCL Pin Input Current	I_{VCCL}	V_{INxL} = 0 V	—	2.2	3.0	mA	
		V_{INxL} = 5 V	—	2.8	4.0		
VBx−VSx Input Current	$I_{VBx-VSx}$	$V_{VBx-VSx}$ = 15 V, V_{INxH} = 0 V, in 1-phase operation	—	0.09	0.30	mA	
		$V_{VBx-VSx}$ = 15 V, V_{INxH} = 5 V, in 1-phase operation	—	0.11	0.30		
Input Signal							
INxH Pin High-level Input Threshold Voltage	V_{INxH_H}		—	2.0	2.5	V	
INxH Pin Low-level Input Threshold Voltage	V_{INxH_L}		1.0	1.5	—	V	
INxH Pin Hysteresis	V_{INxH_HYS}		—	0.5	—	V	
INxL High-level Input Threshold Voltage	V_{INxL_H}		—	2.0	2.5	V	
INxL Pin Low-level Input Threshold Voltage	V_{INxL_L}		1.0	1.5	—	V	
INxL Pin Hysteresis	V_{INxL_HYS}		—	0.5	—	V	
INxH Pin Input Current	I_{INxH}	V_{INxH} = 5 V, each pin	—	0.23	0.50	mA	
INxL Pin Input Current	I_{INxL}	V_{INxL} = 5 V, each pin	—	0.23	0.50	mA	
INxH Pin Minimum Response Pulse Width (On)(1)	$t_{INXH\_MIN(ON)}$		—	0.34	0.50	µs	

(1) Guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
INxH Pin Minimum Response Pulse Width (Off) (2)	$t_{INXH\_MIN(OFF)}$		—	0.36	0.50	µs	
INxL Pin Minimum Response Pulse Width (On) (2)	$t_{INXL\_MIN(ON)}$		—	0.26	0.50	µs	
INxL Pin Minimum Response Pulse Width (Off) (2)	$t_{INXL\_MIN(OFF)}$		—	0.27	0.50	µs	
Fault Signal Output and Shutdown Signal Input							
VFO Pin Shutdown Release Voltage	V_{VFO_H}		—	2.0	2.5	V	
VFO Pin Shutdown Threshold Voltage	V_{VFO_L}		1.0	1.5	—	V	
VFO Pin Shutdown Hysteresis	V_{VFO_HYS}		—	0.5	—	V	
VFO Pin Output Voltage in Normal Operation	V_{VFO_H}	V_{VFO_PU} = 5 V, R_{VFO} = 10 kΩ, V_{OCP} = 0 V	4.8	5.0	—	V	
VFO Pin Error Signal Output Voltage	V_{VFO_L}	V_{VFO_PU} = 5 V, R_{VFO} = 10 kΩ, V_{OCP} = 1 V	—	0.05	0.50	V	
VFO Pin OCP Hold Time (2) (3)	t_{VFO}	C_{CFO} = 0 µF	0.022	0.032	0.044	ms	
		C_{CFO} = 0.001 µF	0.22	0.32	0.44	ms	
		C_{CFO} = 0.01 µF	2.2	3.2	4.2	ms	
		C_{CFO} = 0.1 µF	22	32	42	ms	
		C_{CFO} = 1 µF	220	320	420	ms	
Protection							
OCP Pin Overcurrent Detection Voltage	V_{OCP_H}		0.46	0.50	0.54	V	
OCP Pin Overcurrent Release Voltage	V_{OCP_L}		0.32	0.38	0.44	V	
OCP Pin Overcurrent Hysteresis	V_{OCP_HYS}		—	0.12	—	V	
OCP Pin Detection Delay Time	t_{OCP_DELAY}	(4)	—	2.7	5.0	µs	
OCP Pin Input Current	I_{OCP}	V_{OCP} = 0.5 V	—	0	—	mA	

(2) Guaranteed by design.
(3) For a relation between t_{VFO} and C_{CFO}, see Figure 13-3. The shipping test is performed with the condition at C_{CFO} = 0.01 µF only.
(4) For the measurement circuit for the OCP Pin Detection Delay Time, see Figure 4-1 (all the pins that are not represented in the figure are open). Figure 4-2 provides the definition of the OCP Pin Detection Delay Time.

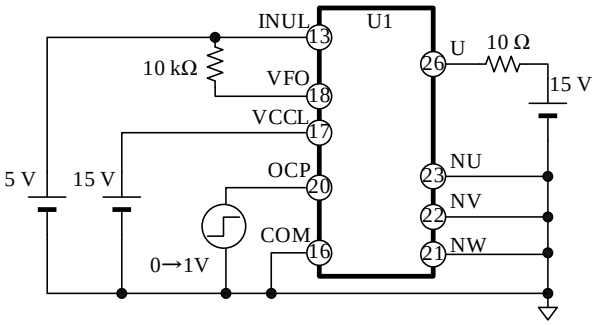


Figure 4-1. Measurement Circuit for OCP Pin Detection Delay Time

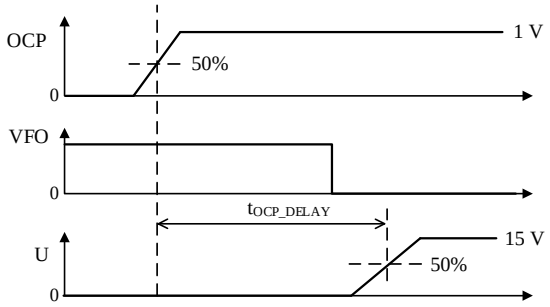


Figure 4-2. OCP Pin Detection Delay Time Definition

4.2. Transistor Characteristics

Figure 4-3 provides the definitions of switching characteristics described in this and the following sections.

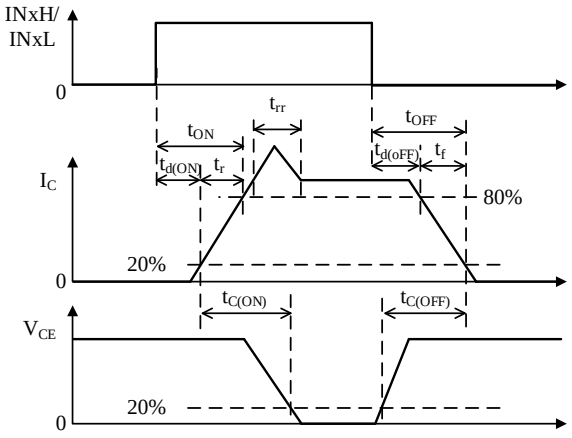


Figure 4-3. Switching Characteristics Definitions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 650 V, T_J = 25 °C	—	—	0.1	mA
		V_{CE} = 650 V, T_J = 125 °C	—	—	0.5	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 A, T_J = 25 °C	—	1.6	2.1	V
		I_C = 30 A, T_J = 125 °C	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 30 A, T_J = 25 °C	—	1.4	1.9	V
High-side Switching						
Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, I_C = 30 A, V_{IN} = 0 ↔ 5 V, T_J = 25 °C, inductive load	—	0.17	—	µs
Turn-on Time*	t_{ON}		—	1.28	—	µs
Turn-on Delay Time*	$t_{d(ON)}$		—	1.18	—	µs
Rise Time*	t_r		—	0.10	—	µs
Turn-on Switching Time*	$t_{C(ON)}$		—	0.38	—	µs
Turn-off Time*	t_{OFF}		—	1.24	—	µs
Turn-off Delay Time*	$t_{d(OFF)}$		—	1.17	—	µs
Fall Time*	t_f		—	0.07	—	µs
Turn-off Switching Time*	$t_{C(OFF)}$		—	0.17	—	µs
Low-side Switching						
Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, I_C = 30 A, V_{IN} = 0 ↔ 5 V, T_J = 25 °C, inductive load	—	0.14	—	µs
Turn-on Time*	t_{ON}		—	1.03	—	µs
Turn-on Delay Time*	$t_{d(ON)}$		—	0.95	—	µs
Rise Time*	t_r		—	0.09	—	µs
Turn-on Switching Time*	$t_{C(ON)}$		—	0.24	—	µs
Turn-off Time*	t_{OFF}		—	1.03	—	µs
Turn-off Delay Time*	$t_{d(OFF)}$		—	0.97	—	µs
Fall Time*	t_f		—	0.07	—	µs
Turn-off Switching Time*	$t_{C(OFF)}$		—	0.12		µs

* Guaranteed by design.

4.3. Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Forward Voltage	V_{F_BS}	I_{F_BS} = 0.1 A	2.1	3.1	4.1	V	Including voltage drop of series resistor
Bootstrap Diode Series Resistor*	R_{S_BS}		15	24	33	Ω	

* Guaranteed by design.

4.4. Thermistor Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Thermistor Resistance*	R_{25}	T_A = 25 °C	—	30	—	kΩ	Including voltage drop of series resistor

* Guaranteed by design.

4.5. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance[1] [2]	$R_{(J-C)Q}$[3]	1 element operating (IGBT)	—	—	1.0	°C/W	
	$R_{(J-C)F}$[4]	1 element operating (freewheeling diode)	—	—	2.0	°C/W	

[1] Guaranteed by design.
[2] Refers to a case temperature at the measurement point described in Figure 4-4, below.
[3] Refers to steady-state thermal resistance between the junction of the built-in IGBTs and the case. For transient thermal characteristics, see Section 15.1.
[4] Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

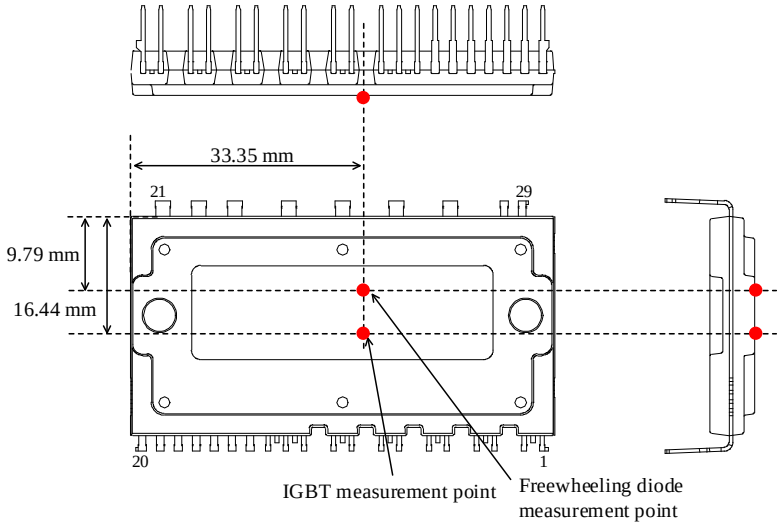


Figure 4-4. Case Temperature Measurement Point

5. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Heatsink Mounting Screw Torque[1]	[2]	0.80	1.00	1.20	N·m
		8.2	10.2	12.2	kgf·cm
Flatness of Heatsink Attachment Area[1]	See Figure 5-1	−50	—	100	μm
Package Weight[1]		—	29	—	g

[1] Guaranteed by design.
[2] When mounting a heatsink, it is recommended to use a metric screw of M4 and a plain washer, which is 9 mm (φ) of outside diameter, together at each end of it. For more details about screw tightening, see Section 14.2.

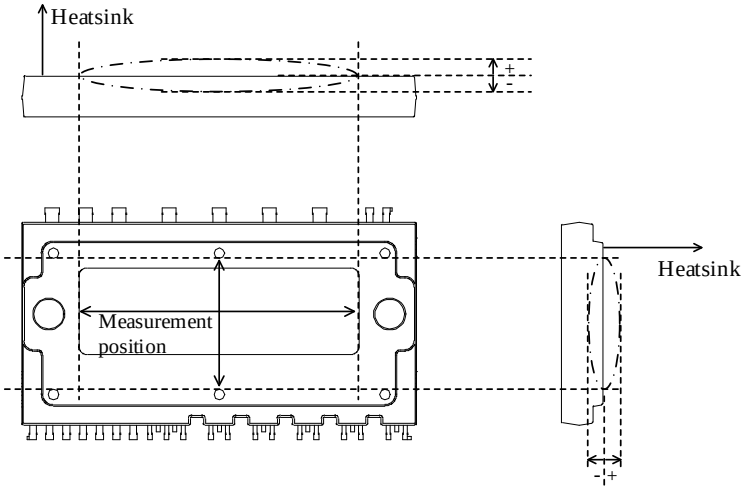


Figure 5-1. Flatness Measurement Position

6. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Clearance[1]	Between heatsink* and leads. See Figure 6-1.	2.9	3.1	—	mm
Creepage [1] [2]		5.0	5.5	—	mm

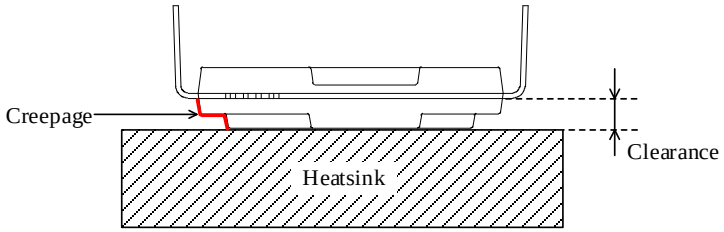


Figure 6-1. Insulation Distance Definitions

[1] Guaranteed by design.
[2] Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

7. Truth Table

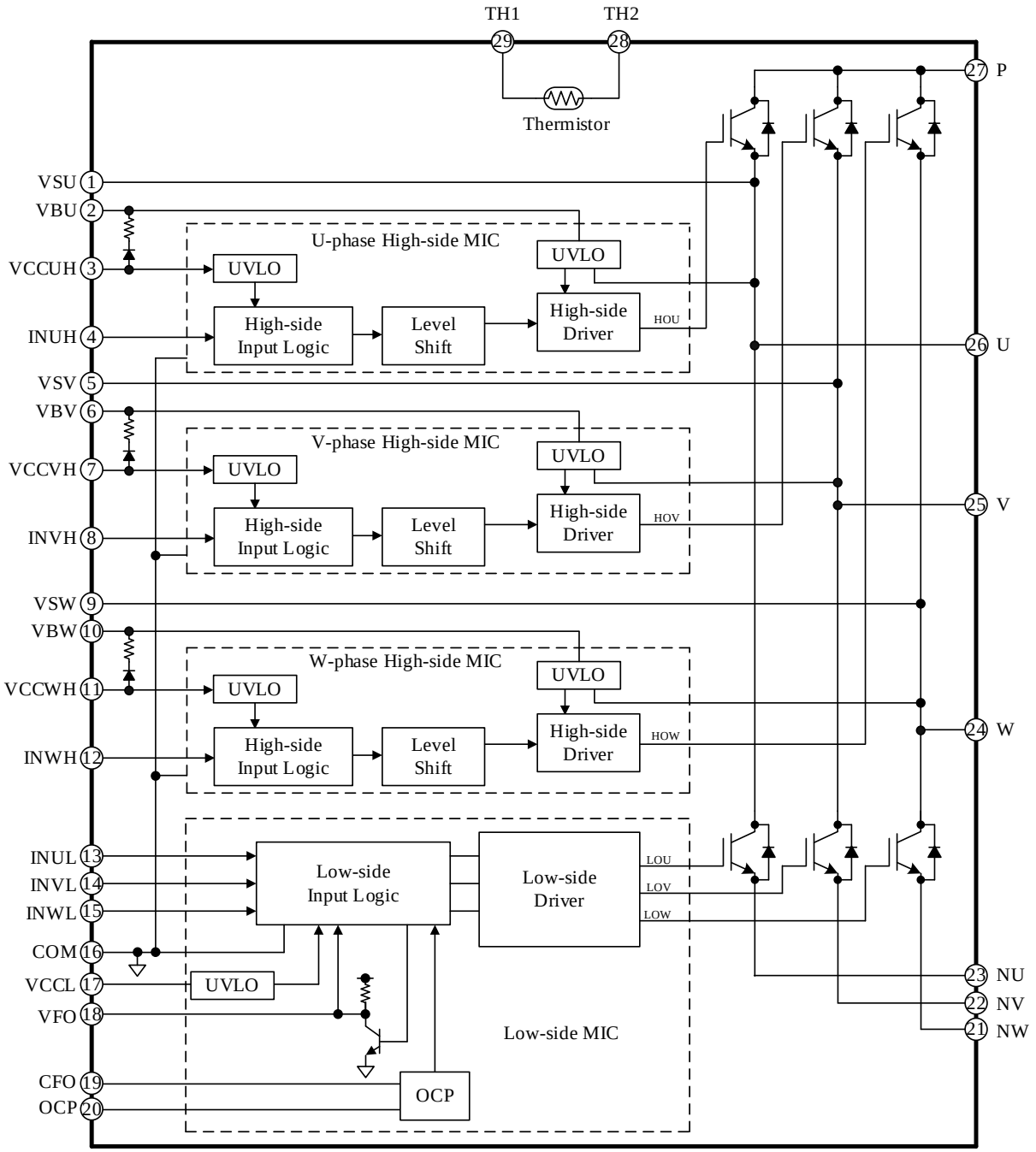
Table 7-1 is a truth table that provides the logic level definitions of operation modes.

In the case where the INxH and INxL in each phase are high at the same time, both the high- and low-side IGBTs become on (simultaneous on-state). Therefore, INxH and INxL signals, the input signals for the INxH and INxL pins, require dead time setting so that such a simultaneous on-state event can be avoided.

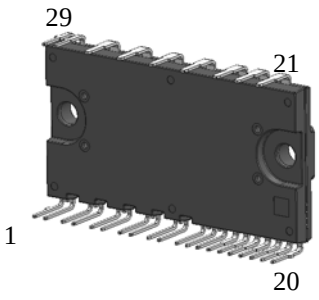
Table 7-1. Truth Table for Operation Modes

Mode	INxH	INxL	High-side IGBT	Low-side IGBT	VFO Pin Output
Normal Operation	L	L	OFF	OFF	H
	H	L	ON	OFF	
	L	H	OFF	ON	
	H	H	ON	ON	
External Shutdown Signal Input VFO = L	L	L	OFF	OFF	—
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	
VBx Pin Undervoltage Lockout Operation (UVLO_VBx)	L	L	OFF	OFF	H
	H	L	OFF	OFF	
	L	H	OFF	ON	
	H	H	OFF	ON	
VCCxH Pin Undervoltage Lockout Operation (UVLO_VCCxH)	L	L	OFF	OFF	H
	H	L	OFF	OFF	
	L	H	OFF	ON	
	H	H	OFF	ON	
VCCL Pin Undervoltage Lockout Operation (UVLO_VCCL)	L	L	OFF	OFF	L
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	
Overcurrent Protection (OCP)	L	L	OFF	OFF	L
	H	L	ON	OFF	
	L	H	OFF	OFF	
	H	H	ON	OFF	

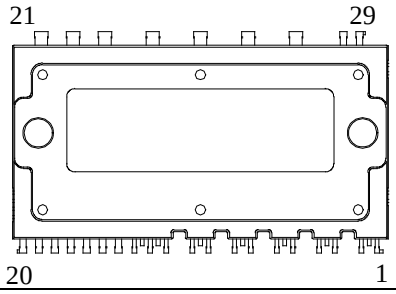
8. Block Diagram



9. Pin Configuration Definitions



Heatsink side



Pin Number	Pin Name	Description
1	VSU	U-phase high-side floating supply ground
2	VBU	U-phase high-side floating supply voltage input
3	VCCUH	U-phase high-side logic supply voltage input
4	INUH	Logic input for U-phase high-side gate driver
5	VSV	V-phase high-side floating supply ground
6	VBV	V-phase high-side floating supply voltage input
7	VCCVH	V-phase high-side logic supply voltage input
8	INVH	Logic input for V-phase high-side gate driver
9	VSW	W-phase high-side floating supply ground
10	VBW	W-phase high-side floating supply voltage input
11	VCCWH	W-phase high-side logic supply voltage input
12	INWH	Logic input for W-phase high-side gate driver
13	INUL	Logic input for U-phase low-side gate driver
14	INVL	Logic input for V-phase low-side gate driver
15	INWL	Logic input for W-phase low-side gate driver
16	COM	Logic ground
17	VCCL	Low-side logic supply voltage input
18	VFO	Fault signal output and shutdown signal input
19	CFO	Capacitor connection for overcurrent protection hold time setting
20	OCP	Overcurrent protection signal input
21	NW	W-phase low-side IGBT emitter
22	NV	V-phase low-side IGBT emitter
23	NU	U-phase low-side IGBT emitter
24	W	W-phase output
25	V	V-phase output
26	U	U-phase output
27	P	Positive DC bus supply voltage
28	TH2	Thermistor output 2
29	TH1	Thermistor output 1

10. Typical Application

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

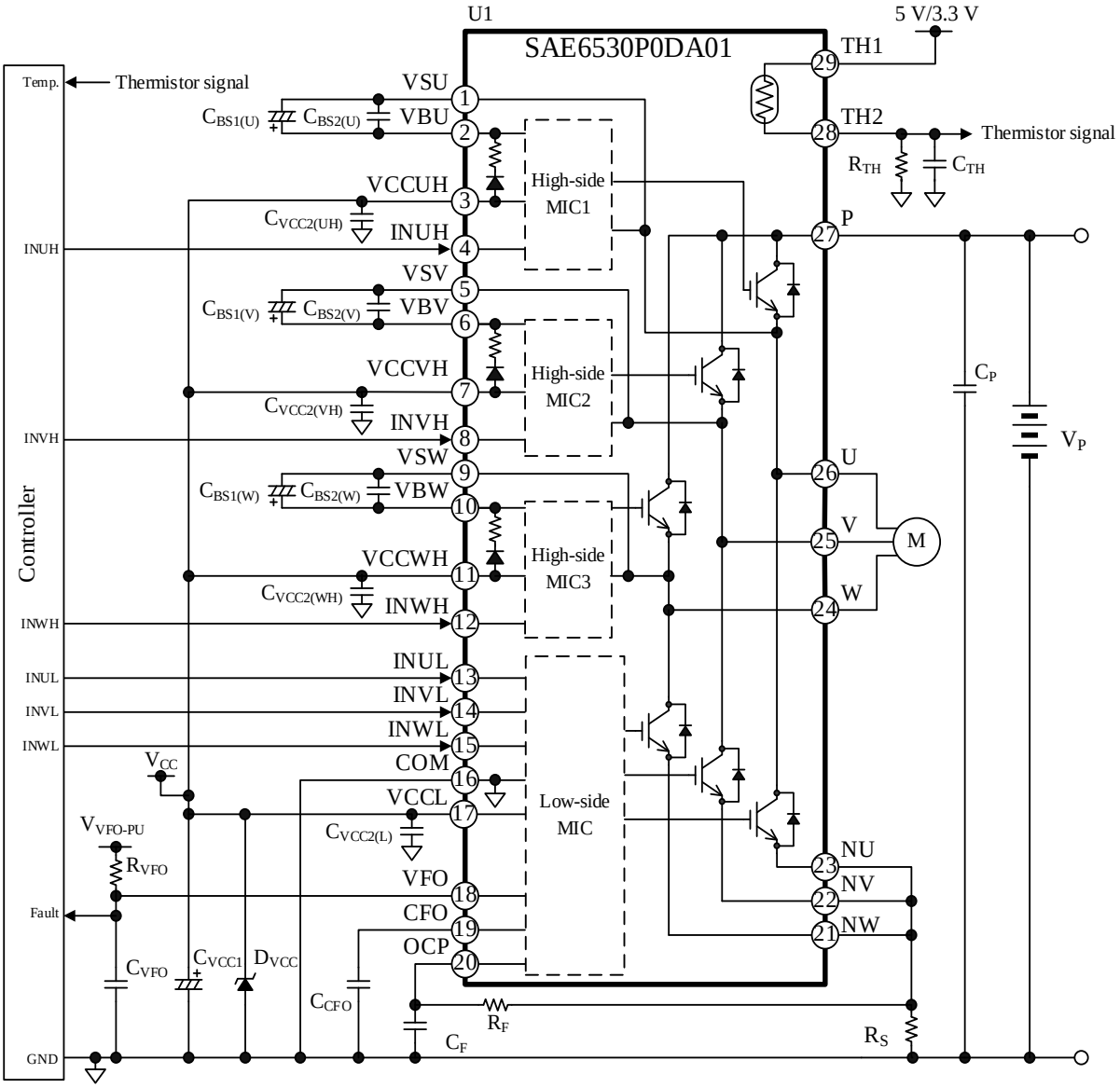
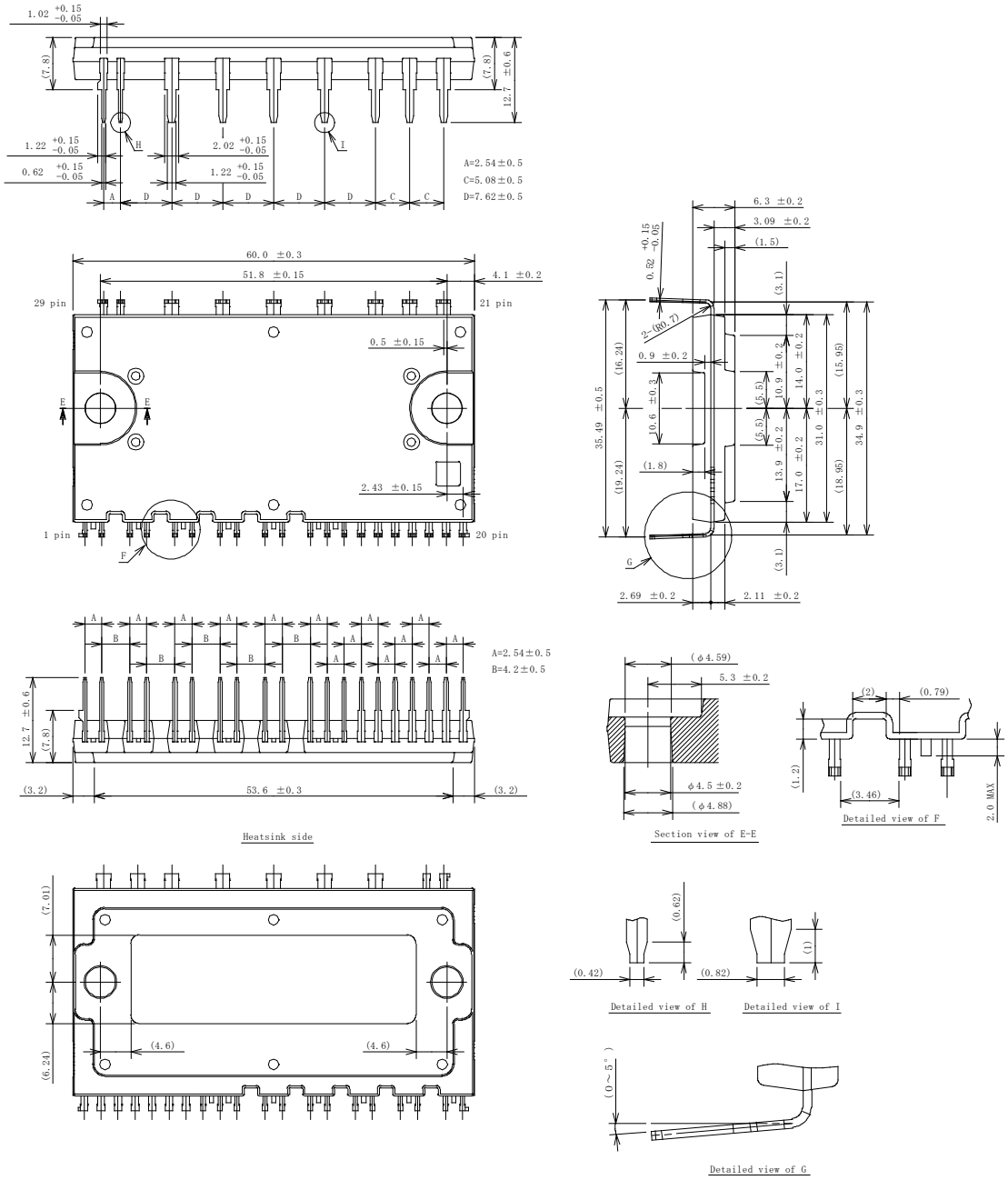


Figure10-1. Typical Application

11. Physical Dimensions

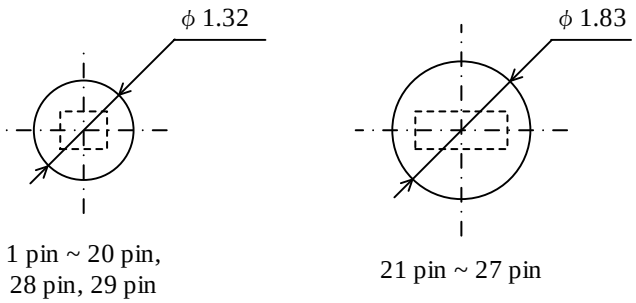
11.1. DIP29



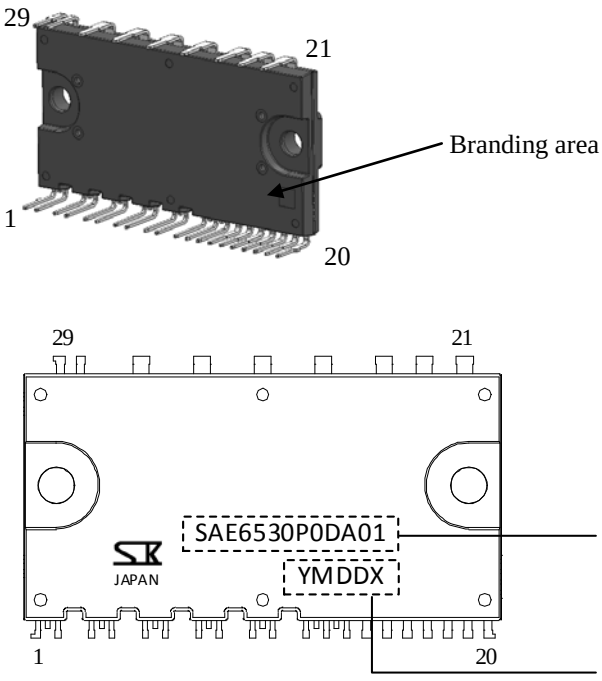
NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)

11.2. Reference PCB Hole Sizes



12. Marking Diagram



Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

13. Functional Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Also, the symbols of the electrical characteristics in Section 4 and the electrical symbol names in Section 10 are used.

For the notation system such as pin name used in this section, see Section 1.

13.1. Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences.

To turn on the IC properly, do not apply any voltage to the INxH and INxL pins until the VCCL pin voltage has reached the maximum value ($V_{VCCL\_H} \geq 13.5$ V). It is required to charge bootstrap capacitors, C_{BS1} and C_{BS2}, up to full capacity at startup (see Section 13.2.3).

To turn off the IC, set the input signals to the INxH and INxL pins to logic low (or "L"), and then decrease the VCCL pin voltage.

13.2. Pin Descriptions

13.2.1. P

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin. Voltages to be applied between the P and COM pins should be regulated within the recommended operational range of the main supply voltage, 150 V to 450 V.

To suppress the surge voltage, a capacitor of 22 µF or more (C_P), should be connected between the P and COM pins. When connecting C_P, place it as near as possible to the IC with a minimum length of traces to the P and Nx pins. For more details about PCB pattern layout, see Section 14.1.

13.2.2. U, V, and W

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The U, V, and W pins are internally connected to the VSU, VSV, and VSW pins, respectively.

13.2.3. NU, NV, and NW

These are the emitter pins of the low-side IGBTs. For current detection, the NU, NV, and NW pins should be connected externally on a PCB via a shunt resistor, R_S.

When connecting R_S, place it as near as possible to the IC with a minimum length of traces to the Nx pin and C_P. For more details about PCB pattern layout, see Section 14.1.

13.2.4. VBU, VBV, and VBW

These are the inputs of the high-side floating power supplies for the individual phases. Voltages to be applied between the VBx and VSx pins (hereafter "VBx–VSx") of each phase should be regulated within the recommended operational range, 13.5 V to 16.5 V.

The capacitors for bootstrap circuit, C_{BS1} and C_{BS2}, are connected between VBx–VSx of each phase, respectively. The value of C_{BS1} should be 4.7 µF to 22 µF. The value of C_{BS2} should be 0.47 µF to 2.2 µF. To protect the VBx pin against such a noise effect, add the bootstrap capacitors, C_{BS1} and C_{BS2}, in each phase. C_{BS1} and C_{BS2} must be placed near the IC, and be connected between VBx–VSx with a minimal length of traces.

For proper startup, turn on the low-side IGBTs first, and then fully charge the bootstrap capacitors, C_{BS1} and C_{BS2}. As Figure 13-1 shows, a bootstrap diode, D_{BOOTx}, and an inrush current-limiting resistor, R_{BOOTx}, are internally placed in series between the VCCxH and VBx pins.

Even while the high-side IGBT is off, voltages of C_{BS1} and C_{BS2} keep decreasing due to power dissipation in the IC. When the VBx–VSx voltage decreases to $V_{VBx-VSx\_L}$= 11.1 V or less, the VBx pin undervoltage lockout is activated (see Section 13.3.3.1). Therefore, actual board checking should be done thoroughly to validate that VBx–VSx voltage maintains over 12.0 V (VBx–VSx > $V_{VBx-VSx\_L}$) during a low-frequency operation such as a startup period.

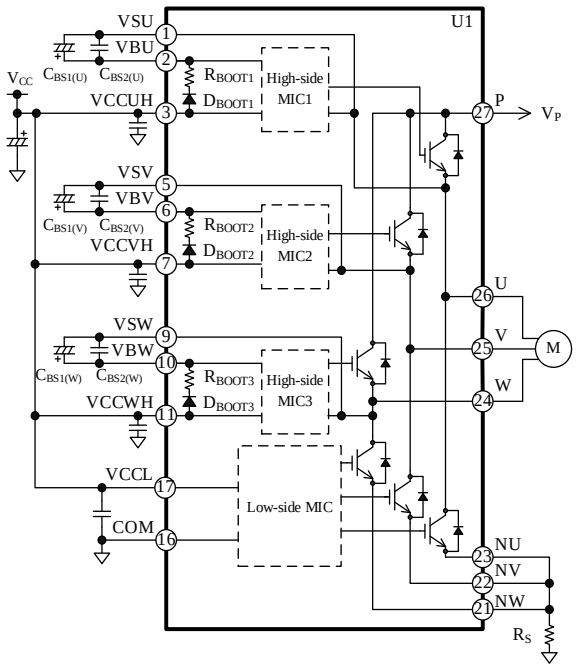


Figure 13-1. Bootstrap Circuit

13.2.5. VSU, VSV, and VSW

These pins are the grounds of the high-side floating power supplies for each phase, and are connected to the negative nodes of bootstrap capacitors, C_{BS1} and C_{BS2}. The VSU, VSV, and VSW pins are internally connected to the U, V, and W pins, respectively.

13.2.6. VCCUH, VCCVH, VCCWH, and VCCL

The VCCUH, VCCVH, and VCCWH pins are the high-side logic supply voltage input pins of each phase. The VCCL pin is the low-side logic supply voltage input pin. The VCCxH and VCCL pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put the capacitors, C_{VCC1} and C_{VCC2}, near these pins. C_{VCC1} and C_{VCC2} should be set ≥22 µF and 0.47 µF to 2.2 µF, respectively. To prevent damage caused by surge voltages, put a 16.5 V to 20 V Zener diode, D_{VCC}, between the VCCL and COM pins.

Voltages to be applied across the VCCxH-COM, and the VCCL-COM pins should be regulated within these recommended operational ranges, 13.5 V to 16.5 V.

13.2.7. COM

This is the logic ground pin for the built-in pre-driver IC. For proper control, the control parts used in the IC must be connected to the logic ground pin. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, extreme care should be taken when wiring so that currents from the power ground do not affect the COM pin. For more details about PCB pattern layout, see Section 14.1.

13.2.8. INUH, INVH, and INWH; INUL, INVL, and INWL

These are the input pins of the internal motor drivers for each phase. The INxH pin acts as a high-side controller; the INxL pin acts as a low-side controller. Figure 13-2 shows an internal circuit diagram of the INxH or INxL pin. This is a CMOS Schmitt trigger circuit with a built-in 25 kΩ pull-down resistor, and its input logic is active high. Input signals applied across the INxH-COM and the INxL-COM pins in each phase should be set within the ranges provided in Table 13-1, below. Note that dead time setting must be done for INxH and INxL signals because the IC does not have a dead time generator.

Table 13-1. Input Signals for INxH and INxL Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 µs	≥0.5 µs
PWM Carrier Frequency	5 kHz ≤ f_{PWM} ≤ 20 kHz	
Dead Time	≥2.0 µs	

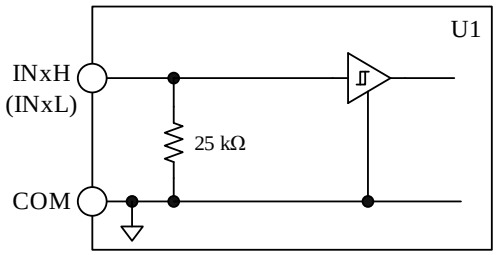


Figure 13-2. Internal Circuit Diagram of INxH or INxL Pin

13.2.9. OCP

This pin serves as the input of the overcurrent protection (OCP) for monitoring the currents going through the output IGBTs. Section 13.3.4 provides further information about the OCP circuit configuration and its mechanism.

13.2.10. CFO

A capacitor, C_{CFO}, is connected to the CFO pin. The VFO pin OCP hold time, t_{VFO}, in OCP operation is determined by C_{CFO} which is set in range of 0.01 µF to 1 µF. Figure 13-3 shows the relationship between t_{VFO} and C_{CFO}.

For more details on the OCP, see Section 13.3.4.

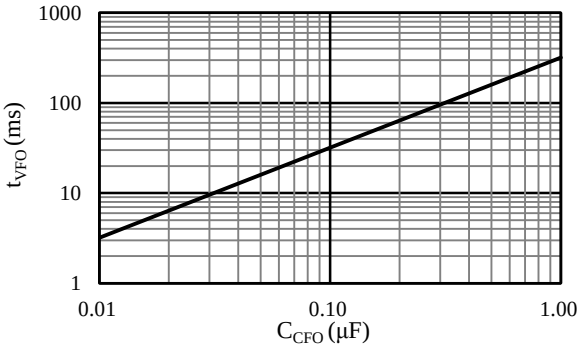


Figure 13-3. C_{CFO} – t_{VFO} Characteristics

13.2.11. VFO

This pin operates as the fault signal output and the shutdown signal input. Sections 13.3.1 and 13.3.2 explain the two functions in detail, respectively.

Figure 13-4 illustrates an internal circuit diagram of the VFO pin and its peripheral circuit. Because of its open-collector nature, the VFO pin should be tied by a pull-up resistor, R_{VFO}, to the external power supply. R_{VFO} should range from 5.5 kΩ to 33 kΩ. The external power supply voltage (i.e., the VFO Pin Pull-up Voltage, V_{VFO_PU}) should range from 3.0 V to 5.5 V.

To suppress noise, add a filter capacitor, C_{VFO}, near the IC with minimizing a trace length between the VFO and COM pins. The value of C_{VFO} must be set to ≤3300 pF.

To avoid the repetition of OCP activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_{VFO}, which occurs after the internal transistor (Q_{VFO}) turn-on (for more details, see Section 13.3.4).

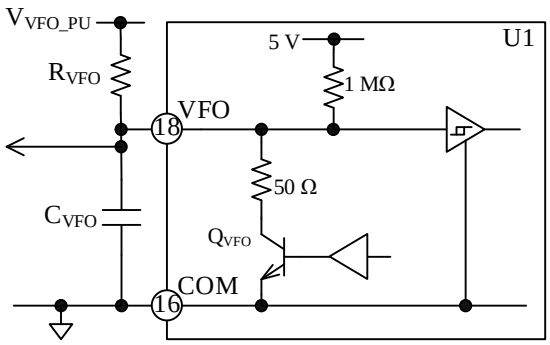


Figure 13-4. Internal Circuit Diagram of VFO Pin and Its Peripheral Circuit

13.2.12. TH1 and TH2

The IC incorporates a thermistor which monitors the IC temperature. Both ends of the internal thermistor are connected to the TH1 and TH2 pins, respectively. Figure 13-5 shows a circuit example when the output voltage has a positive temperature characteristic. Figure 13-6 shows a circuit example when the output voltage has a negative temperature characteristic. In addition, connect a noise filter capacitor, C_{TH}, to the THx pin which is connected to the external microcontroller.

The thermistor should be connected to the external power supply of 3.0 V to 5.5 V. R_{TH} must be set so that the thermistor current ≤0.3 mA. C_{TH} is the noise reduction capacitor, and should be set ≥0.1 μF. Then, place C_{TH} as close as possible to the IC, and connect it to the THx pin connected to the microcontroller and the COM pin with minimizing respective trace lengths.

Figure 13-7 shows a typical thermistor resistance vs. temperature curve. For the detailed data such as variation in thermistor resistance, see Table 15-1.

The IC does not have any protection against overtemperature; therefore, the motor must be externally controlled when a temperature rise occurs, or be controlled with such protective measures. Moreover, note that the THx pin output does not provide the temperature followability, especially when a rapid temperature rise in the output IGBTs occurs during motor lock and short circuit conditions.

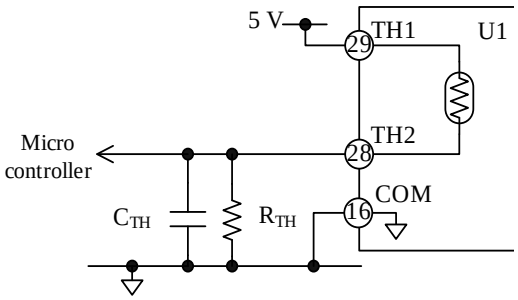


Figure 13-5. When Output Voltage Has Positive Temperature Characteristic

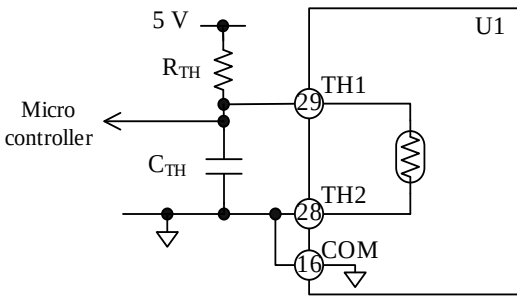


Figure 13-6. When Output Voltage Has Negative Temperature Characteristic

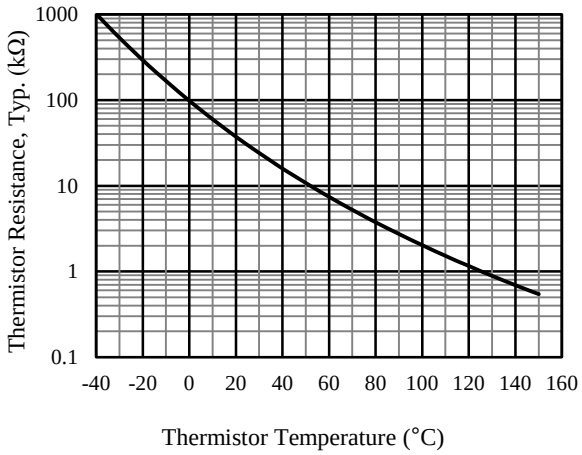


Figure 13-7. Typical Thermistor Resistance vs. Temperature Curve

13.3. Protections

This section describes the various protection circuits provided in the IC. The protection circuits include the undervoltage lockout for power supplies (UVLO) of the VBx, VCCxH, and VCCL pins, and the overcurrent protection (OCP).

In case the UVLO_VCCL or the OCP is activated, the IC outputs a fault signal. In addition, an external shutdown signal can input to the IC.

In the following functional descriptions, "HOx" denotes a gate input signal on the high-side IGBT, whereas "LOx" denotes a gate input signal on the low-side IGBT (see also the diagram in Section 8). "VBx−VSx" represents between VBx and VSx pins.

13.3.1. Fault Signal Output

In case the VCCL pin undervoltage lockout (UVLO_VCCL) or the overcurrent protection (OCP) is actuated, an internal transistor (Q_{VFO}) connected to the VFO pin turns on, then the VFO pin becomes logic low (≤0.50 V), i.e., error signal output. While the VFO pin is in the low state, all the low-side IGBTs turn off.

In normal operation, the VFO pin outputs a high signal of 5 V. The VFO pin OCP hold time, t_{VFO}, at OCP activation is determined by the value of the CFO pin capacitor (C_{CFO}, see Section 13.2.10).

To avoid the repetition of OCP activations, the external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to shut off any input signals to the IC within the predetermined t_{VFO} (for more details, see Section 13.3.4).

13.3.2. Shutdown Signal Input

The VFO pin also acts as the input pin of shutdown signals. Figure 13-8 shows an operational waveforms of shutdown signal input. Figure 13-9 illustrates a schematic diagram of the VFO pin and its peripheral circuit. When the VFO pin becomes logic low, all the low-side IGBTs turn off. When the VFO pin becomes logic low, the low-side IGBTs operate according to the INxL pin input signal. In addition, the VFO pin has an internal filter circuit of about 2.5 µs, in order to prevent noise-induced malfunctions. The voltages and pulse widths of the shutdown signals to be input to the VFO pin are listed in Table 13-2.

Table 13-2. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	3.0 V < V_{VFO} < 5.5 V	0 V < V_{VFO} < 0.5 V
Input Pulse Width	≥3.0 µs	≥3.0 µs

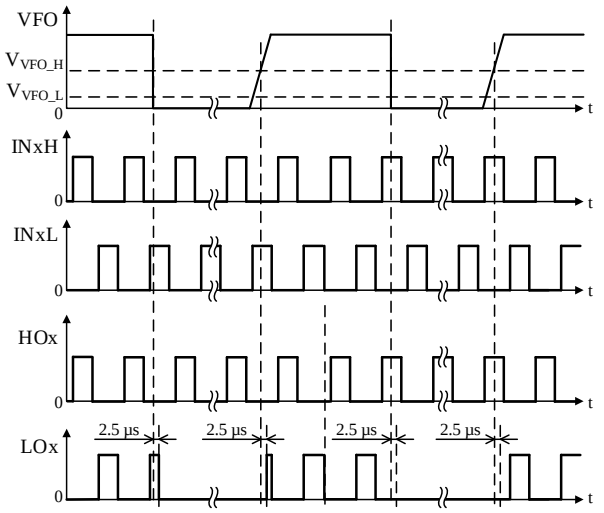


Figure 13-8. Operational Waveforms of Shutdown Signal Input

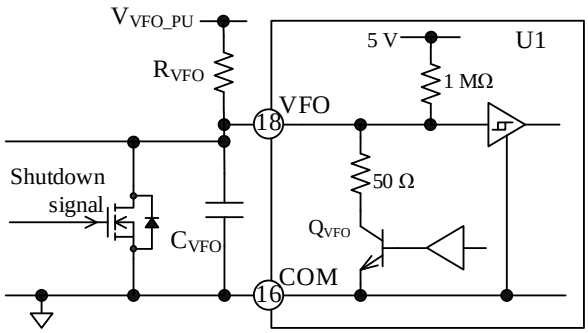


Figure 13-9. Internal Circuit Diagram of VFO Pin and Its Peripheral Circuit

13.3.3. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output IGBTs decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the IC has the undervoltage lockout (UVLO) circuits for each of the VBx, VCCxH, and VCCL pins.

13.3.3.1. VBx Pin Undervoltage Lockout

Figure 13-10 shows operational waveforms of the VBx pin undervoltage lockout operation (i.e., UVLO_VBx).

When the voltage between the VBx and VSx pins (VBx–VSx) decreases to $V_{VBx\text{-}VSx\_L}$ (11.1 V) or less, the UVLO_VBx circuit in the corresponding phase gets activated and sets an HOx signal to logic low. When the VBx–VSx voltage increases to $V_{VBx\text{-}VSx\_H}$ (11.6 V) or more, the IC releases the UVLO_VBx operation. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VBx release. Any fault signals are not output from the VFO pin during the UVLO_VBx operation. In addition, the VBx pin has an internal filter circuit of about 1.8 µs, in order to prevent noise-induced malfunctions.

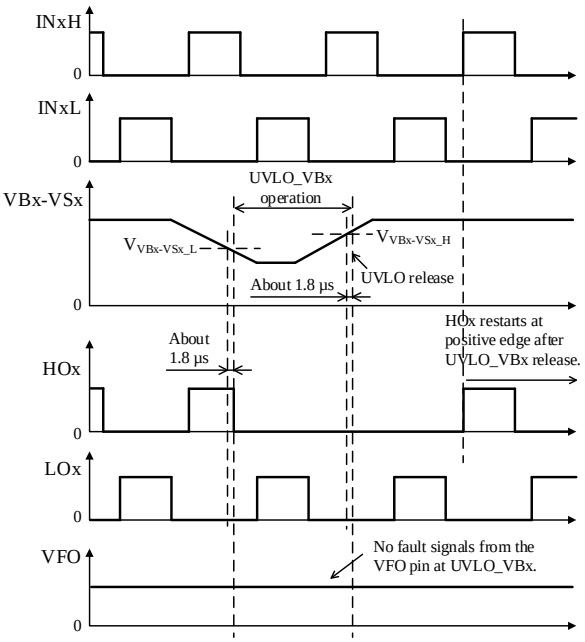


Figure 13-10. UVLO_VBx Operational Waveforms

13.3.3.2. VCCxH Pin Undervoltage Lockout

As Figure 13-11 shows, when the VCCxH pin voltage decreases to V_{VCCxH_L} (11.6 V) or less, the VCCxH pin undervoltage lockout (i.e., UVLO_VCCxH) circuit gets activated and sets an HOx signal to logic low. When the VCCxH pin voltage increases to V_{VCCxH_H} (11.1 V) or more, the IC releases the UVLO_VCCxH operation. Then, the HOx signal outputs according to the INxH input signal. Any fault signals are not output from the VFO pin during the UVLO_VCCxH operation. In addition, the VCCxH pin has an internal filter circuit of about 1.8 µs, in order to prevent noise-induced malfunctions.

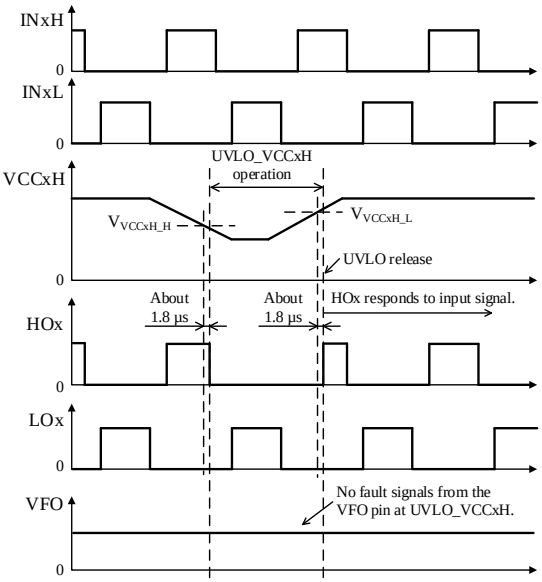


Figure 13-11. UVLO_VCCxH Operational Waveforms

13.3.3.3. VCCL Pin Undervoltage Lockout

As Figure 13-12 shows, when the VCCL pin voltage decreases to V_{VCCL_L} (12.1 V) or less, the VCCL pin undervoltage lockout (i.e., UVLO_VCCL) circuit gets activated and sets an LOx signal to logic low. When the VCCL pin voltage increases to V_{VCCL_H} (12.6 V) or more, the IC releases the UVLO_VCCL operation. Then, the LOx signal outputs according to the INxL input signal. During the UVLO_VCCL operation, the VFO pin becomes logic low and sends fault signals. In addition, the VCCL pin has an internal filter circuit of about 1.8 µs, in order to prevent noise-induced malfunctions.

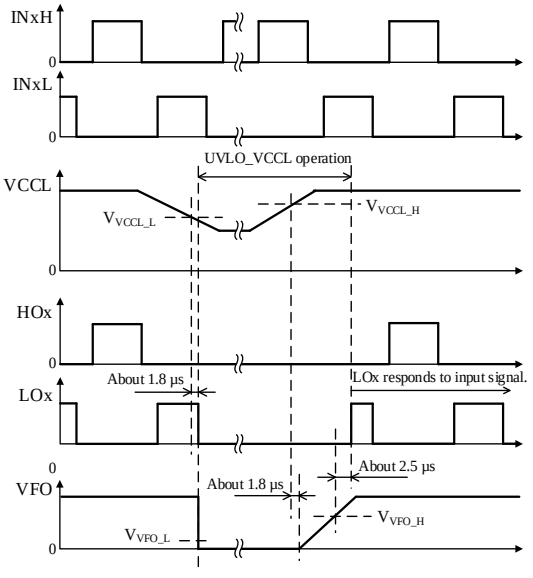


Figure 13-12. UVLO_VCCL Operational Waveforms

13.3.4. Overcurrent Protection (OCP)

Figure 13-13 shows an internal circuit diagram of the OCP pin and its peripheral circuit. As shown in Figure 13-13, the OCP pin detects overcurrents with voltage across an external shunt resistor, R_S. Because the OCP pin is internally pulled down, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S.

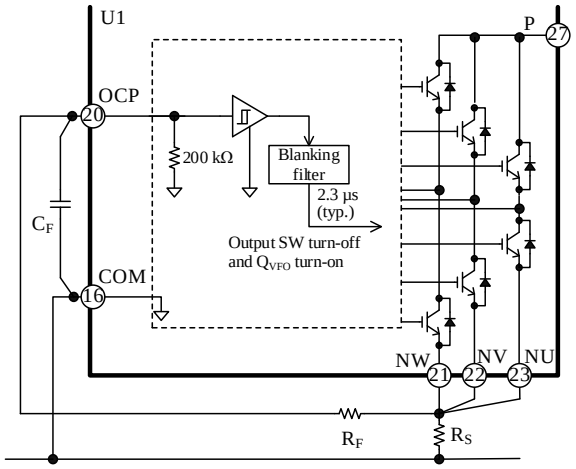


Figure 13-13. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

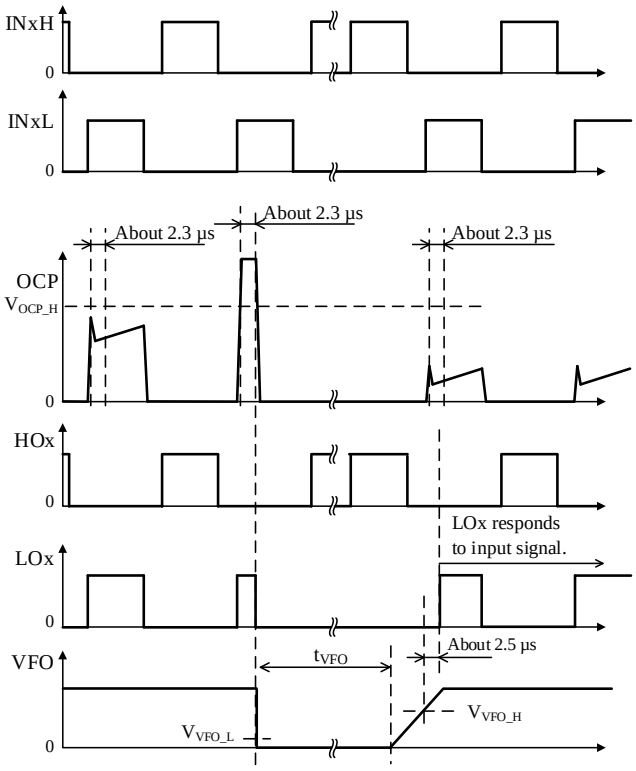


Figure 13-14. OCP Operational Waveforms

Figure 13-14 is a timing chart that represents operational waveforms during OCP operation. When the OCP pin voltage increases to V_{OCP_H} (0.50 V) or more, and remains in this condition for a period of an internal filter circuit (about 2.3 µs) or longer, the OCP circuit is activated. When the OCP is activated, the IC puts both an LOx signal and the VFO pin to logic low. The output IGBTs turn off as the LOx signal becomes logic low; as a result, output current decreases. Even if the OCP pin voltage falls below V_{OCP_L}, the IC holds the VFO pin in the low state for a fixed OCP hold time (t_{VFO}). Then, the output IGBTs operate according to input signals.

In addition, the OCP pin has an internal filter circuit of about 2.3 µs, in order to prevent noise-induced malfunctions.

The OCP hold time, t_{VFO}, can be adjusted by the value of the CFO pin capacitor, (C_{CFO}, see Section 13.2.10).

The OCP is used for detecting abnormal conditions, such as an output IGBT shorted. In case short-circuit conditions occur repeatedly, the output IGBTs can be destroyed. To prevent such event, input the fault signals to the interrupt pin (INT) of the external microcontroller, and be sure to program so that any input signals to the IC shut off within the predetermined OCP hold time, t_{VFO}.

A shunt resistor, R_S, should be set to satisfy the recommended value of 9.0 mΩ to 15.3 mΩ. It is also required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application. A time constant, t_{RFCF}, of the CR filter (R_F, C_F) connected to the OCP pin should be set to satisfy the recommended value of 1.0 µs to 2.0 µs. And place C_F as close as possible to the IC with minimizing a trace length between the OCP and COM pins.

Note that the OCP is not activated when one or more of the U, V, and W pins or their traces are shorted to ground (ground fault) because no current flows through R_S. In case any of these pins falls into a state of ground fault, the output IGBTs may be destroyed.

If the overcurrent protection is required for ground fault mode, a separate correspondence is required (e.g., adding a circuit for detecting the current of the P pin, and setting the input signal of the INxH pin to logic low using the signal).

14. Design Notes

14.1. PCB Pattern Layout

Figure 14-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops (especially, between the P pin, C_P, and the Nx pin) should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

A shunt resistor, R_S, should be placed as close as possible to the IC with minimizing a trace length between the Nx pin and a capacitor, C_P.

Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to the shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 14-1). Moreover, extreme care should be taken when wiring so that currents from the power ground do not affect the logic ground (e.g., the control ground trace is not placed parallel near the power ground, and these traces are not crossed as much as possible).

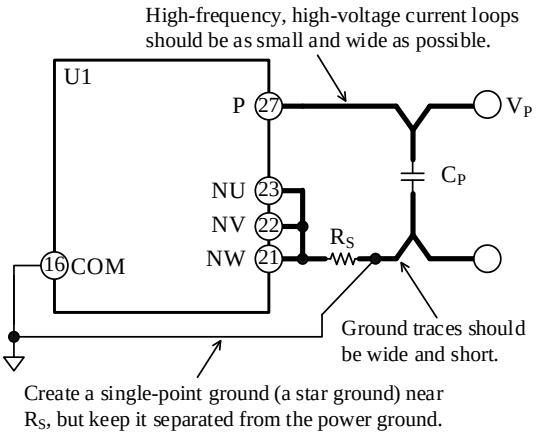


Figure 14-1. High-frequency and High-voltage Current Paths, and Connections to Logic Ground

To reduce noises generated by electromagnetic induction by high-frequency current, use a double-sided board to offset the magnetic field. For example, as shown in Figure 14-2, design the trace from the P pin to C_P on the front side, and the trace from C_P to the Nx pin on the back side. Then, overlap these traces. The currents flowing from the P pin to C_P, and from C_P to the Nx pin are the same value. Thus, overlapping these traces so that their current directions are opposite offsets the generated magnetic field, and reduces the noises.

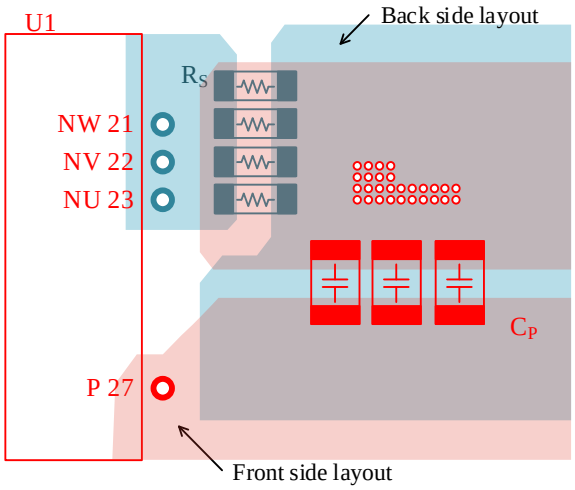


Figure 14-2. Peripheral Layout Example of C_P (Double-sided Board)

14.2. Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- It is recommended to use a pair of a metric screw of M4 and a plain washer, which is 9 mm (φ) of outside diameter. To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to about 20% to 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 5. The order of the screws does not matter to the temporary tightening. Note that the sequence when the screws are tightened finally must be the same order as these are tightened firstly.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there must be no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  - Grease thickness: 100 µm to 200 µm
  - Heatsink flatness: ±100 µm

14.3. Considerations in IC Characteristics Measurement

When checking the characteristics of the internal switching elements (IGBTs and freewheeling diodes), the IGBTs may result in permanent damage unless these are measured appropriately. Therefore, the following should be taken into account. The absolute maximum rating of the Collector-to-Emitter Voltage, V_{CES}, is 650 V.

- Do not measure the withstand voltage of the internal IGBTs. Applying the voltage of V_{CES} or more between the collector and emitter may degrade the IGBTs.
- Measurement condition of the leakage current of the internal IGBTs must be below V_{CES}.
- The leakage current value is the total leakage current of such as IGBT, freewheeling diode, control IC, and bootstrap diode. These leakage currents can not be measured individually.
- When measuring leakage current of the IGBTs, note that the gate and emitter of the IGBT must be the same potential. The gate of the high-side IGBT is pulled down to the emitter inside the IC, but the gate of the low-side IGBT is pulled down to the COM pin inside the IC. To prevent damage of the IGBTs, the Nx and COM pins shoud be shorted and measured.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 14-3 shows the high-side IGBT (Q_{UH}) in the U-phase; Figure 14-4 shows the low-side IGBT (Q_{UL}) in the U-phase.

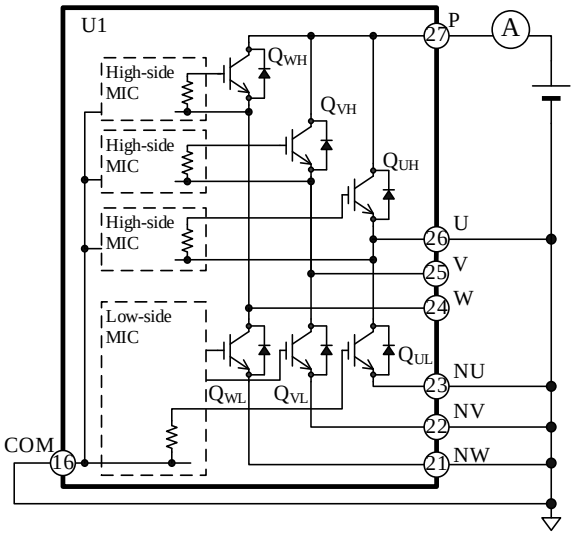


Figure 14-3. Typical Measurement Circuit for High-side IGBT (Q_{UH}) in U-phase

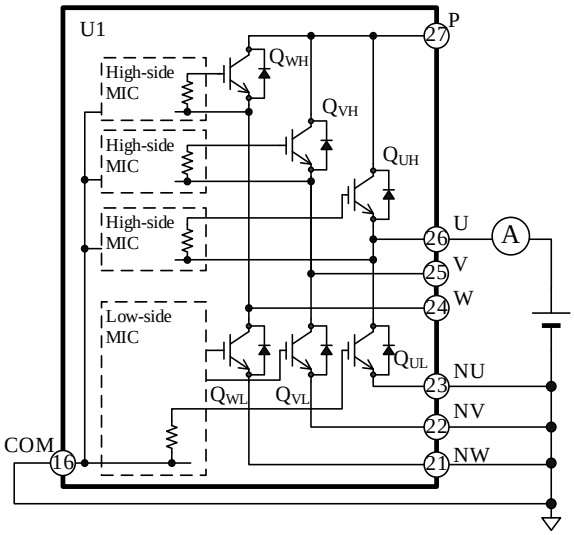


Figure 14-4. Typical Measurement Circuit for Low-side IGBT (Q_{UL}) in U-phase

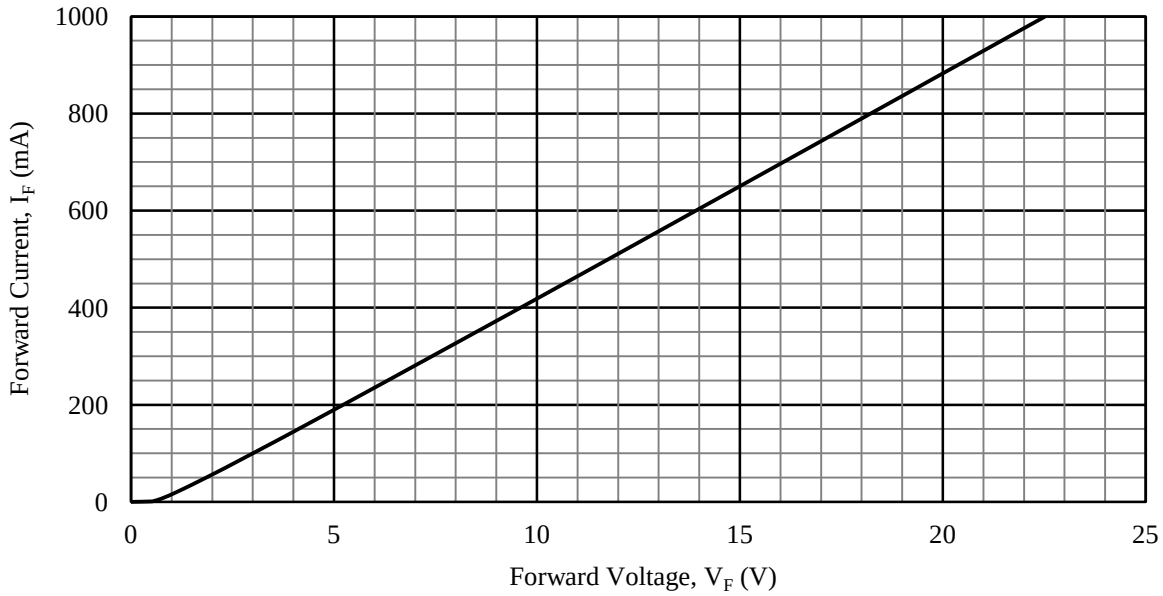
15. Typical Characteristics

15.1. Thermistor Resistance

Table 15-1. Thermistor Resistance

Thermistor Temperature	Thermistor Resistance (kΩ)			Error (%)		
(°C)	Min.	Typ.	Max.	Min.	Typ.	Max.
−40	946	1024	1104	-7.6%	0%	7.8%
−35	684	737	792	-7.3%	0%	7.4%
−30	500	537	575	-6.9%	0%	7.1%
−25	370	396	422	-6.6%	0%	6.7%
−20	276	294	313	-6.3%	0%	6.4%
−15	208	221	235	-6.0%	0%	6.1%
−10	158	168	177	-5.7%	0%	5.8%
−5	121	128	135	-5.5%	0%	5.5%
0	93.5	98.6	104	-5.2%	0%	5.2%
5	72.8	76.6	80.4	-4.9%	0%	5.0%
10	57.1	59.9	62.7	-4.7%	0%	4.7%
15	45.1	47.3	49.4	-4.5%	0%	4.5%
20	35.9	37.5	39.1	-4.2%	0%	4.2%
25	28.8	30.0	31.2	-4.0%	0%	4.0%
30	23.1	24.2	25.2	-4.2%	0%	4.2%
35	18.7	19.6	20.4	-4.4%	0%	4.4%
40	15.2	15.9	16.7	-4.6%	0%	4.6%
45	12.4	13.1	13.7	-4.8%	0%	4.8%
50	10.2	10.8	11.3	-5.0%	0%	5.0%
55	8.46	8.93	9.39	-5.2%	0%	5.2%
60	7.04	7.44	7.84	-5.4%	0%	5.4%
65	5.88	6.22	6.57	-5.5%	0%	5.6%
70	4.94	5.24	5.54	-5.7%	0%	5.8%
75	4.16	4.42	4.69	-5.9%	0%	5.9%
80	3.53	3.75	3.98	-6.0%	0%	6.1%
85	3	3.20	3.4	-6.2%	0%	6.3%
90	2.56	2.74	2.91	-6.3%	0%	6.4%
95	2.2	2.35	2.5	-6.4%	0%	6.6%
100	1.89	2.03	2.16	-6.6%	0%	6.7%
105	1.63	1.75	1.87	-6.8%	0%	6.9%
110	1.42	1.52	1.63	-6.8%	0%	7.0%
115	1.23	1.32	1.42	-7.0%	0%	7.1%
120	1.07	1.16	1.24	-7.2%	0%	7.2%
125	0.938	1.01	1.09	-7.2%	0%	7.5%
130	0.823	0.888	0.955	-7.4%	0%	7.5%
135	0.724	0.782	0.842	-7.5%	0%	7.7%
140	0.639	0.691	0.745	-7.6%	0%	7.8%
145	0.565	0.612	0.661	-7.7%	0%	7.9%
150	0.501	0.544	0.587	-7.8%	0%	8.0%

15.2. Bootstrap Diode Characteristics, I_F vs. V_F



15.3. Transient Thermal Resistance Curve

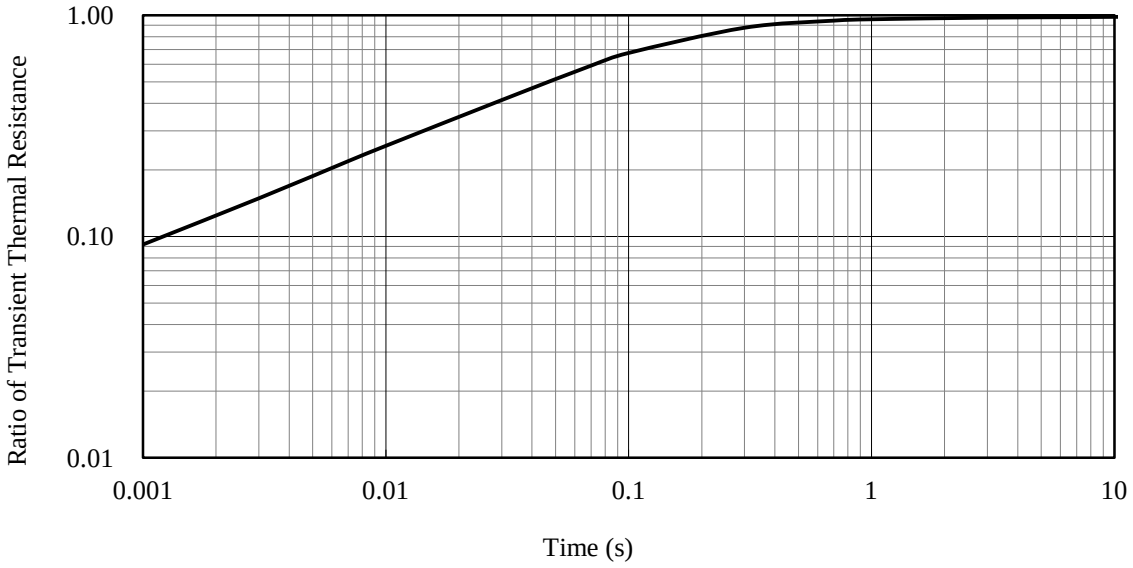


Figure 15-1. Transient Thermal Resistance Curve

15.4. Reference Allowable Effective Current Curves

The following curve represents allowable effective current in 3-phase sine-wave PWM driving with the maximum parameters such as $V_{CE(SAT)}$, V_F, switching loss, recovery loss, and thermal resistance.

Operating conditions:

P pin input voltage, V_P = 300 V; input voltages of VCCxH and VCCL pins, V_{VCCxH} = V_{VCCL} = 15 V; modulation index, M = 1; motor power factor, cosθ = 0.8; carrier frequency, f_{PWM} = 10 kHz; junction temperature, T_J = 150 °C; case-to-heatsink thermal resistance, $R_{(C-F)}$ = 0.44 °C/W; motor rotation speed, 600 rpm; number of motor pole pairs, 3.

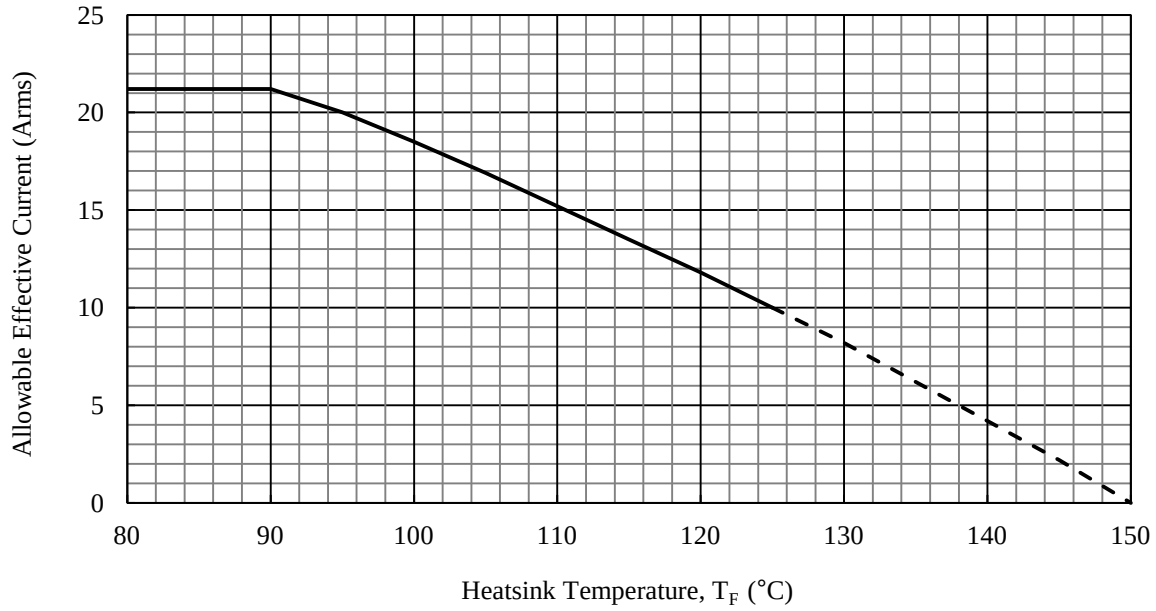


Figure 15-2. Reference Allowable Current Curve

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DSGN-CEZ-16003