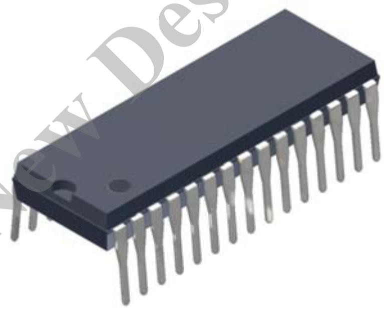
SI-7510
5-Phase New Pentagon Stepper Motor Pre-Driver IC

Introduction

The SI-7510 is a pre-driver IC for driving 5-phase stepper motors wound in the New Pentagon configuration (driver circuit design patented by Oriental Motor Co., Ltd.). Direct external control of motor driving functions are synchronized by the built-in sequencer to an applied clock input (CL) signal. The SI-7510 drive is implemented with a user-configurable output stage consisting of dual N-channel power MOSFETs. This results in lower thermal resistance and greater efficiency.



Not to scale

Figure 1. SI-7510 package is a 30-pin, fully molded DIP, with a 1.778 mm pin pitch.

Features and Benefits

- Main supply voltage, $V_{CC}1$: 10 to 42 V
- Logic supply voltage, $V_{CC}2$: 3 to 5.5 V
- External forward and backward motor rotation control via CW/CCW input
- External selection of 4-phase (full step) and 4-5–phase (half step) driving via F/H pin
- Output enable/disable control via Enable pin (internal sequencer function remains active during Disable state, monitoring the clock input (CL) for automatic sequencing)
- Built-in charge pump circuit for driving external high-side N-channel MOSFETs of all output phases
- Self-excitation constant current control set by external R-C circuit time constant on RC input
- Maximum output current set by the SI-7510 and the combined rating of the dual external MOSFET array as follows:

Output Current I_O(max)	Recommended MOSFET Array	Manufacturer
6 A	SLA5073 and SLA5074	Sanken
7 A	SLA5065 and SLA5068	Sanken

SANKEN ELECTRIC CO., LTD.
http://www.sanken-ele.co.jp/en/
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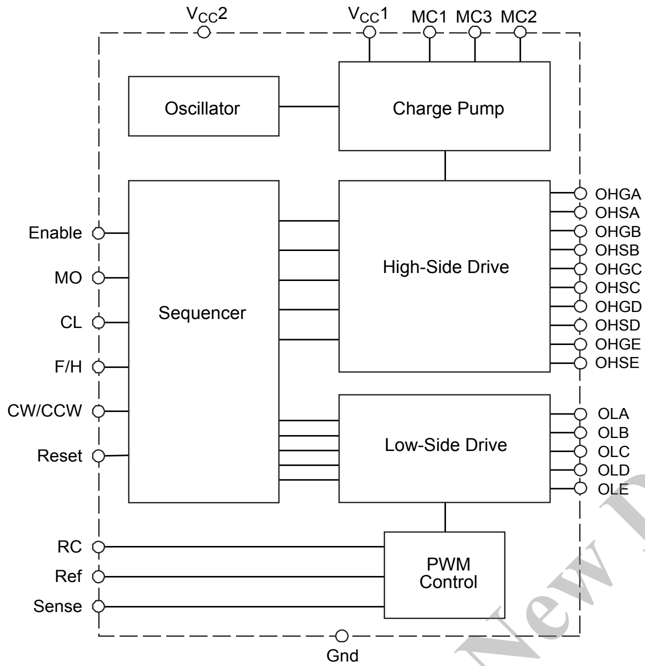
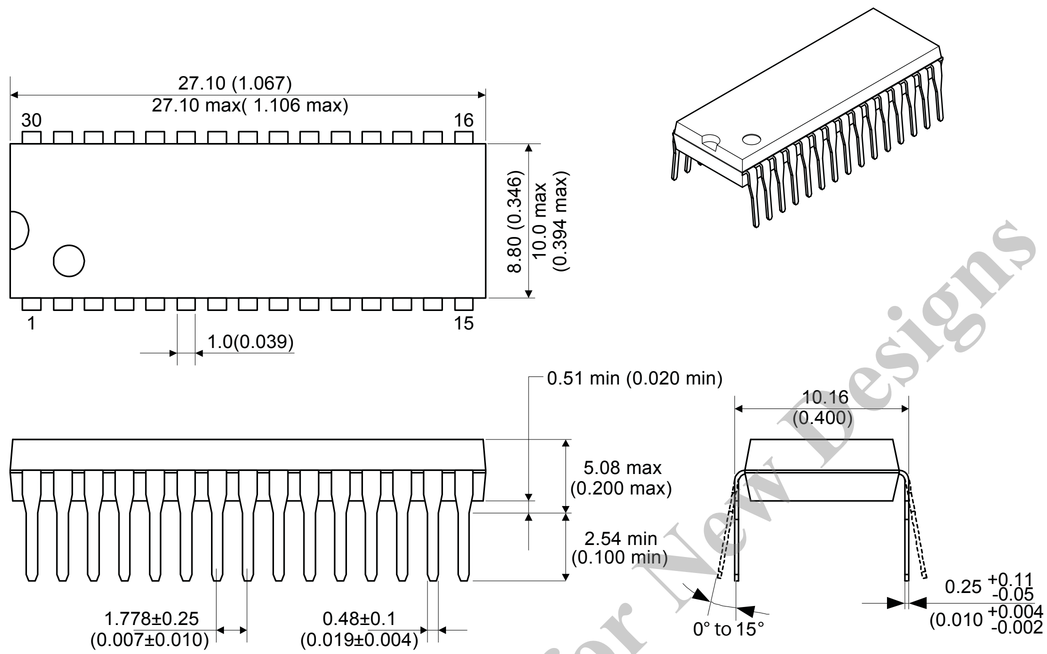
Functional Block Diagram



Pin Assignment and Function Table

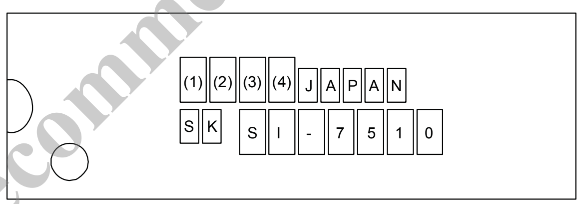
Pin Number	Symbol	Function	Pin Number	Symbol	Function
1	MC1	Capacitor connection terminal for charge pump (connect externally to MC2)	16	OLE	Low-side MOSFET gate connection pin, phase E
2	MC3	Capacitor connection terminal for charge pump (connect externally to GND)	17	OLD	Low-side MOSFET gate connection pin, phase D
3	MC2	Capacitor connection terminal for charge pump (connect externally to MC1)	18	OLC	Low-side MOSFET gate connection pin, phase C
4	$V_{CC}1$	Main supply voltage input	19	OLB	Low-side MOSFET gate connection pin, phase B
5	Enable	Output enable/disable logic input; set low to disable output	20	OLA	Low-side MOSFET gate connection pin, phase A
6	$V_{CC}2$	Logic supply voltage input	21	OHSE	High-side MOSFET source connection pin, phase E
7	MO	Monitor to detect motor position	22	OHGE	High-side MOSFET gate connection pin, phase E
8	CL	Clock logic input; internal sequencer updates on positive edge	23	OHSD	High-side MOSFET source connection pin, phase D
9	F/H	4-phase (full step)/4–5-phase (half-step) switching logic input; set low for full step	24	OHG	High-side MOSFET gate connection pin, phase D
10	CW/CCW	Forward (CW) / backward (CCW) rotation logic input; set low for forward rotation	25	OHSC	High-side MOSFET source connection pin, phase C
11	Reset	Reset logic input; set high to reset	26	OHGC	High-side MOSFET gate connection pin, phase C
12	RC	R-C network connection terminal for chopping off-time setting and blanking time setting.	27	OHSB	High-side MOSFET source connection pin, phase B
13	Ref	Reference voltage input terminal for motor current setting	28	OHGB	High-side MOSFET gate connection pin, phase B
14	Sense	Sense motor current	29	OHSA	High-side MOSFET source connection pin, phase A
15	Gnd	Ground terminal	30	OHGA	High-side MOSFET gate connection pin, phase A

Package Outline Drawing



Dimensions in mm
(Inch dimensions in parentheses, for reference only)

Package Branding



Column	Parameter	Description												
(1)	Year Code*	The last digit of year												
(2)	Month Code*	Month	1	2	3	4	5	6	7	8	9	10	11	12
		Alphabet	1	2	3	4	5	6	7	8	9	O	N	D
(3)	Control Code	1～9, 0												
(4)	Control Code	1～9, 0												

*Year and month are based on when the branding is made.

Pb-free. Device composition compliant with the RoHS directive.

Absolute Maximum Ratings valid at T_A = 25°C, unless otherwise noted

Characteristic	Symbol	Notes	Rating	Unit
Main Supply Voltage	V_{CC1}		44	V
Logic Supply Voltage	V_{CC2}		7	V
Logic Input Voltage	V_{IN}		–0.3 to V_{CC2}	V
REF Input Voltage	V_{REF}		–0.3 to V_{CC2}	V
Sense Input Voltage	V_{SENSE}		2	V
Charge Pump Output Voltage	V_{MC3}		48	V
Power Dissipation	P_D		1.6	W
Operating Ambient Temperature	T_A		–10 to 80	°C
Storage Temperature	T_{STG}		–20 to 150	°C
Junction Temperature	T_J		150	°C

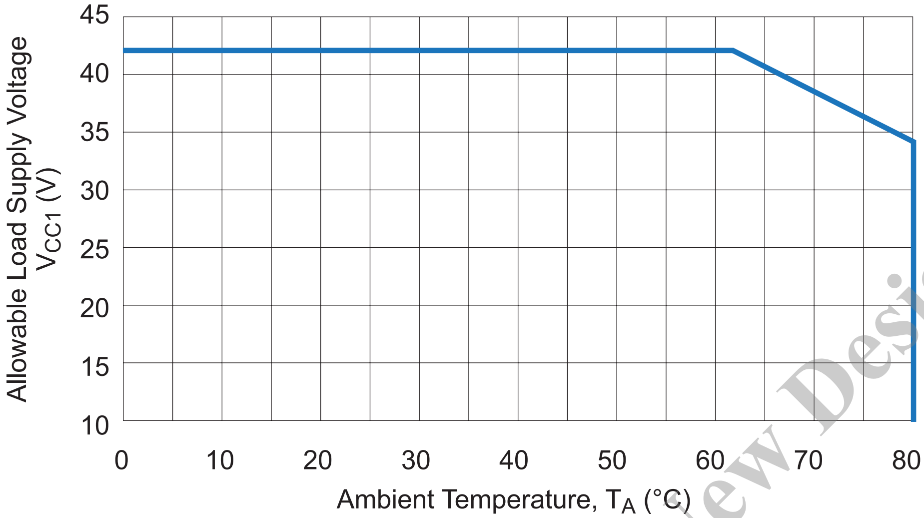
Recommended Operating Conditions

Characteristic	Symbol	Conditions	Min.	Max.	Unit
Main Supply Voltage	V_{CC1}	Insert a 5 V Zener diode between V_{CC1} and V_{MC3} when using the device with a V_{CC1} of 35 V or more	10	42	V
Logic Supply Voltage	V_{CC2}		3	5.5	V
REF Input Voltage	V_{REF}		0.1	1	V

ELECTRICAL CHARACTERISTICS valid at T_A = 25°C,V_{CC}1 = 24 V, V_{CC}2 = 5 V; unless otherwise noted

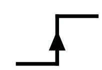
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Main Supply Current	I_{CC1}		–	–	25	mA
Logic Supply Current	I_{CC2}		–	–	10	mA
Logic Input Voltage	V_{IL}	V_{CC2} = 5 V	–	–	1.25	V
	V_{IH}	V_{CC2} = 5 V	3.75	–	–	V
Logic Input Current	I_{IL}	V_{IL} = 0 V	–20	–	20	μA
	I_{IH}	V_{IH} = 5.5 V	–20	–	20	μA
Enable Pin Input Current	I_{ENA}	V_{ENA} = 0 V	–100	–	20	μA
Ref Pin Input Current	I_{REF}	I_{ENA} = 0 to 5.5 V	–20	–	20	μA
Sense Pin Voltage	V_{SENSE}	V_{REF} = 1 V	–	1	–	V
Sense Pin Current	I_{SENSE}	V_{SENSE} at 0 V and at 2 V	–20	–	20	μA
MO Pin Output Voltage	V_{MOL}	I_{MOL} = 1 mA	–	–	1	V
	V_{MOH}	I_{MOH} = –1 mA	4	–	–	V
RC Pin Threshold Voltage	V_{RCL}		–	0.5	–	V
	V_{RCH}		–	1.5	–	V
RC Pin Outflow Current	I_{RC}	V_{RC} = 0 V	–	300	–	μA
Charge Pump Output Voltage	V_{MC3}	No external Zener diode	–	V_{CC1} + 9	–	V
High-Side Output Voltage (Between gate sources)	V_{HGSL}	No external Zener diode	–	–	1	V
	V_{HGSH}		–	8.5	–	V
Low-Side Output Voltage	V_{LGL}		–	–	1	V
	V_{LGH}		–	7.5	–	V
Maximum Clock Frequency	f_{CK}		100	–	–	kHz
Minimum Input Clock Pulse Width	t_{CON}	(On, high portion of pulse)	1	–	–	μs
Power-On Reset Time	t_{PW}		–	1.5	–	μs
Output Delay Time	t_{IO}		–	2	–	μs
CW/CCW and F/H Pins Input Data Setup Time	t_{ICS}	Measured from rising edge of input clock pulse	500	–	–	ns
CW/CCW and F/H Pins Input Data Hold Time	t_{ICH}	Measured from rising edge of input clock pulse	500	–	–	ns

Load Supply Derating



Logic Input Truth Table[1]

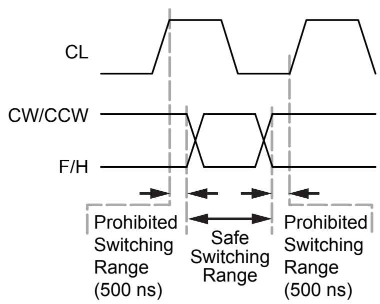
Each function listed below operates independently of the CL input signal

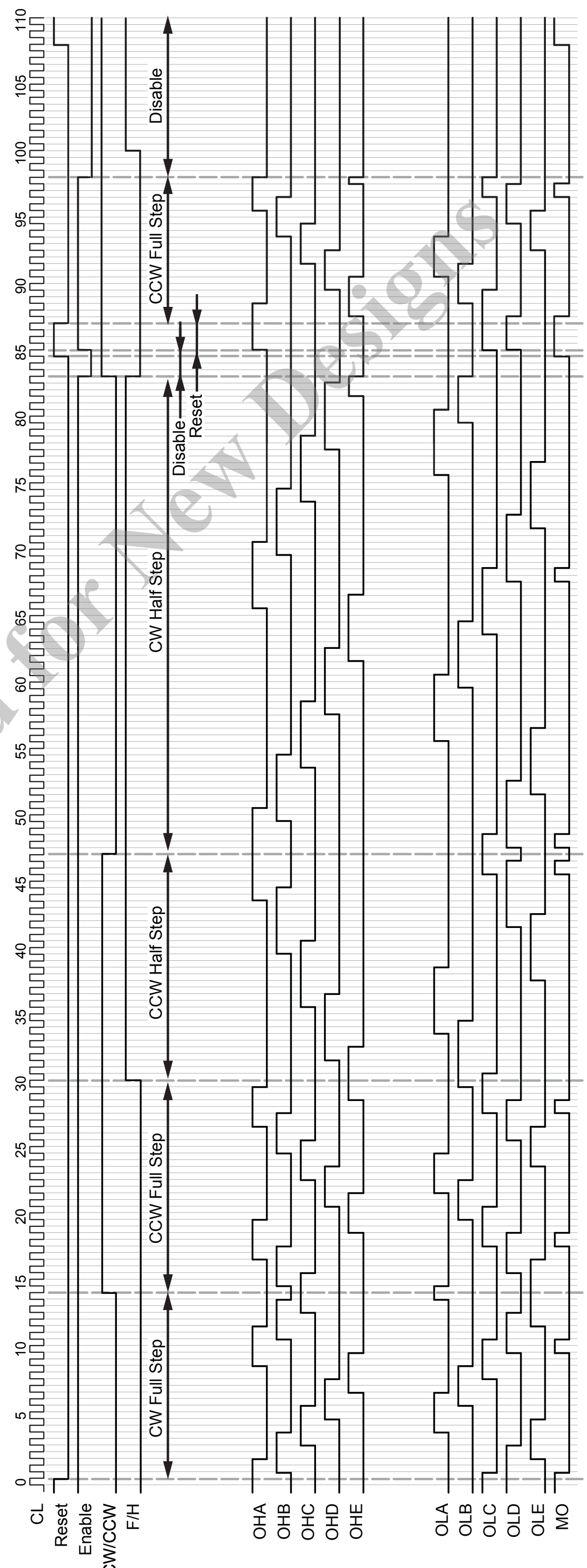
Pin Name (Number)	Function	Low Level	High Level
CL (8)	Clock input	 (Positive edge)	
Enable (5)	Output control	Disable[2]	Enable
F/H (9)	Stepping mode control	Full step	Half step
CW/CCW (10)	Rotation direction control	Forward (CW)	Backward (CCW)
Reset (11)	Asynchronous Reset input	Normal operation	Logic reset[3]

[1]At each CL input positive edge, the internal sequencer automatically responds to current state of logic pins.
[2]Internal sequencer responds to CL input during both Disable and Enable states of Enable pin.
[3]After reset, device turns-on: high-side phase A, low-side phase C, and low-side phase D.

Input and Output Timing Chart and Motor Coil Excitation Sequence

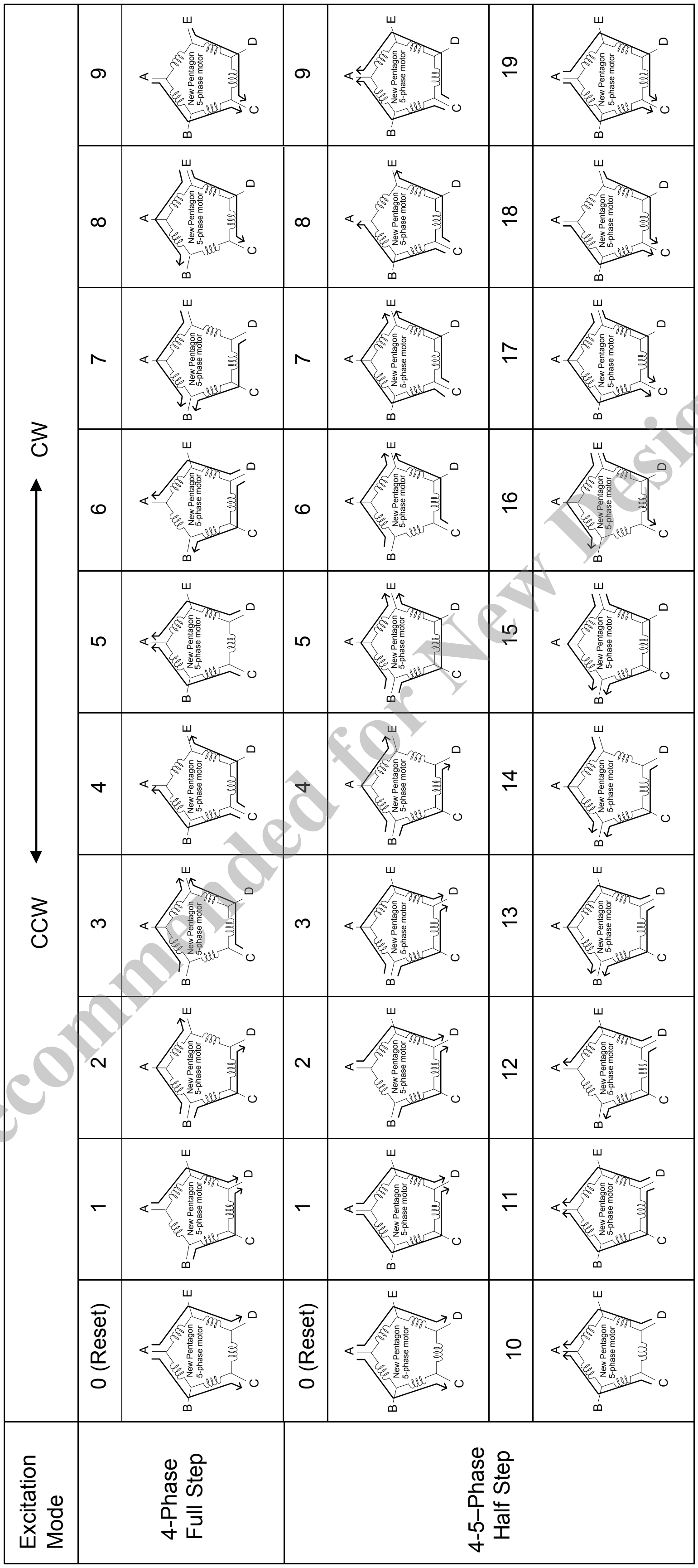
Conditions for Switching Input Logic Signals



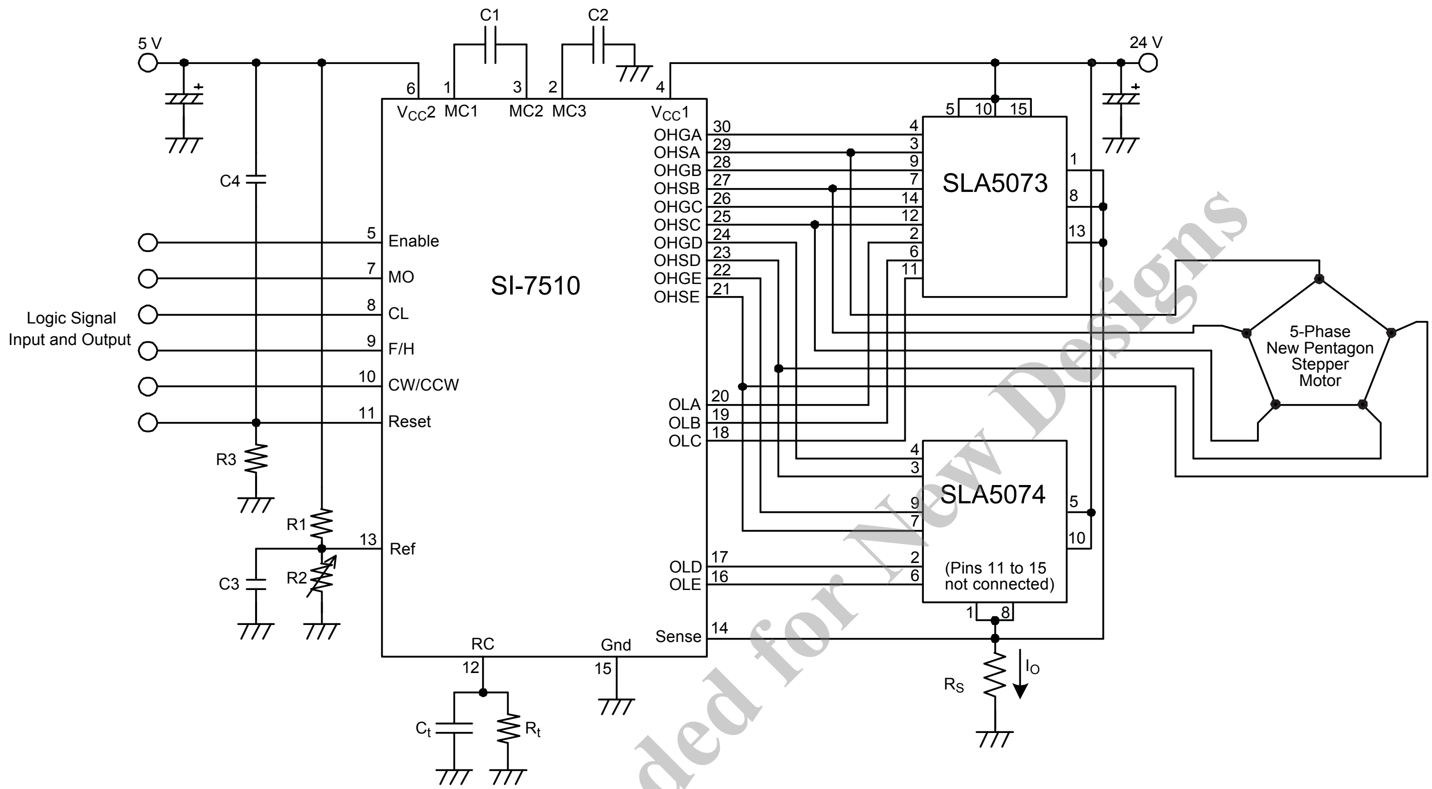


Input and Output Timing

Motor Coil
Excitation Sequence



Typical Connection



External Component Typical Values (for reference use only):

Component	Value	Component	Value
R1	510 Ω	C1	2200 pF
R2	100 Ω (varistor)	C2, C4	0.01 μF
R3	20 kΩ	C3	0.1 μF
R_S	0.33 Ω, 1 to 2 W	C_t	420 to 1100 pF
R_t	15 to 75 kΩ		

- Take precautions to avoid noise on the V_{CC} lines; noise levels greater than 0.5 V on a V_{CC} line may cause device malfunction, so be careful when laying out the traces.
- Calculation of I_O:

  $I_O = V_{RS} / R_S$

  $I_{OM} = I_O / 2$, where I_{OM} is the motor coil current
- Calculation of t_{OFF}:

  $t_{OFF} = 1.1 \times R_t \times C_t$

Functional Description

Reset Control

Reset is non-synchronous reset function. Figure 2 shows the motor current path after the internal sequencer resets the device logic.

Calculating Motor Current

The calculation for setting motor current, I_{OM}, for the SI-7510 is determined by the ratios of the external components R1 and R2, and the current sense resistor, R_S. The SI-7510 controls the total set current, I_O, and the relationship between I_O and I_{OM} is as follows:

$$I_O = 2 \times I_{OM} \quad (1)$$

The current sense voltage, V_{SENSE}, is generated by I_O flowing into the current sense resistor, R_S. The ratio of V_{REF} to V_{SENSE} is 1:1, so I_O can be calculated as follows (refer to figure 3):

$$I_O = V_{REF} / R_S \quad (2)$$

where V_{REF} is calculated as:

$$V_{REF} = V_{CC2} \times R_2 / (R_1 + R_2) \quad (3)$$

Power-Down (Hold) Method

If the motor torque is to be reduced to enter a motor-hold mode, an external circuit consisting of a resistor, R_X, and a transistor, Q1, should be added, as shown in figure 3. For the current, I_{OPD}, required to hold a given torque, the values for the external components can be calculated as follows:

$$I_{OPD} = \frac{1}{1 + \dfrac{R_1 (R_2 + R_X)}{R_2 \times R_X}} \times \frac{V_{CC2}}{R_S} \quad (4)$$

In the above equation, the saturation voltage of the transistor is not taken into consideration.

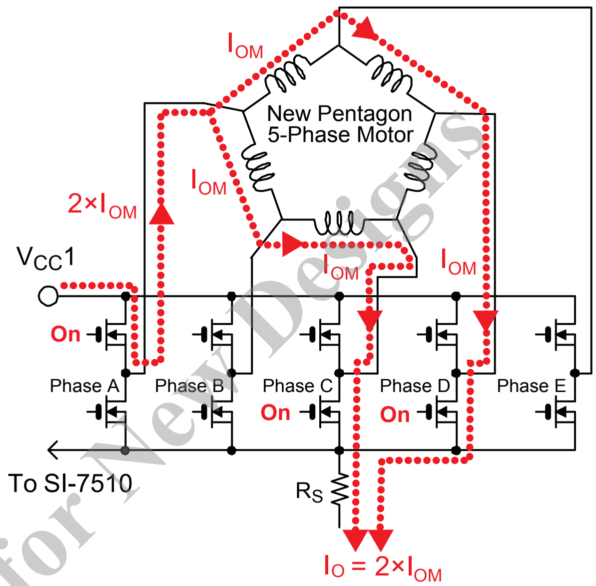


Figure 2. Motor current path after logic reset

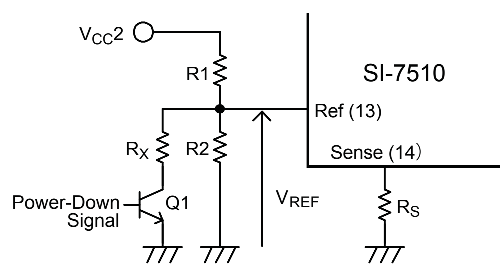


Figure 3. Motor current setting circuit

Output Chopping

The operating output and feedback pins waveforms during chopping are shown in figure 4, and the current paths during chopping are shown in figure 5.

Chopping Off Time This product controls output chopping off-time. Chopping off-time is determined by the time constant of the external R_t - C_t circuit connected to the RC terminal. The off-time is the duration for the RC terminal voltage to decrease from approximately 1.5 V to 0.5 V. The chopping off-time can be calculated as:

$$t_{OFF} \approx 1.1 \times R_t \times C_t \tag{5}$$

where R_t is 15 to 75 kΩ, C_t is 420 to 1100 pF (recommended value).

Blanking Time The R_t - C_t circuit time constant is also related to the blanking time, t_{BRK}. Blanking time prevents malfunction due to ringing noise which occurs after chopping transitions from off to on. Blanking time is the duration for the RC terminal voltage to increase from approximately 0.5 V to 1.5 V. When the RC terminal voltage increases to this level, a current of approximately 200 µA flows out of the RC terminal.

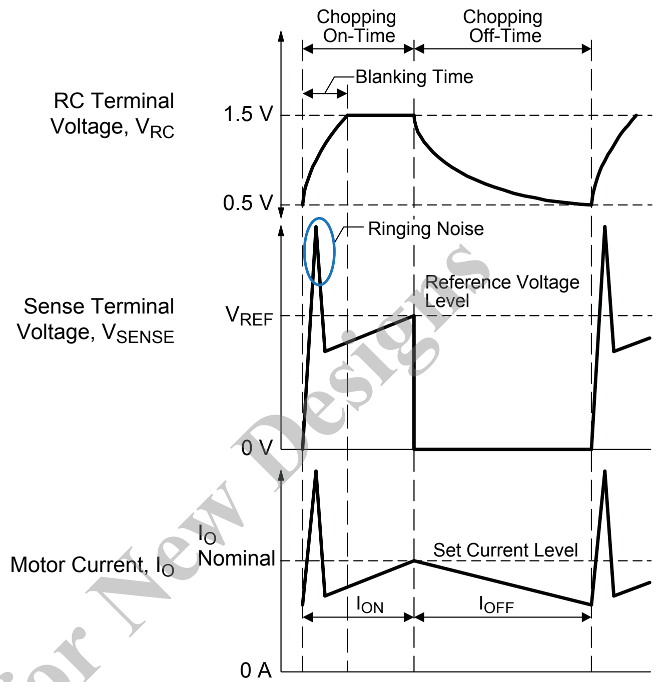


Figure 4. Operating waveforms during chopping

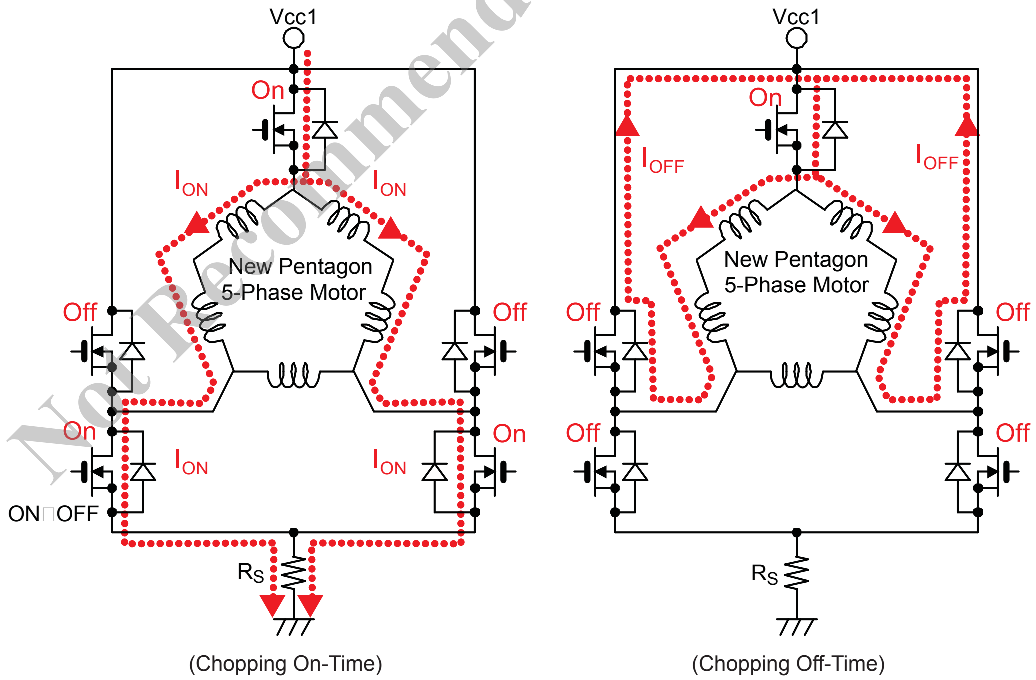


Figure 5. Current path during chopping; dotted red line indicates path of current: (left) during chopping on-time (I_{ON}), and (right) during chopping off-time (I_{OFF})

Blanking time is calculated as:

$$t_{BRK} \approx C_t \,/\, (200\times10^{-6}) \qquad (6)$$

Even if the sense voltage, V_{SENSE}, becomes higher than the reference voltage, V_{REF}, during the blanking time interval, the power control circuit does not operate and the device output always remains in the On state. Because of this, if the C_t value is too large when the output current value must be set small, the output current may not fall to the set value. In addition, if the C_t value is too small, it causes malfunction due to ringing noise.

Chopping On-Time Chopping on-time is determined by: $V_{CC}1$, the motor output time constant, and the chopping off-time.

Note: In addition, during the motor actual operation, chopping on-time changes because the inductance of the coils changes due to crossing magnetic flux lines.

Calculation of Power Dissipation of Power MOSFETs

The SI-7510 connects to the power MOSFETs of the output stage and drives the motor. In this section, a method of calculating an estimate of the power dissipation of the power MOSFETs is shown. This calculation method uses an approximation formula, and factors such as parameter changes during actual operation are not considered in this example. Therefore, please confirm the thermal characteristics of the power MOSFETs in actual operation to determine the final design.

Parameters for Power Dissipation Calculation The following parameters are required to calculate power dissipation of the power MOSFETs:

- Average current ripple, I_{OM}
- Excitation mode
- Chopping time during current control, t_{ON} and t_{OFF}
- Power MOSFET on-resistance, $R_{DS(ON)}$
- Power MOSFET body diode forward voltage, V_{SD}

The maximum specifications of the power MOSFETs should be used for $R_{DS(ON)}$ and $V_{SD.}$ In addition, t_{ON} and t_{OFF} must be confirmed in actual operation.

Sample Power Dissipation Calculation (Estimation) The method shown below calculates a power dissipation case for each phase, in each excitation mode. The example MOSFET array uses the SLA5073 for phases A, B, and C, and the SLA5074 for phases D and E.

The dissipation of each case is given in table 1 for 4-phase excitation (full step) and in table 2 for 4-5–phase excitation (half step). The symbols listing in the tables refer to the following formulas:

- $H1 = I_O^2 \times R_{DS(ON)}$ (W)
- $H2 = I_{OM}^2 \times R_{DS(ON)}$ (W)
- $L1 = I_O^2 \times R_{DS(ON)} \times t_{ON} / (t_{ON} + t_{OFF})$
  $+ I_O \times V_{SD} \times t_{OFF} / (t_{ON} + t_{OFF})$ (W)
- $L2 = I_{OM}^2 \times R_{DS(ON)} \times t_{ON} / (t_{ON} + t_{OFF})$
  $+ I_{OM} \times V_{SD} \times t_{OFF} / (t_{ON} + t_{OFF})$ (W)

where

$I_O = I_{OM} \times 2$, $I_O = V_{REF} / R_S$, and

$t_{ON} : t_{OFF} = 1 : 5$ (estimated).

Table 1. 4-Phase Excitation (Full Step)

MOSFET	Step																												
	Reset (0)			1			2			3			4			5			6			7			8			9		
SLA5073	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
	H1	–	L2	H2	H2	–	–	H1	–	–	H2	H2	L2	–	H1	L1	–	H2	L2	L2	–	–	L1	–	–	L2	L2	H2	–	L1
SLA5074	D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E	
	L2	–		L1	–		L2	L2		–	L1		–	L2		H2	–		H1	–		H2	H2		–	H1		–	H2	

Dissipation in Hold State: If the optional Hold state is used, calculate the dissipation at that step as follows (this example uses step 0, Reset):

- Dissipation of SLA5073: H1 + L2 (W)
- Dissipation of SLA5074: L2 (W)

Dissipation in Rotation: Dissipation during normal operation is calculated as an average dissipation, as follows:

- Dissipation of SLA5073: (H1 × 3 + H2 × 6 + L1 × 3 + L2 × 6) / 10 (W)
- Dissipation of SLA5074: (H1 × 2 + H2 × 4 + L1 × 2 + L2 × 4) / 10 (W)

Table 2. 4-5–Phase Excitation (Half Step)

MOSFET	Step																												
	Reset (0)			1			2			3			4			5			6			7			8			9		
SLA5073	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
	H1	–	L2	H1	–	–	H2	H2	–	–	H1	–	–	H1	–	–	H1	–	–	H2	H2	–	–	H1	L2	–	H1	L1	–	H1
SLA5074	D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E	
	L2	–		L1	–		L1	–		L1	–		L2	L2		–	L1		–	L1		–	L1		–	L2		–	–	
	10			11			12			13			14			15			16			17			18			19		
SLA5073	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
	L1	–	H2	L1	–	–	L2	L2	–	–	L1	–	–	L1	–	–	L1	–	–	L2	L2	–	–	L1	H2	–	L1	H1	–	L1
SLA5074	D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E		D	E	
	H2	–		H1	–		H1	–		H1	–		H2	H2		–	H1		–	H1		–	H1		–	H2		–	–	

Dissipation in Hold State: If the optional Hold state is used, calculate the dissipation at that step as follows (this example uses step 0, Reset):

- Dissipation of SLA5073: H1 + L2 (W)
- Dissipation of SLA5074: L2 (W)

Dissipation in Rotation: Dissipation during normal operation is calculated as an average dissipation, as follows:

- Dissipation of SLA5073: (H1 × 9 + H2 × 6 + L1 × 9 + L2 × 6) / 20 (W)
- Dissipation of SLA5074: (H1 × 6 + H2 × 4 + L1 × 6 + L2 × 4) / 20 (W)

The allowable power dissipation of each MOS array is shown in the follow table:

External Heatsink Connection	MOSFET	Allowable Power Dissipation (W)	MOSFET Thermal Resistance, $R_{\theta j\text{-}a}$ (°C/W)
None	SLA5073	5	25
	SLA5074	4.8	26
Infinite	SLA5073	30	4.17
	SLA5074	25	5

To choose a heatsink, refer to the calculated dissipation, the allowable power dissipation, and figure 6.

When deciding on a heatsink for the SLA5073 or SLA5074, please confirm the temperature of the product in actual operation. The above calculated values include errors because they are approximate values. Please choose a heatsink which keeps the aluminum exposed thermal pad on the back side of the SLA5073 or SLA5074 at a temperature of 100 degrees Celsius or less under worst-case conditions. Please refer to the product specifications for the details of SLA5073 and SLA5074.

Precautions for Use

Noise If a noise is superimposed on $V_{CC}2$ or a logic input, the internal sequencer may react to the noise and a invalid sequence step may occur. Please be careful of noise generation.

Power Supply Sequence When turning off the SI-7510, it is recommended to first turn-off $V_{CC}1$. If $V_{CC}2$ is turned off first, the output stage of the SI-7510 becomes high impedance before charges accumulated on the MOSFET gates are eliminated completely. During self-discharge of charges on the MOSFET gates, the MOSFET is turned on. Please be careful of the overcurrent which occurs during this time.

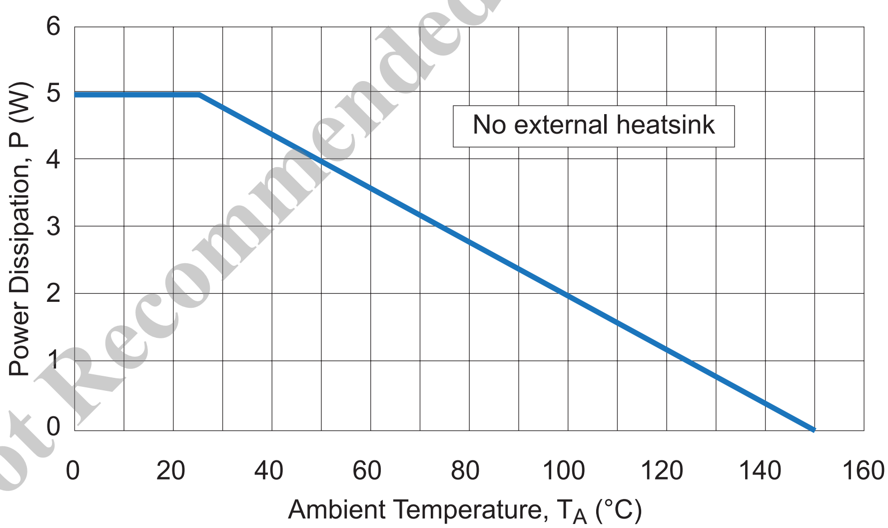


Figure 6. MOSFET power dissipation versus temperature, without heatsink

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