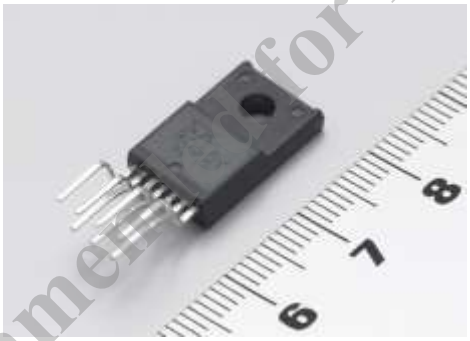
Application Note

Full Mold Chopper Type Switching Regulator IC

SI-8000Y Series



2nd Edition May 2010

SANKEN ELECTRIC CO., LTD.

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1. General Description

The SI-8000Y is a buck switching regulator IC of a current control system. Since the switching transistor includes a low ON resistance Nch MOSFET, a highly efficient DC/DC converter can be realized. In addition, the current control system is adopted to downsize the LC filter. The soft start function is also included and by connecting an external capacitor, the soft start can be set to alleviate the in-rush current at startup.

● 1-1 Features

- Compact size and large output current of 8A

  The maximum output current is 8A for the outline of TO220F class.

- High efficiency of 86% (V_{IN} = 30V / I_O = 3A)

  Heat dissipation is small due to high efficiency to allow for the downsizing of a heat sink.

- Built-in functions for overcurrent and thermal shutdown

  A current limiting type protection circuit against overcurrent and overheat is built in. (automatic restoration type)

- Soft start function (capable of ON/OFF output)

  By setting constant of an external capacitor, it is possible to delay the rise speed of the output voltage. In-rush current at startup can be alleviated. ON/OFF control of the output is also possible by connecting collector-opened transistor.

- No insulation plate required

  No insulation plate is required, when it is fitted to the heat sink, because it is of full molding type.

● 1-2 Applications

For amusements power supplies, power supplies for OA equipment, stabilization of secondary output voltage of regulator and on-board local power supplies.

● 1-3 Type

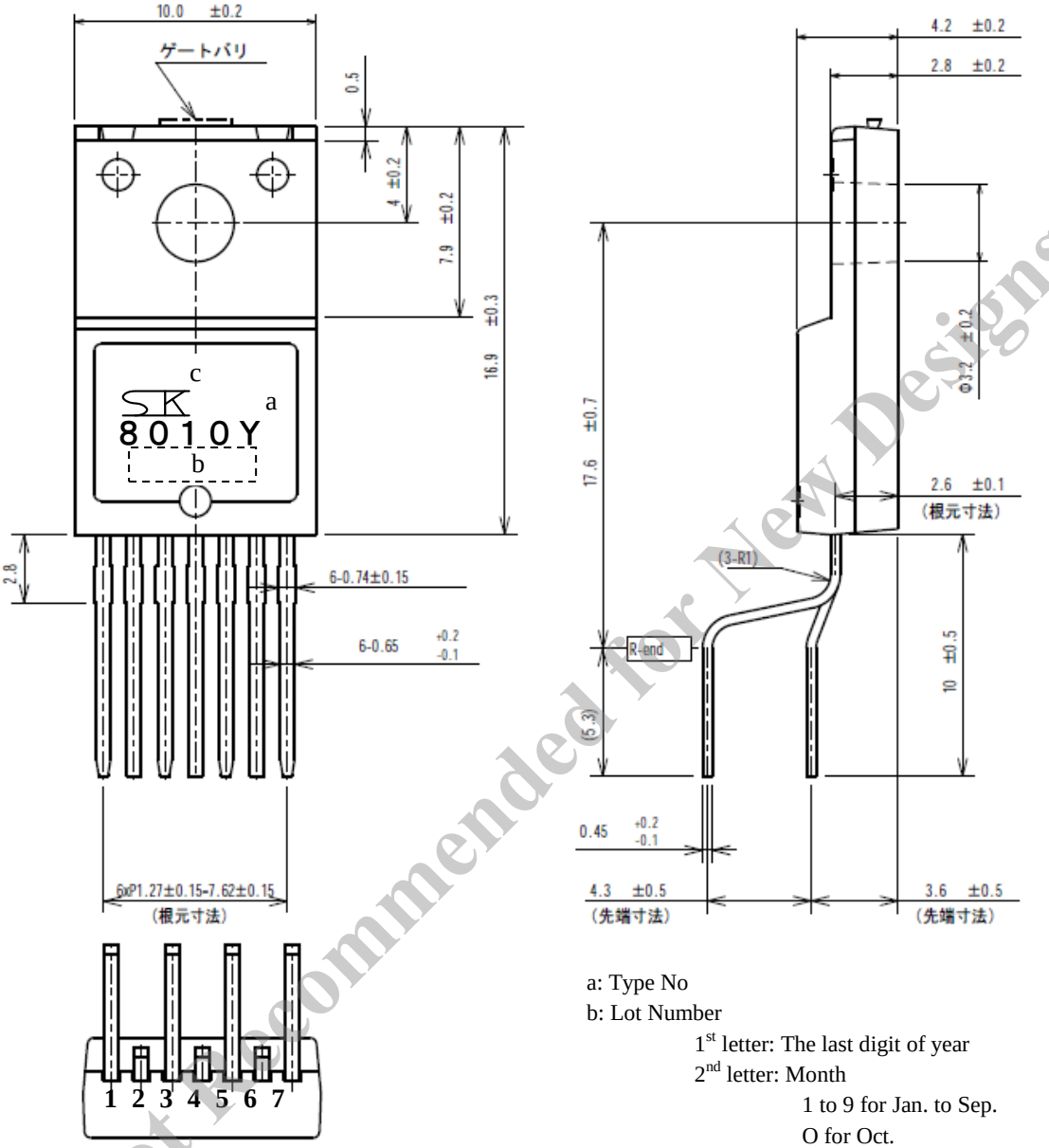
- Type: Semiconductor integrated circuits (monolithic IC)
- Structure: Resin molding type (transfer molding)

2. Specification

DWG No: TG3A-2116

● 2-1 Package Information

Unit: mm



a: Type No

b: Lot Number

1st letter: The last digit of year

2nd letter: Month

1 to 9 for Jan. to Sep.

O for Oct.

N for Nov.

D for Dec.

3rd and 4th letter: Date

01 to 31

c: Logo

Pin Assignment

1. BS
2. SW
3. IN
4. GND
5. COMP
6. FB
7. EN/SS

*1: The dimensions don't include the gate burr.

*2: It shows the dimensions measured at the top of lead.

Weight of product: about 2.3g

External Terminal Processing: Sn-3Ag-0.5Cu dipping

● 2-2 Rating

Table1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Input Voltage V_{IN} *1	VIN	4.5	V
D-S voltage on high side power MOS	BVDSS	55	V
Allowable Power Dissipation at infinite heat dissipation	Pd1	20.8	W
Allowable Power Dissipation without heat sink	Pd2	1.8	W
Junction Temperature	Tj	-30 - 150	°C
Storage Temperature	Tstg	-40 – 150	°C
Thermal resistance (Junction and case)	Θj-c	6	°C/W
Thermal resistance (Junction and ambient)	Θj-c	66.7	°C/W

*1: It is maximum applied voltage including V_{IN} serge.

Table 2 Recommended Conditions

Parameter	Symbol	Rating		Unit	Condition
		MIN	MAX		
Input Voltage	VIN	*2	43 *4	V	
Output Current	Iout	0	8.0	A	*3
Junction Temperature in Operation	Tjop	-30	135	°C	
Operation Temperature	Top	-30	85	°C	*3
Output Voltage	Vo	1	15	V	Only for SI-8010Y

*2: It is whichever higher V_{IN} = 8V or $V_{IN} = V_{OUT} \times 1.3$

*3: It should be used within the thermal derating limit.

*4: In the case of V_{IN} >40V, a snubber circuit should be provided between IN - SW and SW - GND.

Table 3 Electrical Characteristics

Parameter		Symbol	Ratings						Unit
			SI-8010Y *5			SI-8050Y			
			MIN	TYP	MAX	MIN	TYP	MAX	
Reference Voltage (Output Voltage)		VREF (Vout)	0.98	1	1.02	4.9	5	5.1	V
			V_{IN} = 30V, Io = 0.1A			V_{IN} = 30V, Io = 0.1A			
Temperature Coefficient For Reference Voltage		$\Delta V_{REF}/\Delta T$ ($\Delta Vo/\Delta T$)		±0.1			±0.5		mV/°C
			V_{IN} = 30V, Io = 0.1A, Ta = 0 - 100°C			V_{IN} = 30V, Io = 0.1A, Ta = 0 - 100°C			
Efficiency *6		η		86			86		%
			V_{IN} = 30V, Io = 3A			V_{IN} = 30V, Io = 3A			
Operational Frequency		fo		130			130		kHz
			V_{IN} = 30V, Io = 3A			V_{IN} = 30V, Io = 3A			
Line Regulation		VLine		30	90		30	90	mV
			V_{IN} = 10 - 43V, Io = 3A			V_{IN} = 10 - 43V, Io = 3A			
Load Regulation		VLoad		30	90		30	90	mV
			V_{IN} = 30V, Io = 0.1 - 8A			V_{IN} = 30V, Io = 0.1 - 8A			
Overcurrent Protection Start Current		IS	8.1			8.1			A
			V_{IN} = 20V			V_{IN} = 20V			
Circuit Current in Non-operation 1		Iq		8			8		mA
			V_{IN} = 30V, Io = 0A, $V_{EN/SS}$ = open			V_{IN} = 30V, Io = 0A, $V_{EN/SS}$ = open			
Circuit Current in Non-operation 2		Iq (off)		250	500		250	500	uA
			V_{IN} = 30V, $V_{EN/SS}$ = 0V			V_{IN} = 30V, $V_{EN/SS}$ = 0V			
EN/SS Terminal *7	Flow-out Current at Low	I_{SSL}		10	30		10	30	μA
			V_{IN} = 30V ,$V_{EN/SS}$ = 0V			V_{IN} = 30V ,$V_{EN/SS}$ = 0V			
	Low level Voltage	$V_{C/EL}$			0.5			0.5	V
			V_{IN} = 30V			V_{IN} = 30V			

*5: When Ta=25°C, Vo = 5V, R1 = 8kΩ, R2 = 2kΩ

*6: Efficiency is calculated by the following equation.

$$\eta(\%) = \frac{Vo \cdot Io}{Vin \cdot Iin} \times 100$$

*7: Pin no.7 is an EN/SS terminal and soft start can be made by connecting to a capacitor. Also, the output can be stopped by setting the EN/SS terminal voltage below V_{SSL}. The switch-over of potential of EN/SS terminal can be made by the open collector driving of the transistor.

In the case that both soft start and ON/OFF of transistor are used, since the discharge current of C6 flows across the transistor of ON/OFF, protection such as current limiting etc. should be made if the capacitance of C6 is large. The EN/SS terminal is pulled up to the internal power supply of IC therefore no external voltage can be applied. In the case of no use, the EN/SS terminal should be made open.

● 2-3 Circuit Diagram

2-3-1 Internal Equivalent Circuit

SI-8010Y

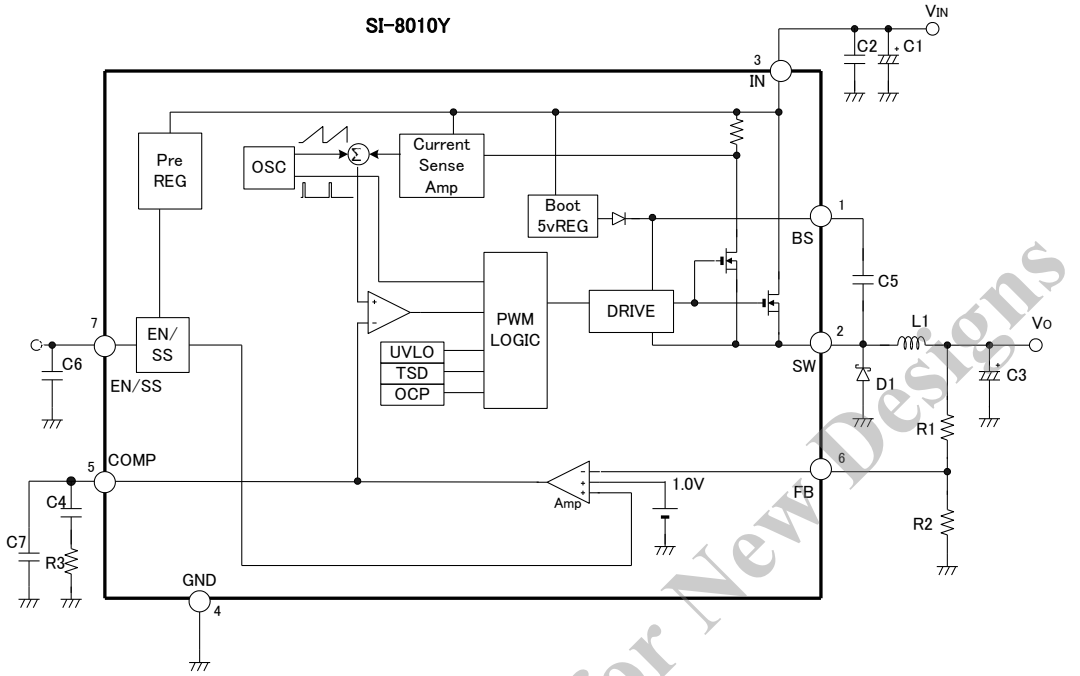


Fig.1

SI-8050Y

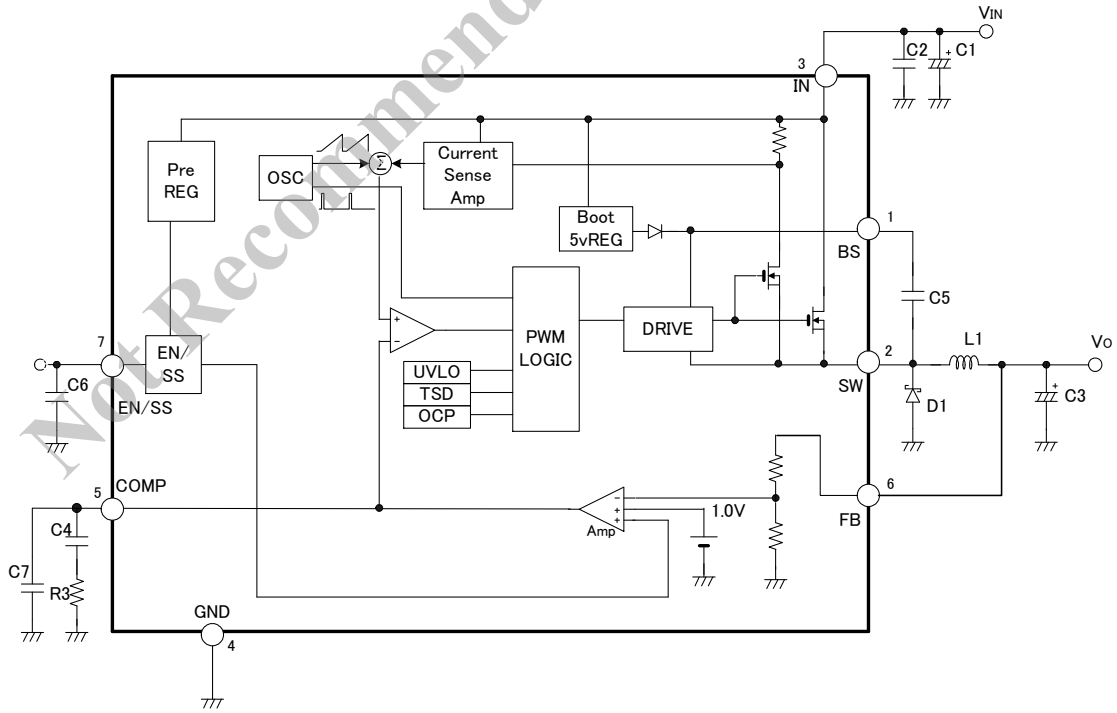


Fig.2

2-3-2 Typical Connection Diagram

SI-8010Y

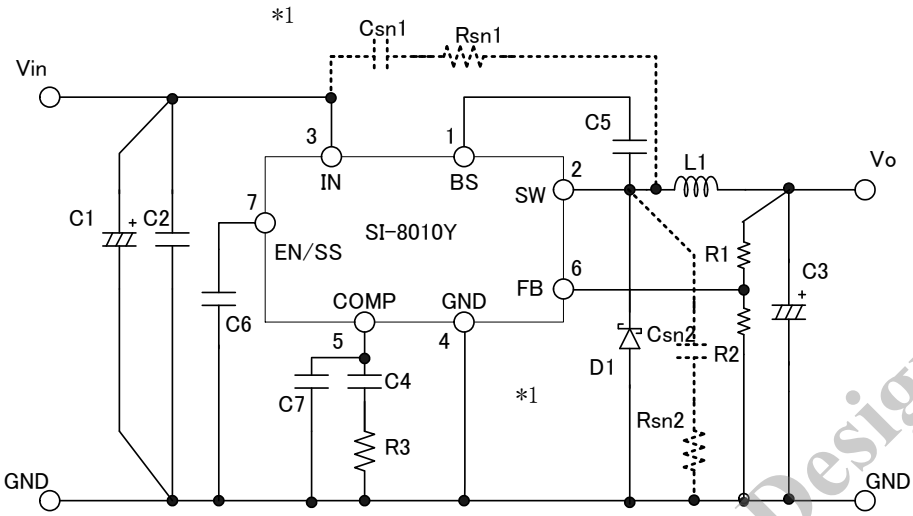


Fig.3

C1: 2200µF/50V C2: 4.7µF/50V (RPER11H475K5 by MURATA)

C3: 470µF/25V C4: 1200pF (Vo = 5V)

C5: 0.22µF/50V C6: 0.1 - 1uF

C7: 680pF (Vo = 5V) L1: 47µH

D1: FMB-26L by Sanken R1: 8kΩ (Vo = 5V)

R2: 2kΩ R3: 39kΩ (Vo = 5V)

Csn1,2 = 2200pF (VIN >40V) *1

Rsn1,2 = 10

*1 In the case of V_{IN} >40V, a snubber circuit should be provided between IN - SW and SW - GND.

SI-8050Y

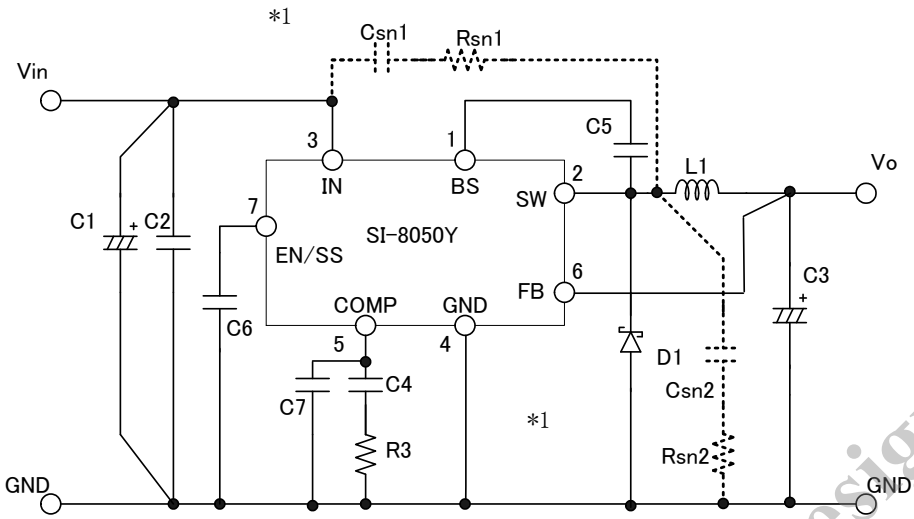


Fig.4

C1: 2200µF/50V C2: 4.7µF/50V (RPER11H475K5 by MURATA)

C3: 470µF/25V C4: 1200pF

C5: 0.22µF/50V C6: 0.1 - 1uF

C7: 680pF L1: 56µH

D1: FMB-26L by Sanken R3: 39kΩ

Csn1,2 = 2200pF (V_{IN} >40V)*1

Rsn1,2 = 10Ω (V_{IN} >40V)*1

*1 In the case of V_{IN} >40V, a snubber circuit should be provided between IN - SW and SW - GND.

3. Terminal Description

● 3-1 Terminal List

Table 4

Terminal	SI-8010Y/8050Y	
	Symbol	Description
1	BS	High side boost terminal
2	SW	Switching output terminal
3	VIN	Input terminal
4	GND	GND terminal
5	COMP	Phase compensation terminal
6	FB	Feedback voltage terminal
7	EN/SS	Soft start and ON/OFF terminal

● 3-2 Functional Description of Terminal

- BS (terminal No. 1)

  It is an internal power supply for driving the gate of high side switch Nch - MOS. A capacitor of 0.22nF (recommended) is connected between the SW terminal and BS terminal to drive the high side Nch - MOS.

- SW (terminal No. 2)

  It is a switching output terminal which supplies power to the output.

- VIN (terminal No. 3)

  It is an input voltage of IC.

- GND (terminal No. 4)

  It is a grand terminal.

- Comp (terminal No. 5)

  It is a phase compensation terminal for controlling the loop stably.

- FB (terminal No. 6)

  It is a terminal for setting the output voltage. The output voltage is set by R1 and R2 for SI-8010Y.

- EN/SS (terminal No. 7)

  A capacitor is connected to this terminal to set the soft start of output voltage. In the case that the IC is turned ON/OFF, an open collector transistor is connected to turn OFF by making it low.

4. Operational Description

● 4-1 Operational Description

The SI-8000Y is composed of an error amplifier which compares the division of resistance with the reference voltage of 1V. The current control feedback is a loop which feeds back the inductor current for PWM control and the inductor current shunted by using a sense MOS is detected by a current sense amplifier. With respect to the slope compensation, in consideration of current control system, in order to avoid the sub harmonic oscillation, slope compensation is made for the current control slope. As shown in Fig.5, in the SI-8000Y, by means of voltage control feedback, current control feedback and calculation of slope compensation, the PWM control by current control system is made.

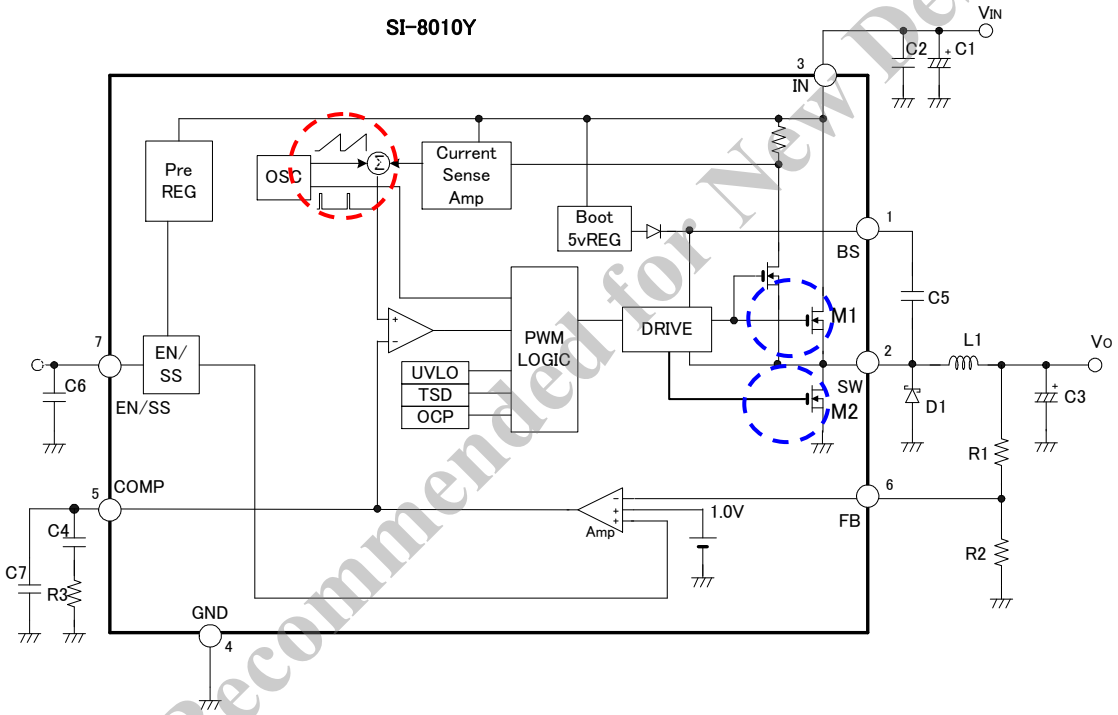


Fig.5 Current Control PWM Chopper Regulator Basic Configuration

Since the SI-8000Y is a current control regulator, the COMP terminal voltage is proportional to the peak value of the inductor current. When the ULVO is released or the EN/SS terminal exceeds the threshold value (about 1.5V), the switching operation is made. At first, switching operation is made in MIN ON duty or MAX ON duty and the high side switch (hereinafter called as M1) and the switch for BS capacitor charging (hereinafter called as M2) turn ON and OFF alternately. M1 is a switching MOS which provides power to the output, while M2 charges the capacitor C5 for boost which drives M1.

At M1: ON / M2: OFF, inductor current is increased by applying voltage to the SW switch and inductor, and the output of the current detection amplifier which detects it also rises. The signal to which the output of this current detection amplifier and the Ramp compensation signal are added is compared with the

output of the error amplifier by the current comparator (CUR COMP). When the added signal exceeds the output of the error amplifier (COMP terminal voltage), the output of the current comparator becomes “H” to reset the RS flip-flop. Then, M1 turns off and M2 turns on. Thereby, the regenerated current flows through the external SBD (D1).

In the SI-8000Y, the reset signal is generated at each cycle to reset the RS flip-flop. In the case the added signal does not exceed the COMP terminal voltage, the RS flip-flop is reset without fail by the signal of the 10% OFF Duty circuit.

● 4-2 Overcurrent Protection / Thermal Shutdown

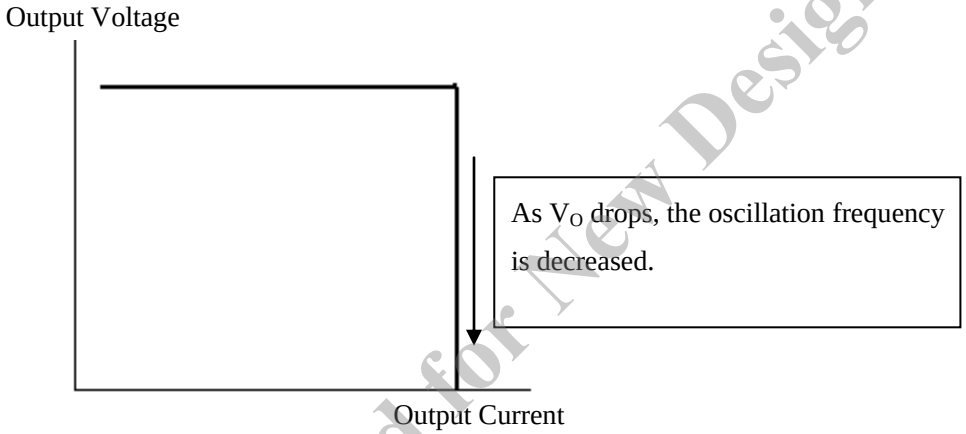


Fig.6 Output Voltage Characteristics in Overcurrent

The SI-8000Y integrates a current limiting type overcurrent protection circuit. The overcurrent protection circuit detects the peak current of a switching MOSFET and when the peak current exceeds the set value, the ON time of the transistor is compulsorily shortened to limit the current by lowering the output voltage. In addition, when the output voltage is lowered, the increase of current at low output voltage is prevented by dropping the switching frequency to about 25KHz. When the overcurrent condition is released, the output voltage will be automatically restored.

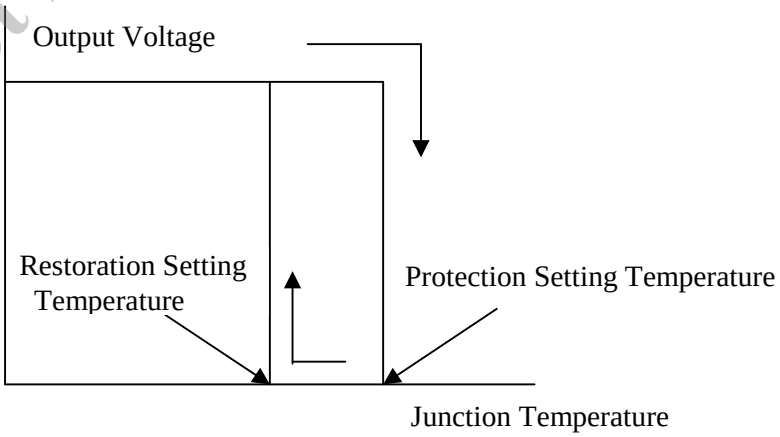


Fig.7 Output voltage Characteristics in Thermal Shutdown

The thermal shutdown circuit detects the semiconductor junction temperature of the IC and when the junction temperature exceeds the set value (around 160°C), the output transistor is stopped and the output is turned OFF. When the junction temperature drops from the set value for overheat protection by around 25°C, the output transistor is automatically restored.

* Note for thermal shutdown characteristic

This circuit protects the IC against overheat resulting from the instantaneous short circuit, but it should be noted that this function does not assure the operation including reliability in the state that overheat continues due to long time short circuit.

5. Cautions

● 5-1 External Components

5-1-1 Choke coil L1

The choke coil L1 plays a main role in the chopper type switching regulator. In order to maintain the stable operation of the regulator, such dangerous state of operation as saturation state and operation at high temperature due to heat generation must be avoided.

The following points should be taken into consideration for the selection of the choke coil.

a) The choke coil should be fit for the switching regulator.

The coil for a noise filter should not be used because of large loss and generated heat.

b) For the peak detection current control, the inductance current may fluctuate at the cycle of integral multiple of switching operation frequency.

Such phenomenon is called as sub harmonic oscillation and it may theoritically occur in the peak detection current control mode.

Therefore, in order to assure stable operation, the inductance current is compensated inside the IC, and it is required to select a proper inductance value to the output voltage.

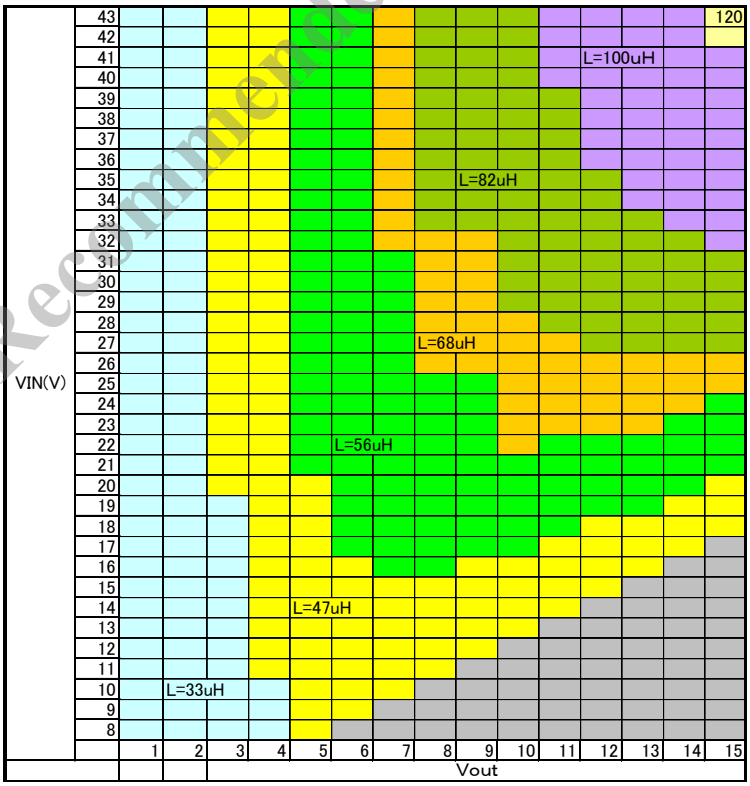


Fig.8 The selection range of the inductance L value to avoid the sub harmonic oscillation

Since the SI-8010Y sets Vout by an external resistor, it is required to optimize the inductance value subject to setting conditions.

In the SI-8050Y, when the external resistor is added to make Vout variable for rising, it is also required to adjust the inductance value.

In the case that Vo is changed, it is required to reset complementary constants (C4, C7, R3). (Refer to page 18.)

The pulse current of choke coil ΔIL and the peak current ILp are expressed by the following equation:

$$\Delta IL = \frac{(Vin - Vout) \cdot Vout}{L \cdot Vin \cdot f} \quad \text{---} \quad (A)$$

$$ILp = \frac{\Delta IL}{2} + Iout \quad \text{---} \quad (B)$$

From this equation, you will see that as the inductance L of choke coil is decreased, ΔIL and ILP are increased. In the event that the inductance is too small, the fluctuation of choke coil current is larger, resulting in unstable operation of the regulator.

Care should be taken of decrease of inductance of choke coil due to magnetic saturation of overload, load short circuit etc.

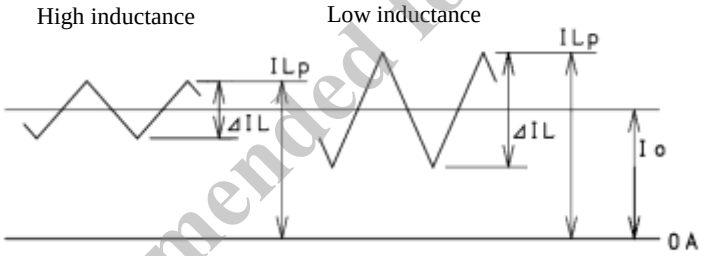


Fig.9 Relation between Ripple current I_{LP} and Output Current I_O

c) The rated current shall be met.

The rated current of the choke coil must be higher than the maximum load current to be used. When the load current exceeds the rated current of the coil, the inductance is sharply decreased to the extent that it causes saturation state at last. Please note that overcurrent may flow since the high frequency impedance becomes low.

d) Noise shall be low.

In the open magnetic circuit core which is of drum shape, since magnetic flux passes outside the coil, the peripheral circuit may be damaged by noise. It is recommended to use the toroidal type, EI type or EE type coil which has a closed magnetic circuit type core as much as possible.

5-1-2 Input Capacitor C1, C2

The input capacitor is operated as a bypass capacitor of the input circuit to supply steep current to the

regulator during switching and to compensate the voltage drop of the input side. Therefore, the input capacitor should be connected as close as to the regulator IC. Especially for C2, a ceramic capacitor or film capacitor which has good frequency characteristics should be used to be laid out near the IN – GND terminal of the product.

Even in the case that the rectifying capacitor of the AC rectifier circuit is located in the input circuit, the input capacitor cannot play a role of the rectifying capacitor unless it is connected near the SI-8000Y.

The selection of C1 shall be made in consideration of the following points:

a) The requirement of withstand voltage shall be met.

b) The requirement of the allowable ripple voltage shall be met.

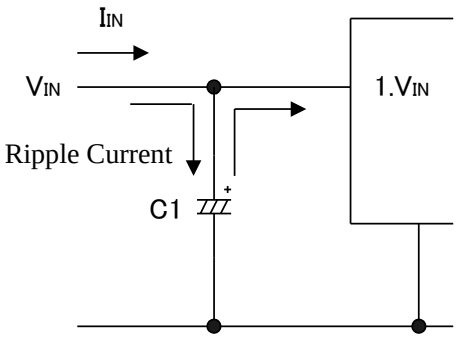


Fig.10 Current Flow of C1

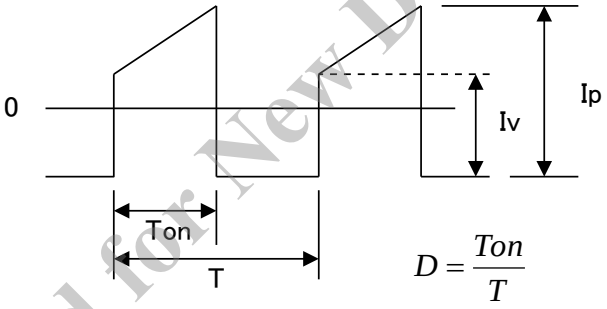


Fig. 11 Current Waveform of C1

The ripple current of the input capacitor is increased in accordance with the increase of the load current.

If the withstanding voltages or allowable ripple voltages are exceeded or used without derating, it is in danger of causing not only the decreasing the capacitor lifetime (burst, capacitance decrease, equivalent impedance increase, etc) but also the abnormal oscillations of regulator.

Therefore, the selection with sufficient margin is needed.

The effective value of ripple current flowing across the input capacitor can be calculated by the following equation (2):

$$Irms \approx 1.2 \times \frac{Vo}{Vin} \times Io \quad --(2)$$

For instance, where V_{IN} = 20V, Io = 3A and Vo= 5V,

$$Irms \approx 1.2 \times \frac{5}{20} \times 3 = 0.9A$$

Therefore, it is necessary to select the capacitor with the allowable ripple current of 0.9A or higher.

5-1-3 Output Capacitor C3

The output capacitor C3 composes a LC low pass filter together with a choke coil L1 and functions as a

rectifying capacitor of switching output.

The current equivalent to the pulse current ΔIL of the choke coil current is charged and discharged in the output capacitor.

Therefore, it is necessary to meet the requirements of withstand voltage and allowable ripple current with sufficient margin like the input capacitor.

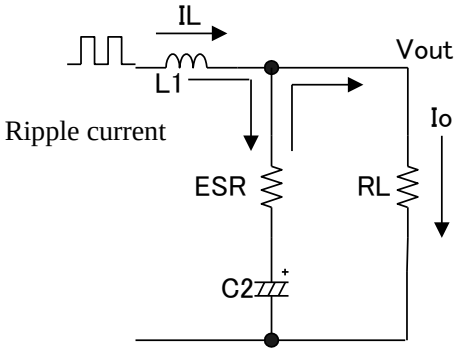


Fig.10 C3 current flow

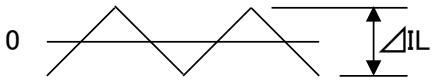


Fig.11 C3 current curve

The ripple current of the output capacitor is equal to the ripple current of the choke coil and does not vary even if the load current increases or decreases.

The ripple current effective value of the output capacitor is calculated by the equation (3).

$$Irms = \frac{\Delta IL}{2\sqrt{3}} \quad ---(3)$$

When ΔIL = 0.5A,

$$Irms = \frac{0.5}{2\sqrt{3}} \fallingdotseq 0.14A$$

Therefore a capacitor having the allowable ripple current of 0.14A or higher is required.

In addition, the output ripple voltage Vrip of the regulator is determined by a product of the pulse current ΔIL of the choke coil current (= C2 charging/discharging current) and the equivalent series resistance ESR of the output capacitor.

$$Vrip = \Delta IL \cdot C2ESR \quad ---(4)$$

It is therefore necessary to select a capacitor with low equivalent series resistance ESR in order to lower the output ripple voltage. As for general electrolytic capacitors of same product series, the ESR shall be lower, for the products of higher capacitance with same withstand voltage, or with higher withstand voltage (almost proportional to larger externals) with same capacitance.

When ΔIL=0.5A, Vrip=40mV,

$$C2esr = 40 \div 0.5 = 80m\Omega$$

As shown above, a capacitor with the ESR of 80mΩ or lower should be selected. In addition, since the ESR varies with temperature and increases at low temperature, it is required to examine the ESR at the actual operating temperatures. It is recommended to contact capacitor manufacturers for the ESR value since it is

peculiar to capacitors. However, in the case that an output capacitor with extremely small ESR (30 mΩ or less) is used, it may be used by reviewing phase compensation constants of the Comp terminal(Refer to page 18).

5-1-4 The flywheel Diode D1

The flywheel diode D1 is to discharge the energy which is stored in the choke coil at switching OFF.

For the flywheel diode, the Schottky barrier diode must be used. If a general rectifying diode or fast recovery diode is used, the IC may be damaged by applying reverse voltage due to the recovery and ON voltage.

In addition, since the output voltage from the SW terminal (pin 2) of the SI-8000Q series is almost equivalent to the input voltage, the flywheel diode with the reverse withstand voltage of the input voltage or higher should be used.

If a ferrite bead is inserted into a fly wheel Di for noise prevention, excessive negative potential will be generated, therefore please refrain from doing so by all means.

5-1-5 Phase compensation elements C4, C7, R3

The stability and responsiveness of the loop are controlled through the COMP terminal.

The COMP terminal is an output of the internal trans-conductance amplifier.

The series combination of a capacitor and resistor sets the combination of pole and zero which determines characteristics of the control system. The DC gain of voltage feedback loop can be calculated by the following equation:

$$Adc = Rl \times \mathrm{Gcs} \times \mathrm{A_{EA}} \times \frac{\mathrm{V_{FB}}}{\mathrm{Vout}}$$

Here, VFB is feedback voltage (1.0V). AEA is the voltage gain of error amplifier, G_{CS} trans-inductance of current detection and R1 a load resistance value. There are 2 important poles. One is produced by a phase compensation capacitor (C4) and an output resistor of the error amplifier.

Another one is produced by a output capacitor (C3) and a load resistor. These poles appear at the following frequencies:

$$fp1 = \frac{G_{EA}}{2\pi \times C4 \times A_{EA}}$$

$$fp2 = \frac{1}{2\pi \times C3 \times Rl}$$

Here, G_{EA} is the trans-conductance of error amplifier. In this system, one zero is important. This zero is produced by phase compensation capacitor C3 and phase compensation resistance R3. This zero appears in the following frequencies:

$$fz1 = \frac{1}{2\pi \times C4 \times R3}$$

If the output capacitor is large and/or ESR is large like an electrolytic capacitor, this system may have another important zero. This zero is produced by the ESR and capacitance of the output capacitor C3. And

it exists in the following frequencies:

$$fESR = \frac{1}{2\pi \times C3 \times RESR}$$

In this case, the third pole which is set by the phase compensation capacitor (C7) and phase compensation resistor (R3) is used to compensate the effect of ESR zero on the loop gain.

This pole exists in the following frequencies:

$$p3 = \frac{1}{2\pi \times C7 \times R3}$$

The objective of design of phase compensation is to form the converter transfer function to obtain the desired loop gain. The system crossover frequency where the feedback loop has a single gain is important. The lower crossover frequency will produce the slower line and load transient. In the meantime, the higher crossover frequency may cause instability of the system. The selection of the most suitable phase compensation element is described below.

Table 5

Parameter	Symbol	Value	Unit
Error Amplifier Voltage Gain	AEA	300	V/V
Error Amplifier Trans-conductance	GEA	800	μA/V
Current Sense Amplifier Impedance	1/GCS	0.16	V/A

1. A phase compensation resistor (R3) is selected to set the resistor at the desired crossover frequency.

The calculation of R3 is made by the following equation:

$$R3 = \frac{2\pi \times C3 \times fc}{GEA \times GCS} \times \frac{Vout}{VFB} < \frac{2\pi \times C3 \times 0.1 \times fs}{GEA \times GCS} \times \frac{Vout}{V_{FB}}$$

Here, fc is a desired crossover frequency. It should be one tenth or lower of the normal switching frequency (fs).

2. In order to achieve the desired phase margin, a phase compensation capacitor (C4) is selected.

For the application having a representative inductance value, adequate phase margin is provided by setting the zero compensation of one fourth or lower of the crossover frequency.

C4 is calculated by the following equation.

$$C4 > \frac{4}{2\pi \times R3 \times fc}$$

R3 is a phase compensation resistor.

3. It is required to judge whether the second compensation capacitor C7 is necessary or not.

It will be necessary, when the ESR zero of the output capacitor is located at a frequency which is lower than the half of the switching frequency.

Namely, it is necessary, when the following equation is applicable.

$$\frac{1}{2\pi \times C3 \times RESR} < \frac{fs}{2}$$ (C3: capacitance of output capacitor)

In this case, the second compensation capacitor C7 is added and the frequency fp3 of ESR zero is set.

C6 is calculated from the following equation.

$$C7 = \frac{C3 \times RESR}{R3}$$

5-1-6 Example of calculation of C4, C7 and R3

- Calculation of R3

R3 is calculated by the following equation.

$$R3 = \frac{2\pi \times C3 \times fc}{GEA \times GCS} \times \frac{Vout}{VFB}$$

From Table 5,

GEA: 800×10^{-6} , GCS: 6.25 (reciprocal number of 1/GCS = 0. 16)

fc: 13×10^{3} (1/10 of oscillating frequency)

C3: capacitance of output capacitor, V_{OUT}: set Vo, VFB: 1V

When $C_O = 560\mu F$ at $V_O = 5V$,

$R3 = \{ (2 \times 3.14 \times 560 \times 10^{-6} \times 13 \times 10^{3}) / (800 \times 10^{-6} \times 6.25) \} \times (5/1)$

$= 45.718k\Omega$

As an approximated value, it is 43kΩ which is less than the calculated value.

- Calculation of C4

$$C4 > \frac{4}{2\pi \times R3 \times fc}$$

$C4 = 4 / (2 \times 3.14 \times 43 \times 10^{3} \times 13 \times 10^{3}) = 1139 \times 10^{-12}$

$= 1139pF$

As an approximated value, it is 1200pF or so which is larger than the calculated value.

- Calculation of C7

$$C7 = \frac{C3 \times RESR}{R3}$$ RESR: ESR of C3 (C_{OUT})

When calculated as C3 = 560μF and assumed as RESR = 50mΩ

$C7 = (560 \times 10^{-6} \times 0.05) / 43 \times 10^{3} = 651 \times 10^{-12}$

$= 651pF$

As an approximated value, it is 680 pF or so which is more than the calculated value.

The constants for each output setting voltage in the case that aluminum electrolytic capacitors are used are shown in the following table.

Reference Comp terminal phase compensation constants (C4, C7, R3)

Table 6 Constants for each setting voltage (C_O = 470μF)

Vo (V)	R3 (kΩ)	C4 (pF)	C7 (pF)
3.3	27	2000	1000
5	39	1200	620
9	68	680	340
12	91	580	255

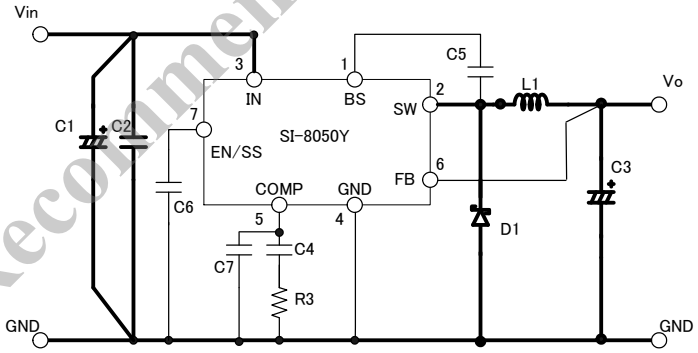
Table 7 Constants for each setting voltage (C_O = 1000μF)

Vo (V)	R3 (kΩ)	C4 (pF)	C7 (pF)
3.3	54	1000	1000
5	82	620	620
9	150	330	360
12	200	270	270

● 5-2 Pattern Design Notes

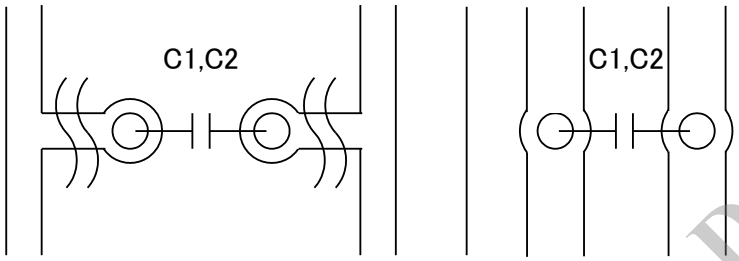
5-2-1 High Current Line

Since high current flows in the bold lines in the connection diagram, the pattern should be as wide and short as possible.



5-2-2 Input/ Output Capacitor

The input capacitor C1, C2 and the output capacitor C3 should be connected to the IC as close as possible. If the rectifying capacitor for AC rectifier circuit is on the input side, it can be used as an input capacitor. However, if it is not close to the IC, the input capacitor should be connected in addition to the rectifying capacitor. Since high current is discharged and charged through the leads of input/output capacitor at high speed, the leads should be as short as possible. A similar care should be taken for the patterning of the capacitor.



Improper Pattern Example Proper Pattern Example

● 5-3 Output Voltage Setting

5-3-1 Output Voltage Setting for SI-8010Y

The FB terminal is a feedback detection terminal for controlling the output voltage. It is recommended to connect it as close as possible to the output capacitor C3. When they are not close, the abnormal oscillation may be caused due to the poor regulation and increase of switching ripple.

Since the SI-8010Y is of variable type, the output voltage set-up is achieved by connecting R1 and R2.

I_{SENSE} should be set to be around 2mA.

(The I_{SENSE} lower limit is 1.6mA, and the upper limit is not defined. However, it is necessary to consider that the consumption current shall increase according to the I_{FB} value, resulting in lower efficiency.)

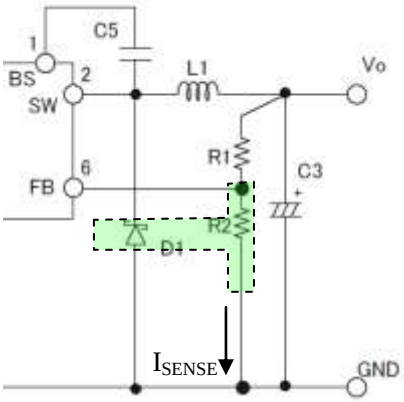
R1, R2 and output voltage are calculated from the following equations:

$I_{SENSE} = V_{FB} / R2$ (V_{FB} = 1.0V ±2%)

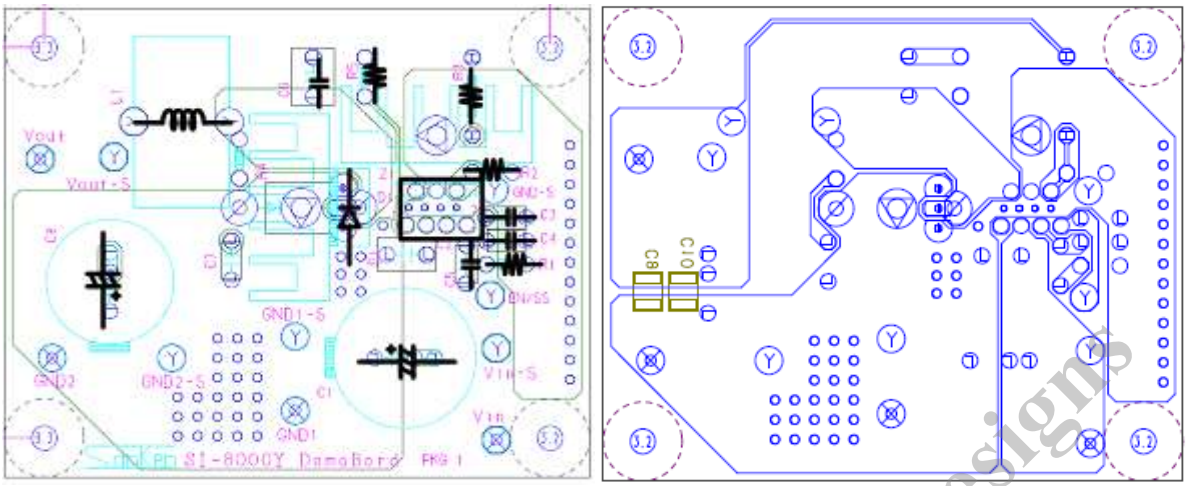
$R1 = (Vo - V_{FB}) / I_{SENSE}$, $R2 = V_{FB} / I_{SENSE}$

$Vout = R1 \times (V_{FB} / R2) + V_{FB}$

The wiring of FB terminal, R1 and R2 that run parallel to the flywheel diode should be avoided, because switching noise may interfere with the detection voltage to cause abnormal oscillation. It is recommended to implement the wiring from the FB terminal to R1 and R2 as short as possible.



- Mounting Board Pattern Example



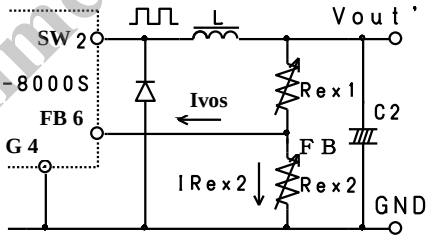
Recommended pattern　　Backside GND plane

*It is so important in term of the pattern design to lay out C2 and D1 near the product.

*For optimum operation conditions, the GND line shall be wired at one point, centered on No. 4 terminal and each part shall be wired in the shortest distance.

5-3-2 Variable Output Voltage for SI-8050Y

Even for SI-8050Y with fixed output voltage, the output voltage can be increased by adding a resistor to the No. 6 FB terminal (not applicable to voltage drop).



The output voltage adjustment resistors Rex1 and 2 are calculated by the following equation.

$$\mathrm{Re}\,x1 = \frac{Vout' - Vos}{S \cdot IV_{FB}}$$

$$\mathrm{Re}\,x2 = \frac{V_{FB}}{(S-1) \cdot IV_{FB}}$$

S: Stability coefficient

Stability coefficient S means the ratio of Rex 2 to the FB terminal in-flow current Ivos. The larger is S, the more is the variation of temperature characteristic and output voltage improved. (Normally, about 5 - 10)

I_{VOS} on SI-8050Y should be 1mA ±20%.

The tolerance of the output voltage including variation of Rex 1, Rex 2, Ivos, V_{FB} is shown below.

- Maximum output voltage (Vout MAX)

$$Vout'MAX = V_{FB}MAX + Rex1MAX\left(\frac{V_{FB}MAX}{Rex2MIN} + IvosMAX\right)$$

V_{FB}MAX: The maximum value of set output voltage. The MAX value of set output voltage should be put, shown in the electrical characteristics of the specifications.

Rex1MAX: The maximum value of Rex1. It is obtained from the tolerance of the resistor.

Rex2 MIN: The minimum value of Rex2. It is obtained from the tolerance of the resistor.

IvosMAX: The maximum in-flow current of FB terminal, 1.2mA

- The minimum output voltage (VoutMIN)

$$Vout'MIN = V_{FB}MIN + Rex1MIN\left(\frac{V_{FB}MIN}{Rex2MAX} + IvosMIN\right)$$

V_{FB}MIN: The minimum value of the set output voltage. Please fill in the MIN value of the set output voltage which is shown in the electrical characteristics of the specifications.

Rex1 MIN: The minimum value of Rex1. It will be obtained from the tolerance of the resistor.

Rex2MAX: The maximum value of Rex2. It will be obtained from the tolerance of the resistor.

IvosMIN: The minimum in-flow current of FB terminal, 0.8mA.

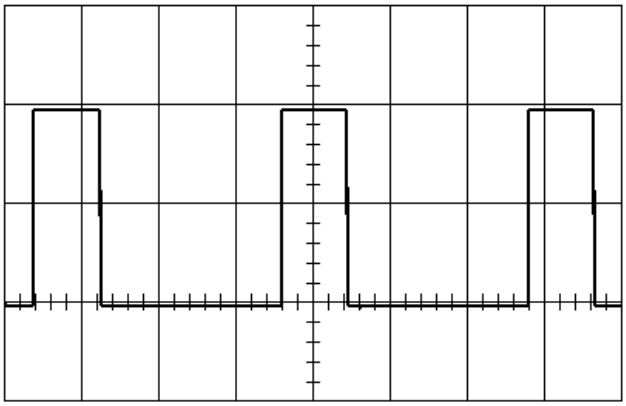
In the case of V_O = 12V, Rex2 = 1250Ω, Rex1 = 1400Ω based on equation above.

● 5-4 Operation Waveform Check

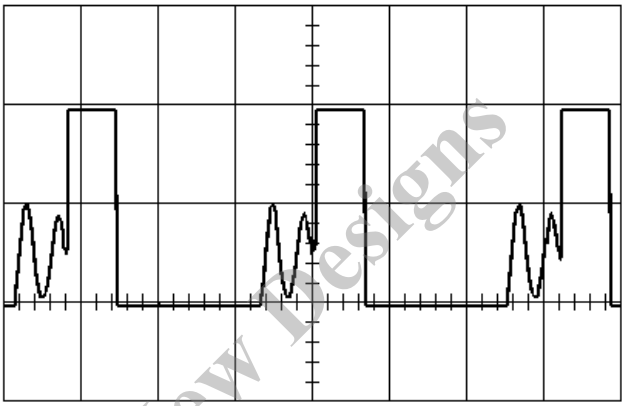
It can be checked by the waveform between the pin 2 and 4 (waveform between SW and GND) of the SI-8000Y whether the switching operation is normal or not.

The examples of waveforms at normal and abnormal operations are shown below:

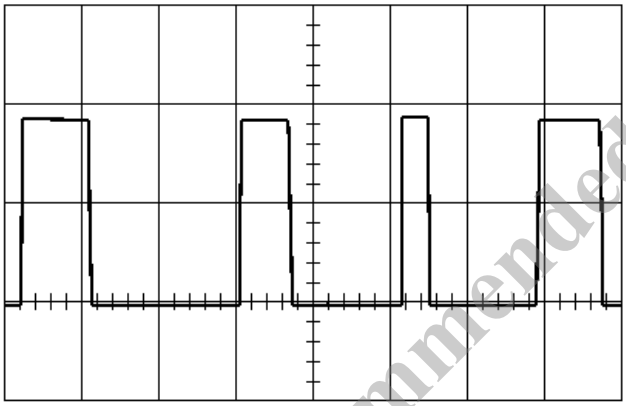
1. Normal Operation (continuous area)



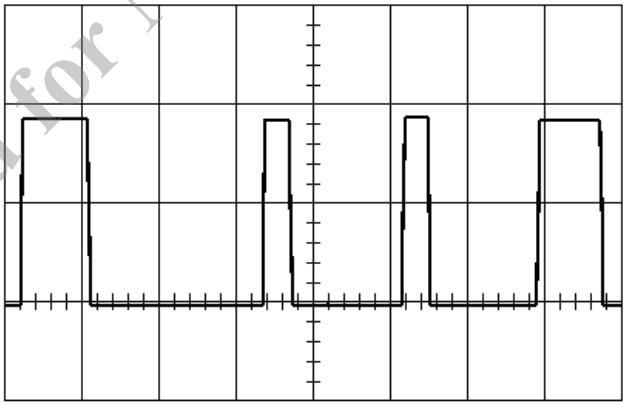
2. Normal Operation (discontinuous area)



3. When C1 is distant from IC



4. When C3 is distant from IC



The continuous area is an area where the DC component of the triangular wave is superimposed on the current flowing across the choke coil and the discontinuous area is an area where the current flowing across the choke coil is intermittent (a period of zero current may happen.) because the current flowing across the choke coil is low.

Therefore, when the load current is high, the area is a continuous area and when the same current is low, the area is a discontinuous area.

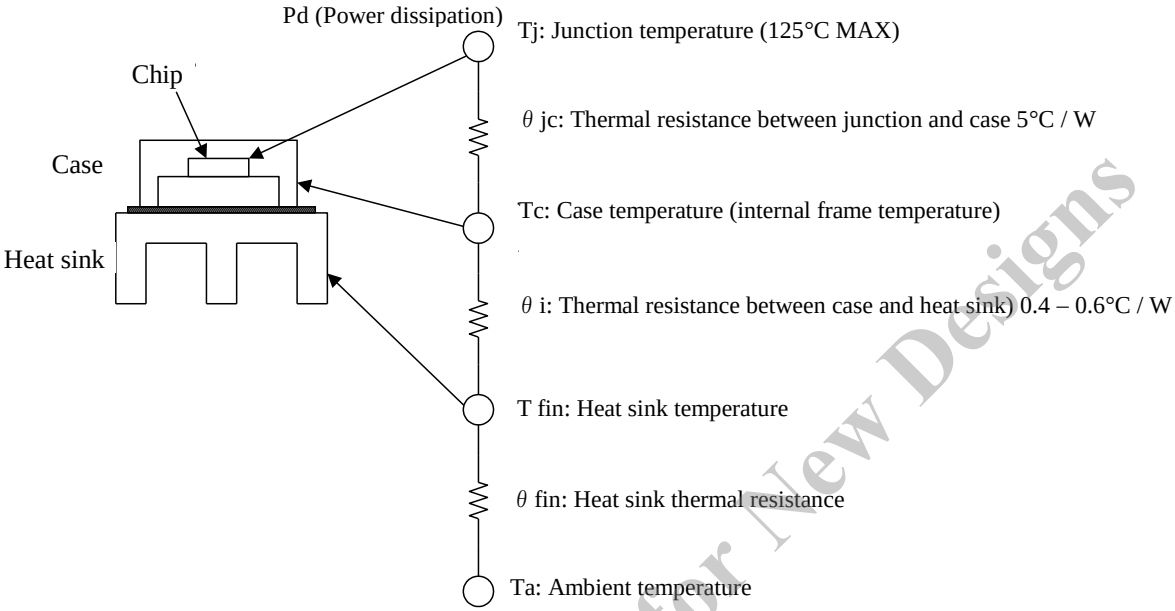
In the continuous area, the switching waveform is formed in the normal rectangular waveform (waveform 1) and in the discontinuous area, damped oscillation is caused in the switching waveform (waveform 2), but this is a normal operation without any problem.

In the meantime, when the IC is far from C1, C2 and C3, jitter which disturbs the ON – OFF time of switching will happen~~,~~ as shown in the waveforms (3, 4). As described above, C1, C2 and C3 should be connected close to the IC.

● 5-5 Thermal Design

5-5-1 Calculation of Heat Dissipation

The relation among the power dissipation Pd of regulator, junction temperature Tj, case temperature Tc, heat sink temperature Tfin and ambient temperature Ta is as follows:



$$Pd = \frac{Tj - Tc}{\theta jc}$$

$$Pd = \frac{Tj - Tfin}{\theta jc + \theta i}$$

$$Pd = \frac{Tj - Ta}{\theta jc + \theta i + \theta fin}$$

The TjMAX is an inherent value for each product, therefore it must be strictly observed. For this purpose, it is required to design the heat sink in compliance with PdMAX, TaMAX (determination of θfin). The heat derating graphically describes this relation.

The designing of the heat sink is carried out by the following procedure:

1) The maximum ambient temperature Ta MAX in the set is obtained.

2) The maximum power dissipation PdMAX is obtained.

$$Pd = VOUT \cdot Io\left(\frac{100}{\eta x} - 1\right) - Vf \cdot Io\left(1 - \frac{VOUT}{VIN}\right)$$

* ηx= efficiency (%), Vf= diode forward voltage

3) The size of heat sink is determined from the intersection of the heat derating.

The required thermal resistance of the heat sink can be also calculated. The thermal resistance required for the heat sink is obtained by the following equation:

$$\theta i + \theta fin = \frac{Tj - Ta}{Pd} - \theta jc$$

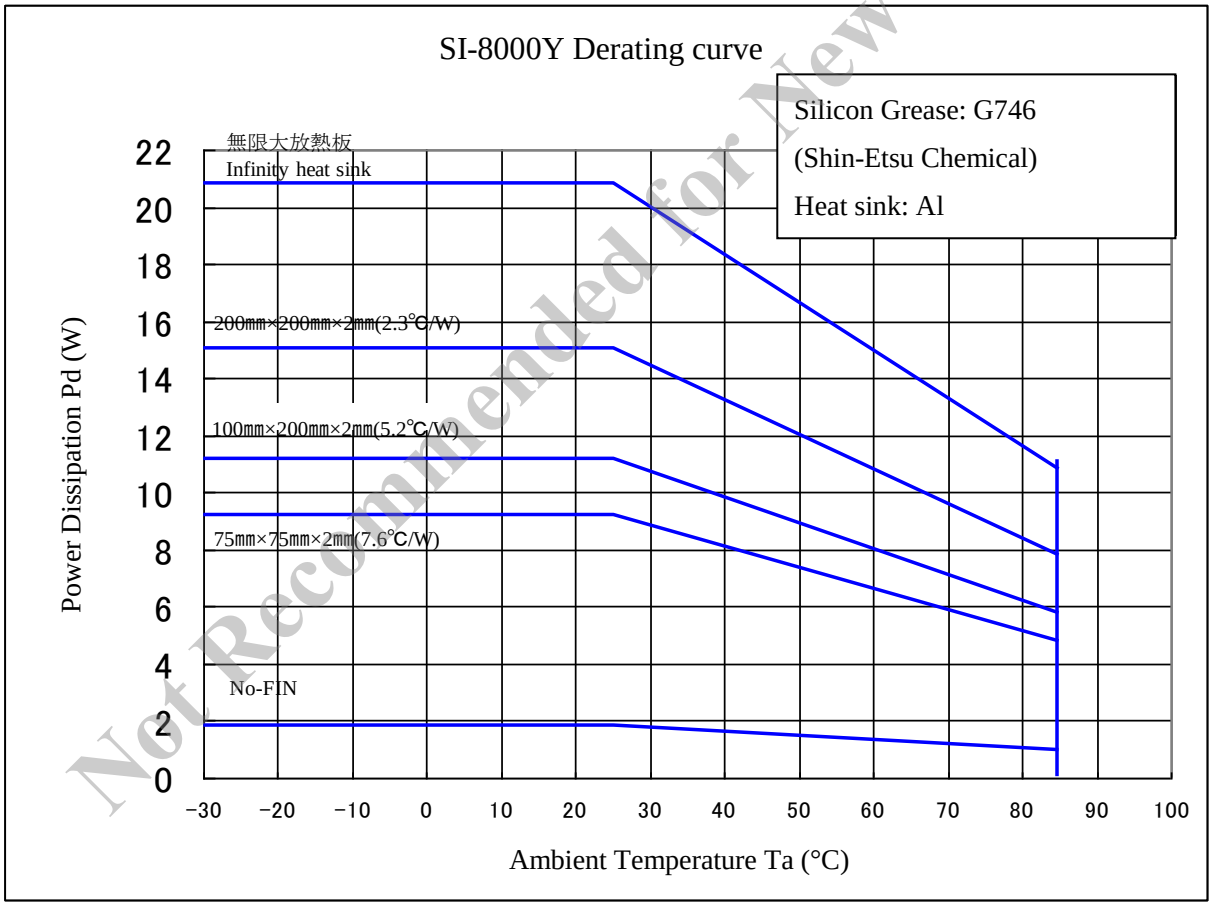
An example of heat calculation for using SI-8010Y under the conditions of V_{IN} = 20V, Io = 6A and Ta = 60°C is shown below.

Where efficiency η = 87.5%, Vf = 0.55V from the typical characteristics, when calculated as Tjmax = 125°C,

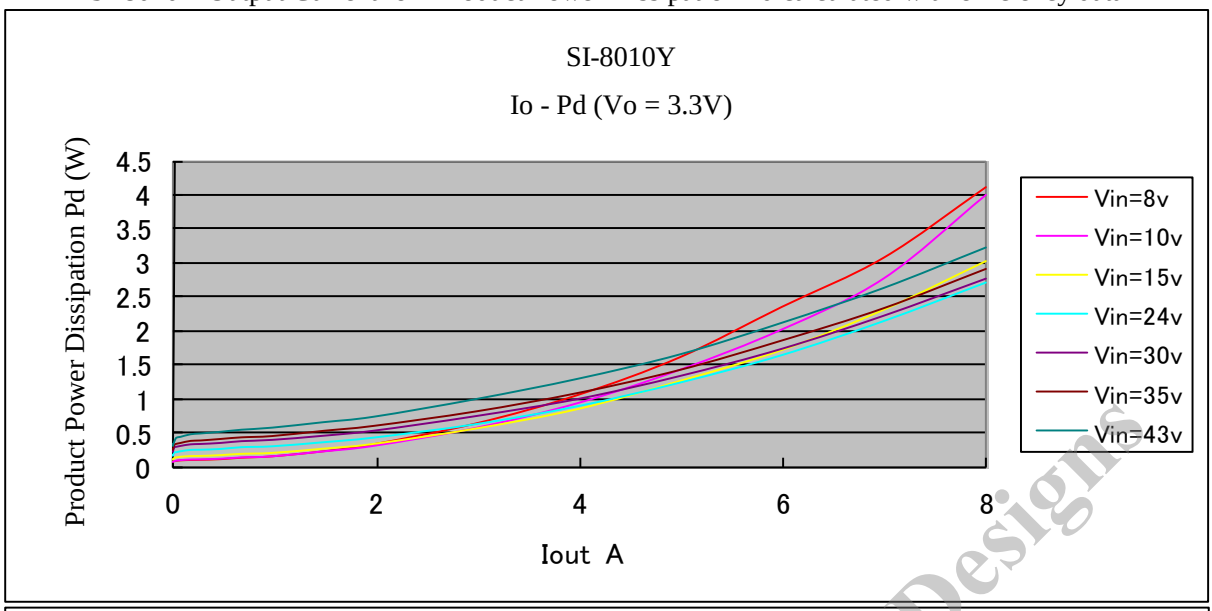
$$Pd = 5 \times 6 \times \left(\frac{100}{87.5} - 1 \right) - 0.55 \times 6 \times \left(1 - \frac{5}{20} \right) \fallingdotseq 1.81W$$

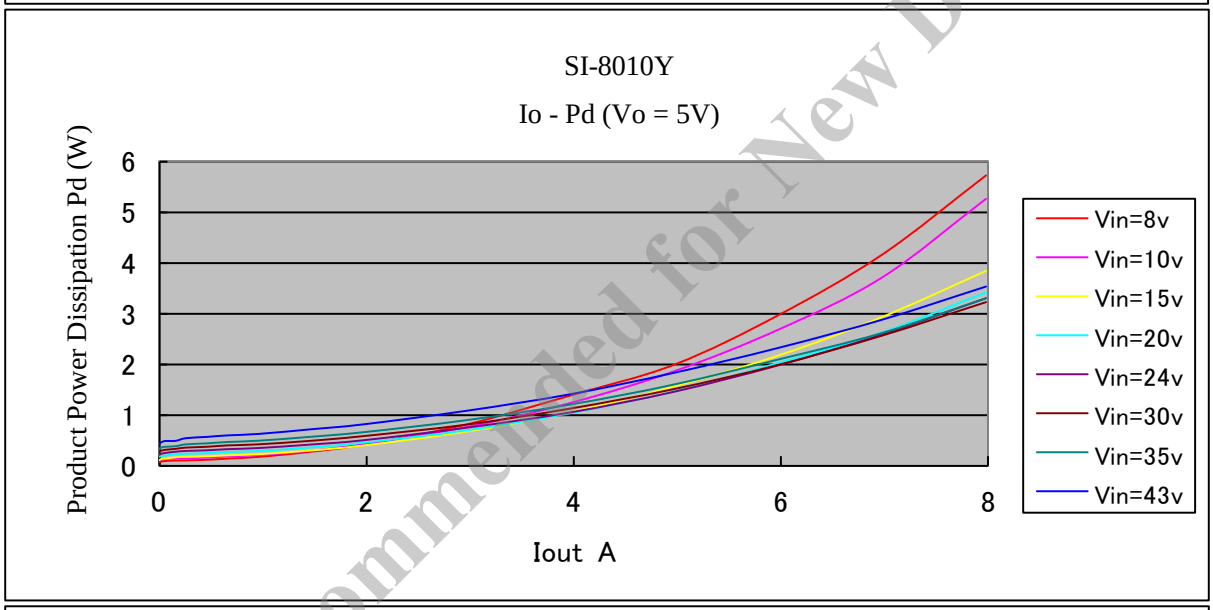
$$\theta fin = \frac{125 - 60}{1.81} - 6 \fallingdotseq 30^{\circ} C/W$$

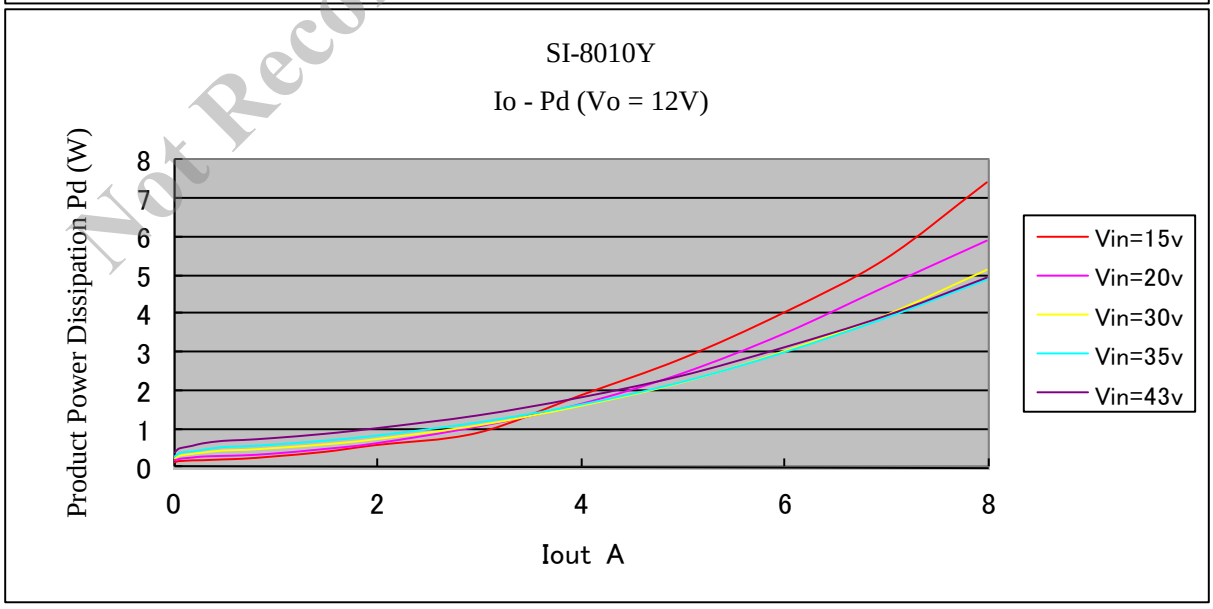
As a result, the heat sink with the thermal resistance of 30°C /W or less is required. As described above, the heat sink is determined, but the derating of 10 - 20% or more is used. Actually, heat dissipation effect significantly changes depending on the difference in component mounting. Therefore, heat sink temperature or case temperature should be checked with the heat sink mounted.



SI-8010Y Output Current Io – Product Power Dissipation Pd calculated with efficiency data







5-5-2 Installation to Heat sink

Selection of silicon grease

When the SI-8000Y is installed to the heat sink, silicon grease should be thinly and evenly coated between the IC and heat sink. Without coating, thermal resistance is significantly increased because of contact failure due to micro concavity/convexity between the backside of the IC and the surface of the heat sink to accelerate the heating of the IC, resulting in shorter life of the IC.

In some kind of silicon grease to be used, oil component may be separated to penetrate into the IC, resulting in the deformation of packages or the adverse effect on built-in elements.

Any other silicon grease than one based on the modified silicon oil shall not be used.

The recommended silicon greases are as follows:

Sanken's recommended silicon greases:

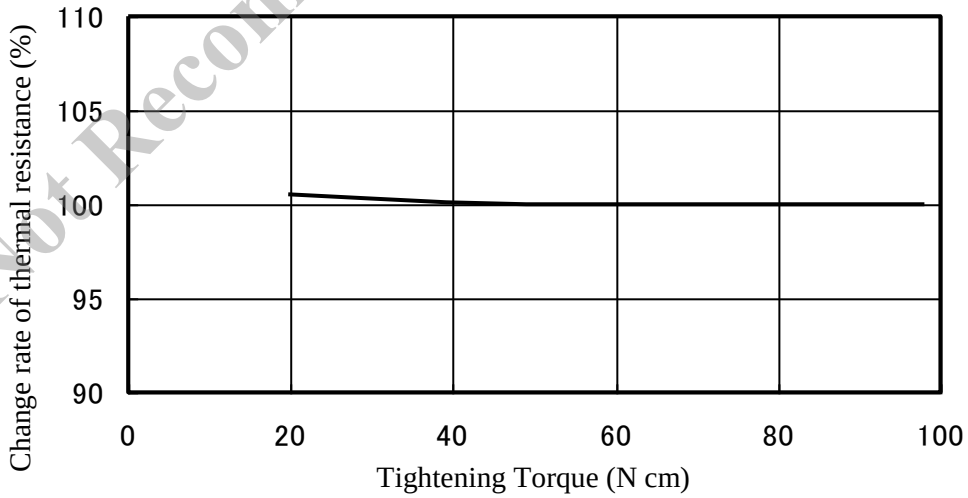
Types	Suppliers
G746	Shin-Etsu Chemical Co., Ltd.
SC102	Toray Silicone Co., Ltd.
YG6260	Momentive Performance Materials Inc.

Tightening torque of fixing screws

In order to keep the thermal resistance between the IC and the heat sink at low level without damaging the IC package, it is necessary to control the torque of fixing screws in a proper way.

Even if silicon grease is coated, the thermal resistance θi increases if the tightening torque is not enough.

For the SI-8000Y, 58.8 - 68.6Ncm (6.0 - 7.0 kg cm) are recommended.



* 1. The change rate of thermal resistance in the case that 58.8N cm (6kg cm) is expressed as 100% is shown above.

* 2. The silicon grease G746 shall be used.

6. Applications

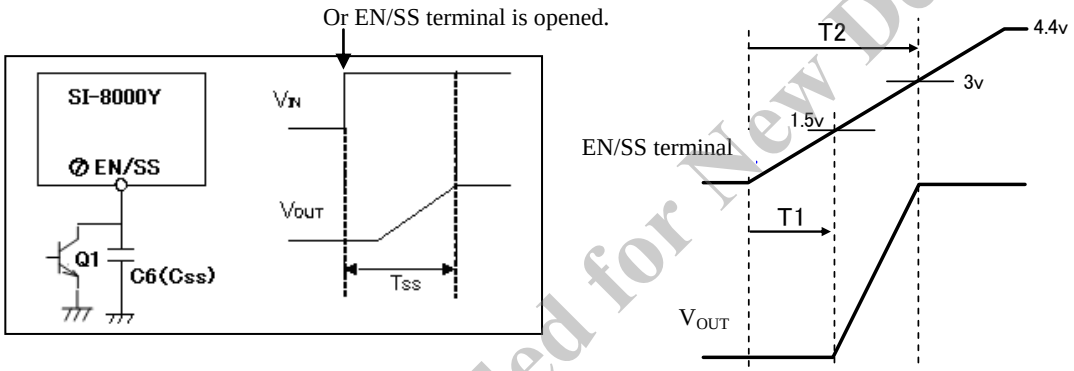
● 6-1 Soft Start

When a capacitor is connected to terminal 7 (EN/SS), the soft start is activated when the input voltage is applied or EN/SS terminal is opened. Unless soft start is applied, excessive in-rush current will flow at startup, therefore it is recommended to set soft start without fail.

V_{OUT} rises in relation with the charging voltage of Css when soft start is activated. Therefore, the rough estimation of enable time is done by the time constant calculation of Css charging.

The capacitor Css controls the rise time by controlling the OFF period of PWM control. The rise time tss is calculated approximately by the following equation:

$$tss = (Css \times Vss) / IssL \ (sec)$$



Since the EN/SS terminal is pulled up (4.4V TYP) with the internal power supply of IC, the external voltage can not be applied.

In the SI-8000Y, V_{OUT} starts rising, when the voltage of EN/SS terminal is about 1.5V and when it goes up to about 3V, it does not rise any more.

It takes longer to discharge C_{SS} after turning V_{IN} off if capacitance of C_{SS} is increased. The discharge of C_{SS} is made, when Q1 is ON or V_{IN} falls to 0V. It is recommended to use C_{SS} at the value of about 10μF or less.

$I_{SS}L$: Charging current of C_{SS} {10μA or so (real value)}

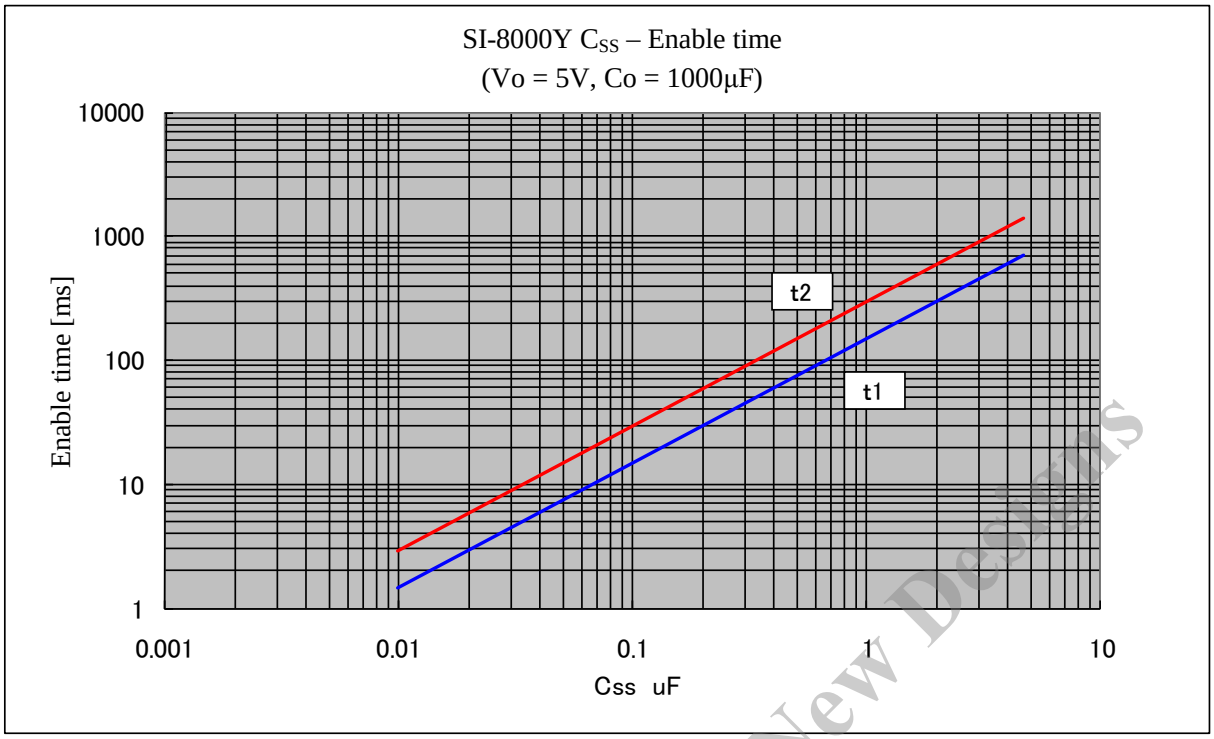
$V_{SS}A$: Voltage at which C_{SS} rises and V_{OUT} is stabilized (about 3V)

$V_{SS}B$: Voltage at which C_{SS} rises and V_{OUT} starts rising (about 1. 5V)

C_{SS}: Capacitance of capacitor connected to SS terminal

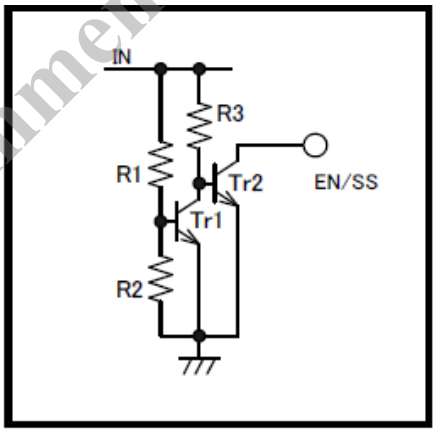
T1 = (C_{SS} x $V_{SS}B$)/ISSL (sec) The time from release of terminal to start of rising

T2 = (C_{SS} x $V_{SS}A$)/IAAL (sec) The time from release of terminal to startup of V_{OUT}



In the case that a transistor Q1 for ON/OFF control is not connected, CSS is discharged from the IN terminal, when Vin falls. Therefore, in the case of restart (rise of Vin) after fall of Vin and drop of Vo, but prior to the complete drop of Vin, the discharge of Css is not made and the soft start may not be applied.
This situation can be resolved by connecting a discharge circuit as shown in the below figure.

Circuit of Discharging C_{SS}

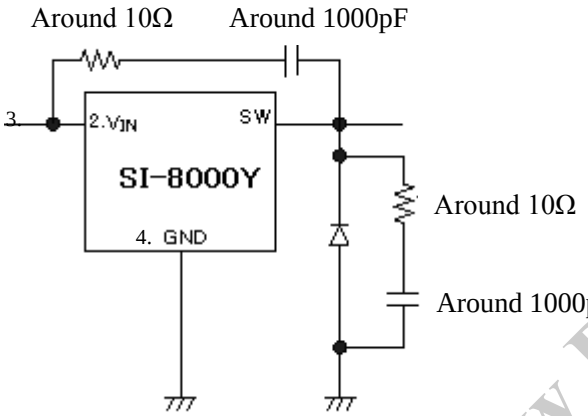


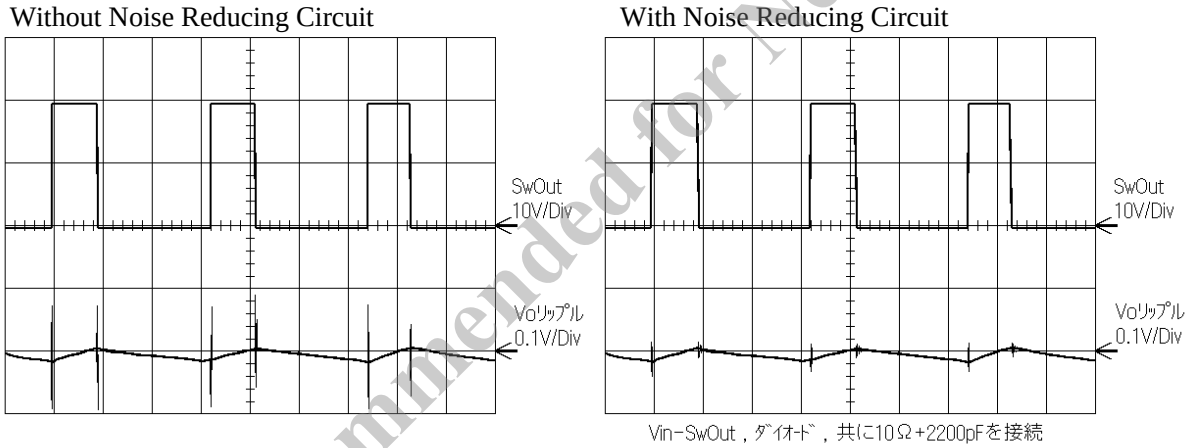
● 6-2 Output ON/ OFF Control

The output ON / OFF control is possible using the EN/SS (No.7) terminal. The output is turned OFF when the terminal 5 voltage falls below V_{SSL} (0.5V) by opening collector or so.
Since the EN/SS terminal is pulled up (4.4V TYP) with the internal power supply of IC, the external voltage cannot be applied.

● 6-3 Spike Noise Reduction

In order to reduce the spike noise, it is possible to compensate the output waveform of the SI-8000Y and the recovery time of the diode by a capacitor, but it should be noted that the efficiency is also slightly reduced.

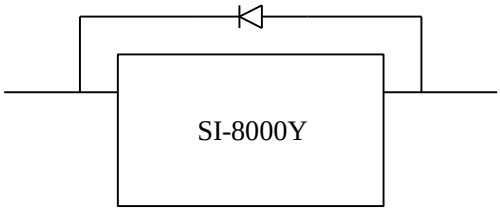




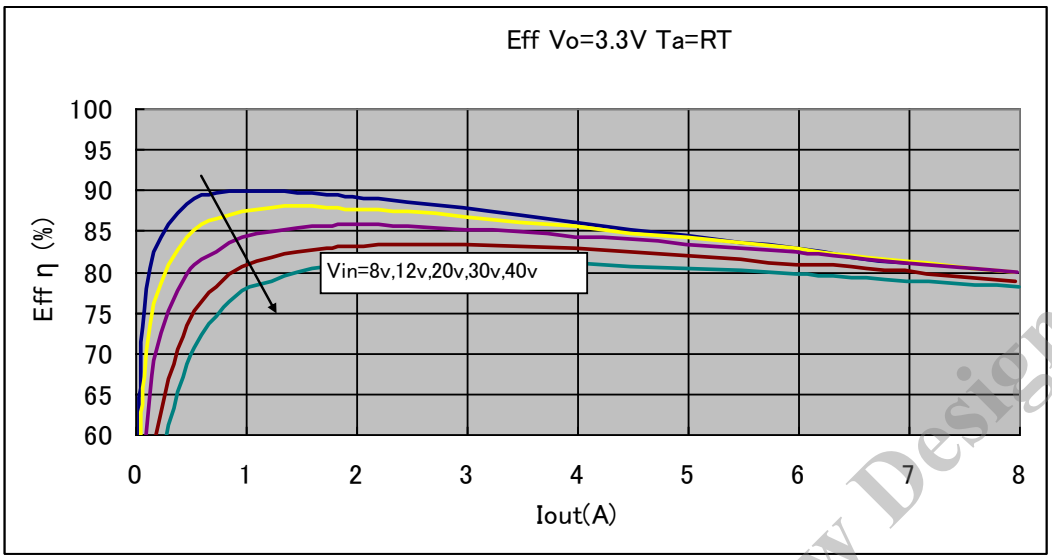
*When the spike noise is observed with an oscilloscope, the lead wire may function as an antenna and the spike noise may be observed extremely higher than usual because the probe GND lead wire is long. In order to monitor spike noise, it is necessary to disconnect the lead wire of probe and connect wire to the base of the output capacitor by soldering for measurement.

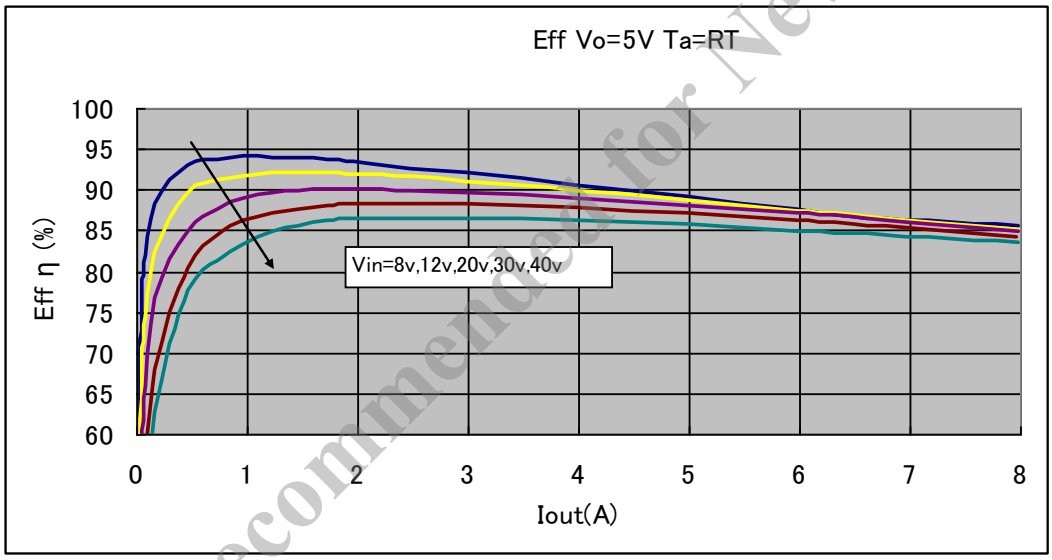
● 6-4 Reverse Bias Protection

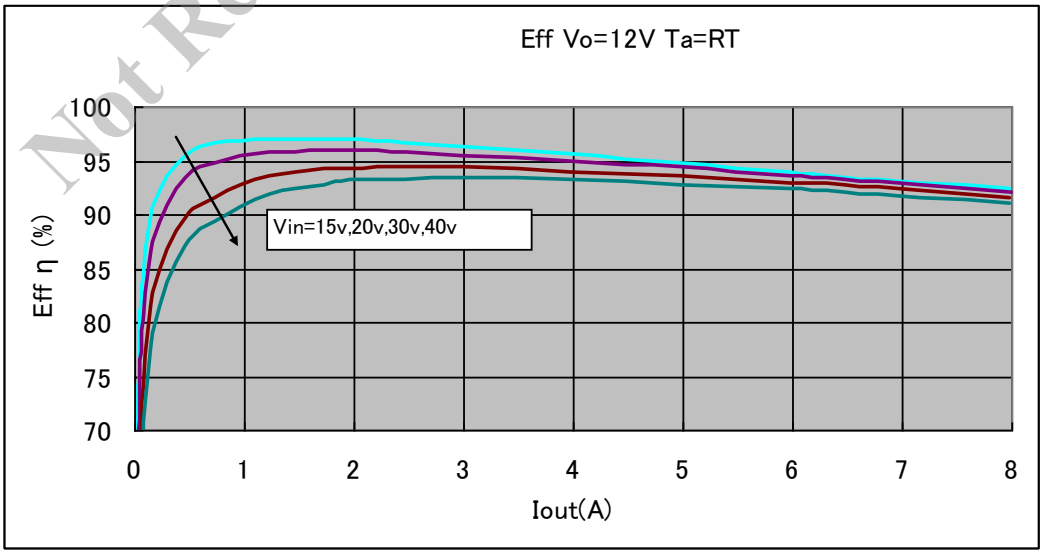
A diode for reverse bias protection will be required between input and output when the output voltage is higher than the input terminal voltage, such as in battery chargers.



7. Typical Characteristics

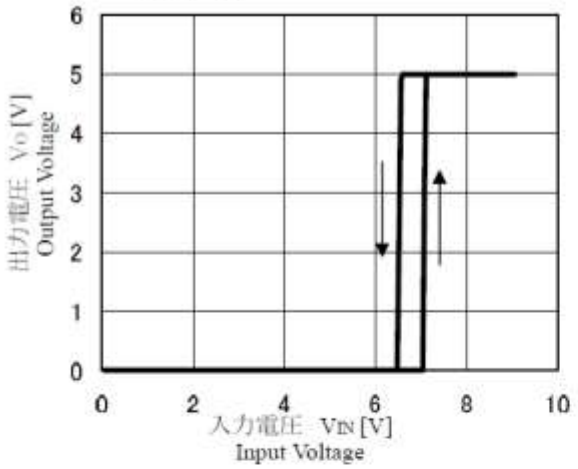




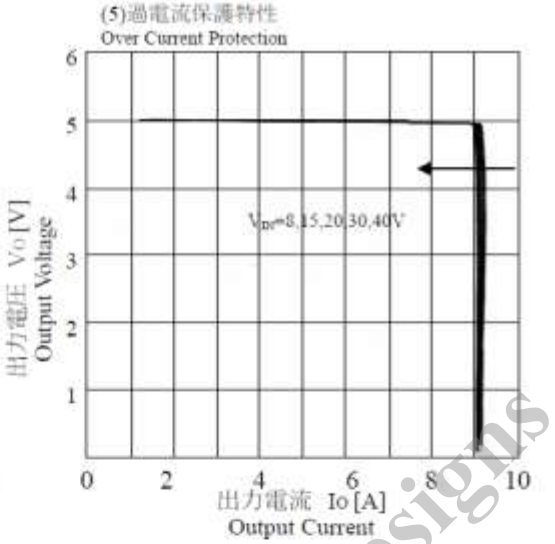


Ta = 25°C, R2 = 2kΩ at Vo = 5V if no specific comment

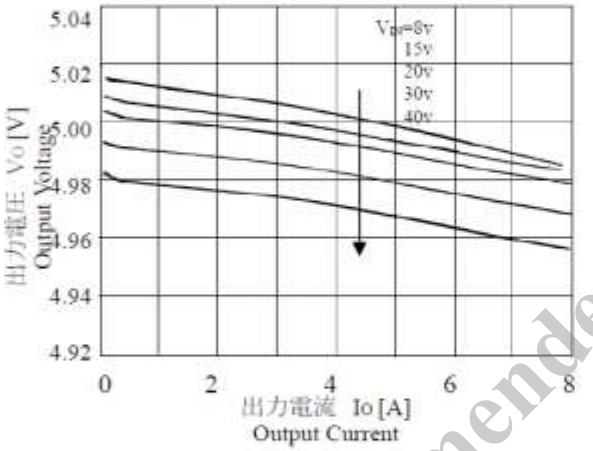
(2)出力電圧立上り Load=CR
Vin vs Vo



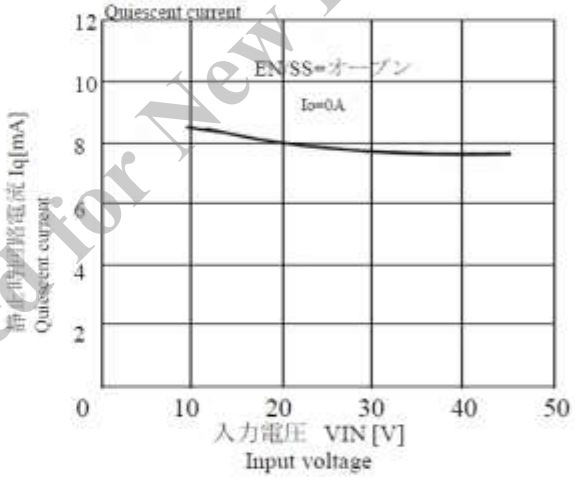
(5)過電流保護特性
Over Current Protection



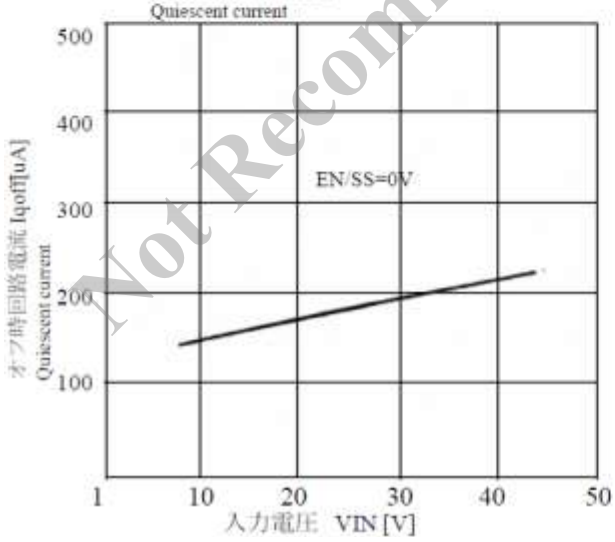
(3)ロードレギュレーション
Load Reguration



(6)無負荷時回路電流
Quiescent current



(4)オフ時回路電流
Quiescent current



8. Terminology

- Jitter

It is a kind of abnormal switching operations and is a phenomenon that the switching pulse width varies in spite of the constant condition of input and output. The output ripple voltage peak width is increased when a jitter occurs.

- Recommended Conditions

It shows the operation conditions required for maintaining normal circuit functions. It is required to meet the conditions in actual operations.

- Absolute Maximum Ratings

It shows the destruction limits. It is required to take care so that even one item does not exceed the specified value for a moment during instantaneous or normal operation.

- Electrical Characteristics

It is the specified characteristic value in the operation under the conditions shown in each item. If the operating conditions are different, it may be out of the specifications.

- PWM (Pulse Width Modulation)

It is a kind of pulse modulation systems. The modulation is achieved by changing the pulse width in accordance with the variation of modulation signal waveform (the output voltage for chopper type switching regulator).

- ESR (Equivalent Series Resistance)

It is the equivalent series resistance of a capacitor. It acts in a similar manner to the resistor series-connected to the capacitor.

Notice

・The contents of this description are subject to change without prior notice for improvement etc. Please make sure that any information to be used is the latest one.

・Any example of operation or circuitry described in this application note is only for reference, and we are not liable to any infringement of industrial property rights, intellectual property rights or any other rights owned by third parties resulting from such examples.

・In the event that you use any product described here in combination with other products, please review the feasibility of combination at your responsibility.

・Although we endeavor to improve the quality and reliability of our product, in the case of semi-conductor components, defects or failures which occur at a certain rate of probability are inevitable.
The user should take into adequate consideration the safety design in the equipment or the system in order to prevent accidents causing death or injury, fires, social harms etc..

・Products described here are designed to be used in the general-purpose electronic equipment (home appliances, office equipment, communication terminals, measuring equipment etc.).
If used in the equipment or system requiring super-high reliability (transport machinery and its control equipment, traffic signal control equipment, disaster/crime prevention system, various safety apparatus etc.), please consult with our sales office. Please do not use our product for the equipment requiring ultrahigh reliability (aerospace equipment, atomic control, medical equipment for life support etc.) without our written consent.

・The products described here are not of radiation proof type.

・The contents of this brochure shall not be transcribed nor copied without our written consent.