Application Note

Surface Molding synchronized rectification Chopper Regulator Control IC

SI-8511NVS

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SANKEN ELECTRIC CO., LTD.

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1. General Description

SI-8511NV series are a synchronized rectification chopper type switching regulator IC which is provided with various functions required for the buck switching regulator and protection functions. The synchronized rectification type switching regulator with high precision and high efficiency can be composed by connecting external logic Nch-MOS FET, diode etc.

● 1-1 Features

- Surface mounting type and compact size

  VSOP24 package which is compact and thin

- High efficiency 93% (V_{IN} = 5V, Vo = 2.5V, Io = 1A)

  Since the synchronized rectification type buck regulator can be composed, so high efficiency will be realized.

- Reference voltage accuracy ±1.25%

  Internal reference voltage is so accurate as 1.1V ±1.25%.

- Output voltage can be adjusted by an external resistor.

  Two resistors are used and the output voltage is made variable within the range of 1.1 – 6V.

- Operating frequency variable

  The operating frequency may be made variable in 400 KHz – 100KHz.

- Overcurrent protection

  Overcurrent protection (automatically restoration type) is built in and the threshold value can be set by an external resistor.

- Output overvoltage protection

  The output overvoltage protection function is built in. In the case that the output voltage exceeds the set voltage due to the destruction of high side MOSFET etc., the low side MOS is compulsorily turned on to blow a fuse on the input side.The operating voltage may also be changed by an external resistor.

- Soft start function (capable of ON/OFF output)

  By adding an external capacitor, it is possible to delay the rise speed of the output voltage. ON/OFF control of the output is also possible.

- Output ON/OFF function

  The ON/OFF control of output is made at Lo/Hi level. Control can be made by an external CPU etc.

- Power Good output

  The state of output voltage (Vo) is outputted.

● 1-2 Applications

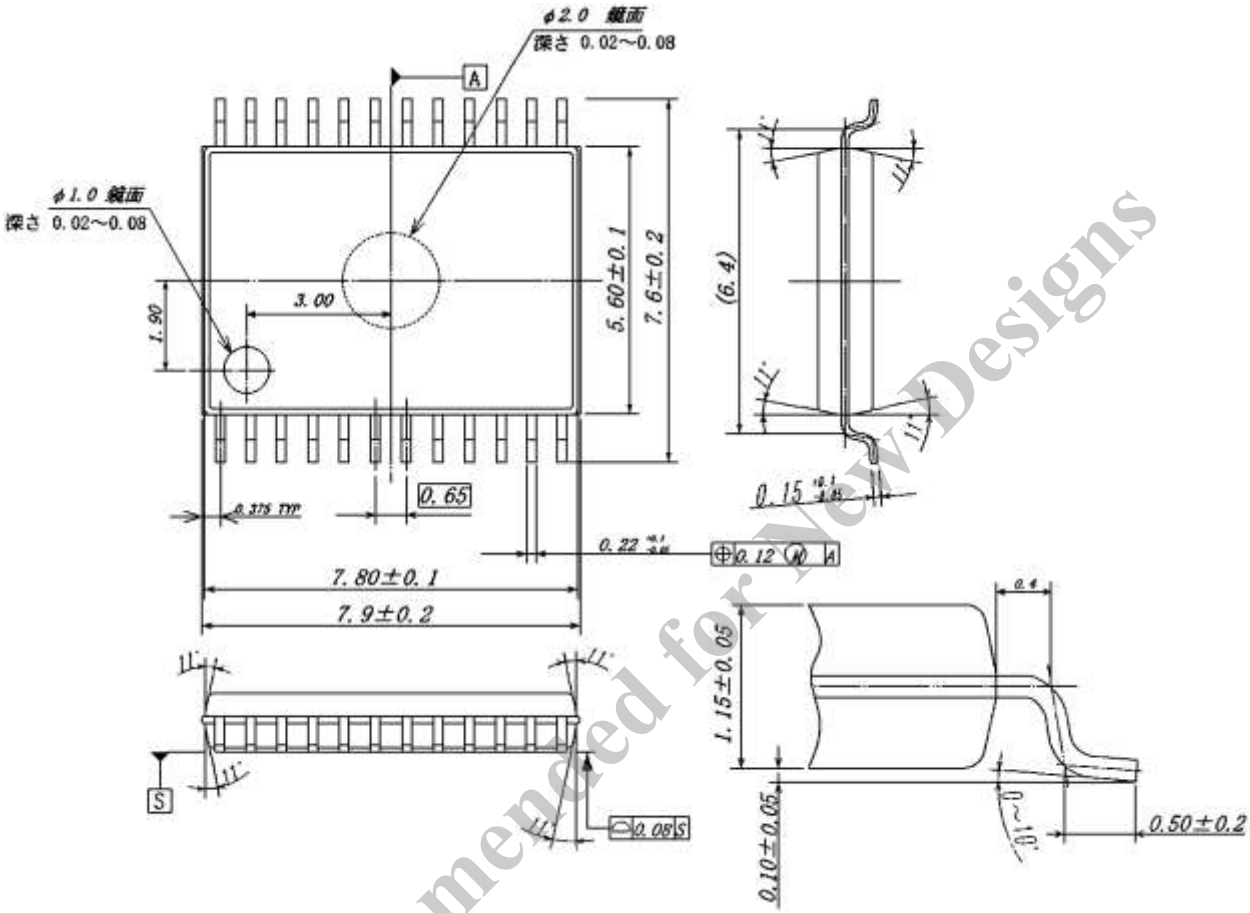
For power supply for laptop PC, power supplies for OA equipment, stabilization of secondary output voltage of regulators, power supply for communication equipment and power supply for amusement/leisure instruments.

● 1-3 Type

- Type: Semiconductor integrated circuits (monolithic IC)
- Structure: Resin molding type (transfer molding)

2. Specification

● 2-1 Package Information



● 2-2 Ratings

Absolute Maximum Rating

Characteristic	Symbol	Ratings	Unit
DC input voltage (VCC pin)	VCC	7	V
DC input voltage (VIN pin)	VIN	25	V
DC input voltage for Boost Block	VH	30	V
EN pin input voltage	Ven	VCC	V
PWRGD supply voltage	Vpwrgd	7	V
Junction Temperature	Tj	150	℃
Storage Temperature	Tstg	-40 - 150	℃

*1: Absolute Maximum Ratings shows the destruction limits. It is required to take care so that even one item does not exceed the specified value for a moment during instantaneous or normal operation.

Recommended Conditions

Characteristic	Symbol	Rating		Unit
		MIN	MAX	
DC input voltage range 1	VCC	4.5	5.5	V
DC input voltage range 2	VIN	3	18	V
Output voltage range 2	Vo	1.1	6	V
Operation temperature range	Top	-20	85	℃

*2: Recommended Conditions shows the operation conditions required for maintaining normal circuit functions. It is required to meet the conditions in actual operations.

Electrical Characteristics (Unless otherwise note Ta = 25°C)

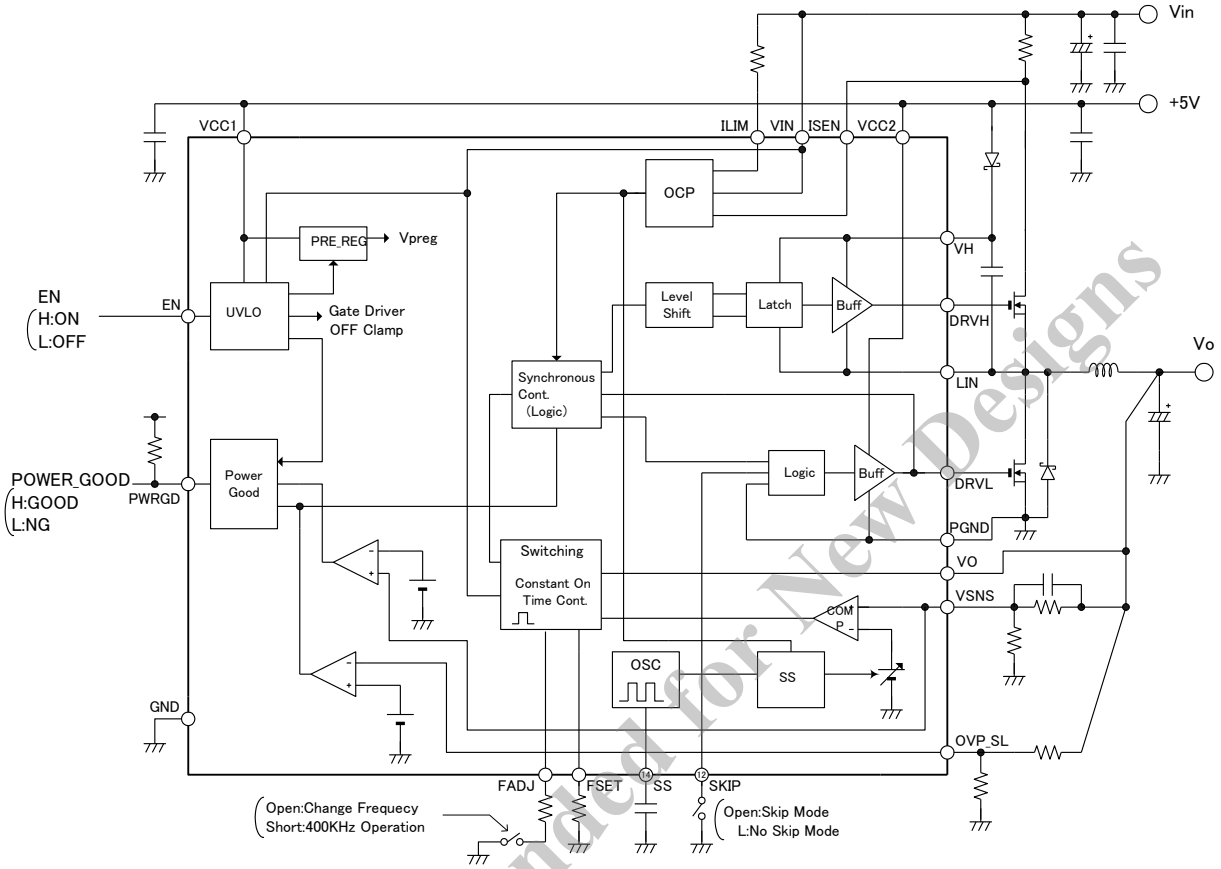
Characteristic	Symbol	Ratings			Unit	Remark
		MIN	TYP	MAX		
Loop Characteristic						
Output voltage	Vo	-1.2%	1.1	+1.2%	V	VIN=5V,VCC=5V, VSNS shorted to Vo, Io=0
Output voltage temperature coefficient	ΔVo/ΔT		±0.03		mV/°C	VIN=5V, VCC=5V, Vo=1.1V, Io=0, Ta=0-85°C
Circuit Current						
Current (VCC pin)	Iop			6	mA	VCC=5V, EN=H, FADJ:open
Cureent (VIN pin)	Iop			1	mA	VIN=5V, EN=H
Standby Current (VCC pin)	Istd1			100	μA	VCC=5V,EN＝L
Standby Current (VIN pin)	Istd2			50	μA	VIN=5V,EN=L
UVLO Block						
UVLO starting voltage1 (VCC)	Vuvlo1	3.7		4.4	V	VIN=5V
UVLO starting voltage2 (VIN)	Vuvlo2	2.5		2.9	V	VCC=5V
ON Time Control Block						
On time	Ton		1.27		μS	VCC=5V, VIN=5V, Vo=2.5V
Minimum off time	Toff		0.7		μS	VCC=5V
FSET pin output voltage	Vref	1.1	1.2	1.3	V	VCC=5V
FSET pin source current	Iref			100	μA	VCC=5V
High Side Drive Block						
ON Resistance (Pull-Up)	Ron		5.5		Ω	VH-VLIN=5V
ON Resistance (Pull-Down)	Ron		5.5		Ω	VH-VLIN=5V
Low Side Drive Block						
ON Resistance (Pull-Up)	Ron		5.5		Ω	VCC=5V
ON Resistance (Pull-Down)	Ron		5.5		Ω	VCC=5V

Electrical Characteristics (Unless otherwise note Ta = 25°C)

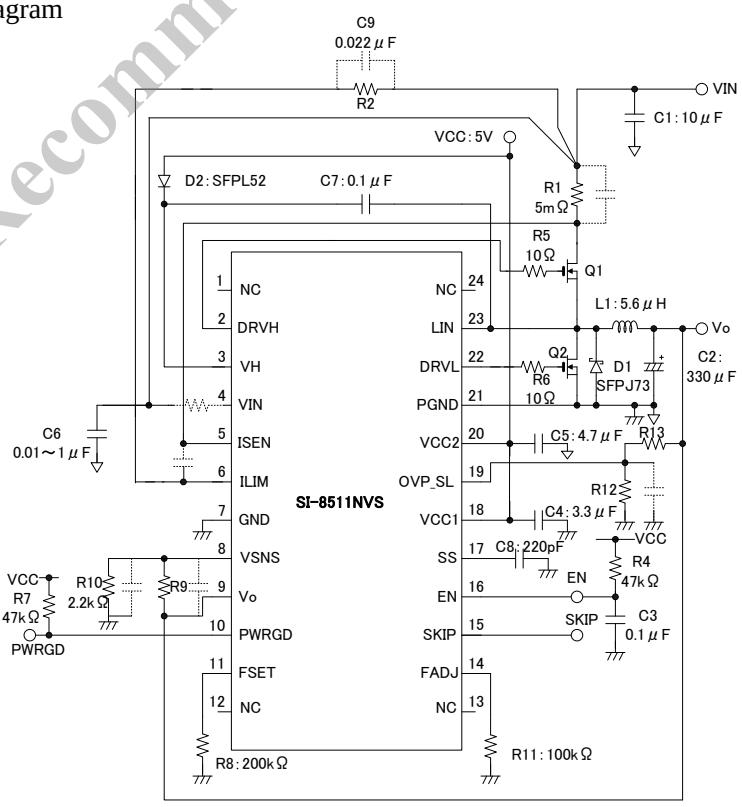
Characteristic	Symbol	Ratings			Unit	Remark
		MIN	TYP	MAX		
Bootstrap Block						
Bootstrap Voltage	VH-VLIN	4.5	5	5.5	V	
Protection Block						
Reference Current	Ilim	90	100	110	μA	VCC=5V, VIN=5V
Soft Start pin current	Iss		±20		μA	VCC=5V
EN Input Low Voltage	Vcelo	0		0.8	V	VCC=5V
EN Input High Voltage	Vcehi	2.4		VCC	V	VCC=5V
EN Bias Current	ICE			5	μA	VCC=5V, EN=5V
OVP operation Voltage	Vsns		1.32		V	VCC=5V
PERGD Trip Threshold	Vsns		0.88		V	VCC=5V
PERGD Low level Vlotage	Vpwrgd			0.4	V	VCC=5V, Ipergd=120μA
PWRGD pin current	Ipwrgd			120	μA	VCC=5V, Vpwrgd=0.4V
PERGD leakage Current	Ipwrgd			5	μA	Vpwrgd=5V

● 2-3 Circuit Diagram

Block Diagram



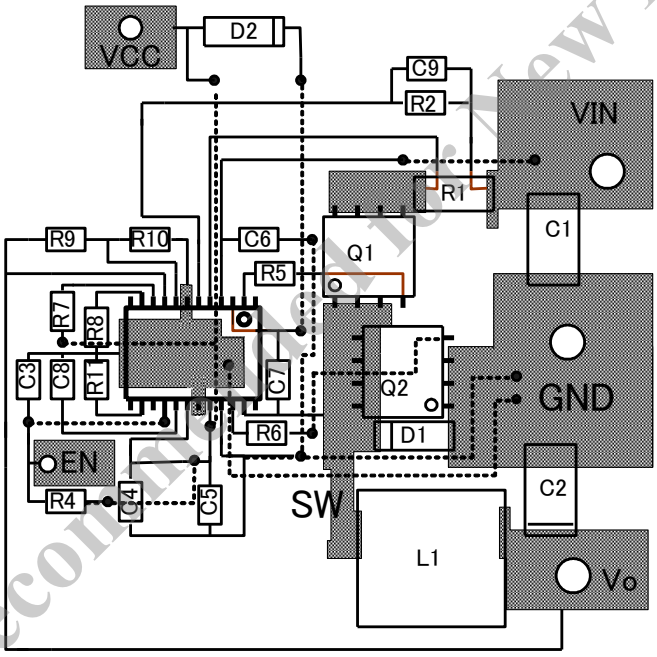
Typical Connection Diagram



Major Component List

Component	Description	Maker
Q1	N-ch MOS FET IRF7807	IR
Q2	N-ch MOS FET IRF7807	IR
L1	Inductor 10µH SLF12575-5R6N6R3	TDK
D1	First Recovery Diode 1A SFPL-52	SANKEN
D2	Schottky Diode 3A SFPJ-73	SANKEN
C1	Ceramic Capacitor 10µF/25V GRM43-2X7R106K25	MURATA
C2	Functional Polymer Tantalum Capacitor 330µF/6.3V PSLD0J337M	NEC

Component Layout Example



3. Terminal Description

● 3-1 Terminal List

No.	Terminal	Description
1	NC	Non-connected terminal
2	DRVH	High side drive terminal
3	VH	Boot Strap capacitor connected terminal
4	VIN	Input voltage terminal (power)
5	ISEN	Overcurrent detection resistor connected terminal
6	ILIM	Overcurrent limiting resistor connected terminal
7	GND	Ground terminal for analogue
8	VSNS	Output voltage sensing terminal
9	VO	Output voltage input terminal
10	PWRGD	Power Good terminal
11	FSET	Operating frequency setting terminal
12	NC	Non-connected terminal
13	NC	Non-connected terminal
14	FADJ	Operating frequency adjustment terminal
15	SKIP	SKIP mode select terminal
16	EN	Circuit enable terminal
17	SS	Soft start terminal
18	VCC1	Input voltage terminal (control)
19	OVP_SL	Overvoltage detection terminal
20	VCC2	Input voltage terminal (Low side drive)
21	PGND	Ground terminal for power
22	DRVL	Low side drive terminal
23	LIN	Switching terminal
24	NC	Non-connected terminal

● 3-2 Functional Description of Terminal

1. VCC1 and VCC2 terminals

These are +5V input terminals. VCC1 is a power supply terminal for internal power supplies and control circuits of SI-8511NVS. VCC2 is a power supply terminal for the low side drive circuit. Since much switching noise is imposed on VCC2, care should be taken not to affect the VCC1.

2. VIN terminal

This is an input terminal for the external main voltage (3 - 18V). The VIN terminal is used for the frequency setting and overcurrent protection circuit. Please take care of switching noise not to cause adverse effect.

3. EN terminal

This is an ON/OFF control terminal of the SI-8511NVS. When VCC is 5V, the output is turned ON by setting the EN terminal at H (2.4V or higher) and it is turned OFF by setting it at L (0.8V or lower). Since this is CMOS logic input, it should be set either at H or L instead of floating.

4. PWRGD terminal

The PWRGD terminal is in open drain output. The sink ability is 120μA (MAX). It should be pulled up to the power supply externally. The PWRGD signal also shows the state of output voltage Vo (VSNS voltage). When the VSNS voltage is 0.88V or lower or 0.88V or higher, L or H is outputted respectively. However, the voltage of OVP_SL terminal is 1.32V or higher, L is outputted to maintain the operating condition as it is.

5. FADJ terminal

This is a terminal for the selection of operating frequency. When the FADJ terminal is connected to GND by a resistor of 100kΩ or so, this is a 400kHz fixed mode of the maximum frequency. If the FADJ terminal is made OPEN, this is the variable operation frequency mode. In this case, the operation frequency can be changed subject to the resistance value connected to the FSET terminal. When 200kΩ is connected to the FSET terminal, the operating frequency of 250kHz or so is set.

6. FSET terminal

This is a 1.2V DC output terminal (source only). When the SI-8511NVS is in the operating frequency variable mode, the operating frequency can be changed subject to the resistor connected to the FSET terminal.

7. SS terminal

The soft start time can be set by varying the frequency of a dedicated oscillator (OSC) from a capacitor connected to the SS terminal.

8. ISEN terminal

This is an overcurrent value detection terminal. One side of the current detection resistor is connected.

9. ILIM terminal

This is an overcurrent value setting terminal. Current flowing into ILIM is set to be 100μA. The voltage drop caused by the resistor connecting this current to Vin is a reference of threshold of the overcurrent value.

10. VH terminal

This is an input voltage terminal for boost strap. An external capacitor and diode should be connected in accordance with the standard connecting circuit.

11. DRVH terminal

This is a terminal for driving a high side MOS.

12. DRVL terminal

This is a terminal for driving a low side MOS.

13. LIN terminal

This is a switching node terminal. The switching side of external inductor should be connected.

14. GND terminal

This is an analog ground terminal.

15. PGND terminal

This is a power ground terminal.

16. Vo terminal

This is an output voltage detection terminal. This is used for setting the operating frequency.

17. VSNS terminal

This is a terminal for setting the output voltage. A resistor for the detection of output voltage should be connected.

18. SKIP terminal

This is a terminal for skip mode selection. If the SKIP terminal is connected to GND, the oscillating frequency can be stabilized to some extent even at light load. And if it is in OPEN, the operation is in skip mode (frequency varies.).

19. OVP SL terminal

This is a terminal for setting the operation voltage value of output overvoltage protection.

When the voltage of the terminal exceeds the threshold value (1.32 V), the high side MOS turns off immediately and the low side MOS turns on. If it is connected to GND, the output overvoltage protection function does not work anymore.

4. Operational Description

● 4-1 ON time fixed PWM output voltage control

The SI-8511NVS is not provided with an internal oscillator for operating frequency. The SI-8511NVS adopts a PWM control system with constant ON time. ON time is controlled by the relation between voltage of VIN and Vo for 400 MHz operation. By using this system, rapid response to the steep variation of load is made possible.

● 4-2 Overcurrent Protection

The SI-8511NVS uses two external resistors for the detection of overcurrent. R1 is used for the purpose of detection of current flowing on the high side of MOS, while R2 for the purpose of determining the detection point. The reference current of 100μA constantly flows across the R2. When the potential difference produced in the current which flows across R1 exceeds the potential difference produced in the reference current and R2, the overcurrent protection operation starts.

5. Cautions

● 5-1 External Components

5-1-1 Choke coil L1

The choke coil L supplies current to the load side when the switching transistor is OFF. The coil is one of the most important components in the chopper type switching regulator. In order to maintain the stable operation of the regulator, such dangerous state of operation as saturation state and operation at high temperature due to heat generation must be avoided.

The following points should be taken into consideration for the selection of the choke coil.

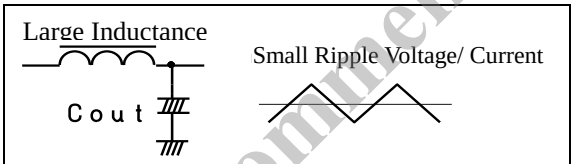
a) The choke coil should be fit for the switching regulator.

The coil for a noise filter should not be used because of large loss and generated heat.

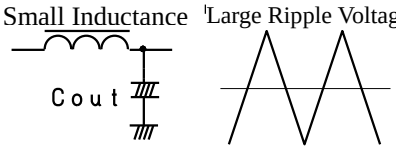
b) The inductance value should be appropriate.

The larger is the inductance of the choke coil, the less is the ripple current flowing across the choke coil, and the output ripple voltage drops and as a result, the overall size of the coil becomes larger.

On the other hand, if the inductance is small, the peak current flowing across the switching transistor and diode is increased to make the ripple voltage higher and this operation state is not favorable for maintaining the stable operation.



The larger is the inductance, the smaller will be the ripple current/voltage. But the outer size of the coil becomes larger.



The smaller is the inductance, the larger will be the ripple curtent/voltage.

Although the outer size of the coil is smaller, the operation is likely to be unstable.

The inductance value shown in typical connection diagram should be considered as a reference value for the stable operation and the appropriate inductance value can be calculated by the following equation.

ΔIL shows the ripple current value of the choke coil and the lower limit of inductance is set as described in the following.

- In the case that the output current is about 3A: output current × 0.2 - 0.6
- In the case that the output current is over 5A: output current × 0.2 – 0.3

$$L = \frac{(Vin - Vout) \cdot Vout}{\Delta IL \cdot Vin \cdot f} \quad ---(1)$$

For example, where V_{IN} = 10V, V_{Out} = 2.5V, ΔIL = 0.9A, frequency = 400KHz,

$$L = \frac{(10-2.5)\times 2.5}{0.9\times 10\times 400\times 10^{3}} \fallingdotseq 5.2uH$$

As shown above, the coil of about 220μH may be selected.

c) The rated current shall be met.

The rated current of the choke coil must be higher than the maximum load current to be used. When the load current exceeds the rated current of the coil, the inductance is sharply decreased to the extent that it causes saturation state at last. Please note that overcurrent may flow since the high frequency impedance becomes low.

d) Noise shall be low.

In the open magnetic circuit core, since magnetic flux passes outside the coil, the peripheral circuit may be damaged by noise. Especially, when noise is imposed on the Vo detection line, it is likely to cause mal function. It is recommended to use a closed magnetic circuit type core as much as possible.

5-1-2 Input Capacitor C1

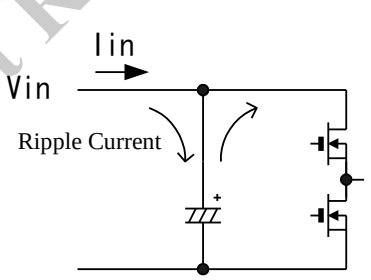
The input capacitor is operated as a bypass capacitor of the input circuit to supply steep current to the regulator during switching and to compensate the voltage drop of the input side. Therefore, the input capacitor should be connected as close as to the regulator IC. In addition, in the case that the smoothing capacitor of the AC rectifier circuit is located in the input circuit, the input capacitor may be also used as a smoothing capacitor, but similar attention should be paid. In order to reduce ringing noise, it will be effective to connect a ceramic capacitor of 0.1 – 0.47μF in parallel with C1.

The selection of C1 shall be made in consideration of the following points:

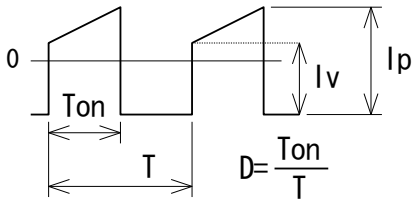
a) The requirement of withstand voltage shall be met.

b) The requirement of the allowable ripple voltage shall be met.

Current Flow of C1



Current Waveform of C1



The ripple current of the input capacitor is increased in accordance with the increase of the load current.

If the withstanding voltages or allowable ripple voltages are exceeded or used without derating, it is in danger of causing not only the decreasing the capacitor lifetime (burst, capacitance decrease, equivalent impedance increase, etc) but also the abnormal oscillations of regulator.

Therefore, the selection with sufficient margin is needed.

The effective value of ripple current flowing across the input capacitor can be calculated by the following equation:

$$Irms \approx 1.2 \times \frac{Vo}{Vin} \times Iout \quad --(2)$$

For instance, where Io = 3A, V_{IN} = 10V, Vo = 2.5V,

$$Irms \approx 1.2 \times \frac{2.5}{10} \times 3 = 0.9A$$

Therefore, it is necessary to select the capacitor with the allowable ripple current of 0.9A or higher.

5-1-3 Output Capacitor C2

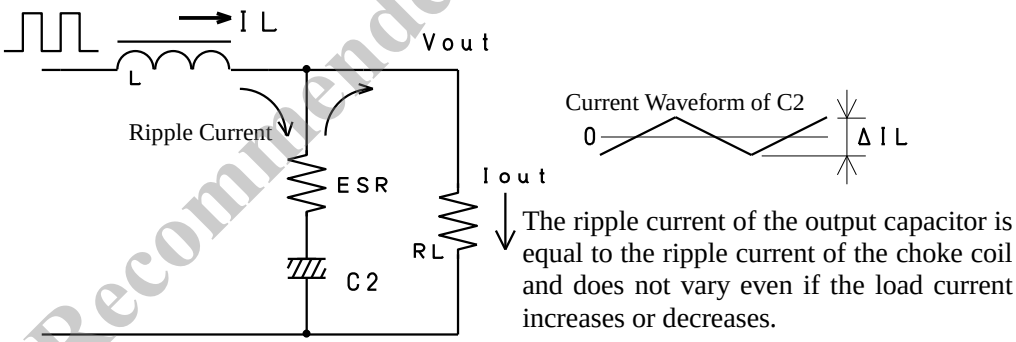
The output capacitor C2 composes a LC low pass filter together with a choke coil L and functions as a rectifying capacitor of switching output.

The current equivalent to the pulse current ΔIL of the choke coil current is charged and discharged in the output capacitor.

Therefore, it is necessary to meet the requirements of withstand voltage and allowable ripple current with sufficient margin like the input capacitor. Additional points to be checked are DC equivalent series resistance (ESR) and capacitance.

The following points should be taken into consideration.

Current Flow of C2



The ripple current of the output capacitor is equal to the ripple current of the choke coil and does not vary even if the load current increases or decreases.

- Allowable Ripple Current

The ripple current effective value of the output capacitor is calculated by the equation.

$$Irms = \frac{\Delta IL}{2\sqrt{3}} \quad ---(3)$$

When ΔIL = 0.5A,

$$Irms = \frac{0.5}{2\sqrt{3}} \fallingdotseq 0.14A$$

Therefore a capacitor having the allowable ripple current of 0.14A or higher is required.

- DC equivalent series resistance (ESR)

It is necessary for the stable operation to select the ESR properly. When the ESR is too large or too small,

abnormal oscillation due to increase of ripple voltage or insufficient phase margin occurs respectively.

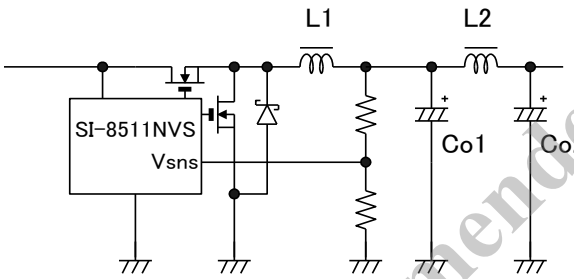
The output ripple voltage is determined by a product of the pulse current ΔIL (=C2 discharge and charge current) of the choke coil current and the ESR, and the output ripple voltage which is 0.5 - 3% of the output voltage (for example, where 1% at Vout = 5V, 50mV) is good for the stable operation. Please refer to the equations (4) and (5) to obtain the output ripple voltage. Please take note that ESR of aluminum electrolytic capacitor varies subject to temperature and ESR falls especially at high temperature.

$$Vrip \approx \frac{(Vin - Vout) \cdot Vout}{L \cdot Vin \cdot f} ESR \quad ---(4)$$

$$Vrip \approx \Delta IL \cdot ESR \quad ---(5)$$

When the ESR is too low (approx. 10Ω or lower), the phase delay becomes larger, resulting in abnormal oscillation. Therefore, it is not appropriate that a tantalum capacitor or a laminated ceramic capacitor is used for the output capacitor as an independent component. However, connecting a tantalum capacitor or a laminated ceramic capacitor in parallel with an electrolytic capacitor is effective in reducing the output ripple voltage only when it is used at low temperature (< 0°C).

In addition, in order to further decrease the ripple voltage, as shown below, it is also effective to add one stage of the LC filter to form the π type filter.



References

L2: 5.6μH

Co2: 47μF

It should be noted that the operating stability is more influenced by the ESR than the capacitance as described above if the requirements of withstand voltage and allowable ripple current are met.

With respect to the layout of the output capacitor, if it is located far from the IC, it will give same effect as the increase of ESR due to wiring resistance etc., therefore it is recommended to connect it near the IC.

5-1-4 Switching MOSFET

The logic type Nch-MOS should be used at low RDSON. If the general purpose MOS is used, ON resistance is not reduced to be inefficient because of shortage of Vgs and significant heat generation may happen. Since the power MOS driving terminal (DRVH, DRVL) of the SI-8511NVS has driving ability of around 0.5A at 2.5V output, a MOSFET should be selected in accordance with this ability.

5-1-5 Overcurrent detection resistor

Resistance values of several dozen mΩ to several mΩ should be used. Please do not use resistors with large L values. When Vin is about 3V, please try to limit the voltage drop produced at R2 within 100mV or so.

5-1-6 Voltage detection resistor

The internal reference voltage of the SI-8511NVS is set at 1.1V. The output voltage is set by connecting two resistors (R9 and R10) to the VSNS terminal. In addition, in order to maintain the stability of operation, please set a resistance value so as to permit the flow of current of 500μA – 2mA.

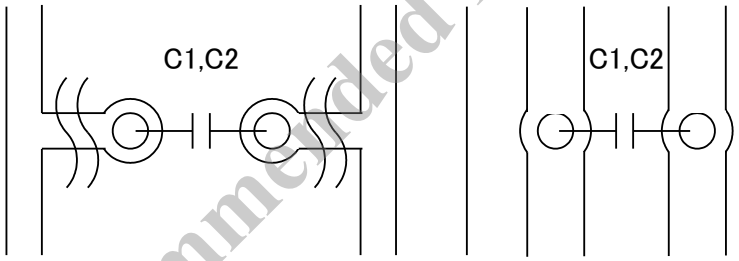
● 5-2 Pattern Design Notes

5-2-1 VCC Line

Since the current of 1A or so flows in the VCC line at the moment of MOS switching, the pattern of appropriate thickness should be used.

5-2-2 Input/ Output Capacitor

The input capacitor C1 and the output capacitor C2 should be connected to the IC as close as possible. If the rectifying capacitor for AC rectifier circuit is on the input side, it can be used as an input capacitor. However, if it is not close to the IC, the input capacitor should be connected in addition to the rectifying capacitor. Since high current is discharged and charged through the leads of input/output capacitor at high speed, the leads should be as short as possible. A similar care should be taken for the patterning of the capacitor.



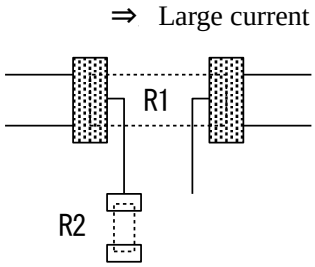
Improper Pattern Example　　Proper Pattern Example

5-2-3 Vo detection Line

For the Vo detection line (see the typical connection diagram.), the shortest patter from the vicinity of the output capacitor C2 should be used. In the case of long pattern, please take note that abnormal oscillation may be caused because of degraded regulation and increase of switching ripples. Interference with the inductance L1 should be avoided. In addition, it is recommended to use the pattern of appropriate thickness in order to reduce the impedance.

5-2-4 Overcurrent detection

For the connection of terminals (ISEN and ILIM) which detect overcurrent, Kelvin wiring should be made at both ends of the current detection resistor. Wiring should be made in a manner that the line connected to the both ends is not affected by large current line. Please refer to the following diagram for wiring.



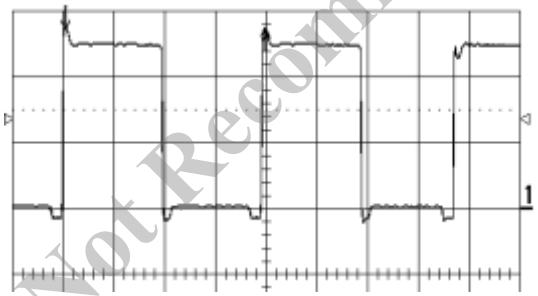
Overcurrent detection resistors R1 and R2 should be of 5 – 30mΩ. In the case that the output current exceeds 5A, they should be 5 – 10mΩ in consideration of decrease of loss and reduction of noise. It is recommended to mount a capacitor in parallel with R2 in order to reduce the effect of switching noise. The capacitance should be several thousand pF – 0.33μF.

In the case that noise due to switching current is intense, the effect of noise may be alleviated, if a resistor (1 – 15Ω) is inserted between the VIN terminal (No.4 pin) and VIN line in series.

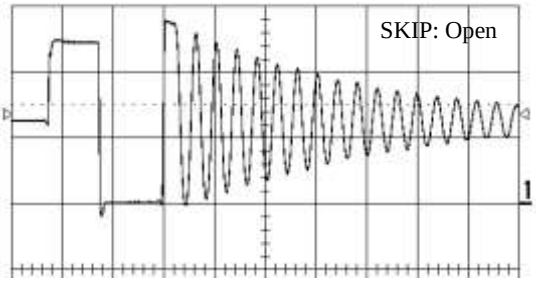
● 5-3 Operation Waveform Check

It can be checked by the waveform between the pin 18 to 20 (SWOut waveform) of the SI-8511NVS whether the switching operation is normal or not. The examples of waveforms at normal operations are shown below:

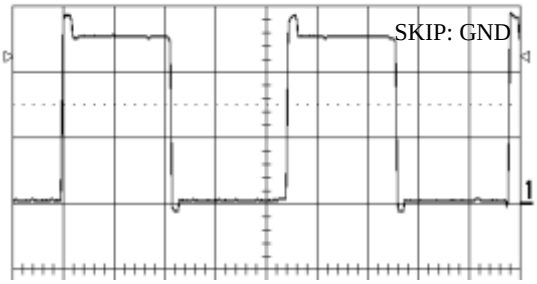
1. Normal Operation (continuous area)



2. Normal Operation (discontinuous area)



3. Normal Operation (discontinuous area)



The continuous area is an area where the DC component of the triangular wave is superimposed on the current flowing across the choke coil and the discontinuous area is an area where the current flowing across the choke coil is intermittent (a period of zero current may happen.) because the current flowing across the choke coil is low. Therefore, when the load current is high, the area is a continuous area and when the same current is low, the area is a discontinuous area.

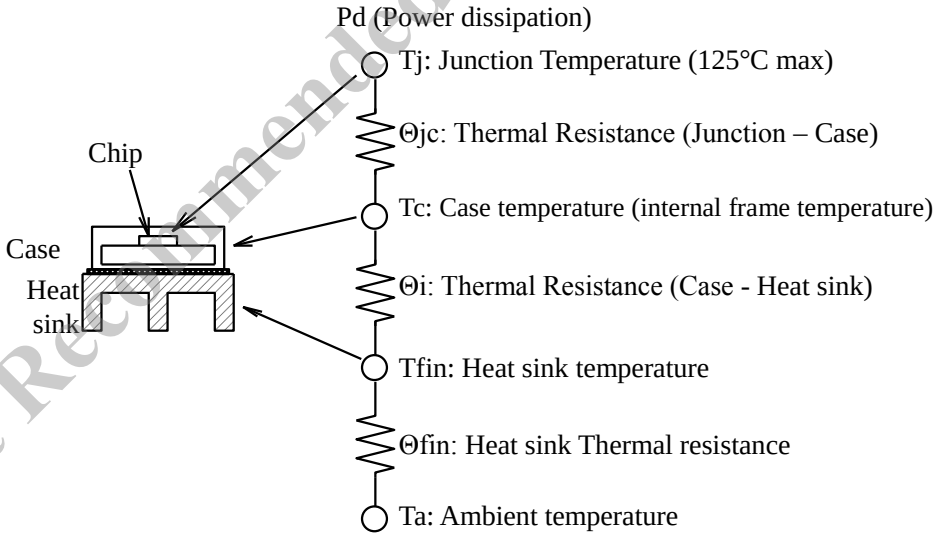
In the continuous area, the switching waveform is formed in the normal rectangular waveform (waveform 1) and in the discontinuous area, damped oscillation in the switching waveform (waveform 2) or lower frequency (waveform 3) are formed, but this is a normal operation without any problem.

When the IC is far from C1 and C2, the ON – OFF time of switching may be disturbed. Therefore, C1 and C2 should be connected close to the IC.

● 5-4 Thermal Design

5-4-1 Calculation of Heat Dissipation

The relation among the power dissipation Pd of MOSFET, junction temperature Tj, case temperature Tc, heat sink temperature Tfin and ambient temperature Ta is as follows:



$$Pd = \frac{Tj - Tc}{\theta jc} \quad --(6)$$

$$Pd = \frac{Tj - Tfin}{\theta jc + \theta i} \quad --(7)$$

$$Pd = \frac{Tj - Ta}{\theta jc + \theta i + \theta fin} \quad --(8)$$

The TjMAX is an inherent value for each product, therefore it must be strictly observed.

For this purpose, it is required to design the heat sink in compliance with PdMAX, TaMAX (determination of

θfin).

The heat derating graphically describes this relation.

The designing of the heat sink is carried out by the following procedure:

1) The maximum ambient temperature Ta MAX in the set is obtained.

2) The maximum power dissipation PdMAX is obtained.

(The following calculation is approximate.)

$$Pd \approx Rdson \cdot Io^2 \cdot \frac{Vo}{Vin} \cdot 1.1 \quad \text{(high side)} \qquad ---(9\text{-}1)$$

$$Pd \approx Rdson \cdot Io^2 \cdot \frac{Vin - Vo}{Vin} \cdot 1.1 \quad \text{(low side)} \qquad ---(9\text{-}2)$$

3) The pattern is determined from the intersection of the heat derating.

The required thermal resistance of the heat sink can be also calculated. The thermal resistance required for the heat sink is obtained by the following equation:

$$\theta i + \theta fin = \frac{Tj - Ta}{Pd} - \theta jc \qquad ---(10)$$

The thermal resistance data should be in accordance with the specifications of MOS to be used.

Generally heat sink will be used in the case of derating is 10 - 20% or more. Actually, heat dissipation effect significantly changes depending on the difference in component mounting. Therefore, heat sink temperature or case temperature at mounted should be checked.

6. Applications

● 6-1 Soft Start

In the case that the capacitance of output capacitor is large, the overcurrent protection circuit may be operated due to the in-rush current of output capacitor at startup and as result, the output may not be activated easily. As a countermeasure, it is effective to suppress the in-rush current by utilizing soft start. When the capacitance of Css is increased, it will have an effect of reduction of load short circuit current. The soft start time can be set by varying the frequency of dedicated oscillator (OSC) from the capacitor connected to the SS terminal. In addition, a 32-bit counter is built in and when this counter counts 32 bits, the output voltage becomes a set voltage value. Since the current flowing into the SS terminal is set at ±20μA, the soft start time can be calculated by the following equation.:

$$Tss = \frac{3 \times C}{20 \times 10^{-6}} \times 32 \quad [S]$$

Tss :soft start time, C: capacitance connected to CSS terminal

For example, when a 220pF capacitor is connected to the SS terminal,

$$Tss = \frac{3 \times 220 \times 10^{-12}}{20 \times 10^{-6}} \times 32 = 1\text{ms}$$

Then, the soft start time can be 1mS.

Since this soft start is used as an overcurrent limiting function, the soft start time should be limited within the range of 0.5 – 100mS.

● 6-2 Output ON / OFF Control

By setting the EN terminal at H (2.4V or higher) or L (0.8V or lower), the output is turned ON or OFF respectively. As logic input is used for the EN terminal it should be fixed either at H or L.

● 6-3 Controllable Output Voltage

The output voltage can be set by changing the values of R9 and R10. The current of 50μA – 2mA should flow across these resistors. The reference voltage of SI-8511NVS is set at 1.1V. For example, when the current of 500μA flows across R9, the result is expressed as R10 = 1.1V/500μA = 2.2KΩ. Then, please set the resistance of R9 by the following equation.

$$R9 = \left[(Vo / 1.1) - 1 \right] \times R10$$

When Vo is 2.5V, then R9 = (2.5 / 1.1 -1 × 2. 2KΩ) ＝ 2.8KΩ.

● 6-4 Overcurrent Setting

The SI-8511NVS compares the voltage produced at a resistor connected to ILIM (reference voltage) with the

voltage produced at a current detection resistor connected to ISEN to perform the overcurrent protection at a voltage value where the voltage drop of current detection resistor is equal to the voltage drop of a resistor connected to ILIM. Since the current which flows into ILIM is set to be 100μA, the overcurrent value is determined by the following equation.

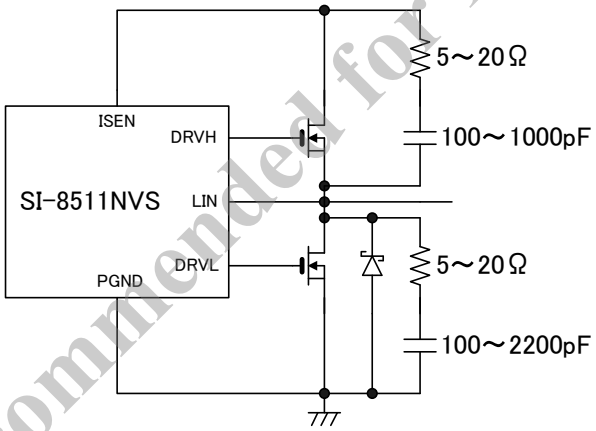
$$Is = \frac{R2}{R1} \times 100 \times 10^{-6} \quad [A]$$

In this equation, R1: current detection resistor value, R2: resistance value connected to ILIM terminal

When VIN is such low voltage as 3V, the voltage drop by R1 and R2 should be below 100mV to ensure the operation of an internal comparator.

● 6-5 Spike Noise Reduction

In order to decrease spike noise, it is effective to compensate the output waveform of high side MOSFET and the recovery time of diodes by capacitors and resistors. It is effective for either high side MOS or diode side. Please set in reference to the following figure. Please take note, however, that in either case, the efficiency is slightly degraded.



● 6-6 Variable Operating Frequency

In order to avoid f trouble, the SI-8511NVS can change the internal ON time by using the FADJ terminal and FSET terminal. When 100kΩ is connected between the FADJ terminal and GND terminal, the maximum frequency is set at 400KHz. When the FADJ terminal is made in OPEN state and a resistor is connected between FSET terminal and GND terminal, the frequency can be variable. This resistance is set at 100kHz or so by a 100kΩ resistor, 250kHz or so by 200kΩ resistor, 300kHz or so by 400kΩ resistor. The resistor connected between FSET and GND should be set in the range of 100kΩ －1MΩ.

● 6-7 Overvoltage Setting

The setting of overvoltage value can be made by using two external resistors. The threshold value is 1.32V.

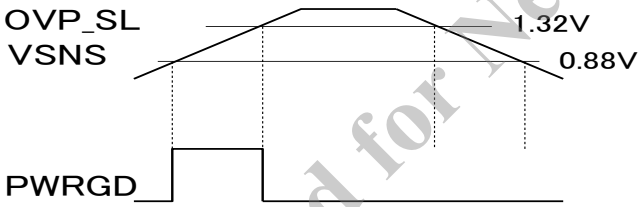
When the same value as the value of a resistor for setting the output voltage is connected, the overvoltage protection operation starts at the voltage of 20% higher than the output voltage. When the overvoltage

protection operation starts, the DRVH terminal is set at low voltage (same voltage as LIN terminal) and the DRVL terminal is set at high voltage (same voltage as VCC2 terminal) and this state is maintained. As the DRVL terminal is in high voltage, the low side MOS turns on to blow the fuse of input side. However, as the fuse may not be blown subject to the ON resistance of MOS, state of input voltage etc., the rated value of fuse should be determined after adequate reviewing. The overvoltage protection is reset, when the power supply is reconnected or the EN terminal is once on low side and then changed to high side.

● 6-8 Power Good Output

The PWRGD terminal is in open drain output. The sink ability is 120μA (Max.). Please pull up the power supply externally. The PWRGD signal shows the state of output voltage (VSNS voltage if defined more accurately). When the VSNS is below 0.88V, L is outputted, while H is outputted, when it is above 0.88V. However, when OVP SL terminal is above 1.32V, L is outputted and this condition is maintained. This state is reset, when the power supply is reconnected or the EN terminal is once made low and then high.

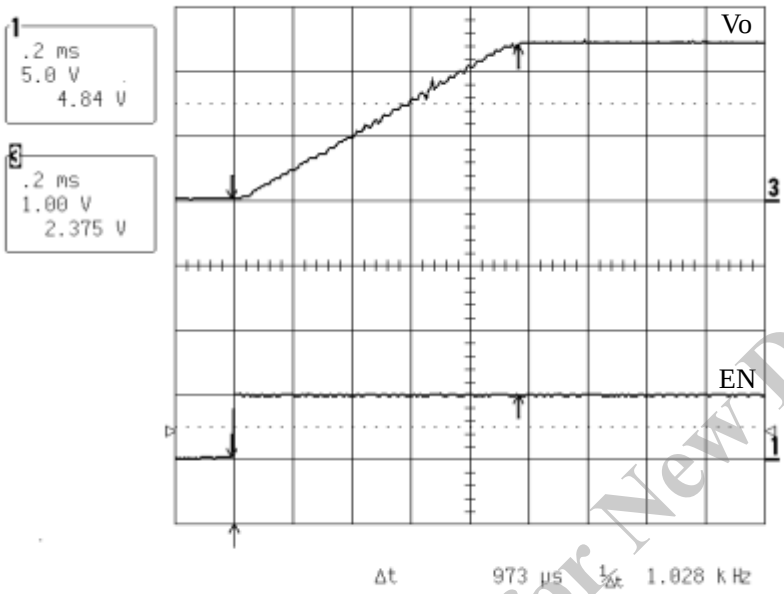
Timing chart



This is effective for forming the power supply sequence. After the PWRGD is made high, load can be applied.

7. Typical Characteristics

Enable Characteristics

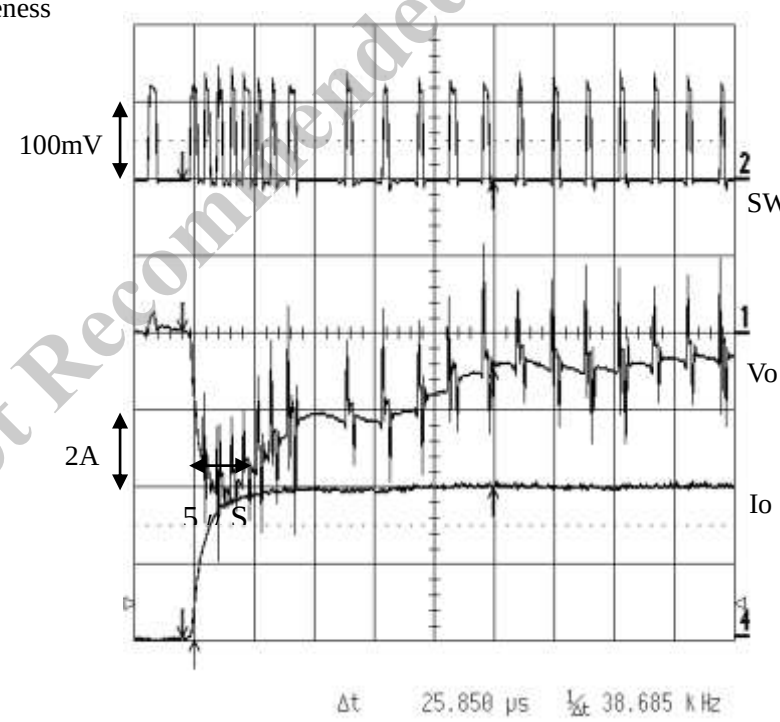


Vin=5V

Vo/Io=2.5V/0A

Css=220pF

Load Responsiveness

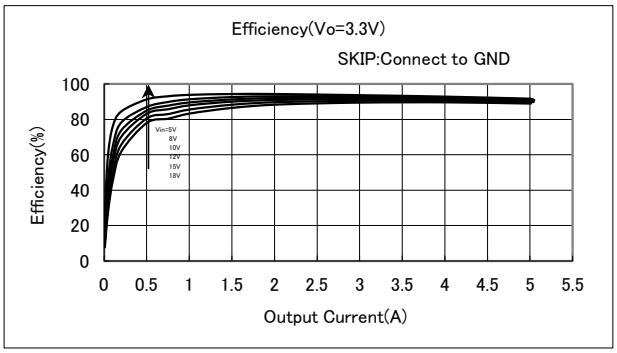


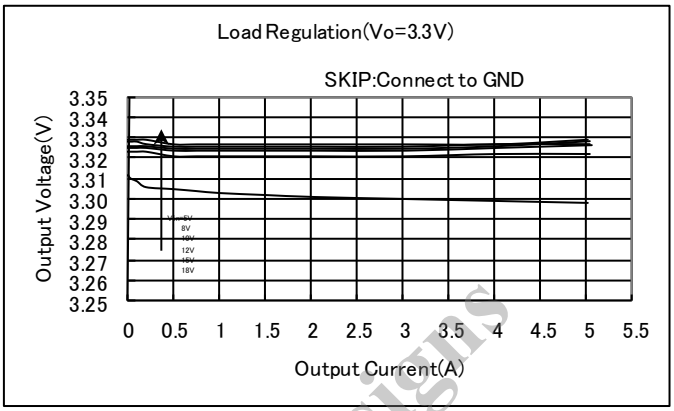
Vin=12V

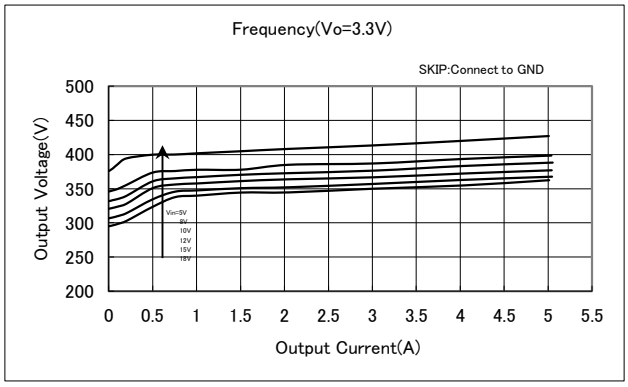
Vo =1.9V

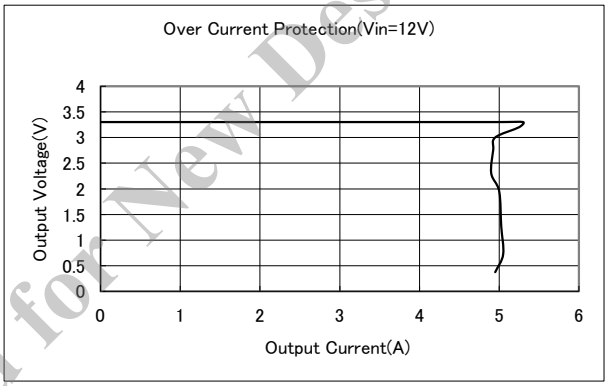
Io＝0 - 4A

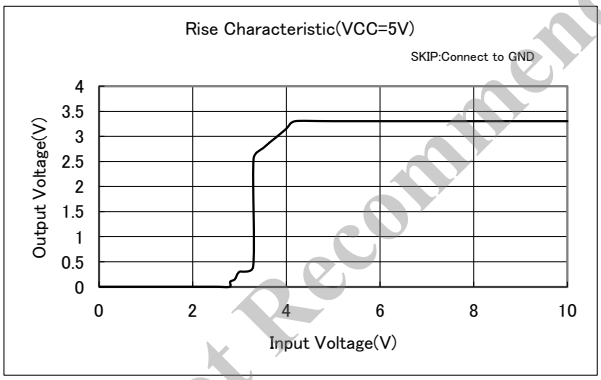
Electrical Characteristics











8. Terminology

- Recommended Conditions

It shows the operation conditions required for maintaining normal circuit functions. It is required to meet the conditions in actual operations.

- Absolute Maximum Ratings

It shows the destruction limits. It is required to take care so that even one item does not exceed the pacified value for a moment during instantaneous or normal operation.

- Electrical Characteristics

It is the specified characteristic value in the operation under the conditions shown in each item. If the operating conditions are different, it may be out of the specifications.

- PWM (Pulse Width Modulation)

It is a kind of pulse modulation systems. The modulation is achieved by changing the pulse width in accordance with the variation of modulation signal waveform (the output voltage for chopper type switching regulator).

- ESR (Equivalent Series Resistance)

It is the equivalent series resistance of a capacitor. It acts in a similar manner to the resistor series-connected to the capacitor.

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