600 V High Voltage 3-phase Motor Driver

SIM1-05A1M

Data Sheet

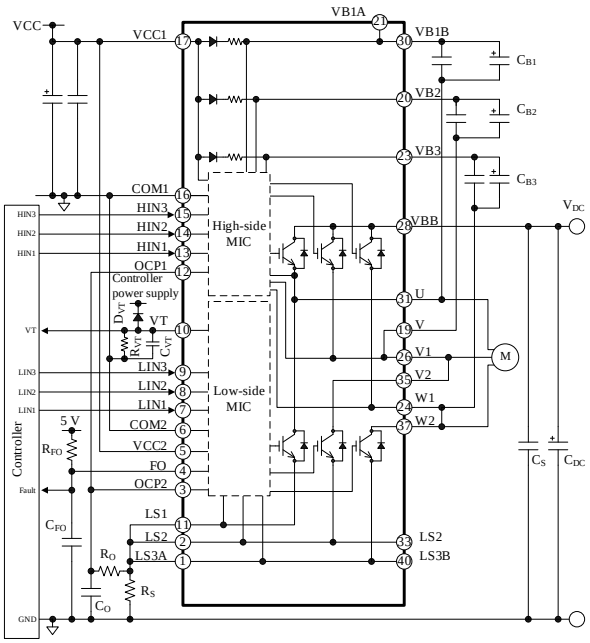
Description

The SIM1-05A1M is a high voltage 3-phase motor driver in which transistors, pre-drive circuits, and bootstrap circuits (diodes and resistors) are highly integrated. The product can optimally control the inverter systems of low- to medium-capacity motors that require universal input standards.

Features

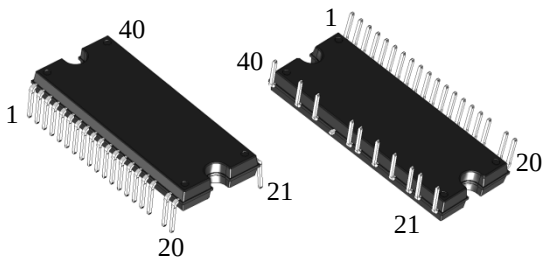
- Pb-free (RoHS Compliant)
- Isolation Voltage: 1500 V (for 1 min)
  UL-recognized Component (File No.: E118037)
- Temperature Sensing Function
- Built-in Bootstrap Diodes with Current Limiting Resistors (60 Ω)
- CMOS-compatible Input (3.3 V or 5 V)
- Fault Signal Output at Protection Activation (FO Pin)
- Protections Include:
  Overcurrent Protection (OCP):
  High-side (OCP1): Auto-restart
  Low-side (OCP2): Auto-restart
  Undervoltage Lockout for Power Supply
  High-side (UVLO_VB): Auto-restart
  Low-side (UVLO_VCC): Auto-restart
  Thermal Shutdown (TSD): Auto-restart

Typical Application



Package

DIP40
Mold Dimensions: 36.0 mm × 14.8 mm × 4.0 mm



Leadform 2971

Not to scale

Specifications

- Breakdown Voltage: 600 V
- I_O : 5.0 A
- Output Transistor: IGBT with FRD

Applications

For motor drives such as:

- Refrigerator Compressor Motor
- Fan Motor and Pump Motor for Washer and Dryer
- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier

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Contents

Description ---- 1
Contents ---- 2
1. Absolute Maximum Ratings ---- 4
2. Recommended Operating Conditions ---- 5
3. Electrical Characteristics ---- 6
3.1 Characteristics of Control Parts ---- 6
3.2 Bootstrap Diode Characteristics ---- 7
3.3 Thermal Resistance Characteristics ---- 7
3.4 Transistor Characteristics ---- 8
4. Mechanical Characteristics ---- 9
5. Insulation Distance ---- 9
6. Truth Table ---- 10
7. Block Diagrams ---- 11
8. Configuration Definitions ---- 12
9. Typical Applications ---- 13
10. Physical Dimensions ---- 14
11. Marking Diagram ---- 15
12. Functional Descriptions ---- 16
12.1 Turning On and Off the IC ---- 16
12.2 Pin Descriptions ---- 16
12.2.1 U, V, V1, V2, W1, and W2 ---- 16
12.2.2 VB1A, VB1B, VB2, and VB3 ---- 16
12.2.3 VCC1 and VCC2 ---- 17
12.2.4 COM1 and COM2 ---- 18
12.2.5 HIN1, HIN2, and HIN3; LIN1, LIN2, and LIN3 ---- 18
12.2.6 VBB ---- 19
12.2.7 LS1, LS2, LS3A, and LS3B ---- 19
12.2.8 OCP1 ---- 19
12.2.9 OCP2 ---- 19
12.2.10 FO ---- 19
12.2.11 VT ---- 19
12.3 Temperature Sensing Function ---- 20
12.4 Protection Functions ---- 20
12.4.1 Fault Signal Output ---- 20
12.4.2 Undervoltage Lockout for Power Supply (UVLO) ---- 21
12.4.3 Overcurrent Protection (OCP) ---- 21
12.4.4 Thermal Shutdown (TSD) ---- 23
13. Design Notes ---- 23
13.1 PCB Pattern Layout ---- 23
13.2 Considerations in Heatsink Mounting ---- 24
13.3 Considerations in IC Characteristics Measurement ---- 24
14. Calculating Power Losses and Estimating Junction Temperatures ---- 26
14.1 IGBT Steady-state Loss, P_{ON} ---- 26
14.2 IGBT Switching Loss, P_{SW} ---- 26
14.3 Estimating Junction Temperature of IGBT ---- 26
14.3.1 Freewheeling Diode Steady-state Loss, P_F ---- 27
14.3.2 Estimating Junction Temperature of Freewheeling Diode ---- 27
15. Performance Curves ---- 28

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15.1 Performance Curves of Control Parts ---- 28
15.2 Transient Thermal Resistance Curves ---- 34
15.3 Performance Curves of Output Parts ---- 35
15.3.1 Output Transistor Performance Curves ---- 35
15.3.2 Switching Loss Curves ---- 35
15.4 Allowable Effective Current Curves ---- 36
15.5 Short Circuit SOAs (Safe Operating Areas) ---- 37
16. Pattern Layout Example ---- 38
17. Typical Motor Driver Application ---- 40
Important Notes ---- 41

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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM, VCC1 = VCC2 = VCC.

Parameter	Symbol	Conditions	Rating	Unit
Main Supply Voltage (DC)	V_{DC}	VBB–LSx	450	V
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBB–LSx	500	V
IGBT Breakdown Voltage	V_{CES}	V_{CC} = 15 V, I_C = 1 mA, V_{IN} = 0 V	600	V
Logic Supply Voltage	V_{CC}	VCC–COM	20	V
	V_{BS}	VB1B–U, VB2–V, VB3–W1	20	V
Output Current(1)	I_O	T_C = 25 °C, T_J < 150 °C	5.0	A
Output Current (Pulse)	I_{OP}	T_C = 25 °C, V_{CC} = 15 V, pulse width ≤ 100 μs, single pulse	7.5	A
Input Voltage	V_{IN}	HINx–COM, LINx–COM	−0.5 to 7	V
FO Pin Voltage	V_{FO}	FO–COM	−0.5 to 7	V
OCP Pin Voltage	V_{OCP}	OCP–COM	−0.5 to 7	V
LSx Pin Voltage (DC)	$V_{LS(DC)}$	LSx–COM	−0.5 to 7	V
LSx Pin Voltage (Surge)	$V_{LS(SURGE)}$	LSx–COM	−4 to 7	V
Operating Case Temperature(2)	$T_{C(OP)}$		−30 to 100	°C
Junction Temperature(3)	T_J		150	°C
Storage Temperature	T_{STG}		−40 to 150	°C
Isolation Voltage(4)	$V_{ISO(RMS)}$	Between surface of the case and each pin; AC, 60 Hz, 1 min	1500	V

(1) Should be derated depending on an actual case temperature. See Section 15.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the control MICs, transistors, and freewheeling diodes.
(4) Refers to voltage conditions to be applied between all of the pins and the case. All the pins have to be shorted.

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2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM, VCC1 = VCC2 = VCC.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Main Supply Voltage	V_{DC}	VBB–COM	—	300	400	V
Logic Supply Voltage	V_{CC}	VCC–COM	13.5	15.0	16.5	V
	V_{BS}	VB1B–U, VB2–V, VB3–W1	13.5	—	16.5	V
Input Voltage (HINx, LINx, OCPx)	V_{IN}		0	—	5.5	V
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	—	—	µs
	$t_{IN(MIN)OFF}$		0.5	—	—	µs
Dead Time of Input Signal	t_{DEAD}		1.0	—	—	µs
FO Pin Pull-up Voltage	V_{FO}		3.0	—	5.5	V
FO Pin Pull-up Resistor	R_{FO}		3.3	—	10	kΩ
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	µF
Bootstrap Capacitor	C_{BOOT}		1	—	220	µF
VT Pin Pull-down Resistor(1)	R_{VT}		100	—	—	kΩ
VT Pin Capacitor	C_{VT}		0.001	—	0.01	µF
Shunt Resistor(2)	R_S	$I_{OP} \leq 7.5$ A	72	—	—	mΩ
RC Filter Resistor	R_O		—	—	100	Ω
RC Filter Capacitor	C_O		1000	—	8200	pF
PWM Carrier Frequency	f_C		—	—	20	kHz
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C

(1) Refers to a combined resistance with the input impedance of the microcontroller.
(2) Should be a low-inductance resistor.

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3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM, VCC1 = VCC2 = VCC.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Operation						
Low-side Logic Operation Start Voltage	$V_{CC(ON)}$	VCC–COM	10.5	11.5	12.5	V
Low-side Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC–COM	10.0	11.0	12.0	V
High-side Logic Operation Start Voltage	$V_{BS(ON)}$	VB1B–U, VB2–V, VB3–W1	9.5	10.5	11.5	V
High-side Logic Operation Stop Voltage	$V_{BS(OFF)}$	VB1B–U, VB2–V, VB3–W1	9.0	10.0	11.0	V
Logic Supply Current	I_{CC}	Total sink current of the VCC1 and VCC2 pins.	—	2.0	—	mA
	I_{BS}	VB1B–U or VB2–V or VB3–W1; HINx = 5 V; VBx pin current in 1-phase operation	—	85	170	µA
Input Signal						
High Level Input Threshold Voltage (HINx, LINx)	V_{IH}		—	2.0	2.5	V
Low Level Input Threshold Voltage (HINx, LINx)	V_{IL}		1.0	1.5	—	V
High Level Input Current (HINx, LINx)	I_{IH}	V_{IN} = 5 V	—	230	500	µA
Low Level Input Current (HINx, LINx)	I_{IL}	V_{IN} = 0 V	—	—	2	µA
Fault Signal Output						
FO Pin Voltage at Fault Signal Output	V_{FOL}	V_{FO} = 5 V, R_{FO} = 10 kΩ	0	—	0.5	V
FO Pin Voltage in Normal Operation	V_{FOH}	V_{FO} = 5 V, R_{FO} = 10 kΩ	4.8	—	—	V
Protection						
High-side OCP Threshold Voltage	$V_{TRIP(H)}$		0.63	0.70	0.77	V
Low-side OCP Threshold Voltage	$V_{TRIP(L)}$		0.46	0.50	0.54	V
High-side OCP Hold Time	$t_{P(H)}$		20	25	—	µs
Low-side OCP Hold Time	$t_{P(L)}$		5.0	10.0	—	ms
OCP Blanking Time	$t_{BK(OCP)}$		—	0.37	—	µs
Temperature Sensing Voltage*	V_T	$T_{J(MIC)}$ = 125 °C	2.997	3.155	3.313	V
TSD Operating Temperature*	T_{DH}		135	150	165	°C
TSD Releasing Temperature*	T_{DL}		105	120	135	°C

* Determined by the junction temperature of the control parts, but not of the output transistors.

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3.2 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	—	—	10	μA
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	—	1.0	1.3	V
Bootstrap Diode Series Resistor	R_B		45	60	75	Ω

3.3 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case Thermal Resistance(1)	$R_{(J-C)Q}$(2)	All IGBTs operating	—	—	3.6	°C/W
	$R_{(J-C)F}$(3)	All freewheeling diodes operating	—	—	4.2	°C/W
Junction-to-Ambient Thermal Resistance	$R_{(J-A)Q}$	All IGBTs operating	—	—	25	°C/W
	$R_{(J-A)F}$	All freewheeling diodes operating	—	—	29	°C/W

(1) Refers to a case temperature at the measurement point described in Figure 3-1, below.
(2) Refers to steady-state thermal resistance between the junction of the built-in transistors and the case.
(3) Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

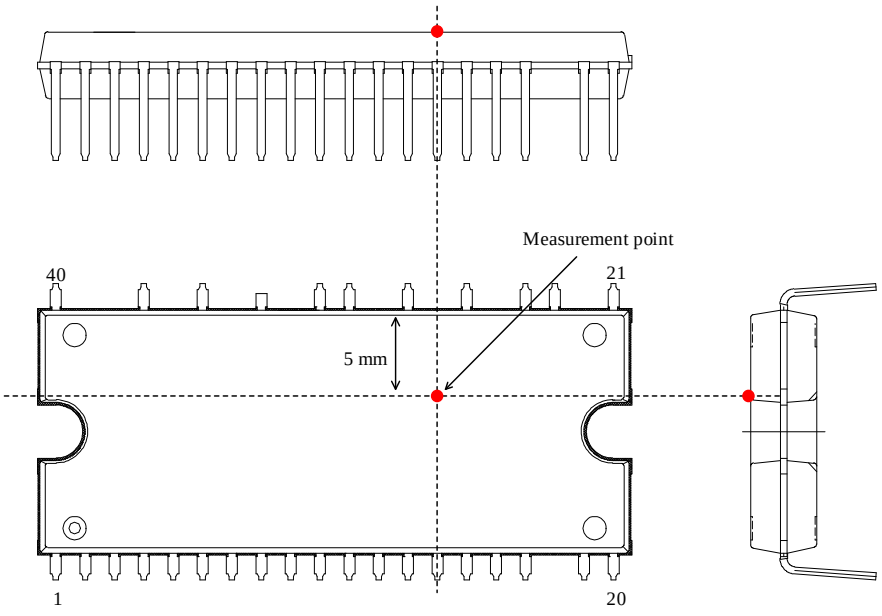

Figure 3-1. Case Temperature Measurement Point

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3.4 Transistor Characteristics

Figure 3-2 provides the definitions of switching characteristics described in this and the following sections.

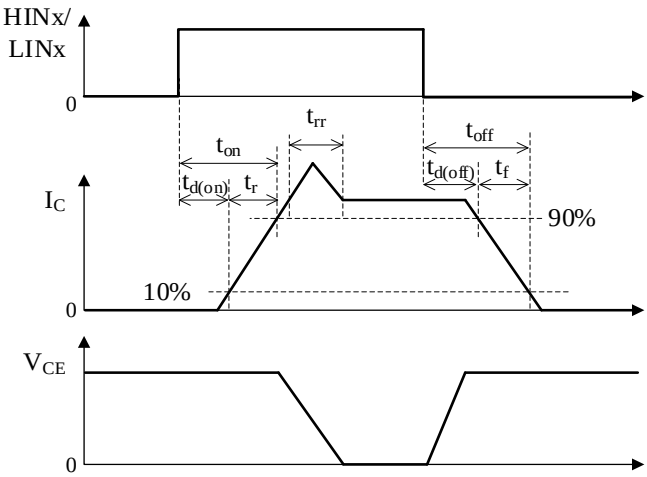

Figure 3-2. Switching Characteristics Definitions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 5.0 A, V_{IN} = 5 V	—	1.75	2.20	V
Diode Forward Voltage	V_F	I_F = 5.0 A, V_{IN} = 0 V	—	2.0	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 5.0 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(ON)}$		—	530	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(OFF)}$		—	740	—	ns
Fall Time	t_f		—	210	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 5.0 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(ON)}$		—	550	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(OFF)}$		—	600	—	ns
Fall Time	t_f		—	210	—	ns

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4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	*	0.294	—	0.441	N·m	
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	100	μm	
Package Weight		—	5.2	—	g	

* Requires using a metric screw of M2.5 and a plain washer of 6.0 mm (φ). For more on screw tightening, see Section 13.2.

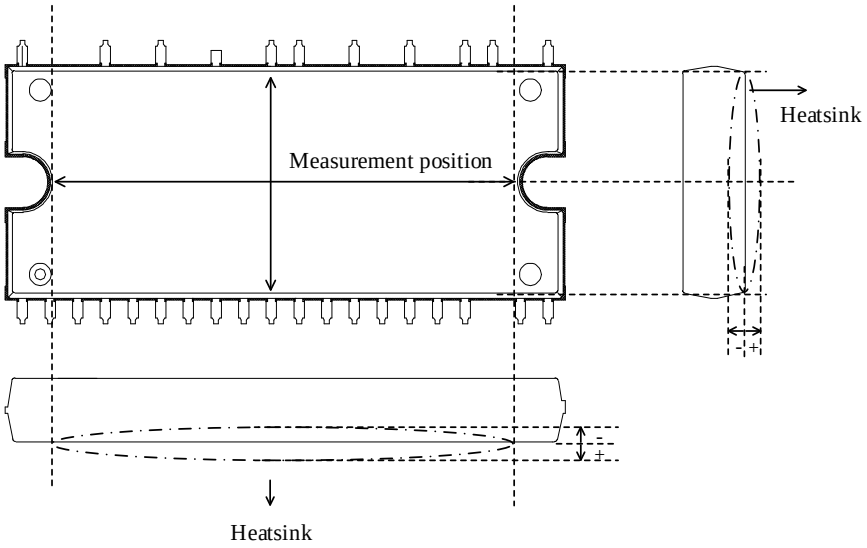

Figure 4-1. Flatness Measurement Position

5. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clearance	Between heatsink* and leads. See Figure 5-1.	1.5	—	2.1	mm	
Creepage		1.7	—	—	mm	

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

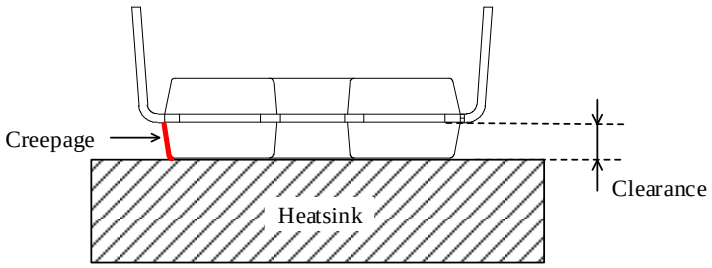

Figure 5-1. Insulation Distance Definitions

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6. Truth Table

Table 6-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx pin signals in each phase are high at the same time, both the high- and low-side transistors become on (simultaneous on-state). Therefore, HINx and LINx signals, the input signals for the HINx and LINx pins, require dead time setting so that such a simultaneous on-state event can be avoided.

After the IC recovers from a UVLO_VCC condition, the high- and low-side transistors resume switching, according to the input logic levels of the HINx and LINx signals (level-triggered).

After the IC recovers from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

Table 6-1. Truth Table for Operation Modes

Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON
Undervoltage Lockout for High-side Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Overcurrent Protection (OCP1, OCP2)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Thermal Shutdown (TSD)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF

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7. Block Diagrams

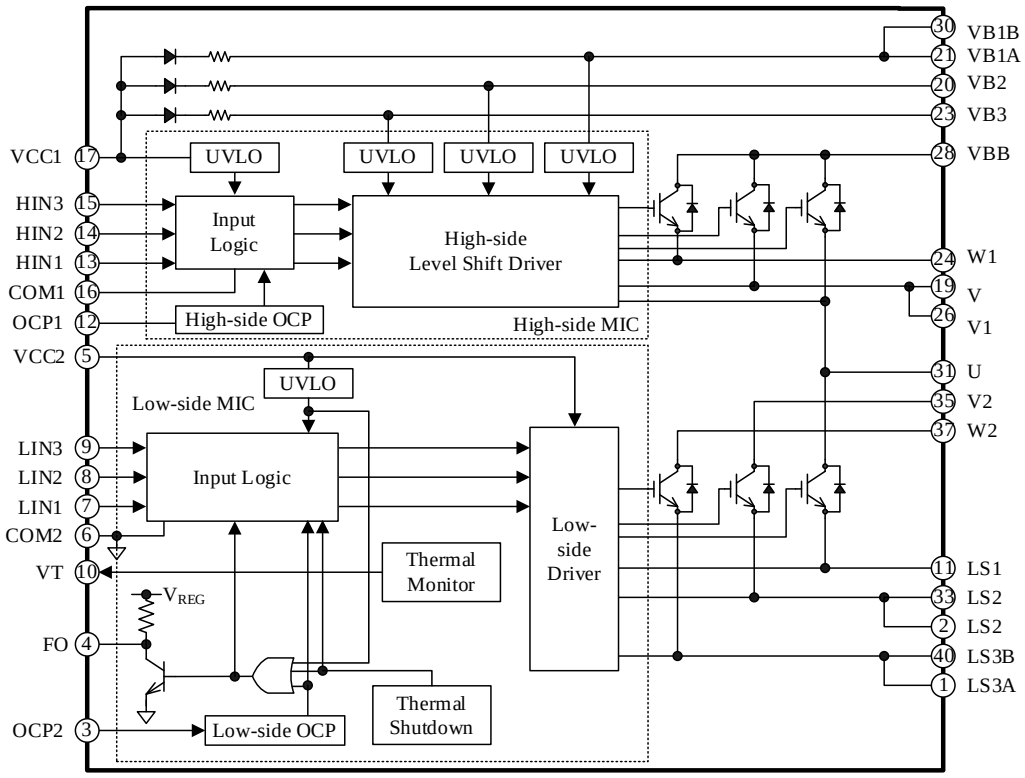

Figure 7-1. Block Diagram

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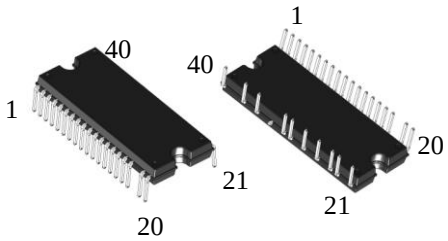
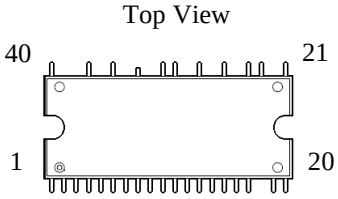
8. Configuration Definitions





Pin Number	Pin Name	Description
1	LS3A	W-phase low-side IGBT emitter
2	LS2	V-phase low-side IGBT emitter
3	OCP2	Input for low-side overcurrent protection
4	FO	Fault signal output
5	VCC2	Low-side logic supply voltage input (connected to VCC1 externally)
6	COM2	Low-side logic ground (connected to COM1 externally)
7	LIN1	Logic input for U-phase low-side gate driver
8	LIN2	Logic input for V-phase low-side gate driver
9	LIN3	Logic input for W-phase low-side gate driver
10	VT	Temperature sensing voltage output
11	LS1	U-phase low-side IGBT emitter
12	OCP1	Input for high-side overcurrent protection
13	HIN1	Logic input for U-phase high-side gate driver
14	HIN2	Logic input for V-phase high-side gate driver
15	HIN3	Logic input for W-phase high-side gate driver
16	COM1	High-side logic ground (connected to COM2 externally)
17	VCC1	High-side logic supply voltage input (connected to VCC2 externally)
18	—	(Pin removed)
19	V	V-phase bootstrap capacitor connection
20	VB2	V-phase high-side floating supply voltage input
21	VB1A	U-phase high-side floating supply voltage input
22	—	(Pin removed)
23	VB3	W-phase high-side floating supply voltage input
24	W1	W-phase output (connected to W2 externally)
25	—	(Pin removed)
26	V1	V-phase output (connected to V2 externally)
27	—	(Pin removed)
28	VBB	Positive DC bus supply voltage (+)
29	—	(Pin removed)
30	VB1B	U-phase high-side floating supply voltage input
31	U	U-phase output
32	—	(Pin removed)
33	LS2	(Pin trimmed) V-phase low-side IGBT emitter
34	—	(Pin removed)
35	V2	V-phase output (connected to V1 externally)
36	—	(Pin removed)
37	W2	W-phase output (connected to W1 externally)
38	—	(Pin removed)
39	—	(Pin removed)
40	LS3B	W-phase low-side IGBT emitter

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9. Typical Applications

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

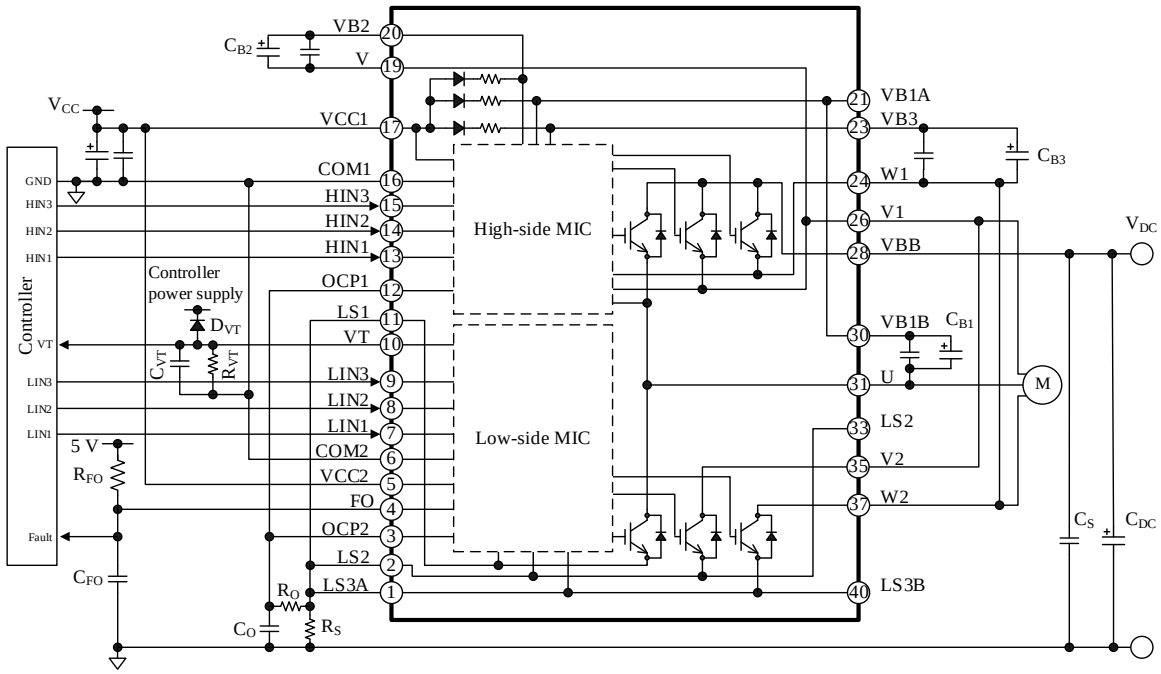

Figure 9-1. Typical Application Using a Single Shunt Resistor

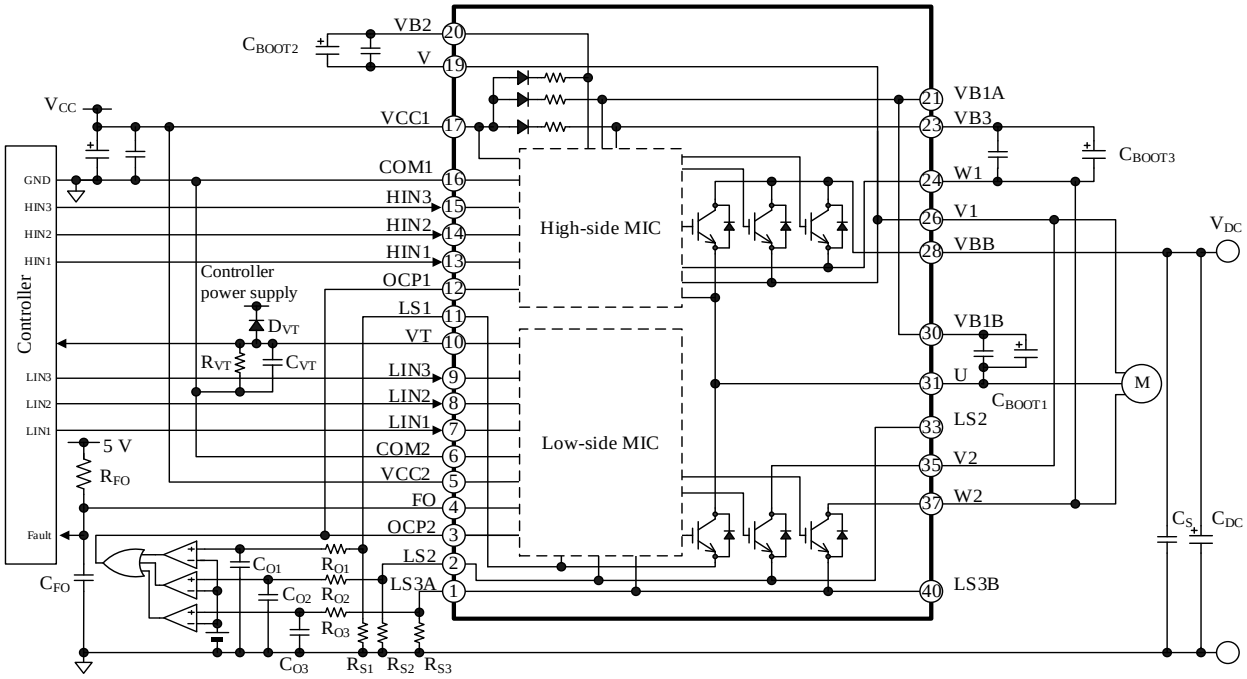

Figure 9-2. Typical Application Using Three Shunt Resistors

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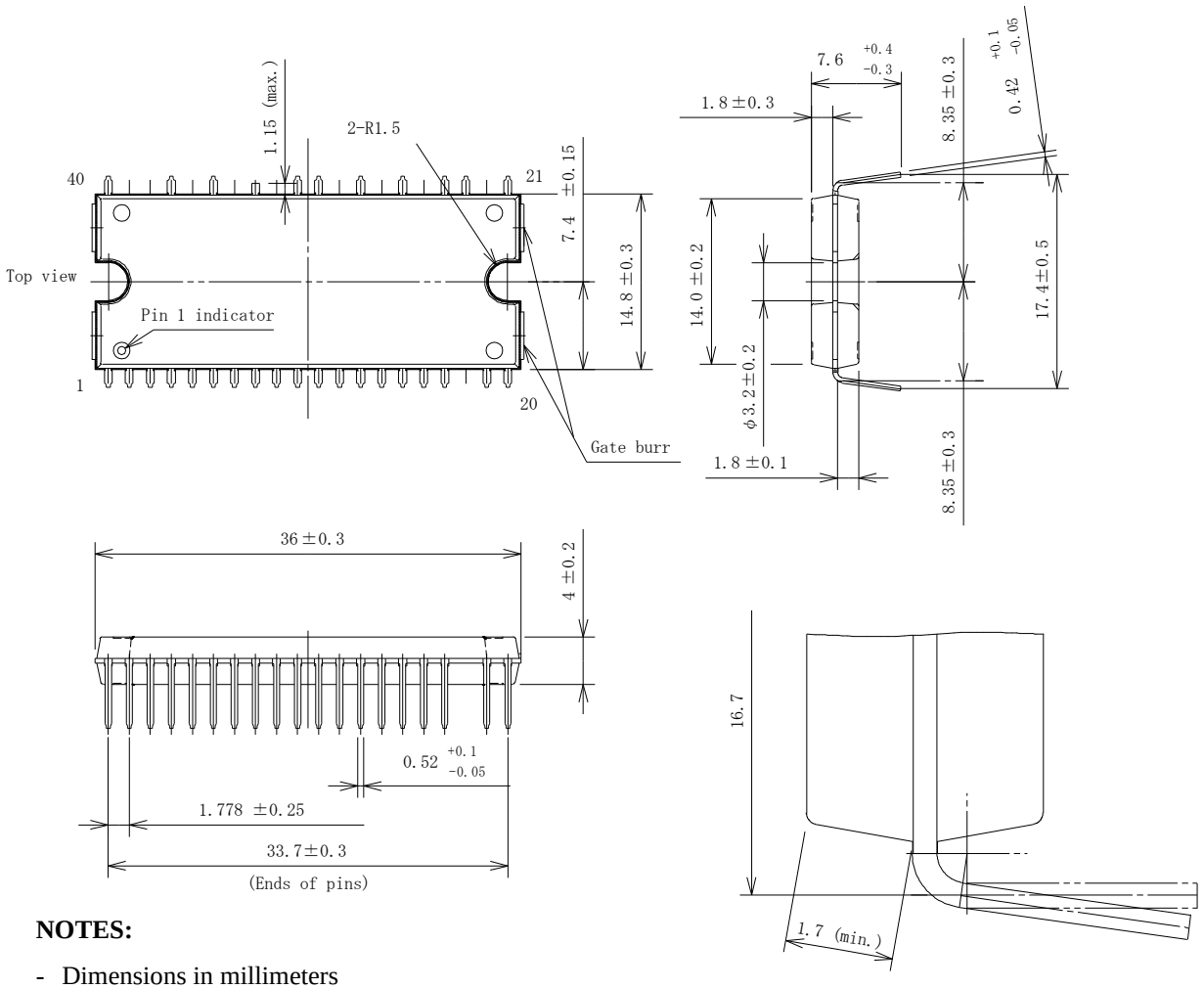
10. Physical Dimensions

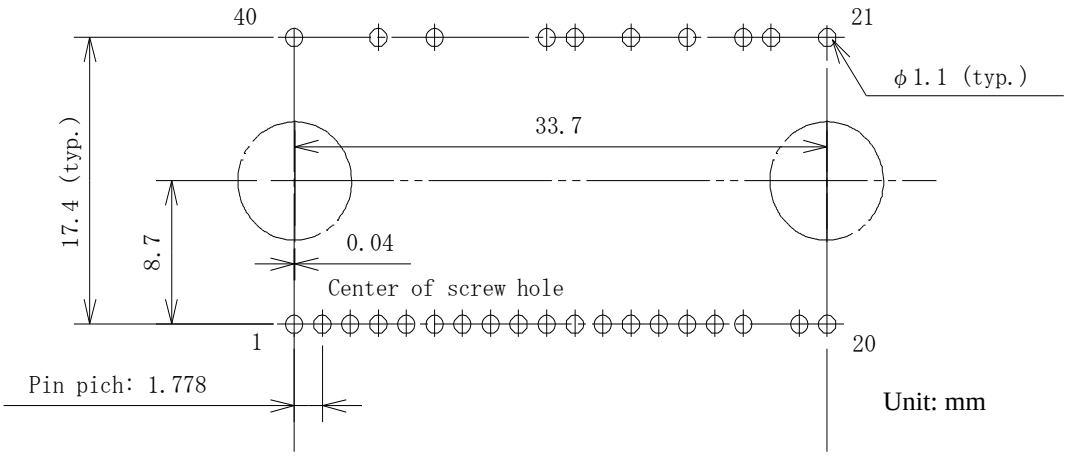
● **DIP40 Package**



NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)
- The leads illustrated above are for reference only, and may not be actual states of being bent.
- Maximum gate burr height is 0.3 mm.

● **Reference Through Hole Size and Layout**



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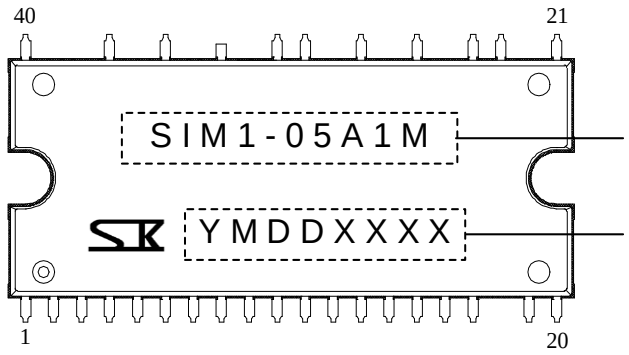
11. Marking Diagram

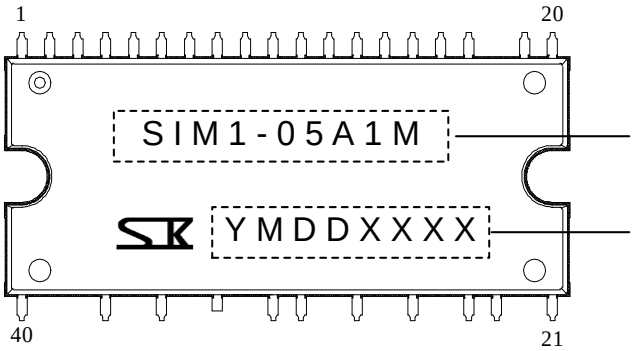
● **Front-side Marking**



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

● **Back-side Marking**



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
XXXX is the control number

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12. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. Thus, "the VCCx pin" is used when referring to either or both of the VCC1 and VCC2 pins.
- The COM1 pin is always connected to the COM2 pin.

12.1 Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 12.5$ V).

It is required to fully charge bootstrap capacitors, C_{Bx}, at startup (see Section 12.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

12.2 Pin Descriptions

12.2.1 U, V, V1, V2, W1, and W2

The U, V1, V2, W1, and W2 pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The V pin must be connected to a bootstrap capacitor of the V-phase. Do not connect the 3-phase motor to the V pin. The V1 and W1 pins must be connected to the V2 and W2 pins on a PCB, respectively.

The U, V (V1) and W1 pins are the grounds for the VB1A (VB1B), VB2, and VB3 pins. The U, V, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{Bx}. The V pin is internally connected to the V1 pin.

Since high voltages are applied to these output pins (U, V1, V2, W1, and W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

12.2.2 VB1A, VB1B, VB2, and VB3

These pins are connected to bootstrap capacitors for the high-side floating supply.

In actual applications, use either of the VB1A or VB1B pin because they are internally connected.

Voltages across the VBx and these output pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

A bootstrap capacitor, C_{Bx}, should be connected in each of the traces between the VB1A (VB1B) and U pins, the VB2 and V pins, the VB3 and W1 pins.

For proper startup, turn on the low-side transistor first, then fully charge the bootstrap capacitor, C_{Bx}.

For the capacitance of the bootstrap capacitors, C_{Bx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{Bx}.

$$C_{Bx}(\mu F) > 800 \times t_{L(OFF)} \quad (1)$$

$$1\ \mu F \leq C_{Bx} \leq 220\ \mu F \quad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{Bx}), measured in seconds.

Even while the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 12.4.2.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 12-1 shows, a bootstrap diode, D_{Bx}, and a current-limiting resistor, R_{Bx}, are internally placed in series between the VCC1 and VBx pins.

Time constant for the charging time of C_{Bx}, τ, can be computed by Equation (3):

$$\tau = C_{Bx} \times R_{Bx}\ , \quad (3)$$

where C_{Bx} is the optimized capacitance of the bootstrap capacitor, and R_{Bx} is the resistance of the current-limiting resistor (60 Ω ± 25%).

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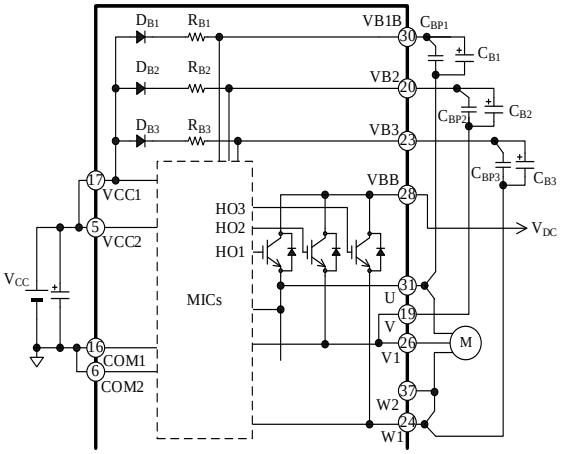

Figure 12-1. Bootstrap Circuit

Figure 12-2 shows an internal level-shifting circuit. A high-side output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a "Set" signal is generated. When the HINx input signal transits from high to low (falling edge), a "Reset" signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 12-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and output pins (U, V, or W1; hereafter "VBx–HSx") occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of an HOx signal stays logic high (or "H") because the SR flip-flop does not respond. With the HOx state being held high (i.e., the high-side transistor is in an on-state), the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition, which may result in critical damage to the IC. To protect the VBx pin against such a noise effect, add a bootstrap capacitor, C_{Bx}, in each phase. C_{Bx} must be placed near the IC and be connected between the VBx and HSx pins with a minimal length of traces. To use an electrolytic capacitor, add a 0.01 µF to 0.1 µF bypass capacitor, C_{BPx}, in parallel near these pins used for the same phase.

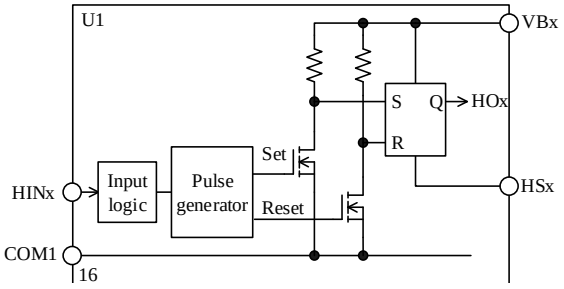

Figure 12-2. Internal Level-shifting Circuit

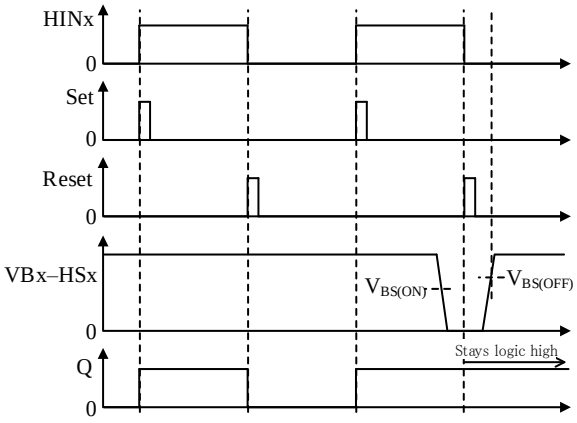

Figure 12-3. Waveforms at VBx–HSx Voltage Drop

12.2.3 VCC1 and VCC2

These are the logic supply pins for the built-in control MICs. The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_P, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins.

Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

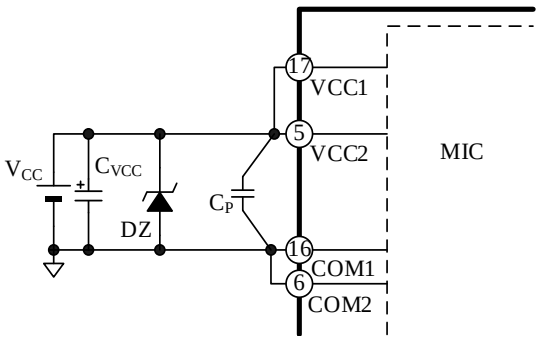

Figure 12-4. VCCx Pin Peripheral Circuit

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12.2.4 COM1 and COM2

These are the logic ground pins for the built-in control MICs. The COM1 and COM2 pins should be connected externally on a PCB because they are not internally connected. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_{Sx}, at a single-point ground (or star ground) which is separated from the power ground (see Figure 12-5).

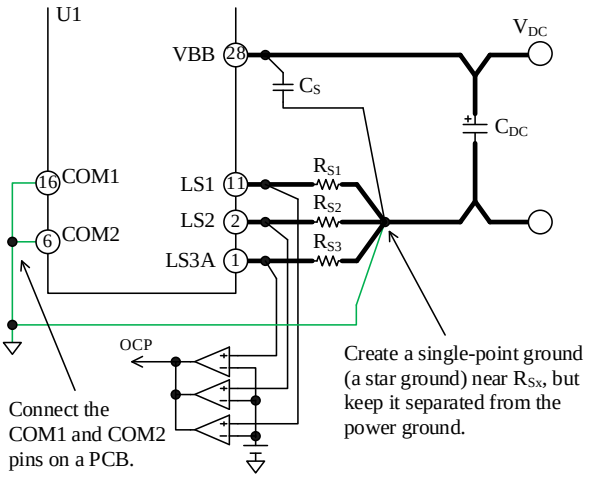

Figure 12-5. Connections to Logic Ground

12.2.5 HIN1, HIN2, and HIN3; LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller.

Figure 12-6 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 20 kΩ pull-down resistor, and its input logic is active high.

Input signals applied across the HINx–COMx and the LINx–COMx pins in each phase should be set within the ranges provided in Table 12-1, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid such malfunctions, set the microcontroller output line not to have high-impedance outputs. Also, if the traces from the microcontroller to the HINx or LINx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 12-7).

Here are filter circuit constants for reference:

- R_{IN1x}: 33 Ω to 500 Ω
- R_{IN2x}: 5 kΩ to 10 kΩ
- C_{INx}: 100 pF to 200 pF

Care should be taken in adding R_{IN1x} and R_{IN2x} to the traces. When they are connected to each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

Table 12-1. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 µs	≥0.5 µs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥1.0 µs	

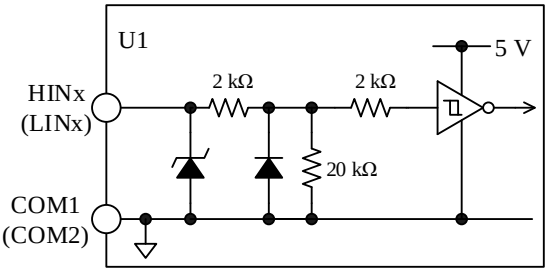

Figure 12-6. Internal Circuit Diagram of HINx or LINx Pin

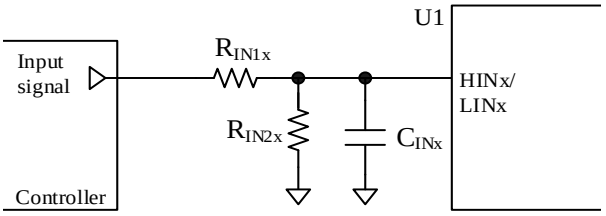

Figure 12-7. Filter Circuit for HINx or LINx Pin

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12.2.6 VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin. Voltages between the VBB and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

12.2.7 LS1, LS2, LS3A, and LS3B

These are the emitter pins of the low-side power IGBTs. For current detection, the LS1, LS2, and LS3A (LS3B) pins should be externally connected to shunt resistors, R_{Sx}. In actual applications, use either of the LS3A or LS3B pin because they are internally connected.

When connecting a shunt resistor, use a resistor with low inductance, and place it as near as possible to the IC with a minimum length of traces to the LSx and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RSx}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

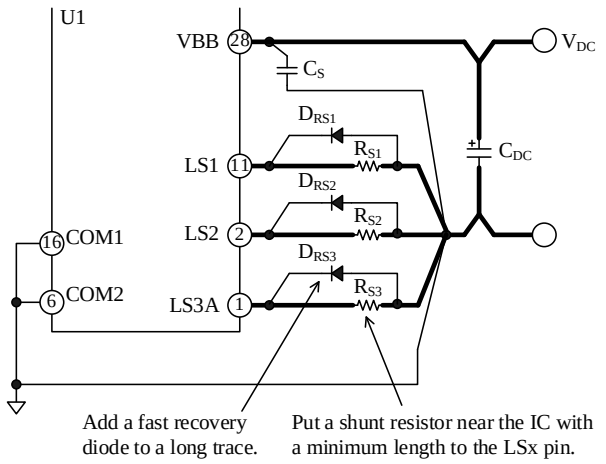

Figure 12-8. Connections to LSx Pin

12.2.8 OCP1

The OCP1 pin serves as the input for the high-side overcurrent protection which monitors the currents going through the output transistors. For more details on the high-side overcurrent protection (OCP1), see Section 12.4.3.1.

12.2.9 OCP2

The OCP2 pin serves as the input for the low-side overcurrent protection which monitors the currents going through the output transistors. For more details on the low-side overcurrent protection (OCP2), see Section 12.4.3.2.

12.2.10 FO

The FO pin operates as the fault signal output. For more details on this function, see Section 12.4.1. Figure 12-9 illustrates an internal circuit diagram of the FO pin and its peripheral circuit. Because of its open-collector nature, the FO pin should be tied by a pull-up resistor, R_{FO}, to the external power supply. The external power supply voltage (i.e., the FO Pin Pull-up Voltage, V_{FO}) should range from 3.0 V to 5.5 V. When the pull-up resistor, R_{FO}, has a too small resistance, the FO pin voltage at fault signal output becomes high due to the saturation voltage drop of a built-in transistor, Q_{FO}. Therefore, it is recommended to use a 3.3 kΩ to 10 kΩ pull-up resistor. To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FO and COMx pins.

For avoiding repeated OCP2 activation, the external microcontroller must shut off any input signals to the IC within a low-side OCP hold time, $t_{P(L)}$ = 5.0 ms (min.), after the internal transistor (Q_{FO}) turn-on. (For more details, see Section 12.4.3.2) Our recommendation is to use a 0.001 µF to 0.01 µF filter capacitor.

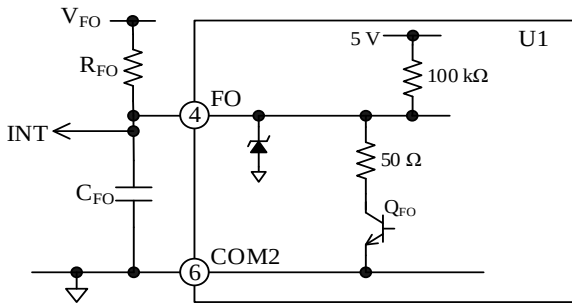

Figure 12-9. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

12.2.11 VT

This pin outputs temperature sensing voltages. The external microcontroller can monitor the junction temperature of the internal control stage, not of the output transistors, with the VT pin. Section 12.3 explains the configuration of the VT pin and its peripheral circuit and the temperature sensing function.

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12.3 Temperature Sensing Function

The microcontroller can monitor the junction temperature of the internal control stage, through temperature sensing voltages that the VT pin outputs. The IC must be set to stop its operation as it detects an abnormal heating state with temperature sensing voltages. A typical example is turning off input signals from the microcontroller. Figure 12-11 shows a relation between the VT pin voltage and temperature. Table 12-2 and Table 12-3 provide the details of variations found in Figure 12-11.

Temperature sensing voltages may exceed 3.0 V, causing permanent damage to the IC in the worst case. To protect the parts connected to the VT pin such as the microcontroller, add a clamp diode, D_{VT}, between the microcontroller power supply and the VT pin (see Figure 12-10).

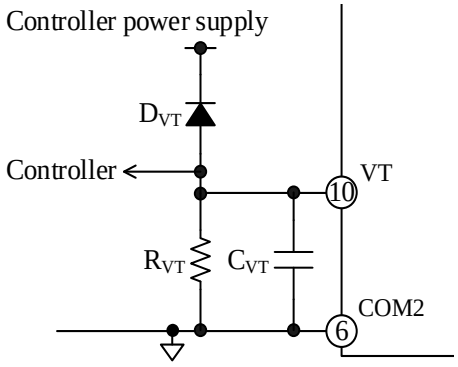

Figure 12-10. VT Pin Peripheral Circuit

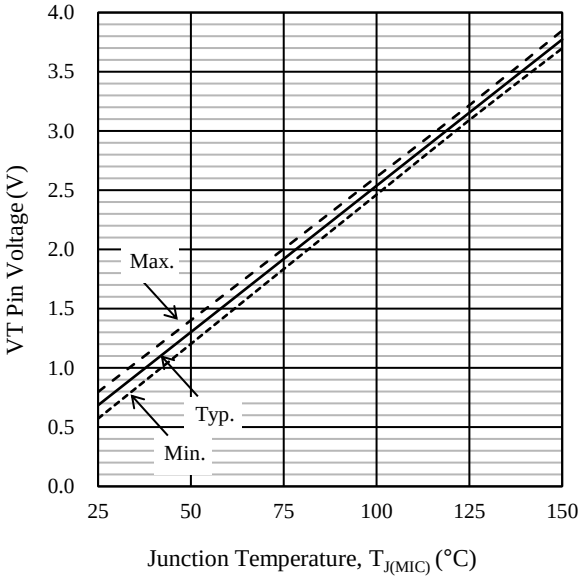

Figure 12-11. VT Pin Voltage vs. Internal Control Stage Junction Temperature, $T_{J(MIC)}$ (Design Value)

Table 12-2. $T_{J(MIC)}$ Variation on VT Pin Voltage (Design Value)

VT Pin Voltage (V)	$T_{J(MIC)}$ (°C)
1.30	50 ± 4
3.15	125 ± 3

Table 12-3. VT Pin Voltage Variation on $T_{J(MIC)}$ (Design Value)

$T_{J(MIC)}$ (°C)	VT Pin Voltage (V)
50	1.30 ± 0.10
125	3.15 ± 0.07

12.4 Protection Functions

This section describes the various protection circuits provided in the IC. The protection circuits include the undervoltage lockout for power supplies (UVLO), the overcurrent protection (OCP), and the thermal shutdown (TSD). In case one or more of these protection circuits are activated, the FO pin outputs a fault signal; as a result, the external microcontroller can stop the operations of the three phases by receiving the fault signal. In the following functional descriptions, "HOx" denotes a gate input signal on the high-side transistor, whereas "LOx" denotes a gate input signal on the low-side transistor. "VBx–HSx" refers to the voltages between the VBx pin and output pins (U, V, and W1).

12.4.1 Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor, Q_{FO}, turns on, then the FO pin becomes logic low (≤0.5 V).

1) Low-side undervoltage lockout (UVLO_VCC)
2) Low-side overcurrent protection (OCP2)
3) Thermal shutdown (TSD)

While the FO pin is in the low state, all the low-side transistors turn off. In normal operation, the FO pin outputs a high signal of about 5 V. Motor operations must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. To prevent the IC from having permanent damage at OCP2 activation, be sure to set the motor operation to stop within $t_{P(L)}$ = 10.0 ms (typ.). $t_{P(L)}$ is the fault signal output time of the FO pin, fixed by a built-in feature of the IC itself (see Section 12.4.3.2). To resume the motor operation thereafter, set the motor to be resumed after a lapse of ≥2 seconds.

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12.4.2 Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SIM1-05A1M has the undervoltage lockout (UVLO) circuits for both of the high- and low-side power supplies.

12.4.2.1. Undervoltage Lockout for High-side Power Supply (UVLO_VB)

Figure 12-12 shows operational waveforms of the undervoltage lockout for high-side power supply (i.e., UVLO_VB).

When the voltage between the VBx and output pins (VBx–HSx) decreases to the High-side Logic Operation Stop Voltage ($V_{BS(OFF)}$ = 10.0 V) or less, the UVLO_VB circuit in the corresponding phase gets activated and sets an HOx signal to logic low. When the voltage between the VBx and HSx pins increases to the High-side Logic Operation Start Voltage ($V_{BS(ON)}$ = 10.5 V) or more, the IC releases the UVLO_VB operation. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VB release. Any fault signals are not output from the FO pin during the UVLO_VB operation. In addition, the VBx pin has an internal UVLO_VB filter of about 3 µs, in order to prevent noise-induced malfunctions.

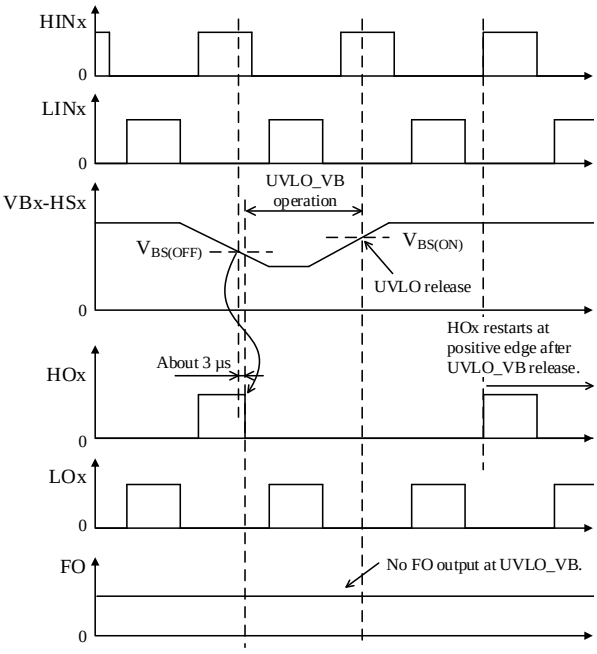

Figure 12-12. UVLO_VB Operational Waveforms

12.4.2.2. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 12-13 shows operational waveforms of the undervoltage lockout for low-side power supply (i.e., UVLO_VCC). When the VCC2 pin voltage decreases to the Low-side Logic Operation Stop Voltage ($V_{CC(OFF)}$ = 11.0 V) or less, the UVLO_VCC circuit in the corresponding phase gets activated and sets both of HOx and LOx signals to logic low. When the VCC2 pin voltage increases to the Low-side Logic Operation Start Voltage ($V_{CC(ON)}$ = 11.5 V) or more, the IC releases the UVLO_VCC operation. The IC then resumes transmitting HOx and LOx signals according to input commands on the HINx and LINx pins, respectively. During the UVLO_VCC operation, the FO pin becomes logic low and sends fault signals.

In addition, the VCC2 pin has an internal UVLO_VCC filter of about 3 µs, in order to prevent noise-induced malfunctions.

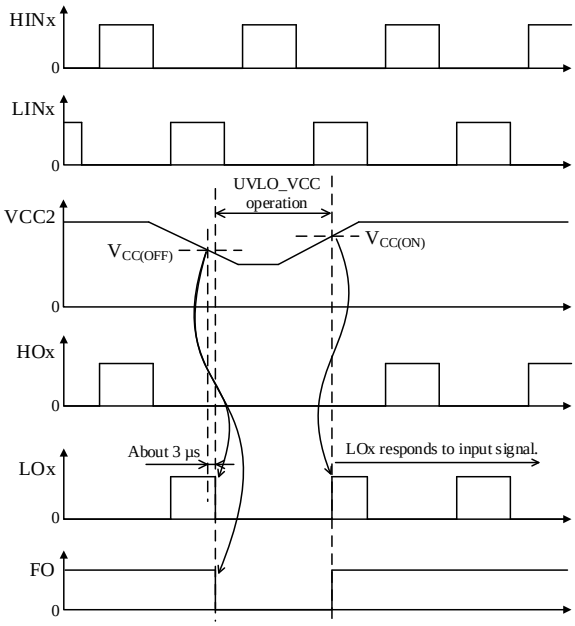

Figure 12-13. UVLO_VCC Operational Waveforms

12.4.3 Overcurrent Protection (OCP)

The OCP has two different protections: the high-side overcurrent protection (OCP1) and the low-side overcurrent protection (OCP2). These overcurrent protections are protections against large inrush currents (i.e., high di/dt).

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. For this reason, motor operations must be controlled by the external microcontroller so that it can

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immediately stop the motor when fault signals are detected.

For proper setting of the shunt resistor connected to the OCPx pin, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_{Sx} (see Section 2).
- Set the OCPx pin input voltage to vary within the rated OCPx pin voltages, V_{OCP} (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistors, R_{Sx}. In addition, choose a resistor with allowable power dissipation according to your application.

When you connect a CR filter (i.e., a pair of a filter resistor, R_O, and a filter capacitor, C_O) to the OCPx pin, care should be taken in setting the time constants of R_O and C_O. The larger the time constant, the longer the time that the OCPx pin voltage rises to V_{TRIP}. And this may cause permanent damage to the transistors. Consequently, a propagation delay of the IC must be taken into account when you determine the time constants. For R_O and C_O, their time constants must be set to ≤ 0.82 µs. And place C_O as close as possible to the IC with minimizing a trace length between the OCPx and COMx pins.

Note that overcurrents are undetectable when one or more of the U, V/V1/V2, and W1/W2 pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

12.4.3.1. High-side Overcurrent Protection (OCP1)

Figure 12-14 is an internal circuit diagram describing the OCP1 pin and its peripheral circuit. The OCP1 pin detects overcurrents with voltage across external shunt resistors, R_{Sx}. Because the OCP1 pin is internally pulled down, the OCP1 pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_{Sx}.

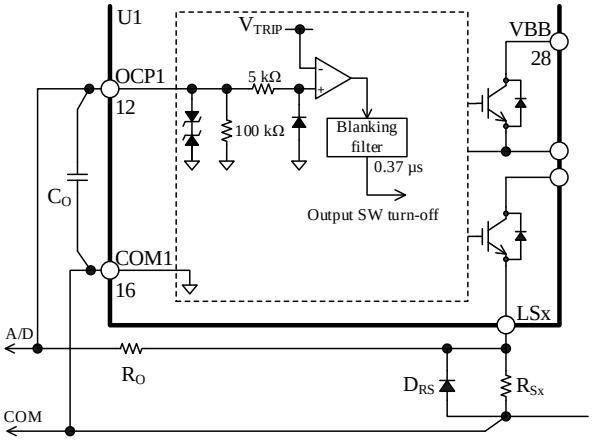

Figure 12-14. Internal Circuit Diagram of OCP1 Pin and Its Peripheral Circuit

Figure 12-15 is a timing chart that represents operation waveforms during OCP1 operation. When the OCP1 pin voltage increases to the OCP1 Threshold Voltage, $V_{TRIP(H)} = 0.70$ V or more, and remains in this condition for a period of the OCP Blanking Time ($t_{BK} = 0.37$ µs) or longer, the OCP1 circuit is activated. The enabled OCP1 circuit shuts off the high-side transistors. The OCP2 circuit is also activated.

Then, output current decreases as a result of the output transistor turn-offs. Even if the OCP1 pin voltage falls below $V_{TRIP(H)}$, the IC holds the high-side output signal, HOx in the low state for a fixed high-side OCP hold time, $t_{P(H)} = 25$ µs (typ.). Then, the HOx signal becomes logic high at the rising edge of the first input command.

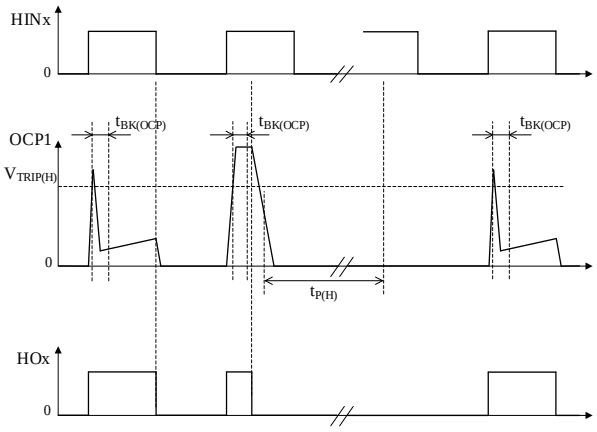

Figure 12-15. OCP1 Operational Waveforms

12.4.3.2. Low-side Overcurrent Protection (OCP2)

Figure 12-16 is an internal circuit diagram describing

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the OCP2 pin and its peripheral circuit. The OCP2 pin detects overcurrents with voltage across external shunt resistors, R_{Sx}. Because the OCP2 pin is internally pulled down, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_{Sx}.

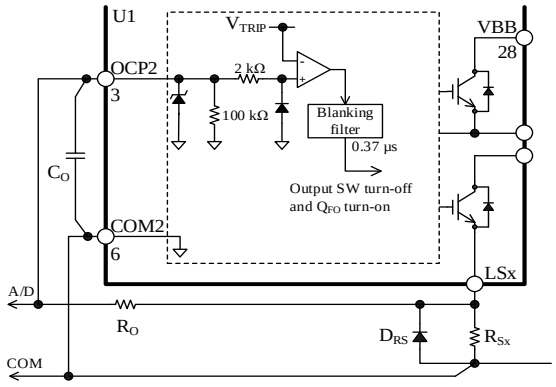

Figure 12-16. Internal Circuit Diagram of OCP2 Pin and Its Peripheral Circuit

Figure 12-17 is a timing chart that represents operation waveforms during OCP2 operation. When the OCP2 pin voltage increases to the OCP2 Threshold Voltage ($V_{TRIP(L)}$ = 0.50 V) or more, and remains in this condition for a period of the OCP Blanking Time (t_{BK} = 0.37 µs) or longer, the OCP2 circuit is activated. The enabled OCP2 circuit shuts off the low-side transistors and puts the FO pin into a low state.

Then, output current decreases as a result of the output transistor turn-offs. Even if the OCP2 pin voltage falls below $V_{TRIP(L)}$, the IC holds the FO pin in the low state for a fixed OCP hold time, $t_{P(L)}$ = 10.0 ms. Then, the output transistors operate according to input signals.

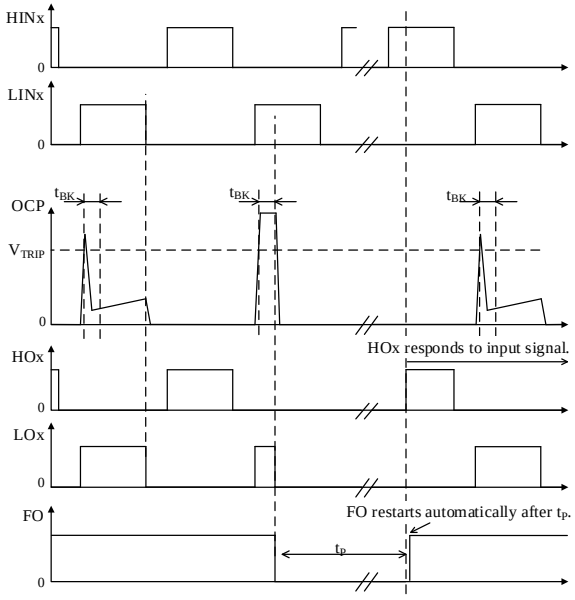

Figure 12-17. OCP2 Operational Waveforms

12.4.4 Thermal Shutdown (TSD)

The SIM1-05A1M incorporates the thermal shutdown (TSD) circuit. Figure 12-18 shows TSD operational waveforms. In case of overheating (e.g., increased power dissipation due to overload, or elevated ambient temperature at the device), the IC shuts down the low-side output transistors.

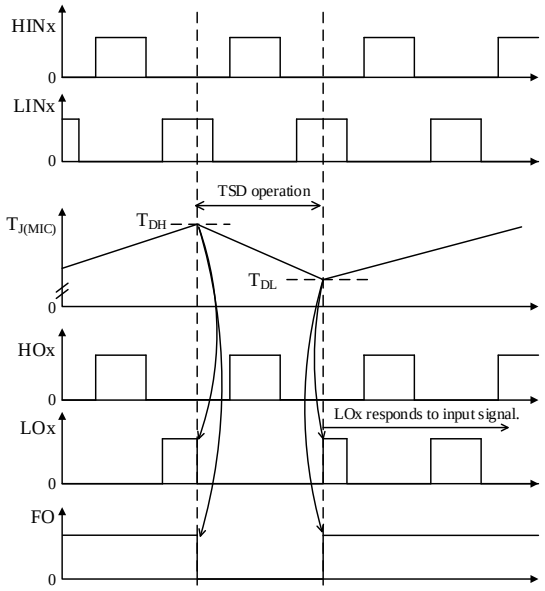

Figure 12-18. TSD Operational Waveforms

The TSD circuit in the low-side MIC monitors temperatures (see Section 7). When the temperature of the low-side MIC exceeds the TSD Operating Temperature (T_{DH} = 150 °C), the TSD circuit is activated. When the temperature of the low-side MIC decreases to the TSD Releasing Temperature (T_{DL} = 120 °C) or less, the shutdown condition is released. The output transistors then resume operating according to input signals. During the TSD operation, the FO pin becomes logic low and transmits fault signals. Note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

13. Design Notes

13.1 PCB Pattern Layout

Figure 13-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB

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trace layouts and component placements play an important role in circuit designing.

Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

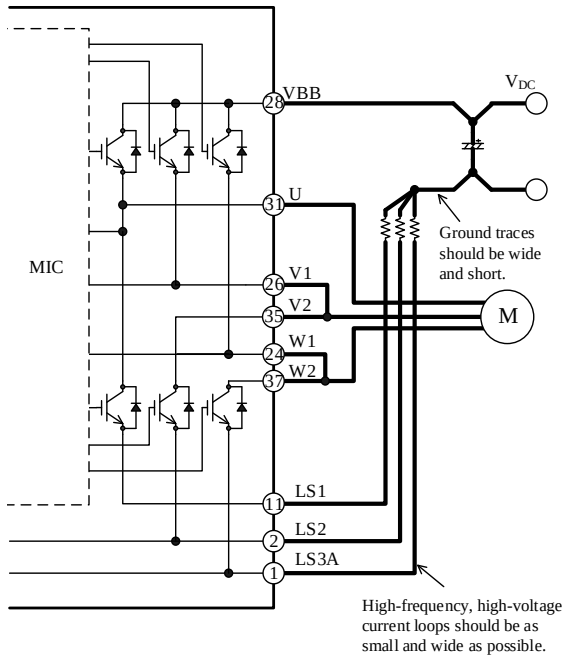

Figure 13-1. High-frequency, High-voltage Current Paths

13.2 Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- Be sure to use a metric screw of M2.5 and a plain washer of 6.0 mm (φ). When tightening the screws, use a torque screwdriver and tighten them within the range of screw torque defined in Section 4. Be sure to avoid uneven tightening. Temporarily tighten the two screws first, then tighten them equally on both sides until the specified screw torque is reached.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  - Grease thickness: 100 μm
  - Heatsink flatness: ±100 μm
  - Apply a silicone grease within the area indicated in Figure 13-2, below.

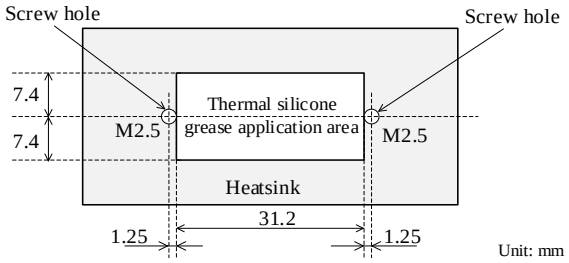

Figure 13-2. Reference Application Area for Thermal Silicone Grease

13.3 Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that the gate and emitter of each transistor should have the same potential. Moreover, care should be taken during the measurement because each transistor is connected as follows:

- All the high-side collectors are internally connected to the VBB pin.
- In the U-phase, the high-side emitter and the low-side collector are internally connected to the U pin. (In the V- and W-phases, the high- and low-side transistors are unconnected inside the IC.)

When measuring the collector-to-emitter leakage current of the low-side transistors, short the VBx pin and the output pins (the collectors of the low-side transistors) so that the VBx pin does not have an electric potential lower than that of the output pins (the collectors of the low-side transistors).

The gates of the high-side transistors are pulled down to the corresponding output (U, V/V1, and W1) pins; similarly, the gates of the low-side transistors are pulled down to the COM2 pin. When measuring the breakdown voltage or leakage current of the transistors, note that all of the output (U, V, and W1), LSx, and COMx pins must be appropriately connected. Otherwise, the output transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 13-3 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 13-4 shows the low-side transistor (Q_{1L}) in the U-phase. And all the pins that are not represented in these figures are open. When measuring the high-side transistors, leave all the non-measuring pins open. When measuring the low-side transistors, connect only the measuring LSx pin to the COMx pin and leave the other

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pins open.

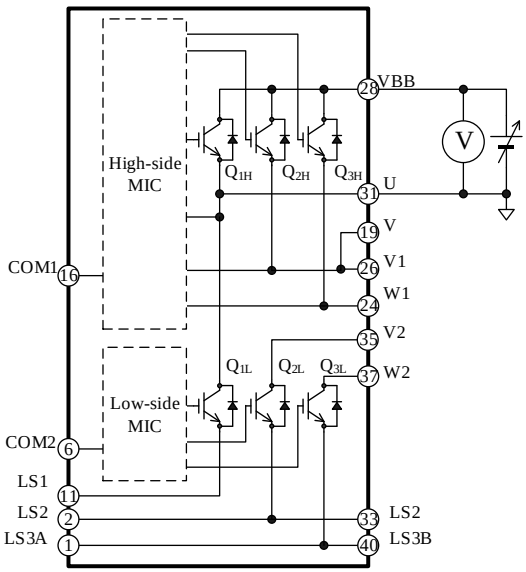

Figure 13-3. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

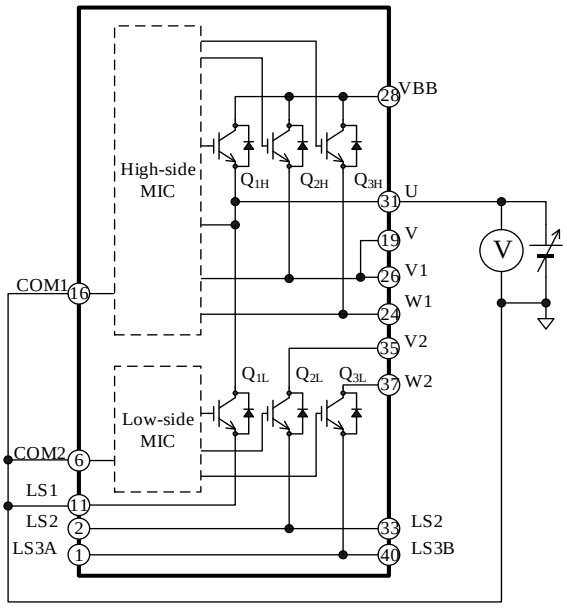

Figure 13-4. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

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14. Calculating Power Losses and Estimating Junction Temperatures

This section describes the procedures to calculate power losses in an output transistor, and to estimate a junction temperature (in all-element operation). Note that the descriptions listed here are applicable to the SIM1-05A1M, which is controlled by a 3-phase sine-wave PWM driving strategy.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0107: SIM1-05A1M Power Loss Calculation Tool
  https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbtall_caltool2_en.html

Total power loss in an output transistor can be obtained by taking the sum of IGBT steady-state loss, P_{ON}, IGBT switching loss, P_{SW}, and freewheeling diode steady-state loss, P_F. The following subsections contain the mathematical procedures to calculate these losses (P_{ON}, P_{SW}, and P_F) and the junction temperature of all IGBTs and freewheeling diodes operating.

14.1 IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, listed in Section 15.3.1. As expressed by the curves in Figure 14-1, a linear approximation at a range the I_C is actually used is obtained by: $V_{CE(SAT)} = \alpha \times I_C + \beta$. The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} + \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} + \frac{\pi}{8}M \times \cos\theta\right) I_M \ . \quad (4)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT (V),
I_C is the collector current of the IGBT (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve, and
β is the intercept of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve.

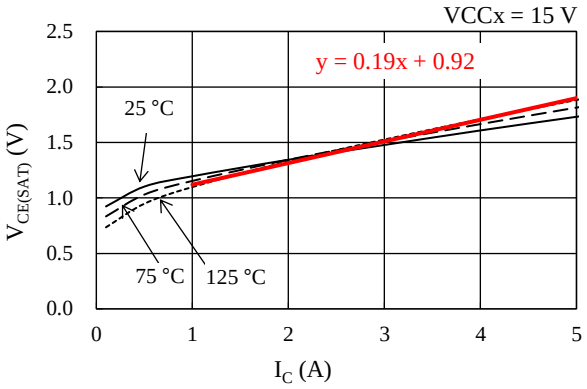

Figure 14-1. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C

14.2 IGBT Switching Loss, P_{SW}

Switching loss in an IGBT can be calculated by Equation (5), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300} \ . \quad (5)$$

Where:

f_C is the PWM carrier frequency (Hz),
V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and
α_E is the slope of the switching loss curve (see Section 15.3.2).

14.3 Estimating Junction Temperature of IGBT

The junction temperature of all IGBTs operating, T_J, can be estimated with Equation (6):

$$T_J = R_{(J-C)Q} \times \{(P_{ON} + P_{SW}) \times 6\} + T_C \ . \quad (6)$$

Where:

$R_{(J-C)Q}$ is the junction-to-case thermal resistance (°C/W) of all the IGBTs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

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14.3.1 Freewheeling Diode Steady-state Loss, P_F

Steady-state loss in a freewheeling diode can be computed by using the V_F vs. I_F curves, listed in Section 15.3.1. As expressed by the curves in Figure 14-2, a linear approximation at a range the I_F is actually used is obtained by: $V_F = \alpha \times I_F + \beta$.

The values gained by the above calculation are then applied as parameters in Equation (7), below. Hence, the equation to obtain the freewheeling diode steady-state loss, P_F, is:

$$P_F = \frac{1}{2\pi}\int_0^{\pi} V_F(\varphi) \times I_F(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right){I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right)I_M . \quad (7)$$

Where:

V_F is the forward voltage of the freewheeling diode (V),

I_F is the forward current of the freewheeling diode (A),

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current (A),

α is the slope of the linear approximation in the V_F vs. I_F curve, and

β is the intercept of the linear approximation in the V_F vs. I_F curve.

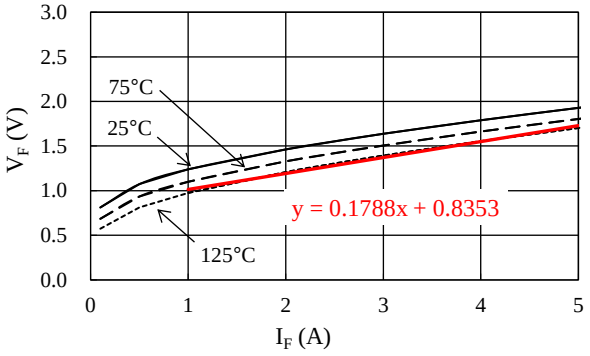

Figure 14-2. Linear Approximate Equation of V_F vs. I_F

14.3.2 Estimating Junction Temperature of Freewheeling Diode

The junction temperature of all freewheeling diodes operating, T_J, can be estimated with Equation (8):

$$T_J = R_{(J-C)F} \times (P_F \times 6) + T_C . \quad (8)$$

Where:

$R_{(J-C)F}$ is the junction-to-case thermal resistance (°C/W) of all the freewheeling diodes operating, and

T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

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15. Performance Curves

15.1 Performance Curves of Control Parts

Figure 15-1 to Figure 15-25 provide performance curves of the control parts integrated in the SIM1-05A1M, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 15-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 15-1	Logic Supply Current in 3-phase Operation, I_{CC} vs. T_C
Figure 15-2	Logic Supply Current in 3-phase Operation, I_{CC} vs. VCC Pin Voltage, V_{CC}
Figure 15-3	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C
Figure 15-4	Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C
Figure 15-5	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. VBx Pin Voltage, V_B
Figure 15-6	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 15-7	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 15-8	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 15-9	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 15-10	UVLO_VB Filtering Time vs. T_C
Figure 15-11	UVLO_VCC Filtering Time vs. T_C
Figure 15-12	Input Current at High Level (HINx or LINx), I_{IN} vs. T_C
Figure 15-13	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 15-14	Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C
Figure 15-15	High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)
Figure 15-16	Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)
Figure 15-17	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 15-18	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 15-19	FO Pin Voltage in Normal Operation, V_{FOH} vs. T_C
Figure 15-20	High-side OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 15-21	High-side OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, $t_{D(OCP)}$ vs. T_C
Figure 15-22	High-side OCP Hold Time, t_P vs. T_C
Figure 15-23	Low-side OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 15-24	Low-side OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, $t_{D(OCP)}$ vs. T_C
Figure 15-25	Low-side OCP Hold Time, t_P vs. T_C

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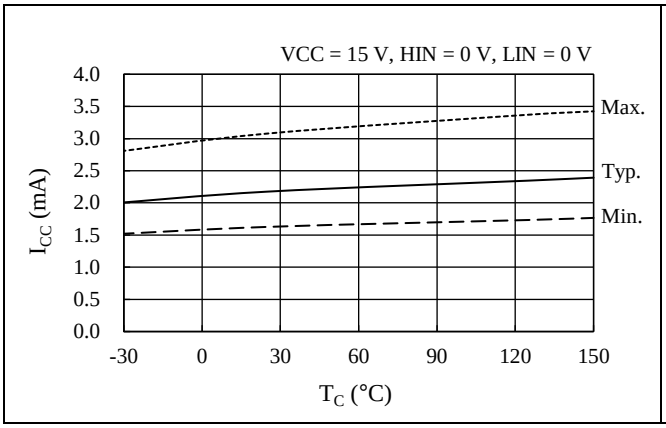

Figure 15-1. Logic Supply Current in 3-phase Operation, I_{CC} vs. T_C

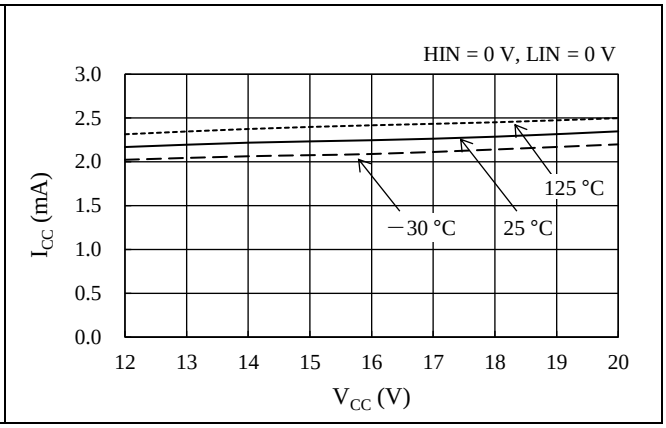

Figure 15-2. Logic Supply Current in 3-phase Operation, I_{CC} vs. VCC Pin Voltage, V_{CC}

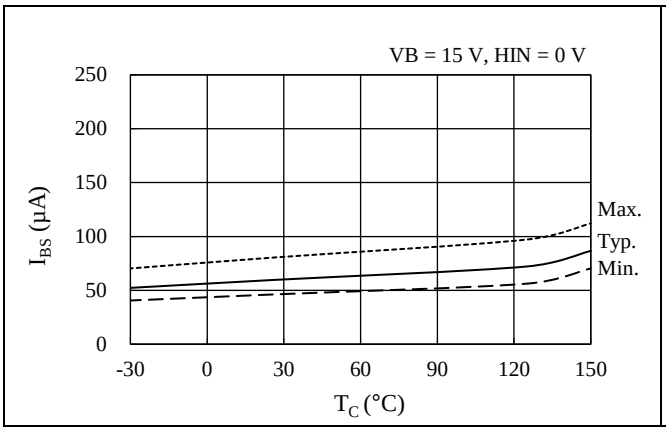

Figure 15-3. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C

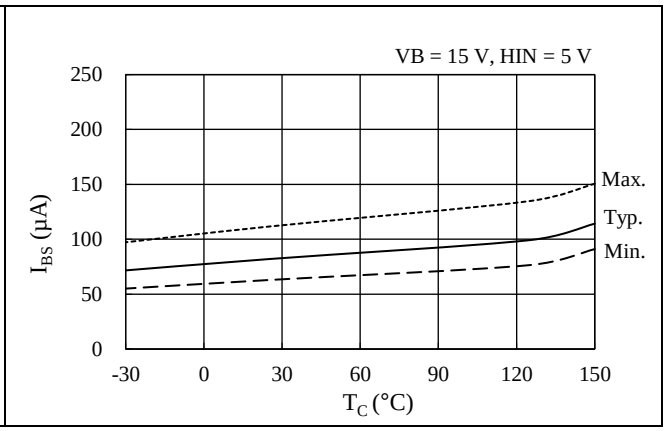

Figure 15-4. Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C

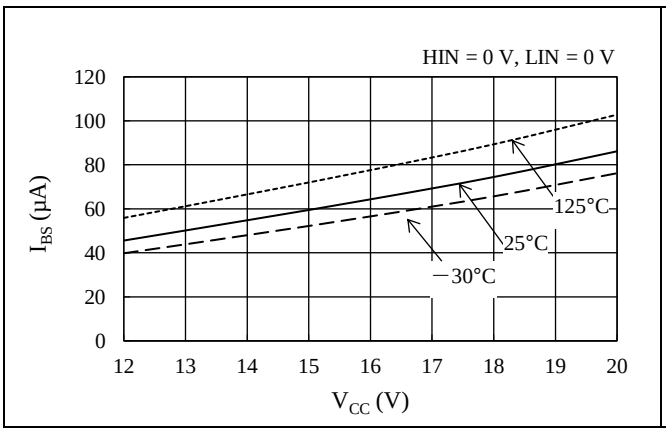

Figure 15-5. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. VBx Pin Voltage, V_B

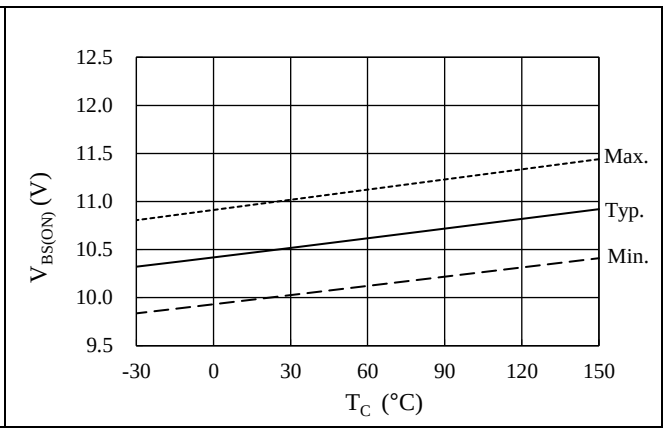

Figure 15-6. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

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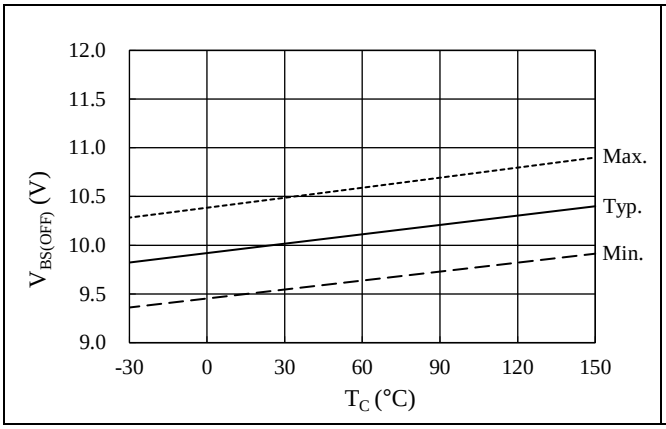

Figure 15-7. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

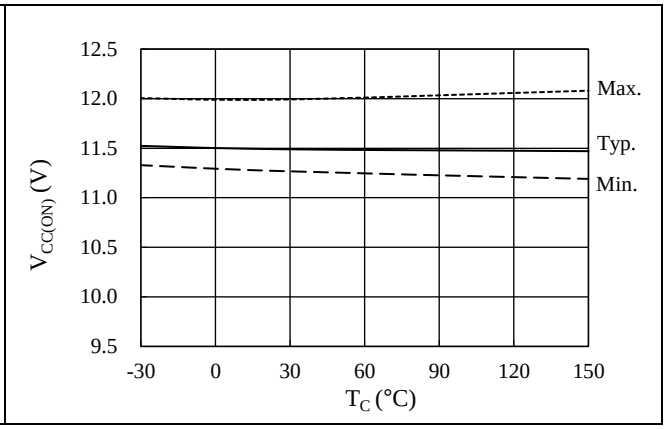

Figure 15-8. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

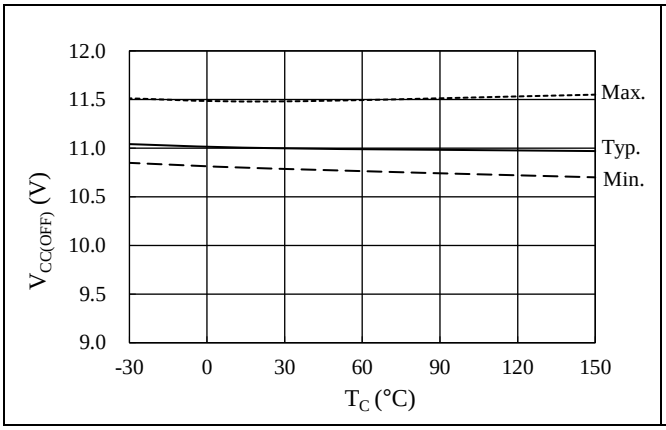

Figure 15-9. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

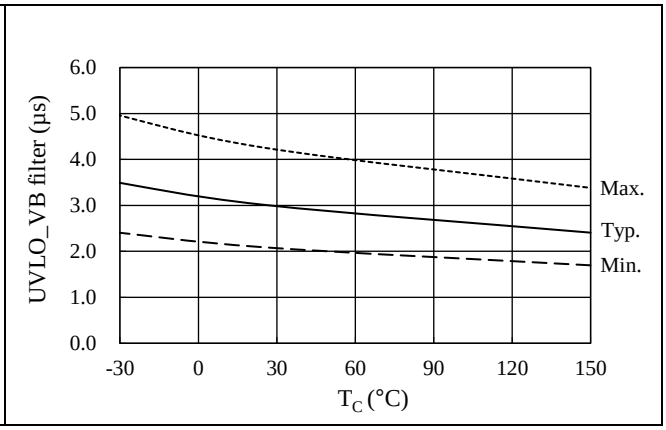

Figure 15-10. UVLO_VB Filtering Time vs. T_C

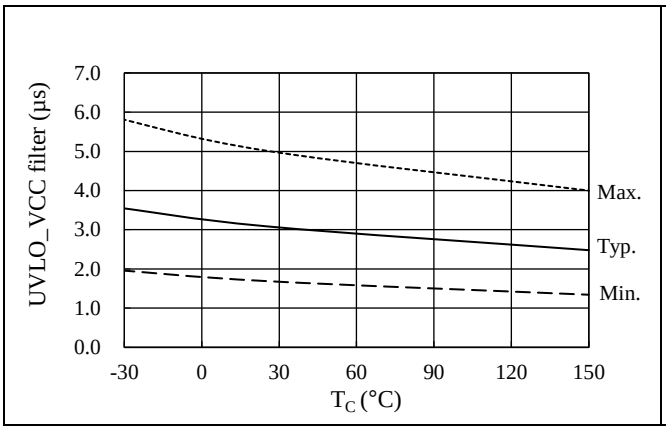

Figure 15-11. UVLO_VCC Filtering Time vs. T_C

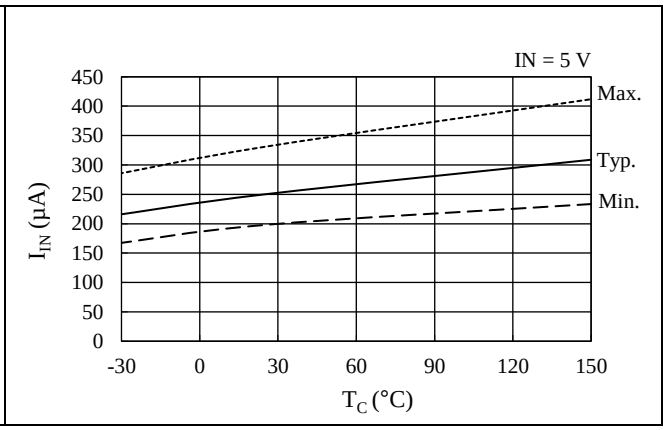

Figure 15-12. Input Current at High Level (HINx or LINx), I_{IN} vs. T_C

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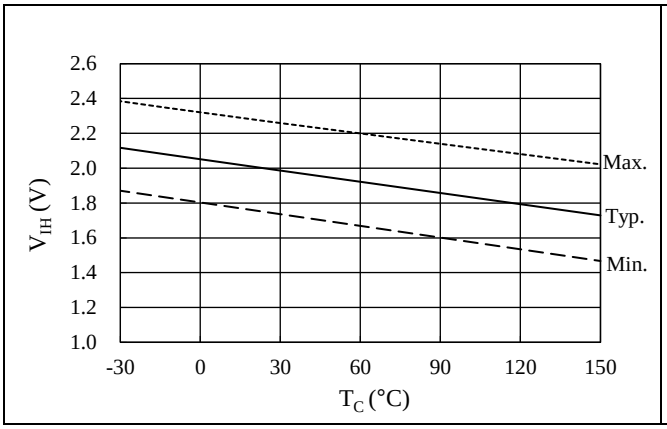

Figure 15-13. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

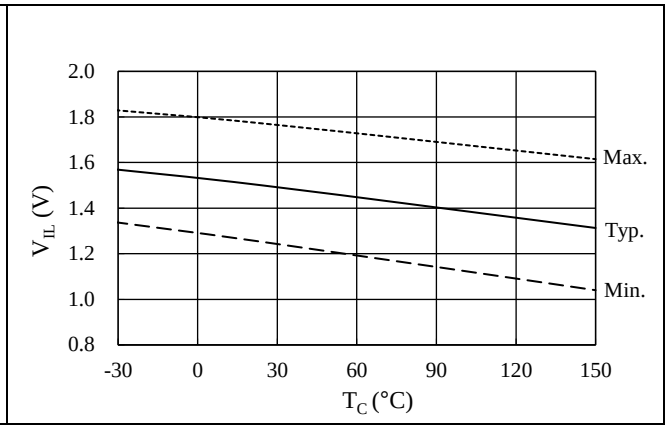

Figure 15-14. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

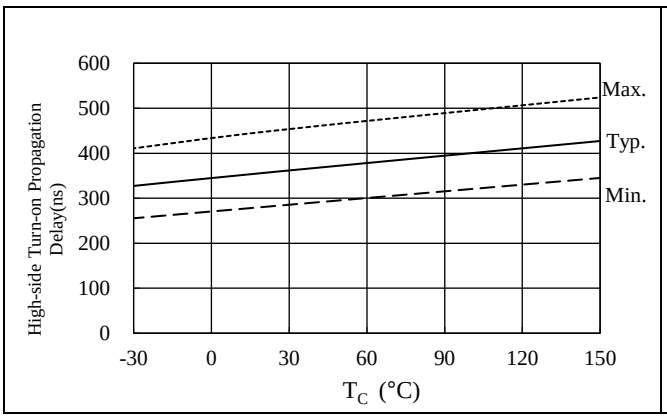

Figure 15-15. High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)

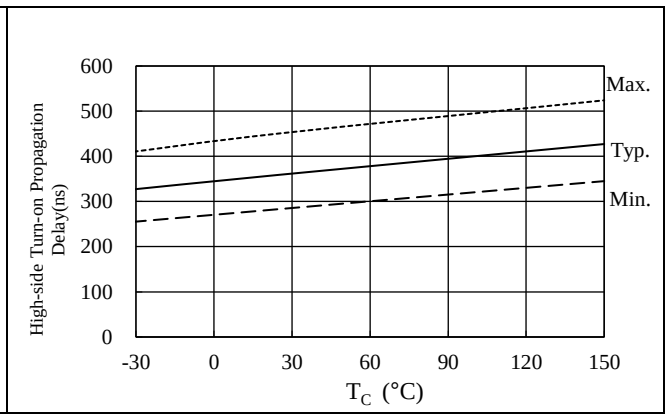

Figure 15-16. Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)

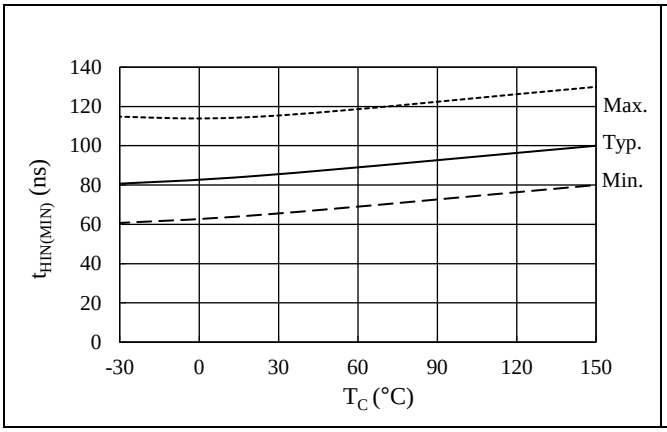

Figure 15-17. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

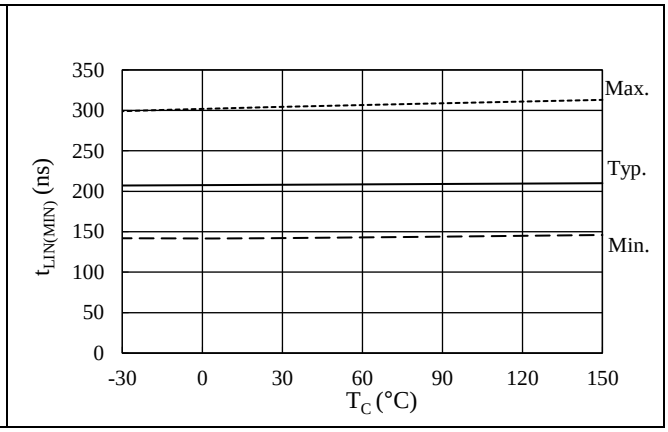

Figure 15-18. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

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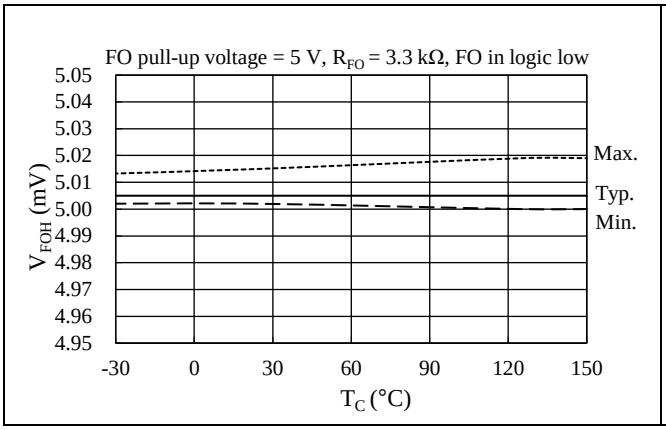

Figure 15-19. FO Pin Voltage in Normal Operation, V_{FOH} vs. T_C

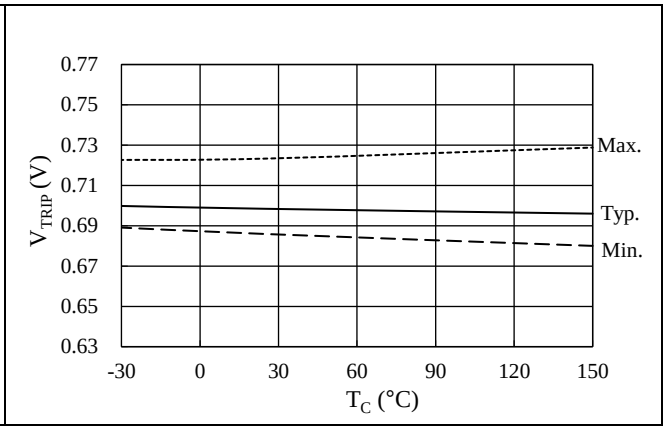

Figure 15-20. High-side OCP Threshold Voltage, V_{TRIP} vs. T_C

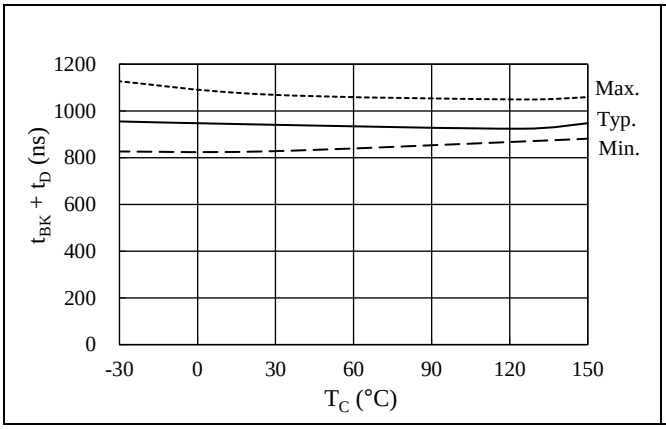

Figure 15-21. High-side OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, $t_{D(OCP)}$ vs. T_C

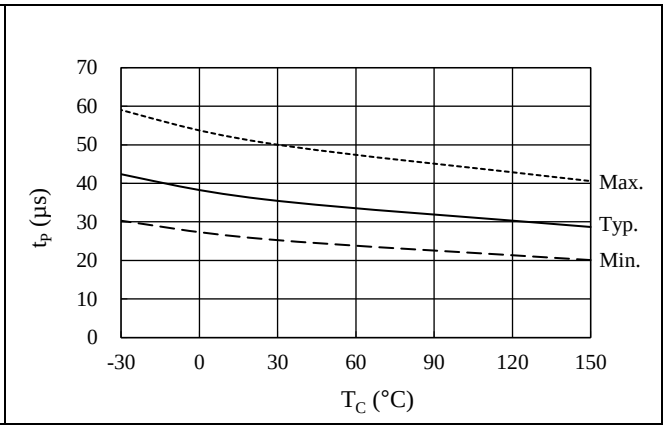

Figure 15-22. High-side OCP Hold Time, t_P vs. T_C

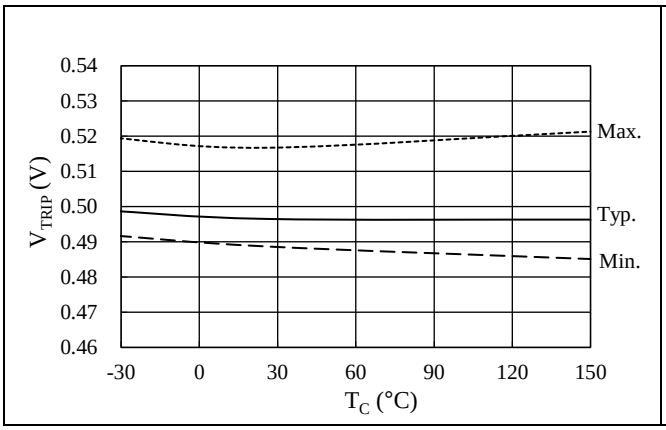

Figure 15-23. Low-side OCP Threshold Voltage, V_{TRIP} vs. T_C

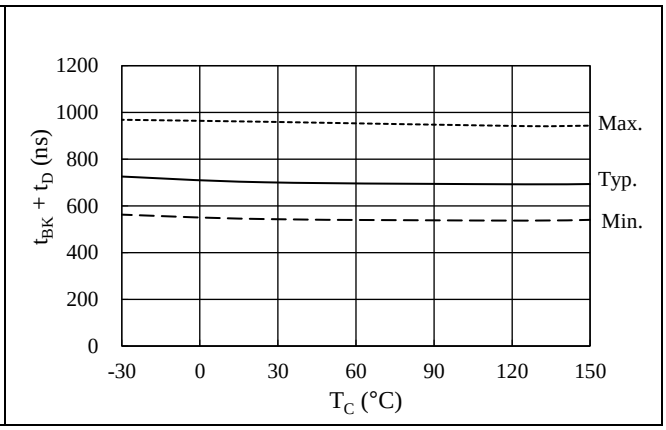

Figure 15-24. Low-side OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, $t_{D(OCP)}$ vs. T_C

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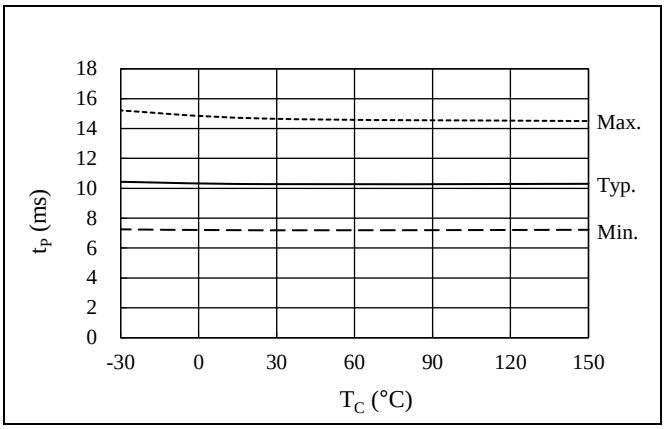

Figure 15-25. Low-side OCP Hold Time, t_P vs. T_C

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15.2 Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state junction-to-case thermal resistance = 1. Note that the graph shows only IGBT characteristics; no freewheeling diode characteristics are included.

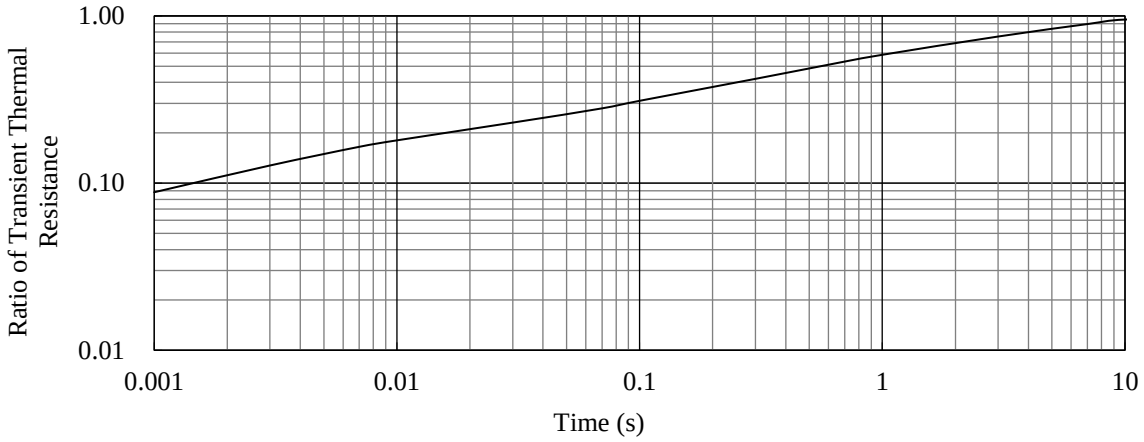

Figure 15-26. Transient Thermal Resistance

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15.3 Performance Curves of Output Parts

15.3.1 Output Transistor Performance Curves

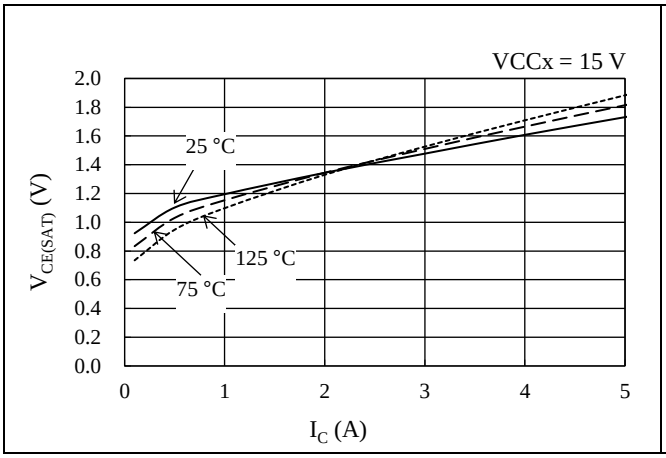

Figure 15-27. IGBT $V_{CE(SAT)}$ vs. I_C

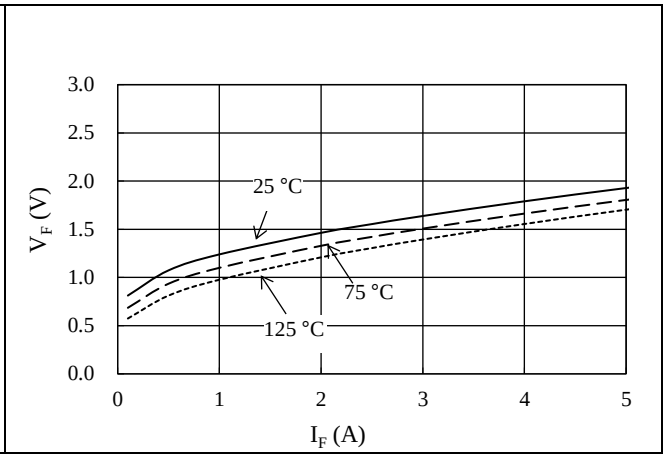

Figure 15-28. FRD V_F vs. I_F

15.3.2 Switching Loss Curves

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

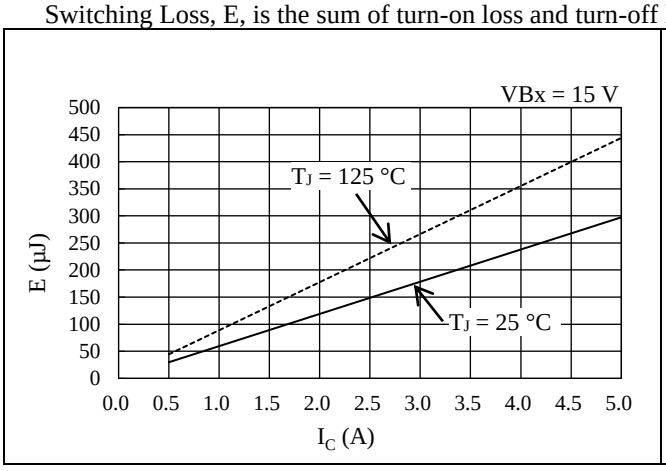

Figure 15-29. High-side Switching Loss

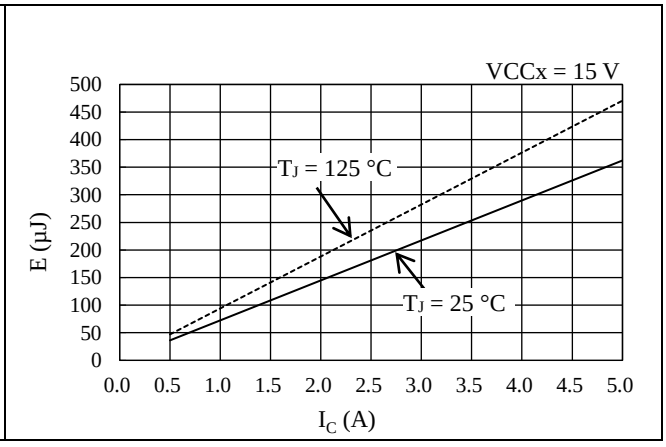

Figure 15-30. Low-side Switching Loss

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15.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $V_{CE(SAT)}$, and typical switching losses.

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCC pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

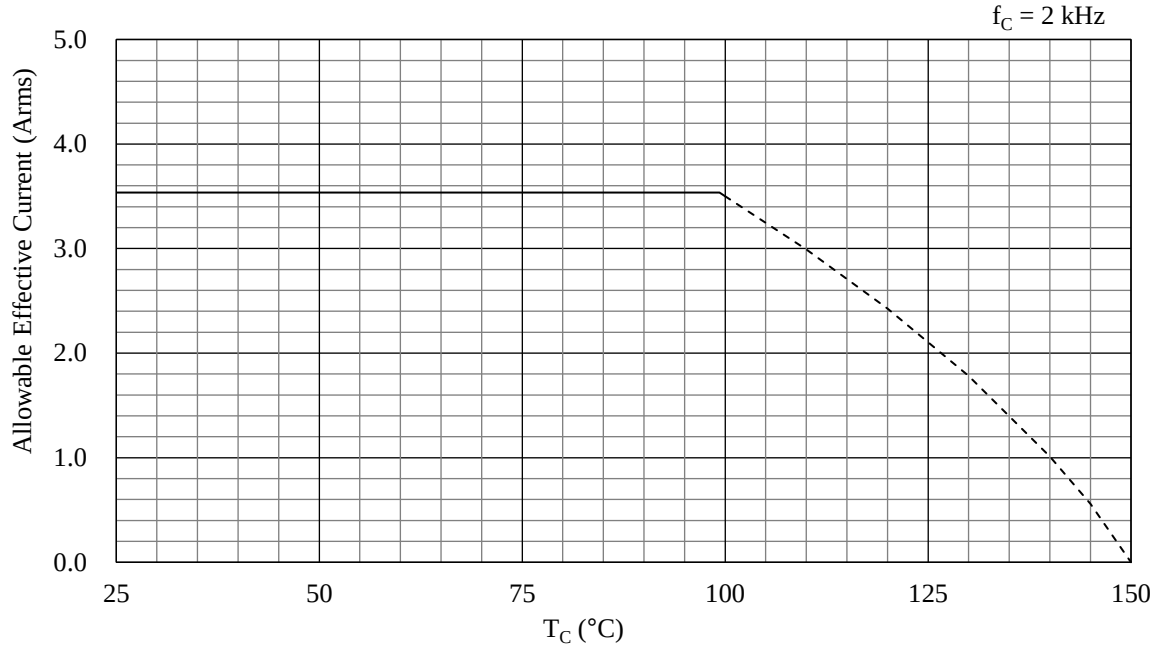

Figure 15-31. Allowable Effective Current (f_C = 2 kHz)

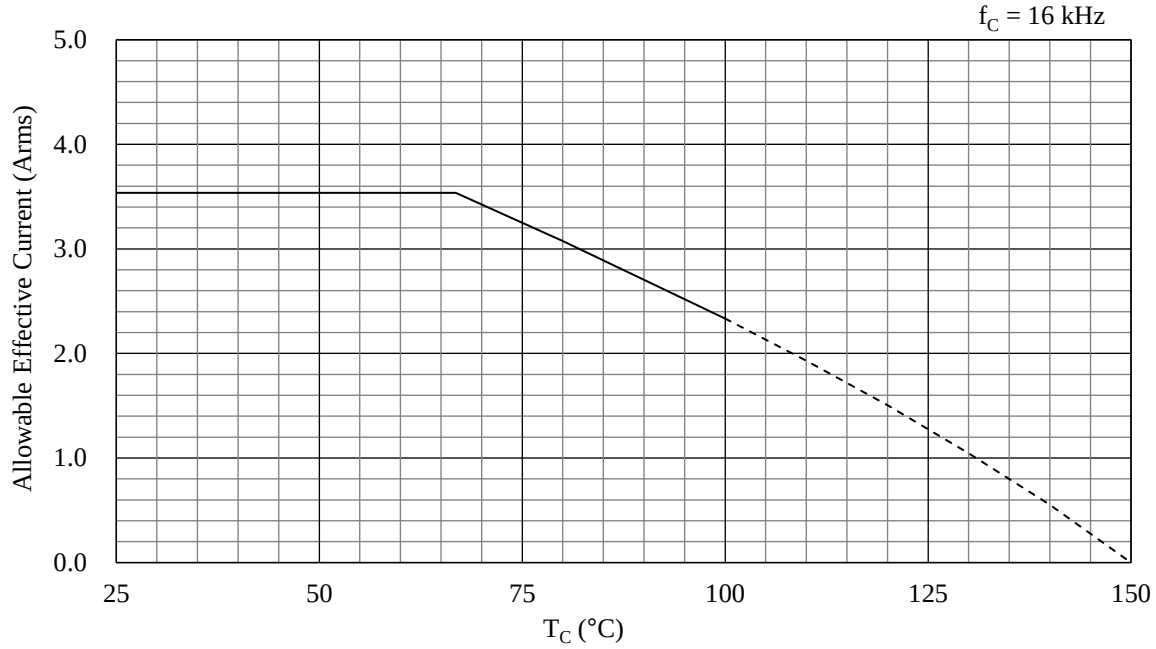

Figure 15-32. Allowable Effective Current (f_C = 16 kHz)

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15.5 Short Circuit SOAs (Safe Operating Areas)

Conditions: $V_{DC} \leq 400$ V, 13.5 V $\leq$ VCC $\leq$ 16.5 V, $T_J = 125$ °C, 1 pulse.

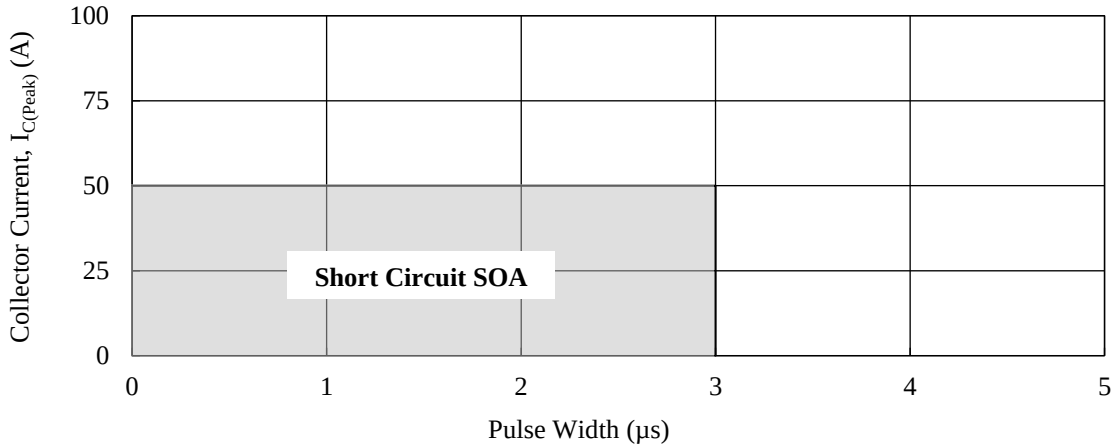

Figure 15-33. Short Circuit SOA

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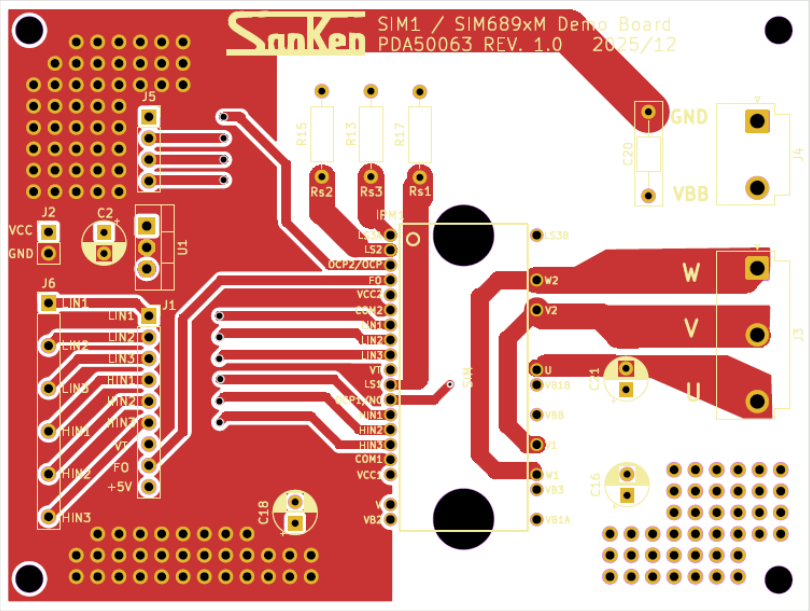
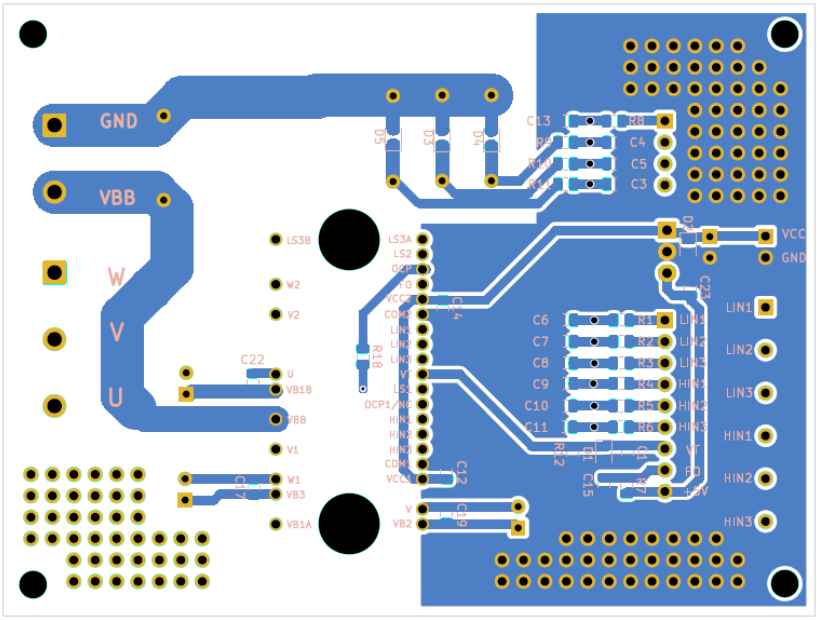
16. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SIM1-05A1M device. Note that the pattern layout example only uses the parts illustrated in the circuit diagram below. For more details on through holes, see Section 10.



(Top View)



(Bottom View)

Figure 16-1. Pattern Layout Example

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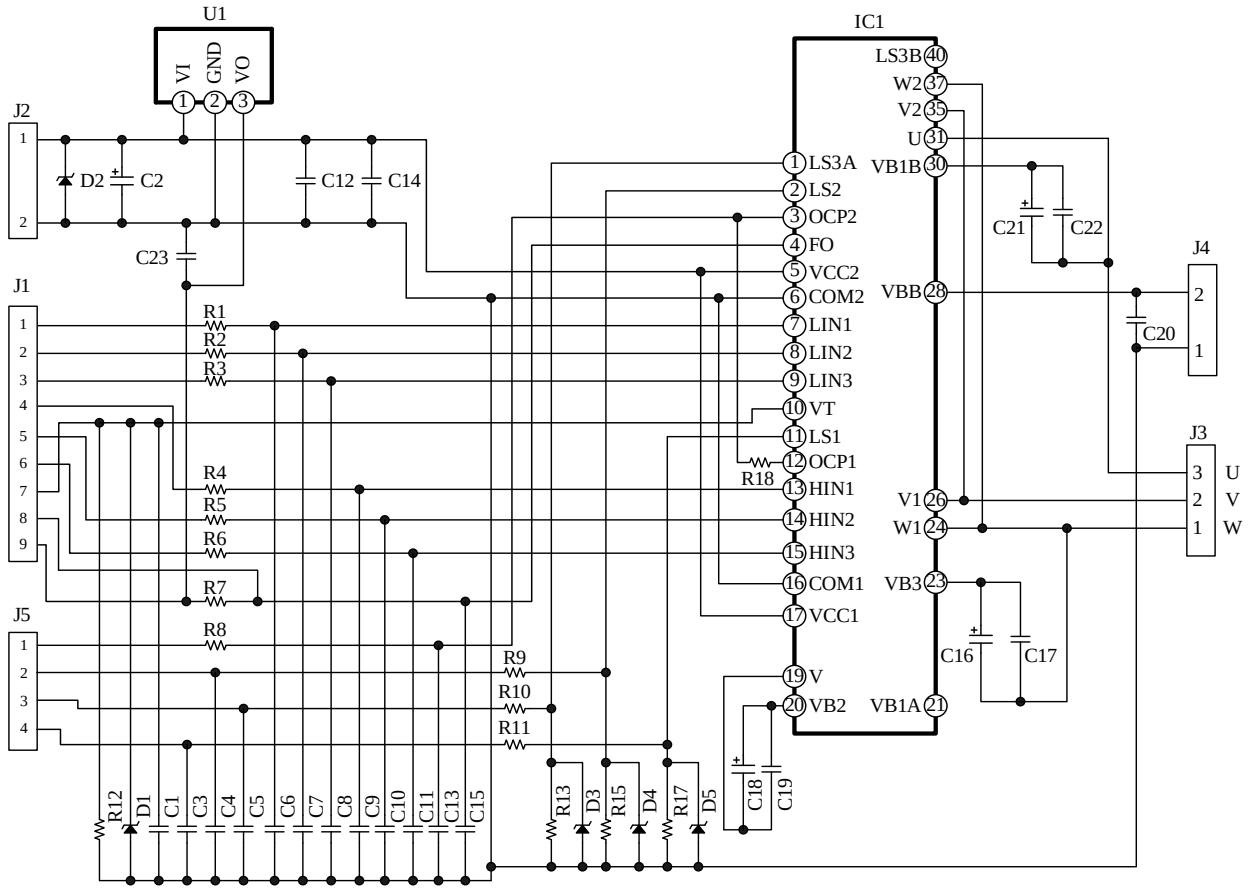

Figure 16-2. Circuit Diagram of PCB Pattern Layout Example

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17. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SIM1-05A1M
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	360 W

- **Circuit Diagram**

See Figure 16-2.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Ceramic	0.01 µF, 50 V	R3	General	100 Ω, 1/8 W
C2	Electrolytic	100 µF, 50 V	R4	General	100 Ω, 1/8 W
C3	Ceramic	100 pF, 50 V	R5	General	100 Ω, 1/8 W
C4	Ceramic	100 pF, 50 V	R6	General	100 Ω, 1/8 W
C5	Ceramic	100 pF, 50 V	R7	General	3.3 kΩ, 1/8 W
C6	Ceramic	100 pF, 50 V	R8	General	100 Ω, 1/8 W
C7	Ceramic	100 pF, 50 V	R9	General	100 Ω, 1/8 W
C8	Ceramic	100 pF, 50 V	R10	General	100 Ω, 1/8 W
C9	Ceramic	100 pF, 50 V	R11	General	100 Ω, 1/8 W
C10	Ceramic	100 pF, 50 V	R12	General	100 kΩ, 1/8 W
C11	Ceramic	100 pF, 50 V	R13*	Metal plate	72 mΩ, 2 W
C12	Ceramic	0.1 µF, 50 V	R15*	Metal plate	72 mΩ, 2 W
C13	Ceramic	8200 pF, 50 V	R17*	Metal plate	72 mΩ, 2 W
C14	Ceramic	0.1 µF, 50 V	R18	General	Short
C15	Ceramic	0.01 µF, 50 V	D1	Zener diode	Open
C16	Electrolytic	47 µF, 50 V	D2	Zener diode	Open
C17	Ceramic	100 pF, 50 V	D3	Zener diode	Open
C18	Electrolytic	47 µF, 50 V	D4	Zener diode	Open
C19	Ceramic	100 pF, 50 V	D5	Zener diode	Open
C20	Film	0.033 µF, 630 V	J1	Connector	Equiv. to MA09-1
C21	Electrolytic	47 µF, 50 V	J2	Connector	Equiv. to MA02-1
C22	Ceramic	100 pF, 50 V	J3	Pin header	Equiv. to B2P5-VH
C23	Ceramic	100 nF, 50 V	J4	Pin header	Equiv. to B2P3-VH
R1	General	100 Ω, 1/8 W	J5	Connector	Equiv. to MA04-1
R2	General	100 Ω, 1/8 W	IC1	IC	SIM1-05A1M
			U1	IC	LM7805

* Refers to a part that requires adjustment based on operation performance in an actual application.

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