

**600 V, 15 A**  
**High Voltage 3-phase Motor Driver**  
**SIM2-151A**

**Description**

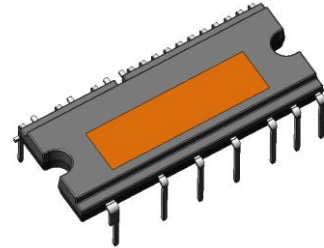
The SIM2-151A is a high voltage 3-phase motor driver in which transistors, pre-drive circuits, and bootstrap diodes with current-limiting resistors are highly integrated. The product can run on a 3-shunt current detection system and optimally control the inverter systems of medium-capacity motors that require universal input standards. The product uses a compact DIP40 package and supports an output current of 15 A.

**Features**

- Pb-free (RoHS Compliant)
- Isolation Voltage: 2000 V (for 1 min)  
UL-recognized Component (File No.: E118037)
- Temperature Sensing Function
- Built-in Bootstrap Diodes with Current Limiting Resistors (250 Ω)
- CMOS-compatible Input (3.3 V or 5 V)
- Fault Signal Output at Protection Activation
- Protections Include:
  - Undervoltage Lockout for Power Supply
    - High-side (UVLO\_VB): Auto-restart
    - Low-side (UVLO\_VCC): Auto-restart
  - Overcurrent Protection (OCP): Auto-restart
  - Thermal Shutdown (TSD): Auto-restart, TSD operation temperature  $\pm 5\text{ }^{\circ}\text{C}$

**Package**

DIP40  
 Pin Pitch: 1.778 mm  
 Mold Dimensions: 35.7 mm × 14.6 mm × 4.2 mm



Not to scale

**Specifications**

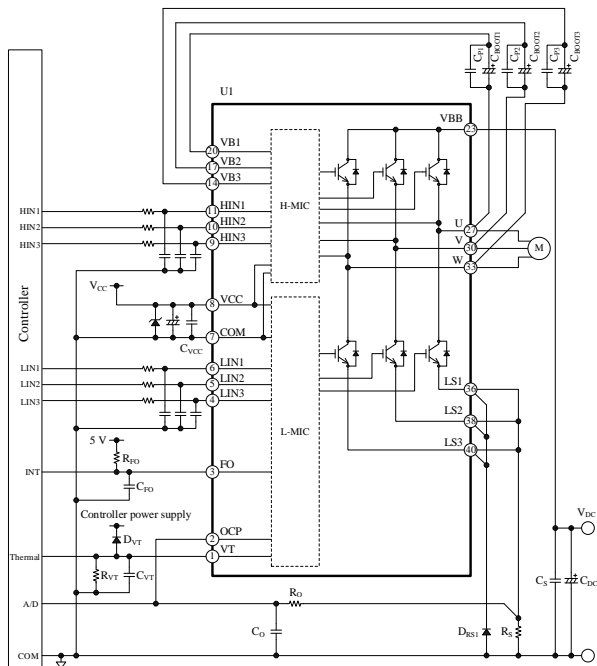
- Breakdown Voltage: 600 V
- Output Current: 15 A

**Applications**

For motor drives such as:

- Refrigerator Compressor Motor
- Air Conditioner Compressor Motor

**Typical Application**



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## 1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (-).

Unless specifically noted,  $T_A = 25\text{ }^\circ\text{C}$ .

| Parameter                                 | Symbol          | Conditions  | Rating     | Unit             |
|---|-----------------|---|------------|------------------|
| Main Supply Voltage (DC)                  | $V_{DC}$        | VBB-LSx   | 450        | V                |
| Main Supply Voltage (Surge)               | $V_{DC(SURGE)}$ | VBB-LSx   | 500        | V                |
| IGBT Breakdown Voltage                    | $V_{CES}$       | $V_{CC} = 15\text{ V}$ , $I_C = 100\text{ }\mu\text{A}$ ,<br>$V_{IN} = 0\text{ V}$                                    | 600        | V                |
| Logic Supply Voltage                      | $V_{CC}$        | VCC-COM   | 20         | V                |
|   | $V_{BS}$        | VBx-U/V/W   | 20         |                  |
| Output Current <sup>(1)</sup>             | $I_O$           | $T_C = 25\text{ }^\circ\text{C}$ , $T_J < 150\text{ }^\circ\text{C}$  | 15         | A                |
| Output Current (Pulse)                    | $I_{OP}$        | $T_C = 25\text{ }^\circ\text{C}$ ,<br>pulse width $\leq 100\text{ }\mu\text{s}$ , duty<br>cycle = 1%,<br>single pulse | 30         | A                |
| Input Voltage                             | $V_{IN}$        | HINx-COM,<br>LINx-COM   | -0.5 to 7  | V                |
| FO Pin Voltage                            | $V_{FO}$        | FO-COM  | -0.5 to 7  | V                |
| OCP Pin Voltage                           | $V_{OCP}$       | OCP-COM   | -10 to 7   | V                |
| Operating Case Temperature <sup>(2)</sup> | $T_{C(OP)}$     |   | -30 to 100 | $^\circ\text{C}$ |
| Junction Temperature <sup>(3)</sup>       | $T_J$           |   | 150        | $^\circ\text{C}$ |
| Storage Temperature                       | $T_{STG}$       |   | -40 to 150 | $^\circ\text{C}$ |
| Isolation Voltage <sup>(4)</sup>          | $V_{ISO(RMS)}$  | Between surface of heatsink<br>side and each pin; AC, 60 Hz,<br>1 min   | 2000       | V                |

<sup>(1)</sup> Should be derated depending on an actual case temperature. See Section 15.3.

<sup>(2)</sup> Refers to a case temperature measured during IC operation.

<sup>(3)</sup> Refers to the junction temperature of each chip built in the IC, including the control MICs, transistors, and freewheeling diodes.

<sup>(4)</sup> Refers to voltage conditions to be applied between all of the pins and the case. All the pins have to be shorted.

## 2. Recommended Operating Conditions

| Parameter                                | Symbol           | Conditions         | Min.  | Typ. | Max. | Unit       |
|--|------------------|--------------------|-------|------|------|------------|
| Main Supply Voltage                      | $V_{DC}$         | VBB-COM            | —     | 300  | 400  | V          |
| Logic Supply Voltage                     | $V_{CC}$         | VCC-COM            | 13.5  | —    | 16.5 | V          |
|  | $V_{BS}$         | VBx-U/V/W          | 13    | —    | 16.5 | V          |
| Input Voltage<br>(HINx, LINx)            | $V_{IN}$         |                    | 0     | —    | 5.5  | V          |
| Minimum Input Pulse Width                | $t_{IN(MIN)ON}$  |                    | 0.5   | —    | —    | $\mu$ s    |
|  | $t_{IN(MIN)OFF}$ |                    | 0.5   | —    | —    | $\mu$ s    |
| Dead Time of Input Signal                | $t_{DEAD}$       |                    | 1.5   | —    | —    | $\mu$ s    |
| FO Pin Pull-up Resistor                  | $R_{FO}$         |                    | 3.3   | —    | 10   | k $\Omega$ |
| FO Pin Pull-up Voltage                   | $V_{FO}$         |                    | 3.0   | —    | 5.5  | V          |
| FO Pin Noise Filter Capacitor            | $C_{FO}$         |                    | 0.001 | —    | 0.01 | $\mu$ F    |
| VT Pin Pull-down Resistor <sup>(1)</sup> | $R_{VT}$         |                    | 100   | —    | —    | k $\Omega$ |
| VT Pin Pull-down Capacitor               | $C_{VT}$         |                    | 0.001 | —    | 0.01 | $\mu$ F    |
| Bootstrap Capacitor                      | $C_{BOOT}$       |                    | 10    | —    | 220  | $\mu$ F    |
| Shunt Resistor <sup>(2)</sup>            | $R_S$            | $I_{OP} \leq 30$ A | 18    | —    | —    | m $\Omega$ |
| RC Filter Resistor <sup>(3)</sup>        | $R_O$            |                    | —     | —    | 100  | $\Omega$   |
| RC Filter Capacitor                      | $C_O$            |                    | —     | —    | 10   | nF         |
| PWM Carrier Frequency                    | $f_C$            |                    | —     | —    | 20   | kHz        |

<sup>(1)</sup> Refers to a combined resistance with the input impedance of the microcontroller.

<sup>(2)</sup> Should be a low-inductance resistor.

<sup>(3)</sup> Requires the time constants that satisfy the following equation (see also Section 12.4.3):  $R_O \times C_O < 1.0 \mu$ s .

### 3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (-).

Unless specifically noted,  $T_A = 25\text{ °C}$ ,  $V_{CC} = 15\text{ V}$ .

#### 3.1. Characteristics of Control Parts

| Parameter  | Symbol        | Conditions   | Min.  | Typ.  | Max.  | Unit               |
|--|---------------|--|-------|-------|-------|--------------------|
| <b>Power Supply Operation</b>                      |               |  |       |       |       |                    |
| Logic Operation Start Voltage                      | $V_{CC(ON)}$  | VCC-COM  | 10.5  | 11.5  | 12.5  | V                  |
|  | $V_{BS(ON)}$  | VBx-U/V/W  | 9.5   | 10.5  | 11.5  | V                  |
| Logic Operation Stop Voltage                       | $V_{CC(OFF)}$ | VCC-COM  | 10.0  | 11.0  | 12.0  | V                  |
|  | $V_{BS(OFF)}$ | VBx-U/V/W  | 9.0   | 10.0  | 11.0  | V                  |
| Logic Supply Current                               | $I_{CC}$      |  | —     | 2.3   | —     | mA                 |
|  | $I_{BS}$      | VBx-U/V/W = 15 V,<br>HINx = 5 V; VBx pin<br>current in 1-phase operation | —     | 85    | 180   | $\mu\text{A}$      |
| <b>Input Signal</b>                                |               |  |       |       |       |                    |
| High Level Input Threshold Voltage<br>(HINx, LINx) | $V_{IH}$      |  | —     | 2.0   | 2.5   | V                  |
| Low Level Input Threshold Voltage<br>(HINx, LINx)  | $V_{IL}$      |  | 1.0   | 1.5   | —     | V                  |
| High Level Input Current<br>(HINx, LINx)           | $I_{IH}$      | $V_{IN} = 5\text{ V}$  | —     | 250   | 500   | $\mu\text{A}$      |
| Low Level Input Current<br>(HINx, LINx)            | $I_{IL}$      | $V_{IN} = 0\text{ V}$  | —     | —     | 2     | $\mu\text{A}$      |
| <b>Fault Signal Output</b>                         |               |  |       |       |       |                    |
| FO Pin Voltage at Fault Signal<br>Output           | $V_{FOL}$     | $V_{FO} = 5\text{ V}$ , $R_{FO} = 10\text{ k}\Omega$                     | 0     | —     | 0.5   | V                  |
| FO Pin Voltage in Normal Operation                 | $V_{FOH}$     | $V_{FO} = 5\text{ V}$ , $R_{FO} = 10\text{ k}\Omega$                     | 4.8   | —     | —     | V                  |
| <b>Protection</b>                                  |               |  |       |       |       |                    |
| OCP Threshold Voltage                              | $V_{TRIP}$    | OCP-COM  | 0.475 | 0.50  | 0.525 | V                  |
| OCP Blanking Time                                  | $t_{BK(OCP)}$ | $V_{OCP} = 1.0\text{ V}$   | —     | 370   | —     | ns                 |
| OCP Hold Time                                      | $t_p$         |  | 5     | 10    | —     | ms                 |
| Temperature Sensing Voltage <sup>(1)(2)</sup>      | $V_T$         | $T_{J(L-MIC)} = 125\text{ °C}$   | 3.003 | 3.130 | 3.256 | V                  |
| TSD Operating Temperature <sup>(2)</sup>           | $T_{DH}$      | No heatsink  | 115   | 120   | 125   | $^{\circ}\text{C}$ |
| TSD Releasing Temperature <sup>(2)</sup>           | $T_{DL}$      | No heatsink  | 95    | 100   | 105   | $^{\circ}\text{C}$ |

<sup>(1)</sup> Determined by the junction temperature of the low-side control parts, but not of the output transistors.

<sup>(2)</sup> Guaranteed by design.

### 3.2. Bootstrap Diode Characteristics

| Parameter                                      | Symbol     | Conditions                        | Min. | Typ. | Max. | Unit          |
|--|------------|-----------------------------------|------|------|------|---------------|
| Bootstrap Diode Leakage Current                | $I_{LBD}$  | $V_R = 600 \text{ V}$             | —    | —    | 10   | $\mu\text{A}$ |
| Bootstrap Diode Forward Voltage <sup>(1)</sup> | $V_{FB}$   | $I_{FB} = 10 \text{ mA}$          | —    | 3.2  | —    | V             |
| Bootstrap Diode Series Resistor                | $R_{BOOT}$ | $T_C = 25 \text{ }^\circ\text{C}$ | —    | 250  | —    | $\Omega$      |

### 3.3. Thermal Resistance Characteristics

| Parameter  | Symbol                      | Conditions                               | Min. | Typ. | Max. | Unit               |
|--|-----------------------------|--|------|------|------|--------------------|
| Junction-to-Case Thermal Resistance <sup>(2)</sup> | $R_{(J-C)Q}$ <sup>(3)</sup> | 1 element operating (IGBT)               | —    | —    | 3.6  | $^\circ\text{C/W}$ |
|  | $R_{(J-C)F}$ <sup>(4)</sup> | 1 element operating (freewheeling diode) | —    | —    | 3.8  | $^\circ\text{C/W}$ |

<sup>(1)</sup> Includes a voltage drop in the current-limiting resistor.

<sup>(2)</sup> Refers to a case temperature at the measurement point described in Figure 3-1, below.

<sup>(3)</sup> Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 15.4.

<sup>(4)</sup> Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

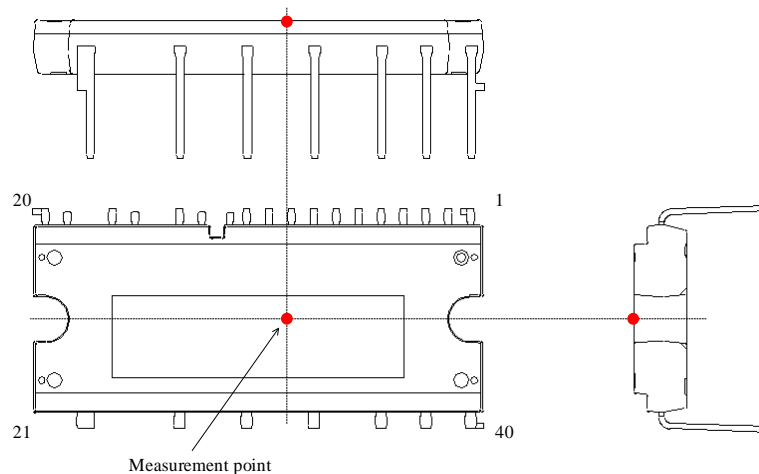


Figure 3-1. Case Temperature Measurement Point

3.4. Transistor Characteristics

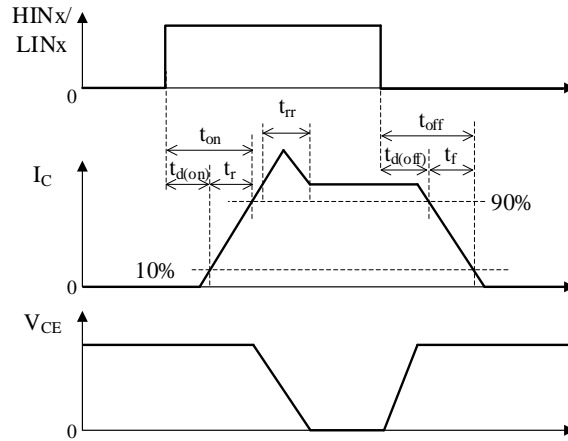


Figure 3-2. Switching Characteristics Definitions

| Parameter                               | Symbol        | Conditions  | Min. | Typ. | Max. | Unit |
|---|---------------|---|------|------|------|------|
| Collector-to-Emitter Leakage Current    | $I_{CES}$     | $V_{CE} = 600\text{ V}, V_{IN} = 0\text{ V}$  | —    | —    | 1    | mA   |
| Collector-to-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C = 10\text{ A}, V_{IN} = 5\text{ V}$  | —    | 1.6  | 2.0  | V    |
| Diode Forward Voltage                   | $V_F$         | $I_F = 10\text{ A}, V_{IN} = 0\text{ V}$  | —    | 1.75 | 2.15 | V    |
| <b>High-side Switching</b>              |               |   |      |      |      |      |
| Diode Reverse Recovery Time             | $t_{rr}$      | $V_{DC} = 300\text{ V},$<br>$I_C = 15\text{ A},$<br>$V_{IN} = 0 \rightarrow 5\text{ V}$ or $5 \rightarrow 0\text{ V},$<br>$T_J = 25\text{ }^\circ\text{C},$<br>inductive load | —    | 145  | —    | ns   |
| Turn-on Delay Time                      | $t_{d(on)}$   |   | —    | 370  | —    | ns   |
| Rise Time                               | $t_r$         |   | —    | 60   | —    | ns   |
| Turn-off Delay Time                     | $t_{d(off)}$  |   | —    | 610  | —    | ns   |
| Fall Time                               | $t_f$         |   | —    | 155  | —    | ns   |
| <b>Low-side Switching</b>               |               |   |      |      |      |      |
| Diode Reverse Recovery Time             | $t_{rr}$      | $V_{DC} = 300\text{ V},$<br>$I_C = 15\text{ A},$<br>$V_{IN} = 0 \rightarrow 5\text{ V}$ or $5 \rightarrow 0\text{ V},$<br>$T_J = 25\text{ }^\circ\text{C},$<br>inductive load | —    | 150  | —    | ns   |
| Turn-on Delay Time                      | $t_{d(on)}$   |   | —    | 370  | —    | ns   |
| Rise Time                               | $t_r$         |   | —    | 65   | —    | ns   |
| Turn-off Delay Time                     | $t_{d(off)}$  |   | —    | 610  | —    | ns   |
| Fall Time                               | $t_f$         |   | —    | 155  | —    | ns   |



4. Mechanical Characteristics

| Parameter                            | Conditions      | Min.  | Typ. | Max.  | Unit |
|--------------------------------------|-----------------|-------|------|-------|------|
| Heatsink Mounting Screw Torque       | *               | 0.588 | —    | 0.784 | N·m  |
| Flatness of Heatsink Attachment Area | See Figure 4-1. | 0     | —    | 100   | μm   |
| Package Weight                       |                 | —     | 6    | —     | g    |

\* Requires using a metric screw of M3 and a plain washer of 7 mm (φ). For more on screw tightening, see Section 13.2.

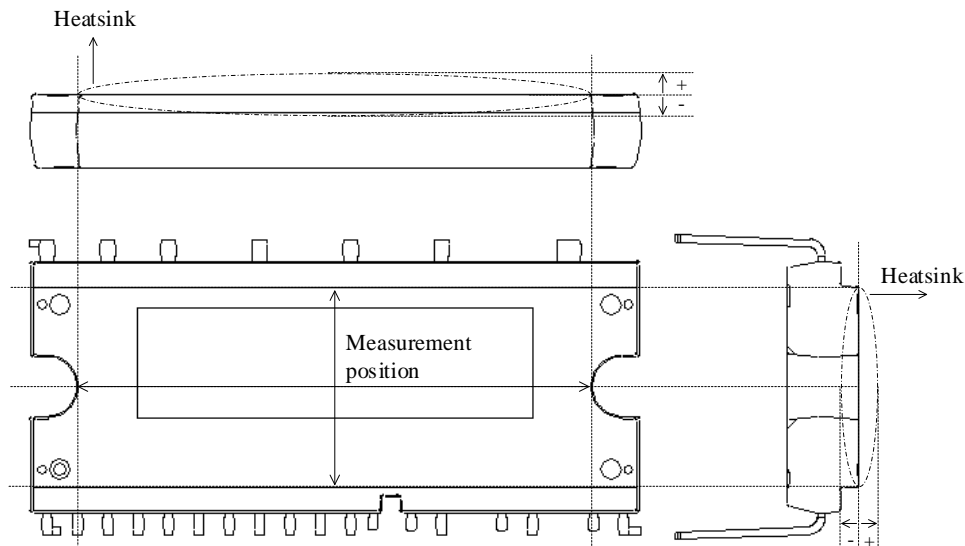


Figure 4-1. Flatness Measurement Position

5. Insulation Distance

| Parameter | Conditions                   | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|------|------|------|------|
| Clearance | Between heatsink* and leads. | —    | 1.98 | —    | mm   |
| Creepage  | See Figure 5-1.              | 3.2  | —    | —    | mm   |

\* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

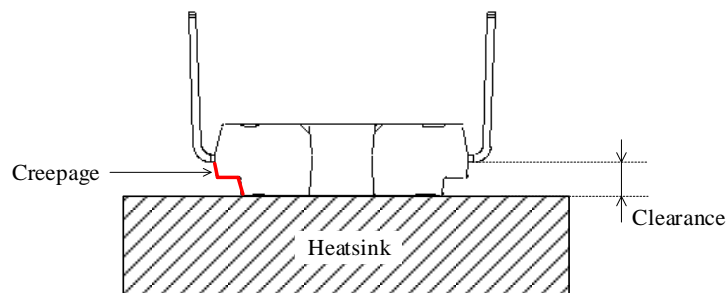


Figure 5-1. Insulation Distance Definitions

## 6. Truth Table

Table 6-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx pin signals in each phase are high at the same time, both the high- and low-side IGBTs become on (simultaneous on-state). Therefore, the input signals for the HINx and LINx pins, require dead time setting so that such a simultaneous on-state event can be avoided.

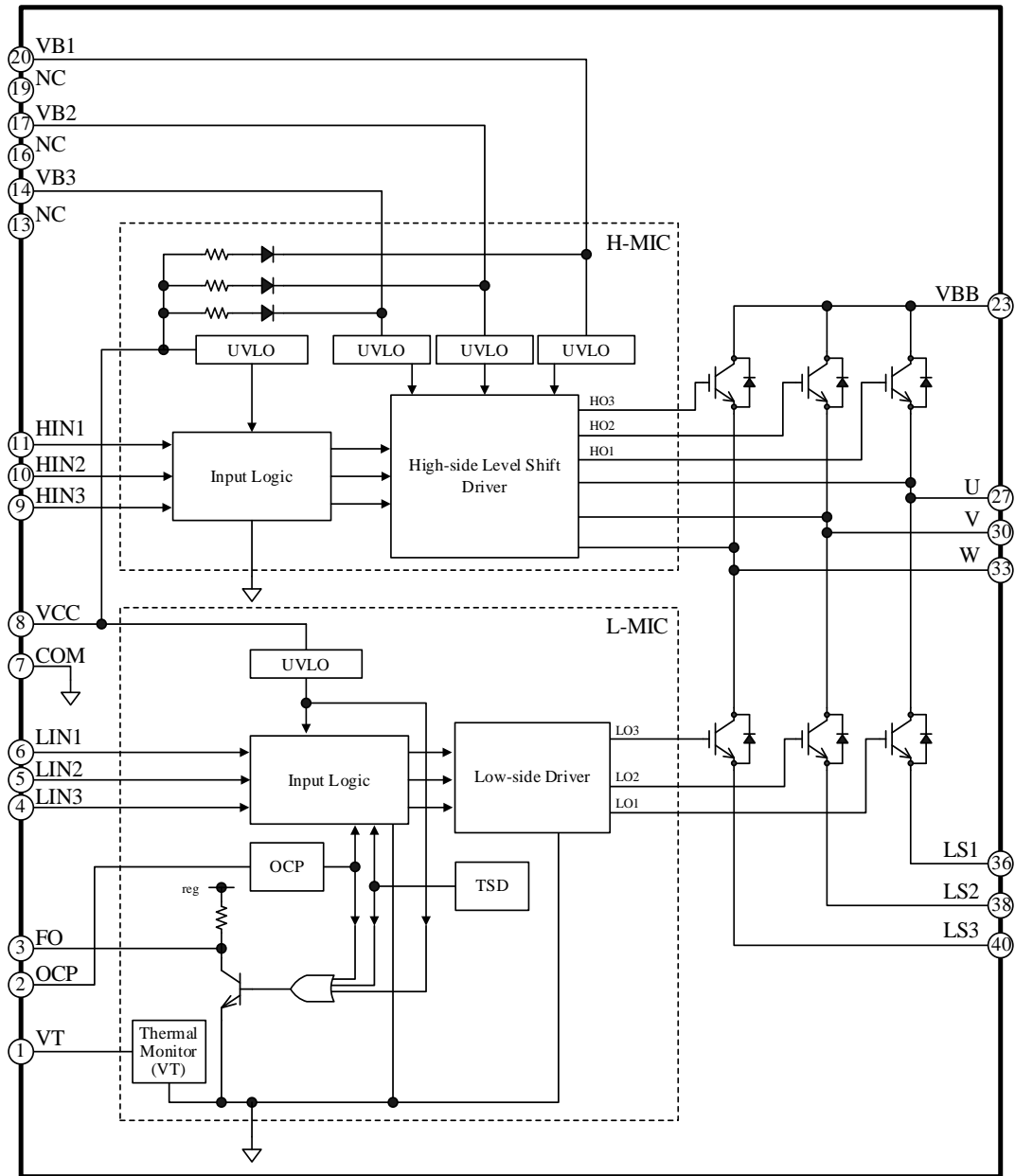
After the IC recovers from a UVLO\_VCC condition, the high- and low-side transistors resume switching, according to the input logic levels of the HINx and LINx signals (level-triggered).

After the IC recovers from a UVLO\_VB condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

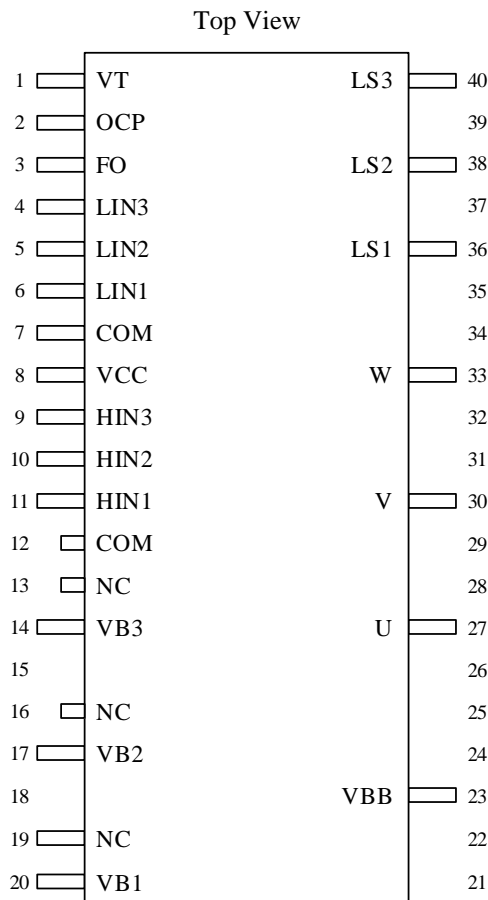
Table 6-1. Truth Table for Operation Modes

| Mode  | HINx | LINx | High-side Transistor | Low-side Transistor |
|---|------|------|----------------------|---------------------|
| Normal Operation  | L    | L    | OFF                  | OFF                 |
|   | H    | L    | ON                   | OFF                 |
|   | L    | H    | OFF                  | ON                  |
|   | H    | H    | ON                   | ON                  |
| Undervoltage Lockout for High-side Power Supply (UVLO_VB) | L    | L    | OFF                  | OFF                 |
|   | H    | L    | OFF                  | OFF                 |
|   | L    | H    | OFF                  | ON                  |
|   | H    | H    | OFF                  | ON                  |
| Undervoltage Lockout for Low-side Power Supply (UVLO_VCC) | L    | L    | OFF                  | OFF                 |
|   | H    | L    | OFF                  | OFF                 |
|   | L    | H    | OFF                  | OFF                 |
|   | H    | H    | OFF                  | OFF                 |
| Overcurrent Protection (OCP)                              | L    | L    | OFF                  | OFF                 |
|   | H    | L    | ON                   | OFF                 |
|   | L    | H    | OFF                  | OFF                 |
|   | H    | H    | ON                   | OFF                 |
| Thermal Shutdown (TSD)                                    | L    | L    | OFF                  | OFF                 |
|   | H    | L    | ON                   | OFF                 |
|   | L    | H    | OFF                  | OFF                 |
|   | H    | H    | ON                   | OFF                 |

7. Block Diagram



## 8. Pin Configuration Definitions



| Pin Number | Pin Name | Description   |
|------------|----------|---|
| 1          | VT       | Temperature sensing voltage output                        |
| 2          | OCP      | Input for overcurrent protection                          |
| 3          | FO1      | Fault signal output                                       |
| 4          | LIN3     | Logic input for W-phase low-side gate driver              |
| 5          | LIN2     | Logic input for V-phase low-side gate driver              |
| 6          | LIN1     | Logic input for U-phase low-side gate driver              |
| 7          | COM      | Logic ground  |
| 8          | VCC      | Logic supply voltage input                                |
| 9          | HIN3     | Logic input for W-phase high-side gate driver             |
| 10         | HIN2     | Logic input for V-phase high-side gate driver             |
| 11         | HIN1     | Logic input for U-phase high-side gate driver             |
| 12         | COM      | (Pin trimmed) logic ground                                |
| 13         | NC       | (Pin trimmed) no connection                               |
| 14         | VB3      | W-phase high-side floating supply voltage input           |
| 15         | —        | Pin removed   |
| 16         | NC       | (Pin trimmed) no connection                               |
| 17         | VB2      | V-phase high-side floating supply voltage input           |
| 18         | —        | Pin removed   |
| 19         | NC       | No connection   |
| 20         | VB1      | U-phase high-side floating supply voltage input           |
| 21         | —        | Pin removed   |
| 22         | —        | Pin removed   |
| 23         | VBB      | Positive DC bus supply voltage                            |
| 24         | —        | Pin removed   |
| 25         | —        | Pin removed   |
| 26         | —        | Pin removed   |
| 27         | U        | U-phase output / U-phase high-side floating supply ground |
| 28         | —        | Pin removed   |
| 29         | —        | Pin removed   |
| 30         | V        | V-phase output / V-phase high-side floating supply ground |
| 31         | —        | Pin removed   |
| 32         | —        | Pin removed   |
| 33         | W        | W-phase output / W-phase high-side floating supply ground |
| 34         | —        | Pin removed   |
| 35         | —        | Pin removed   |
| 36         | LS1      | U-phase IGBT emitter                                      |
| 37         | —        | Pin removed   |
| 38         | LS2      | V-phase IGBT emitter                                      |
| 39         | —        | Pin removed   |
| 40         | LS3      | W-phase IGBT emitter                                      |

### 9. Typical Applications

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

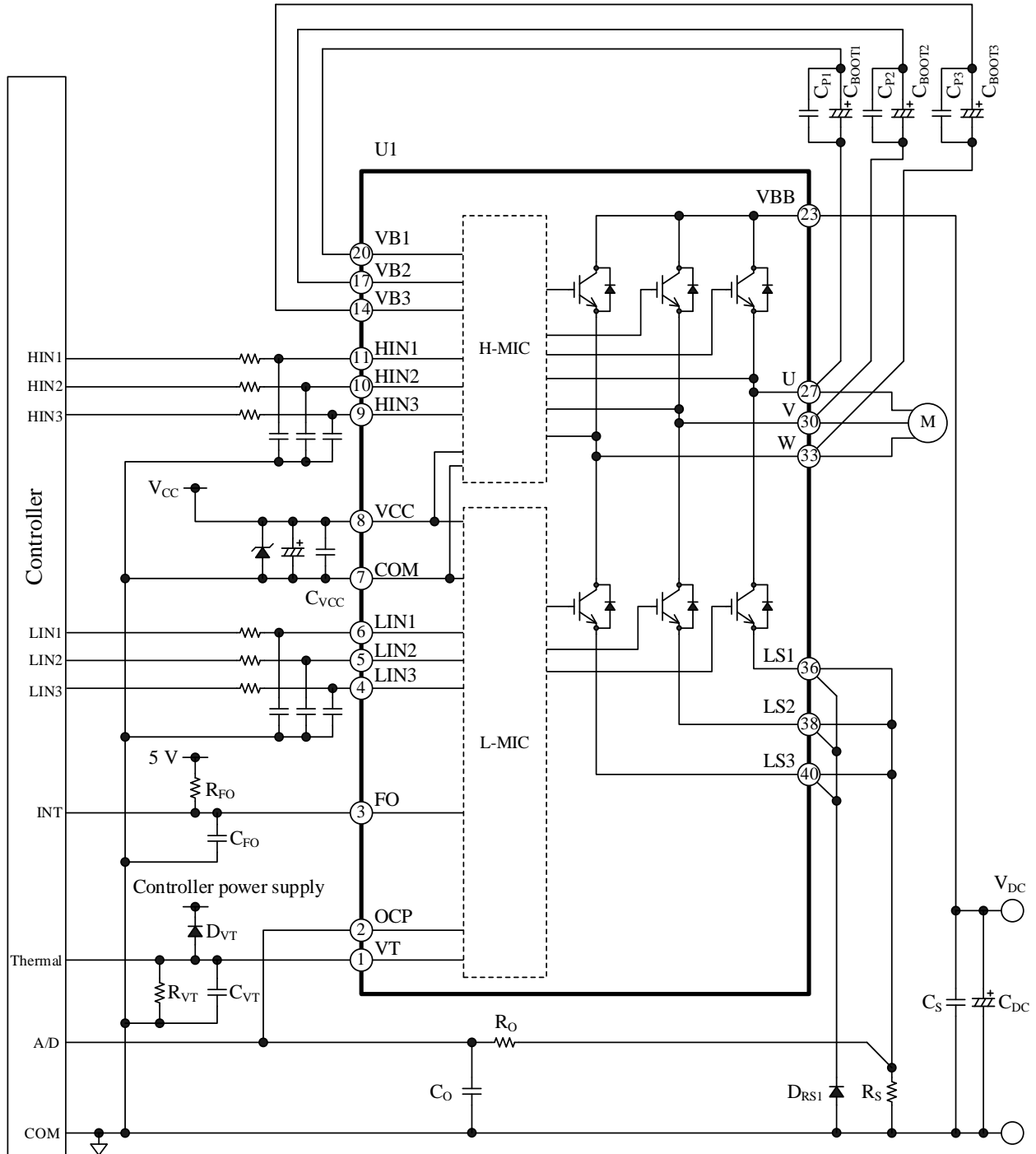


Figure 9-1. Typical Application Using a Single Shunt Resistor

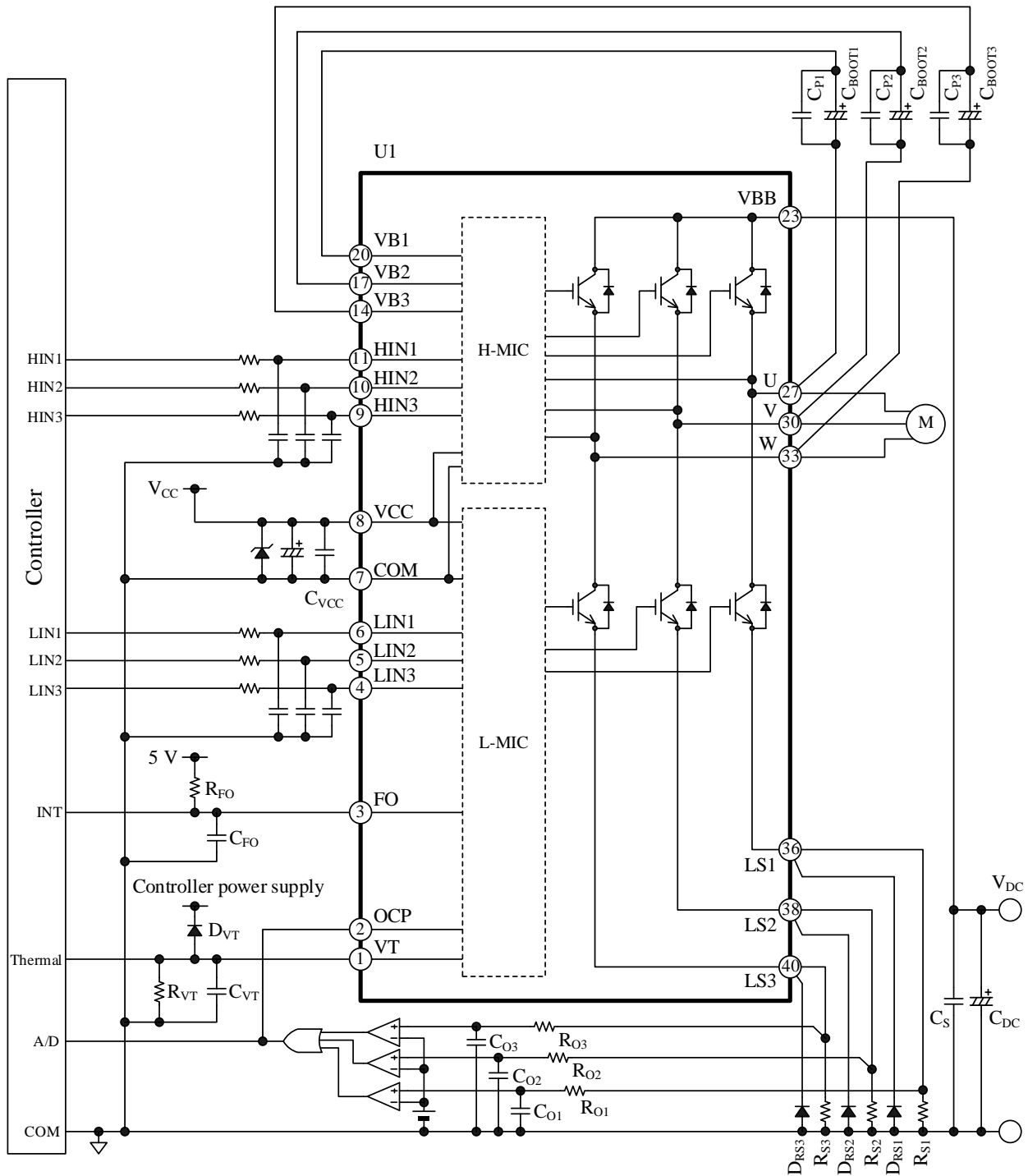
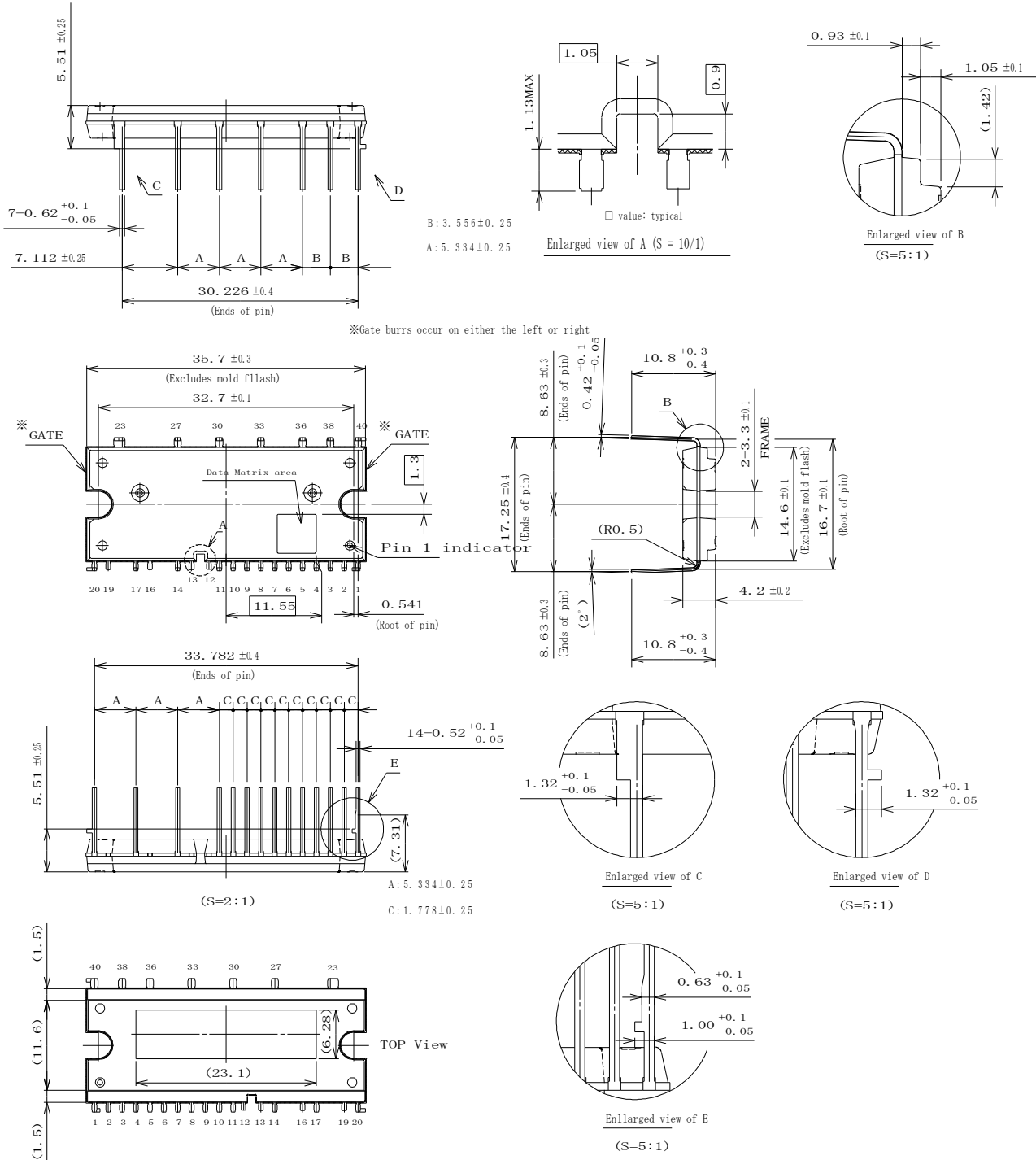


Figure 9-2. Typical Application Using Three Shunt Resistors

10. Physical Dimensions

- DIP40  
(Leadform: 2980)

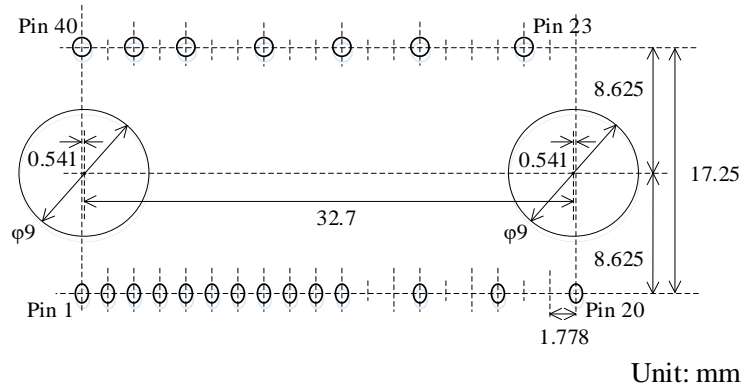


NOTES:

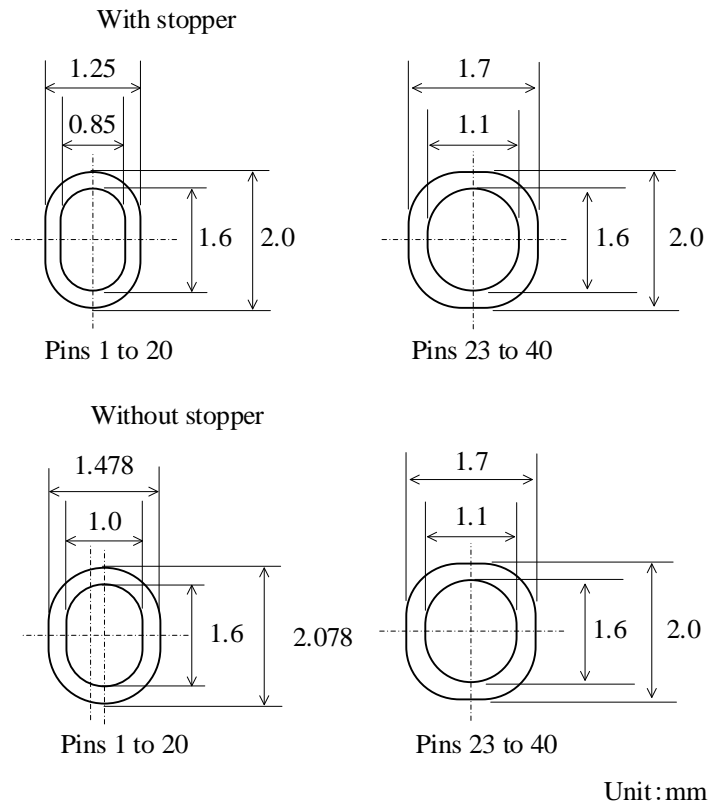
- Dimensions in millimeters
- Dimensions exclude gate burrs. The actual gate may be generated on either the right or left side as illustrated.
- Pb-free (RoHS compliant)
- Ejector pin marks left on the branding side include “○” and “◎”.

# SIM2-151A

## • Land Pattern Example



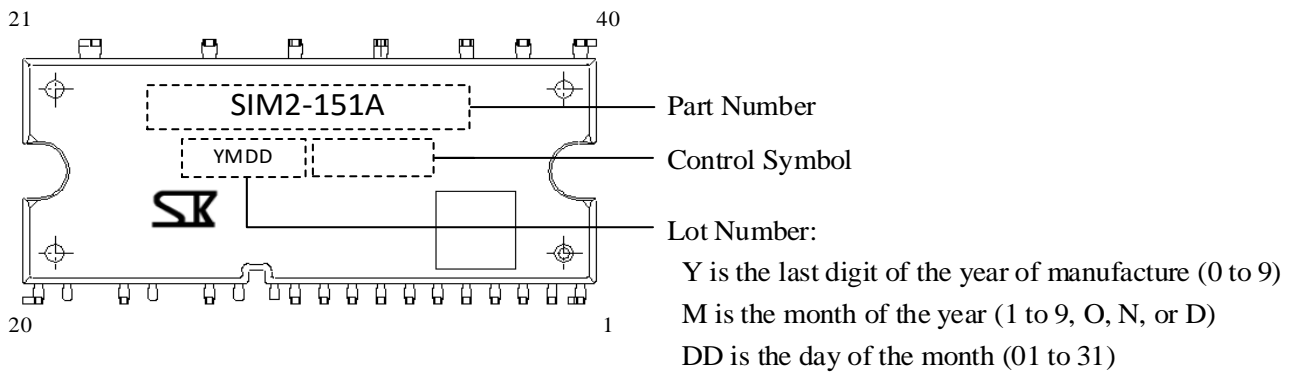
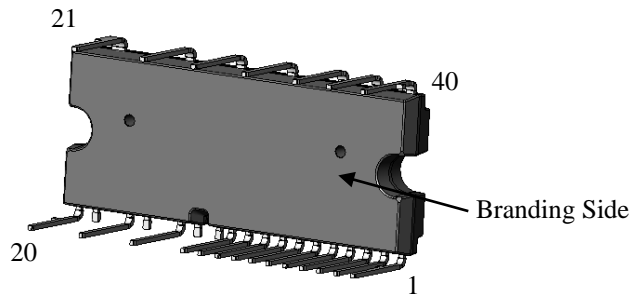
## • Reference PCB Hole Sizes





# SIM2-151A

## 11. Marking Diagram



## 12. Functional Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

For pin descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter “x”, depending on context. The U-, V-, and W-phases are represented as the pin numbers 1, 2, and 3, respectively. Thus, “the VBx pin” is used when referring to any or all of the VB1, VB2, and VB3 pins.

### 12.1. Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the VCC pin voltage has reached a stable state ( $V_{CC(ON)} \geq 12.5$  V). It is required to fully charge bootstrap capacitors,  $C_{BOOTx}$ , at startup (see Section 12.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or “L”), and then decrease the VCC pin voltage.

### 12.2. Pin Descriptions

#### 12.2.1. U, V, and W

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. These pins are the grounds of the high-side floating power supplies for each phase, and are connected to the negative nodes of bootstrap capacitors,  $C_{BOOTx}$ .

#### 12.2.2. VB1, VB2, and VB3

These are the inputs of the high-side floating power supplies for the individual phases.

Voltages across the VBx and U/V/W pins should be maintained within the recommended range (i.e., the Logic Supply Voltage,  $V_{BS}$ ) given in Section 2.

In each phase, a bootstrap capacitor,  $C_{BOOTx}$ , should be connected between the VBx and U/V/W pins. For proper startup, turn on the low-side transistor first, then fully charge the bootstrap capacitor,  $C_{BOOTx}$ . Table 12-1 shows a relation between the charging time and the capacitance of  $C_{BOOTx}$  at startup.

Table 12-1.  $C_{BOOTx}$  Capacitance vs. Charging Time at Startup

| $C_{BOOTx}$ Capacitance ( $\mu\text{F}$ ) | Reference Charging Time (s) |
|---|-----------------------------|
| 10  | 0.5                         |
| 22  | 0.5                         |
| 47  | 0.5                         |
| 100                                       | 1.0                         |
| 220                                       | 1.0                         |

For the capacitance of the bootstrap capacitors,  $C_{BOOTx}$ , choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for  $C_{BOOTx}$ .

$$C_{BOOT} (\mu\text{F}) > 800 \times t_{L(OFF)} (\text{s}) \quad (1)$$

$$10 \mu\text{F} \leq C_{BOOTx} \leq 220 \mu\text{F} \quad (2)$$

In Equation (1), let  $t_{L(OFF)}$  be the maximum off-time of the low-side transistor (i.e., the non-charging time of  $C_{BOOTx}$ ), measured in seconds.

Even while the high-side transistor is off, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to  $V_{BS(OFF)}$  or less, the high-side undervoltage lockout (UVLO\_VB) starts operating (see Section 12.4.2.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V ( $V_{BS} > V_{BS(OFF)}$ ) during a low-frequency operation such as a startup period.

As Figure 12-1 shows, a bootstrap diode,  $D_{BOOTx}$ , and a current-limiting resistor,  $R_{BOOTx}$ , are internally placed in series between the VCC and VBx pins.

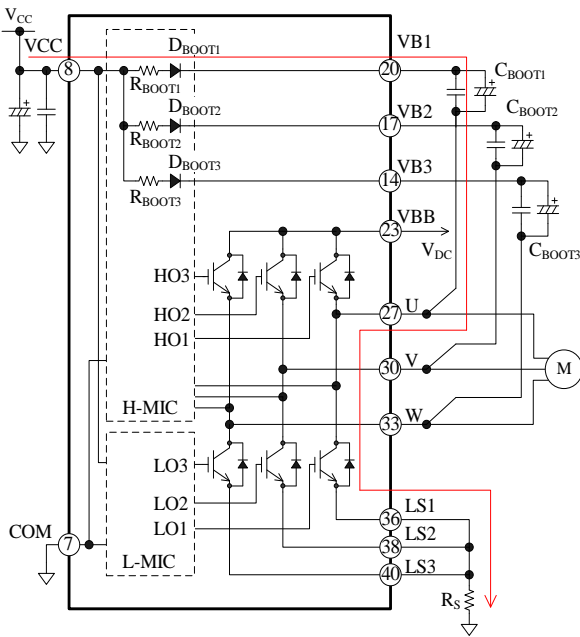


Figure 12-1. Bootstrap Circuit

Figure 12-2 shows an internal level-shifting circuit. A high-side output signal, HO<sub>x</sub>, is generated according to an input signal on the HIN<sub>x</sub> pin. When an input signal on the HIN<sub>x</sub> pin transits from low to high (rising edge), a “Set” signal is generated. When the HIN<sub>x</sub> input signal transits from high to low (falling edge), a “Reset” signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HO<sub>x</sub>).

Figure 12-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VB<sub>x</sub> and U/V/W pins (“VB<sub>x</sub>–U/V/W”) occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of an HO<sub>x</sub> signal stays logic high (or “H”) because the SR flip-flop does not respond. With the HO<sub>x</sub> state being held high (i.e., the high-side transistor is in an on-state), the next LIN<sub>x</sub> signal turns on the low-side transistor and causes a simultaneously-on condition, which may result in critical damage to the IC.

To protect the VB<sub>x</sub> pin against such a noise effect, add a bootstrap capacitor, C<sub>BOOTx</sub>, in each phase. C<sub>BOOTx</sub> must be placed near the IC and be connected between the VB<sub>x</sub> and U/V/W pins with a minimal length of traces.

To use an electrolytic capacitor, add a 0.01 μF to 0.1 μF bypass capacitor, C<sub>Px</sub>, in parallel near these pins used for the same phase.

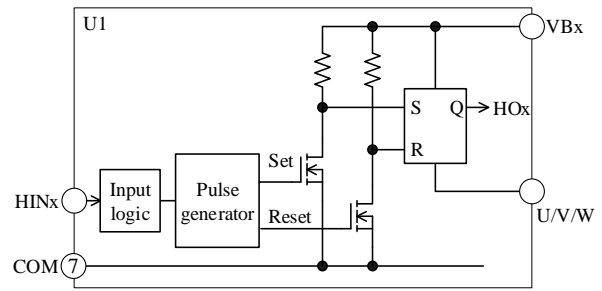


Figure 12-2. Internal Level-shifting Circuit

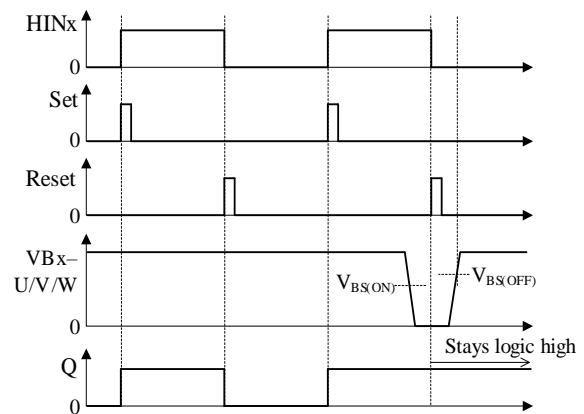


Figure 12-3. Waveforms at VB<sub>x</sub>–U/V/W Voltage Drop

### 12.2.3. VCC

This is the logic supply pin for the built-in control MICs. The VCC pin is internally connected to the high-side MIC and low-side MIC. To prevent malfunction induced by supply ripples or other factors, put a 0.01 μF to 0.1 μF ceramic capacitor, C<sub>VCC</sub>, near this pin. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCC and COM pins.

Voltages to be applied between the VCC and COM pins should be regulated within the recommended operational range of V<sub>CC</sub>, given in Section 2.

### 12.2.4. COM

This is the logic ground pin for the built-in control MICs. The COM pin is internally connected to the high-side MIC and low-side MIC. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R<sub>S</sub>, at a single-point ground (or star ground) which is separated from the power ground (see Figure 12-4). Moreover, extreme care should be taken in designing a PCB so that currents from the power ground do not affect the COM pin.

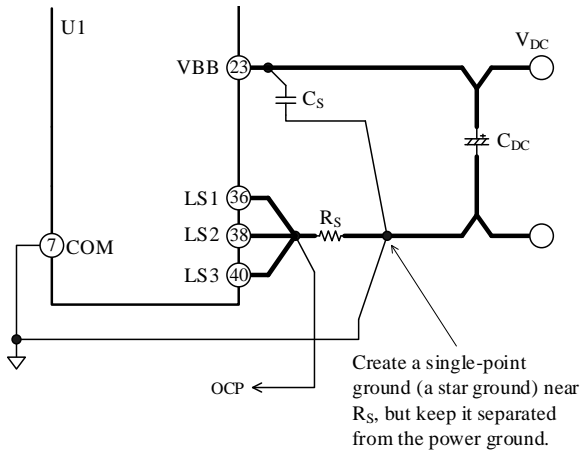


Figure 12-4. Connections to Logic Ground

### 12.2.5. HIN1, HIN2, and HIN3; LIN1, LIN2, and LIN3

These are the logic supply pins for the built-in control MICs. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller. Figure 12-5 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 22 kΩ pull-down resistor, and its input logic is active high.

Input signals across the HINx-COM and the LINx-COM pins in each phase should be set within the ranges provided in Table 12-2, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, the outputs from the microcontroller output line should not be high impedance. Also, if the traces from the microcontroller to the HINx or LINx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 12-6).

Here are filter circuit constants for reference:

- $R_{IN1x}$ : 33 Ω to 100 Ω
- $R_{IN2x}$ : 1 kΩ to 10 kΩ
- $C_{INx}$ : 100 pF to 1000 pF

Care should be taken in adding  $R_{IN1x}$  and  $R_{IN2x}$  to the traces. When they are connected to each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

Table 12-2. Input Signals for HINx and LINx Pins

| Parameter             | High Level Signal                      | Low Level Signal                     |
|-----------------------|--|--------------------------------------|
| Input Voltage         | $2.5\text{ V} < V_{IN} < 5.5\text{ V}$ | $0\text{ V} < V_{IN} < 1.0\text{ V}$ |
| Input Pulse Width     | $\geq 0.5\ \mu\text{s}$                | $\geq 0.5\ \mu\text{s}$              |
| PWM Carrier Frequency | $\leq 20\text{ kHz}$                   |                                      |
| Dead Time             | $\geq 1.5\ \mu\text{s}$                |                                      |

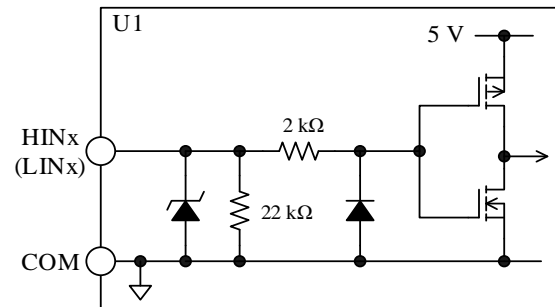


Figure 12-5. Internal Circuit Diagram of HINx or LINx Pin

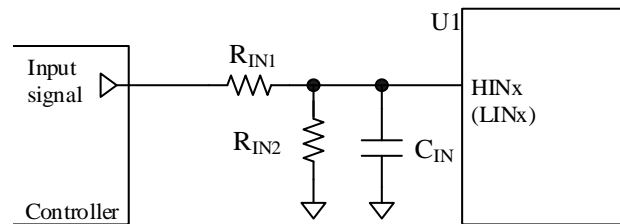


Figure 12-6. Filter Circuit for HINx or LINx Pin

### 12.2.6. VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin. Voltages between the VBB and COM pins should be set within the recommended range of the main supply voltage,  $V_{DC}$ , given in Section 2.

To suppress surge voltages, put a 0.01 μF to 0.1 μF bypass capacitor,  $C_s$ , near the VBB pin and an electrolytic capacitor,  $C_{DC}$ , with a minimal length of PCB traces to the VBB pin.

### 12.2.7. LS1, LS2, and LS3

These are the emitter pins of the low-side IGBTs and are externally connected to a shunt resistor,  $R_s$ .

When connecting a shunt resistor, use a resistor with low inductance, and place it as near as possible to the IC

with a minimum length of traces to the LSx and COM pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode,  $D_{RS}$ , between the LSx and COM pins in order to prevent the IC from malfunctioning.

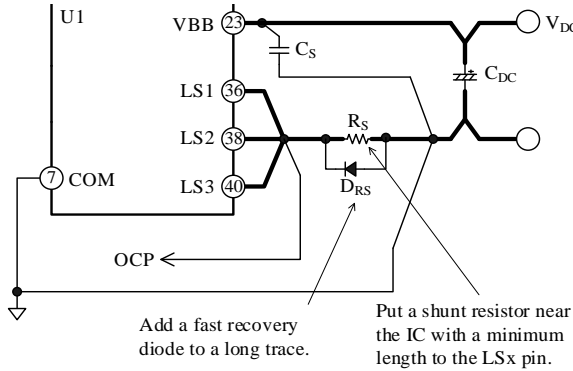


Figure 12-7. Connections to LSx Pin

12.2.8. OCP

This pin serves as the input of the overcurrent protection (OCP) for monitoring the currents going through the output transistors. Section 12.4.3 provides further information about the OCP circuit configuration and its mechanism.

12.2.9. FO

This pin operates as the fault signal output. For more details, see Section 12.4.1.

Figure 12-8 illustrates an internal circuit diagram of the FO pin and its peripheral circuit. The 100 kΩ pull-up resistor is connected to the FO pin in the internal circuit, but the FO pin should be tied by a pull-up resistor,  $R_{FO}$ , to the external power supply to suppress the noise effect. The external power supply voltage (i.e., the FO Pin Pull-up Voltage,  $V_{FO}$ ) should range from 3.3 V to 5.5 V. The filter capacitor of the FO pin,  $C_{FO}$ , should have a capacitance of  $\leq 0.01 \mu F$ .

Figure 12-10 shows a relation between the FO pin voltage and the pull-up resistor,  $R_{FO}$ . When the pull-up resistor,  $R_{FO}$ , has a too small resistance, the FO pin voltage at fault signal output becomes high due to the on-resistance of a built-in transistor,  $Q_{FO}$  (Figure 12-8). Therefore, it is recommended to use a 3.3 kΩ to 10 kΩ pull-up resistor when the Low Level Input Threshold Voltage of the microcontroller,  $V_{IL}$ , is set to 1.0 V.

To suppress noise, add a filter capacitor,  $C_{FO}$ , near the IC with minimizing a trace length between the FO and COM pins. Note that, however, this additional filtering allows a delay time to occur, as seen in Figure 12-9. The delay time is a period of time which starts when the IC

receives a fault flag turning on the internal transistor,  $Q_{FO}$ , and continues until when the FO pin reaches its threshold voltage ( $V_{IL}$ ) of 1.0 V or below (put simply, until the time when the IC detects a low state, “L”). Figure 12-11 shows the relationship between  $C_{FO}$  and the FO pin delay time. For avoiding repeated OCP activations, the external microcontroller must shut off any input signals to the IC within a fixed hold time,  $t_P$ , after the internal transistor ( $Q_{FO}$ ) turn-on.  $t_P$  is 5 ms where minimum values of thermal characteristics are taken into account (for more details, see Section 12.4.3). When  $V_{IL} = 1.0 V$ , the reference value of  $C_{FO}$  is 0.001  $\mu F$  to 0.01  $\mu F$ .

Motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. To resume the motor operation thereafter, set the motor to be resumed after a lapse of  $\geq 2$  seconds.

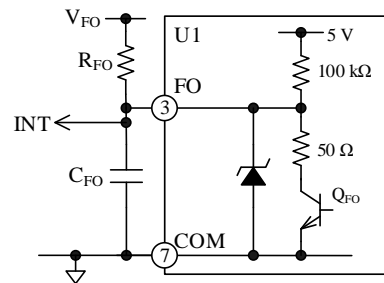


Figure 12-8. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

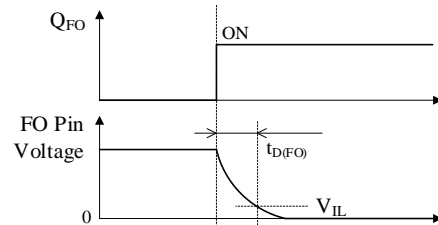


Figure 12-9. FO Pin Delay Time,  $t_{D(FO)}$

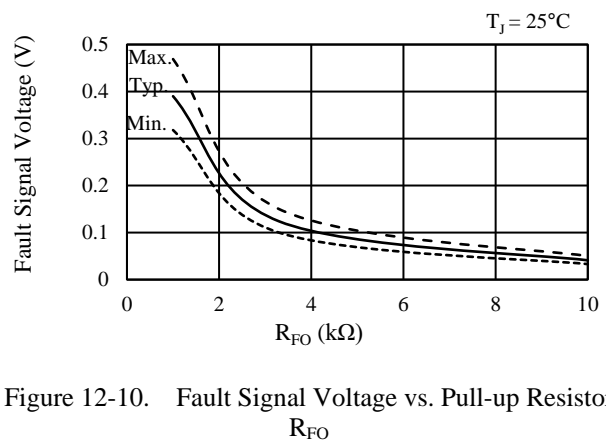


Figure 12-10. Fault Signal Voltage vs. Pull-up Resistor,  $R_{FO}$

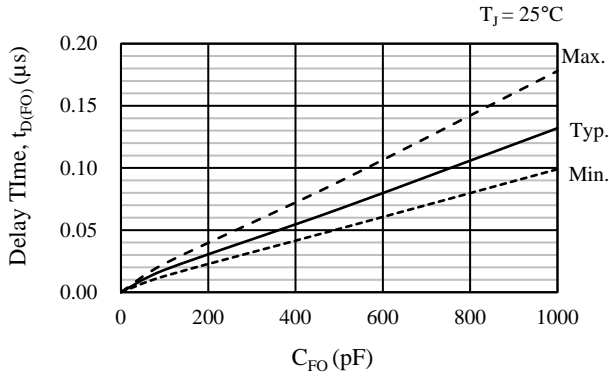


Figure 12-11. Filter Capacitor,  $C_{FO}$  vs. FO Pin Delay Time,  $t_{D(FO)}$

12.2.10. VT

This pin outputs temperature sensing voltages. The external microcontroller can monitor the junction temperature of the internal control IC, not of the output transistors, with the VT pin. For more details, see Section 12.3.

12.3. Temperature Sensing Function

The microcontroller can monitor the junction temperature of the internal control IC, through temperature sensing voltages that the VT pin outputs. The SIM2-151A does not include any protections against overtemperature, such as an IC shutdown or a fault flag. Therefore, the IC must be set to stop its operation as it detects an abnormal heating state with temperature sensing voltages. A typical example is turning off input signals from the microcontroller. Figure 12-13 shows a relation between the VT pin voltage and temperature. Table 12-3 and Table 12-4 provide the details of variations found in Figure 12-13.

Temperature sensing voltages may exceed 3.0 V, causing permanent damage to the IC in the worst case. To protect the parts connected to the VT pin such as the microcontroller, add a clamp diode,  $D_{VT}$ , between the microcontroller power supply and the VT pin (see Figure 12-12).

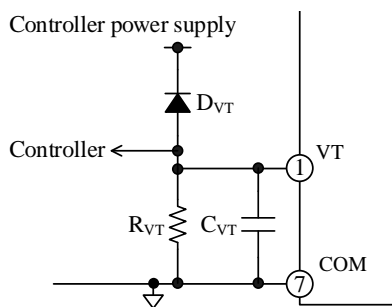


Figure 12-12. VT Pin Peripheral Circuit

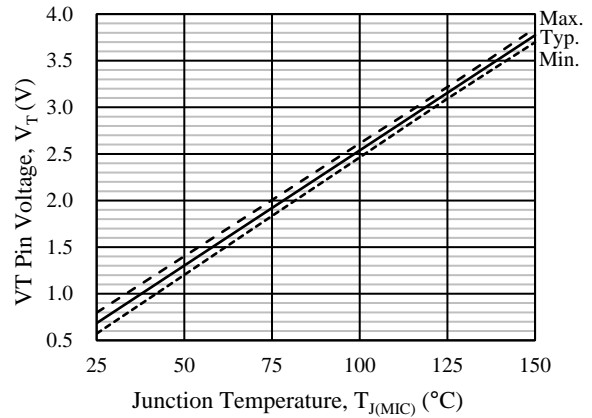


Figure 12-13. VT Pin Voltage,  $V_T$  vs. Internal Control IC Junction Temperature,  $T_{J(MIC)}$  (Design Value)

Table 12-3.  $T_{J(MIC)}$  Variation on VT Pin Voltage (Design Value)

| VT Pin Voltage (V) | $T_{J(MIC)}$ (°C) |
|--------------------|-------------------|
| 1.271              | $50 \pm 3$        |
| 3.130              | $125 \pm 2$       |

Table 12-4. VT Pin Voltage Variation on  $T_{J(MIC)}$  (Design Value)

| $T_{J(MIC)}$ (°C) | VT Pin Voltage (V) |
|-------------------|--------------------|
| 50                | $1.271 \pm 0.07$   |
| 125               | $3.130 \pm 0.05$   |

12.4. Protection Functions

This section describes the various protection circuits provided in the SIM2-151A. The protection circuits include the undervoltage lockout for power supplies (UVLO), the overcurrent protection (OCP), and the thermal shutdown (TSD). In case one or more of these protection circuits are activated, the FO pin outputs a fault signal; as a result, the external microcontroller can stop the operations of the three phases by receiving the fault signal. In the following functional descriptions, “HOx” denotes a gate input signal on the high-side transistor, whereas “LOx” denotes a gate input signal on the low-side transistor (see also the diagram in Section 7). “VBx-U/V/W” refers to the voltages between the VBx and U/V/W pins.

### 12.4.1. Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor,  $Q_{FO}$ , turns on, then the FO pin becomes logic low ( $\leq 0.5$  V).

- 1) Low-side undervoltage lockout (UVLO\_VCC)
- 2) Overcurrent protection (OCP)
- 3) Thermal shutdown (TSD)

While the FO pin is in the low state, the low-side transistors of each phase turn off. In normal operation, the FO pin outputs a high signal of about 5 V. The fault signal output time of the FO pin at OCP activation is the hold time,  $t_P = 10$  ms (typ.), fixed by a built-in feature of the IC itself (see Section 12.4.3). The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HIN<sub>x</sub> and LIN<sub>x</sub> pins to logic low within the predetermined hold time,  $t_P$ . To resume motor operations thereafter, set the motor to be resumed after a lapse of  $\geq 2$  seconds.

### 12.4.2. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SIM2-151A has the undervoltage lockout (UVLO) circuits for both of the high- and low-side power supplies.

#### 12.4.2.1. Undervoltage Lockout for High-side Power Supply (UVLO\_VB)

Figure 12-14 shows operational waveforms of the undervoltage lockout for high-side power supply (i.e., UVLO\_VB).

When the voltage between the VB<sub>x</sub> and U/V/W pins ( $V_{Bx-U/V/W}$ ) decreases to the Logic Operation Stop Voltage ( $V_{BS(OFF)} = 10.0$  V) or less, the UVLO\_VB circuit in the corresponding phase gets activated and sets an HO<sub>x</sub> signal to logic low.

When the voltage between the VB<sub>x</sub> and U/V/W pins increases to the Logic Operation Start Voltage ( $V_{BS(ON)} = 10.5$  V) or more, the IC releases the UVLO\_VB condition. Then, the HO<sub>x</sub> signal becomes logic high at the rising edge of the first input command after the UVLO\_VB release. Any fault signal is not output from the FO pin during the UVLO\_VB operation. In addition, the VB<sub>x</sub> pin has an internal UVLO\_VB filter of about 3  $\mu$ s, in order to prevent noise-induced malfunctions.

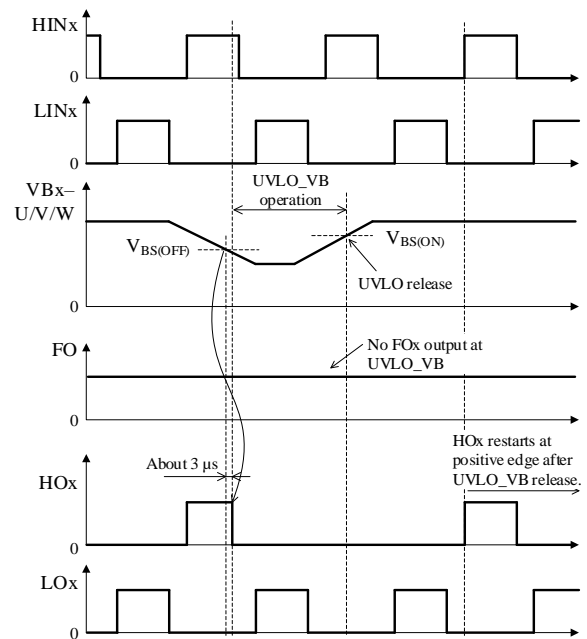


Figure 12-14. UVLO\_VB Operational Waveforms

#### 12.4.2.2. Undervoltage Lockout for Low-side Power Supply (UVLO\_VCC)

The VCC pin has the VCC pin undervoltage lockout (UVLO\_VCC) circuit for low-side power supply.

The description hereafter provides the UVLO\_VCC operation of the VCC pin. As Figure 12-15 shows, when the VCC pin voltage decreases to the Logic Operation Stop Voltage ( $V_{CC(OFF)} = 11.0$  V) or less, the UVLO\_VCC circuit in the U-phase gets activated and sets both of HO1 and LO1 signals to logic low. When the VCC pin voltage increases to the Logic Operation Start Voltage ( $V_{CC(ON)} = 11.5$  V) or more, the IC releases the UVLO\_VCC operation. Then it resumes transmitting the HO1 and LO1 signals according to input commands on the HIN1 and LIN1 pins. During the UVLO\_VCC operation, the FO pin becomes logic low and sends fault signal. In addition, the VCC pin has an internal UVLO\_VCC filter of about 3  $\mu$ s, in order to prevent noise-induced malfunctions.

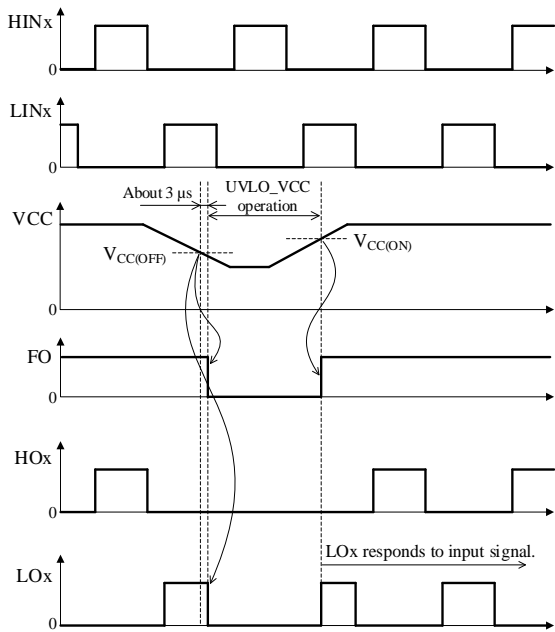


Figure 12-15. UVLO\_VCC Operational Waveforms

### 12.4.3. Overcurrent Protection (OCP)

The OCP pin has the overcurrent protection (OCP) circuit. Figure 12-16 is an internal circuit diagram describing the OCP pin and its peripheral circuit.

The OCP pin detects overcurrents with voltage across an external shunt resistor,  $R_S$ . Because the OCP pin is internally pulled down, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor,  $R_S$ .

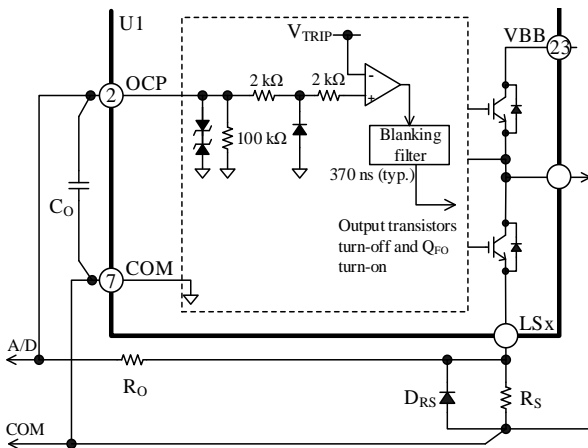


Figure 12-16. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

Figure 12-17 shows operational waveforms when the OCP pin detects an overcurrent condition. When the OCP pin voltage increases to the OCP Threshold

Voltage ( $V_{TRIP} = 0.50\text{ V}$ ) or more, and remains in this condition for a period of the OCP Blanking Time ( $t_{BK(OCP)} = 370\text{ ns}$ ) or longer, the corresponding OCP circuit is activated. When an internal delay time ( $t_{D(OCP)} = 0.13\text{ μs}$ ) has elapsed after the OCP activation, the low-side output transistors turn off and the FO pin becomes low state. Then, output current decreases as a result of the low-side output transistor turn-offs. Even if the OCP pin voltage falls below  $V_{TRIP}$ , the IC holds the FO pin in the low state for a fixed hold time,  $t_p = 10\text{ ms}$ . Then, the output transistors operate according to input signals.

To prevent noise-induced malfunctions, connect a ceramic capacitor,  $C_{FO}$  (about  $0.001\text{ μF}$  to  $0.1\text{ μF}$ ) to the FO pin.

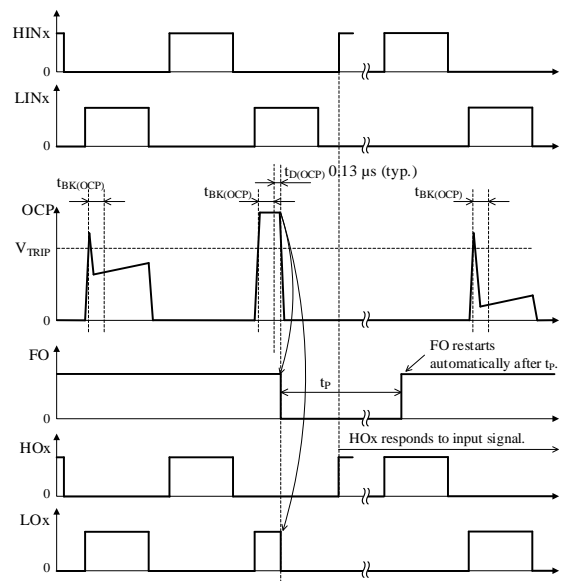


Figure 12-17. OCP Operational Waveforms

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected.

The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HINx and LINx pins to logic low within the predetermined hold time,  $t_p$ . To resume motor operations thereafter, set the motor to be resumed after a lapse of  $\geq 2$  seconds.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance,  $R_S$  (see Section 2).
- Set the OCP pin input voltage to vary within the rated OCP pin voltages,  $V_{OCP}$  (see Section 1).



- Keep the current through the output transistors below the rated output current (pulse),  $I_{OP}$  (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor,  $R_S$ . In addition, choose a resistor with allowable power dissipation according to your application.

When you connect a CR filter (i.e., a pair of a filter resistor,  $R_O$ , and a filter capacitor,  $C_O$ ) to the OCP pin, care should be taken in setting the time constants of  $R_O$  and  $C_O$ . The larger the time constant, the longer the time that the OCP pin voltage rises to  $V_{TRIP}$ . And this may cause permanent damage to the transistors. Consequently, a propagation delay of the IC must be taken into account when you determine the time constants. For  $R_O$  and  $C_O$ , their time constants must be set to  $\leq 1.0 \mu s$ . The filter capacitor,  $C_O$ , should also be placed near the IC, between the OCP and COM pins with a minimal length of traces.

Note that overcurrents are undetectable when one or more of the U, V, and W pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

### 12.4.4. Thermal Shutdown (TSD)

The SIM2-151A incorporates the thermal shutdown (TSD) circuit in the low-side MIC (see Section 7). The TSD circuit protects the IC from overheating, such as increased power dissipation due to overload, or elevated ambient temperature at the device. When the temperature of the low-side MIC exceeds the TSD Operating Temperature ( $T_{DH} = 120 \text{ }^\circ\text{C}$ ) due to such overheating, the TSD circuit is activated. During the TSD operation, the IC turns off the low-side output transistors and outputs a fault signal (see Figure 12-18).

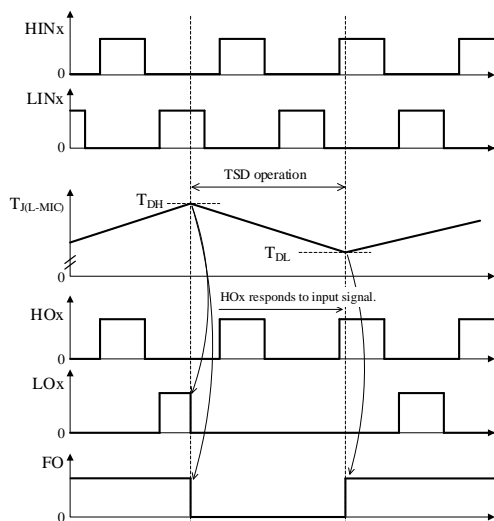


Figure 12-18. TSD Operational Waveforms

When the temperature of the low-side MIC decreases to the TSD Releasing Temperature ( $T_{DL} = 100 \text{ }^\circ\text{C}$ ) or less thereafter, the shutdown condition is released. The output transistors then resume operating according to input signals. Also note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

## 13. Design Notes

This section also employs the notation system described in the beginning of the previous section.

### 13.1. PCB Pattern Layout

Figure 13-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

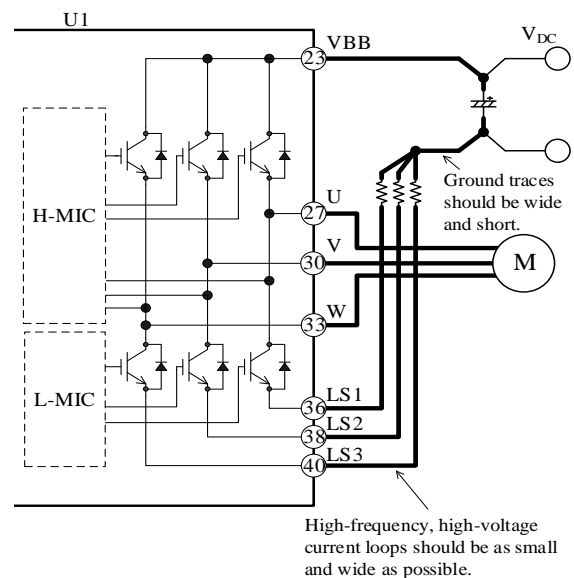


Figure 13-1. High-frequency, High-voltage Current Paths

### 13.2. Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- Be sure to use a metric screw of M3 and a plain washer of 7 mm ( $\phi$ ). When tightening the screws, use a torque screwdriver and tighten them within the range of screw torque defined in Section 4. Be sure to avoid uneven tightening. Temporarily tighten the two screws first, then tighten them equally on both sides until the specified screw torque is reached.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  - Grease thickness: 100  $\mu\text{m}$
  - Heatsink flatness:  $\pm 100 \mu\text{m}$
  - Apply a silicone grease within the area indicated in Figure 13-2, below.

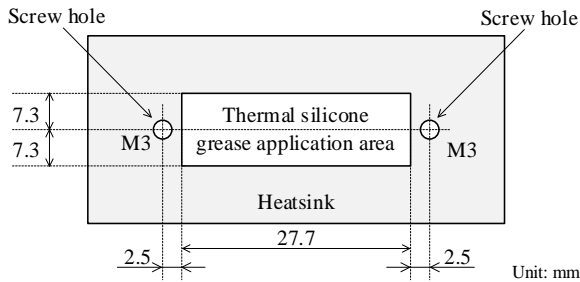


Figure 13-2. Reference Application Area for Thermal Silicone Grease

### 13.3. Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that the gate and emitter of each transistor should have the same potential. Moreover, care should be taken during the measurement because the collectors of the high-side transistors are all internally connected to the VBB pin.

The output (U, V, and W) pins are connected to the emitters of the corresponding high-side transistors, whereas the LSx pins are connected to the emitters of the low-side transistors. The gates of the high-side transistors are pulled down to the corresponding output (U, V, and W) pins; similarly, the gates of the low-side transistors are pulled down to the COM pin.

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that all of the output (U, V, and W), LSx, and COM pins must be appropriately connected. Otherwise, the

switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 13-3 shows the high-side transistor ( $Q_{1H}$ ) in the U-phase; Figure 13-4 shows the low-side transistor ( $Q_{1L}$ ) in the U-phase. And all the pins that are not represented in these figures are open.

Before conducting a measurement, be sure to isolate the ground of the to-be-measured phase from those of other two phases not to be measured. Then, in each of the two phases, which are separated not to be measured, connect the LSx and COM pins each other at the same potential, and leave them unused and floated.

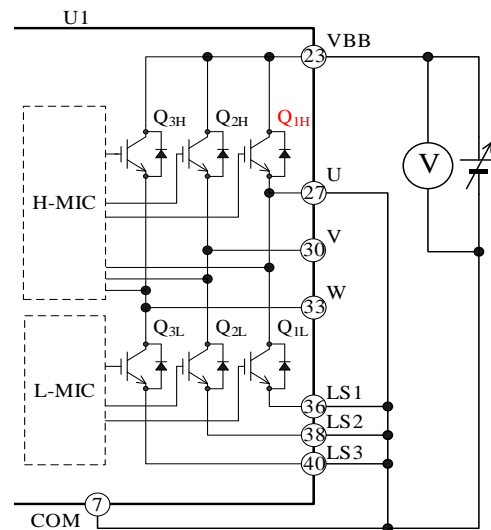


Figure 13-3. Typical Measurement Circuit for High-side Transistor ( $Q_{1H}$ ) in U-phase

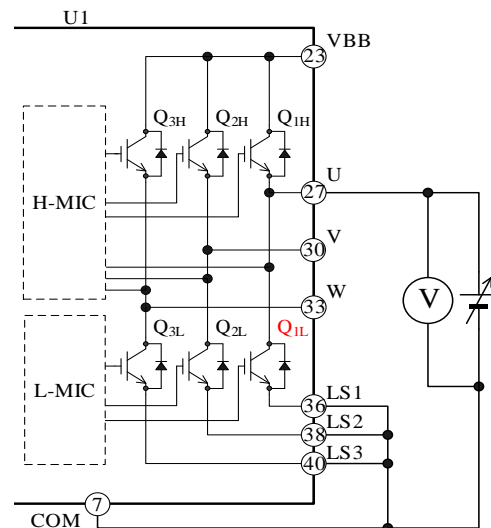


Figure 13-4. Typical Measurement Circuit for Low-side Transistor ( $Q_{1L}$ ) in U-phase

## 14. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in a switching transistor, and to estimate a junction temperature. Note that the descriptions listed here are applicable to the SIM2-151A, which is controlled by a 3-phase sine-wave PWM driving strategy. Total power loss in an IGBT can be obtained by taking the sum of steady-state loss,  $P_{ON}$ , and switching loss,  $P_{SW}$ . The following subsections contain the mathematical procedures to calculate the power losses in an IGBT and its junction temperature.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0051: SIM2-151A Calculation Tool  
[https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbt1\\_caltool\\_en.html](https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbt1_caltool_en.html)

### 14.1. IGBT Steady-state Loss, $P_{ON}$

Steady-state loss in an IGBT can be computed by using the  $V_{CE(SAT)}$  vs.  $I_C$  curves, listed in Section 15.2.1. As expressed by the curves in Figure 14-1, a linear approximation at a range the  $I_C$  is actually used is obtained by:  $V_{CE(SAT)} = \alpha \times I_C + \beta$ .

The values gained by the above calculation are then applied as parameters in Equation (3), below. Hence, the equation to obtain the IGBT steady-state loss,  $P_{ON}$ , is:

$$P_{ON} = \frac{1}{2\pi} \int_0^\pi V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2} \alpha \left( \frac{1}{2} + \frac{4}{3\pi} M \times \cos \theta \right) I_M^2 + \frac{\sqrt{2}}{\pi} \beta \left( \frac{1}{2} + \frac{\pi}{8} M \times \cos \theta \right) I_M \quad (3)$$

Where:

$V_{CE(SAT)}$  is the collector-to-emitter saturation voltage of the IGBT (V),

$I_C$  is the collector current of the IGBT (A),

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),

$\cos \theta$  is the motor power factor (0 to 1),

$I_M$  is the effective motor current (A),

$\alpha$  is the slope of the linear approximation in the  $V_{CE(SAT)}$  vs.  $I_C$  curve, and

$\beta$  is the intercept of the linear approximation in the  $V_{CE(SAT)}$  vs.  $I_C$  curve.

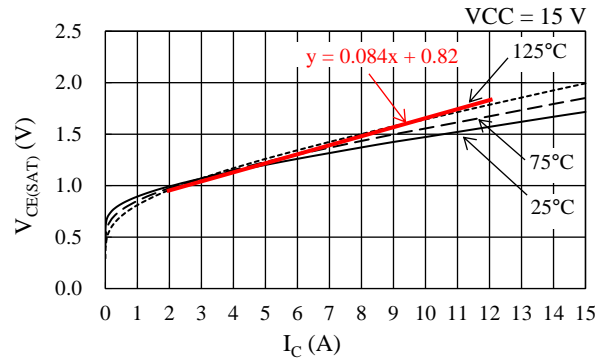


Figure 14-1. Linear Approximate Equation of  $V_{CE(SAT)}$  vs.  $I_C$

### 14.2. IGBT Switching Loss, $P_{SW}$

Switching loss in an IGBT,  $P_{SW}$ , can be calculated by Equation (4), letting  $I_M$  be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_c \times \alpha_E \times I_M \times \frac{V_{DC}}{300} \quad (4)$$

Where:

$f_c$  is the PWM carrier frequency (Hz),

$V_{DC}$  is the main power supply voltage (V), i.e., the VBB pin input voltage, and

$\alpha_E$  is the slope of the switching loss curve (see Section 15.2.2).

### 14.3. Estimating Junction Temperature of IGBT

The junction temperature of an IGBT,  $T_J$ , can be estimated with Equation (5):

$$T_J = R_{(J-C)Q} \times (P_{ON} + P_{SW}) + T_C \quad (5)$$

Where:

$R_{(J-C)Q}$  is the junction-to-case thermal resistance per IGBT ( $^{\circ}C/W$ ), and

$T_C$  is the case temperature ( $^{\circ}C$ ), measured at the point defined in Figure 3-1.

## 15. Performance Curves

### 15.1. Performance Curves of Control Parts

Figure 15-1 to Figure 15-20 provide performance curves of the control parts integrated in the SIM2-151A, including variety-dependent characteristics and thermal characteristics.  $T_J$  represents the junction temperature of the control parts.

Table 15-1. Typical Characteristics of Control Parts

| Figure Number | Figure Caption   |
|---------------|--|
| Figure 15-1   | Logic Supply Current in 3-phase Operation, $I_{CC}$ vs. $T_C$  |
| Figure 15-2   | Logic Supply Current in 3-phase Operation, $I_{CC}$ vs. VCC Pin Voltage, $V_{CC}$                    |
| Figure 15-3   | Logic Supply Current in 1-phase Operation ( $HIN_x = 0$ V), $I_{BS}$ vs. $T_C$                       |
| Figure 15-4   | Logic Supply Current in 1-phase Operation ( $HIN_x = 5$ V), $I_{BS}$ vs. $T_C$                       |
| Figure 15-5   | Logic Supply Current in 1-phase Operation ( $HIN_x = 0$ V), $I_{BS}$ vs. $V_{Bx}$ Pin Voltage, $V_B$ |
| Figure 15-6   | Logic Operation Start Voltage, $V_{BS(ON)}$ vs. $T_C$  |
| Figure 15-7   | Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. $T_C$  |
| Figure 15-8   | Logic Operation Start Voltage, $V_{CC(ON)}$ vs. $T_C$  |
| Figure 15-9   | Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. $T_C$  |
| Figure 15-10  | UVLO_VB Filtering Time vs. $T_C$   |
| Figure 15-11  | UVLO_VCC Filtering Time vs. $T_C$  |
| Figure 15-12  | Input Current at High Level ( $HIN_x$ or $LIN_x$ ), $I_{IN}$ vs. $T_C$                               |
| Figure 15-13  | High Level Input Signal Threshold Voltage, $V_{IH}$ vs. $T_C$  |
| Figure 15-14  | Low Level Input Signal Threshold Voltage, $V_{IL}$ vs. $T_C$   |
| Figure 15-15  | Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. $T_C$                  |
| Figure 15-16  | Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. $T_C$                   |
| Figure 15-17  | FO Pin Voltage in Normal Operation, $V_{FOL}$ vs. $T_C$  |
| Figure 15-18  | OCP Threshold Voltage, $V_{TRIP}$ vs. $T_C$  |
| Figure 15-19  | OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, $t_{D(OCP)}$ vs. $T_C$                         |
| Figure 15-20  | OCP Hold Time, $t_P$ vs. $T_C$   |

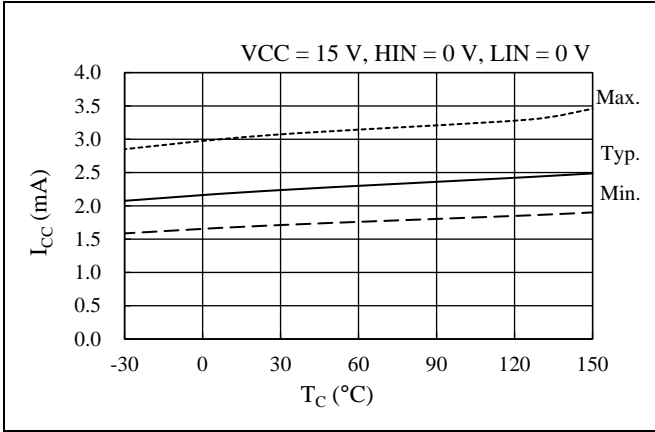


Figure 15-1. Logic Supply Current in 3-phase Operation,  $I_{CC}$  vs.  $T_C$

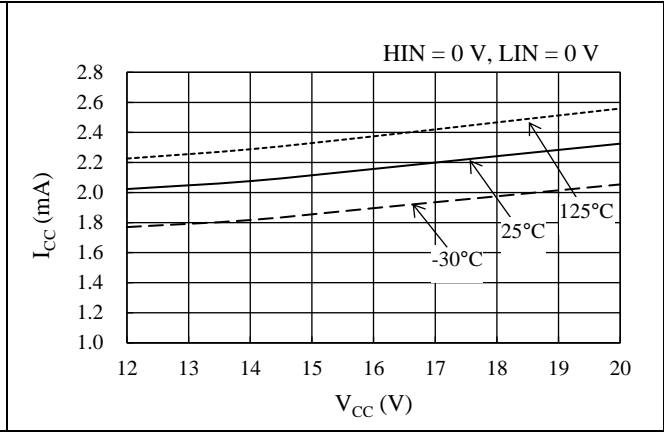


Figure 15-2. Logic Supply Current in 3-phase Operation,  $I_{CC}$  vs.  $V_{CC}$  Pin Voltage,  $V_{CC}$

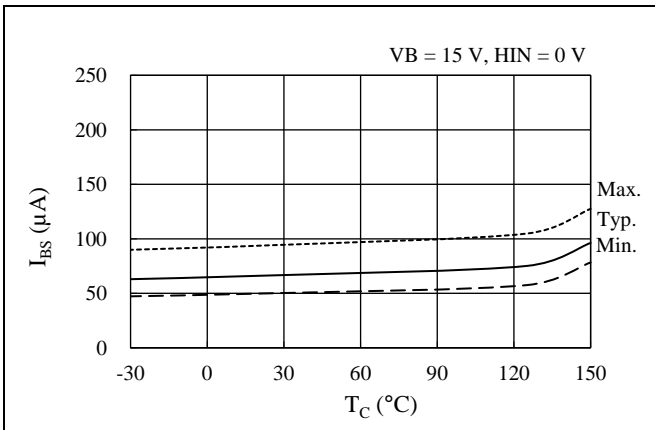


Figure 15-3. Logic Supply Current in 1-phase Operation ( $HIN_x = 0 V$ ),  $I_{BS}$  vs.  $T_C$

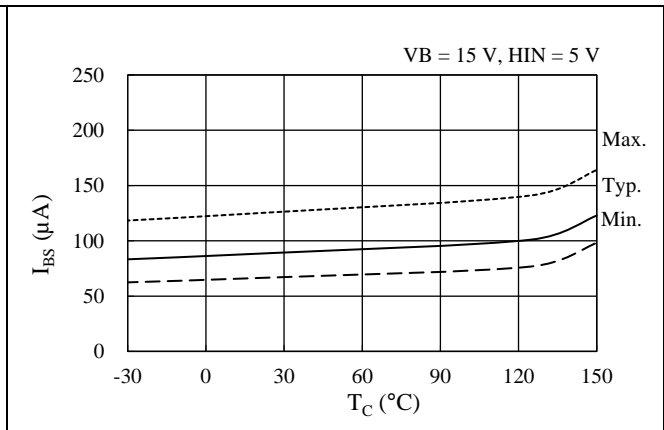


Figure 15-4. Logic Supply Current in 1-phase Operation ( $HIN_x = 5 V$ ),  $I_{BS}$  vs.  $T_C$

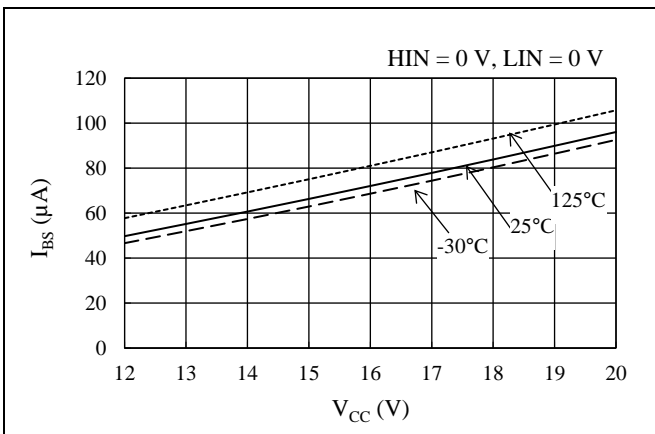


Figure 15-5. Logic Supply Current in 1-phase Operation ( $HIN_x = 0 V$ ),  $I_{BS}$  vs.  $V_{Bx}$  Pin Voltage,  $V_B$

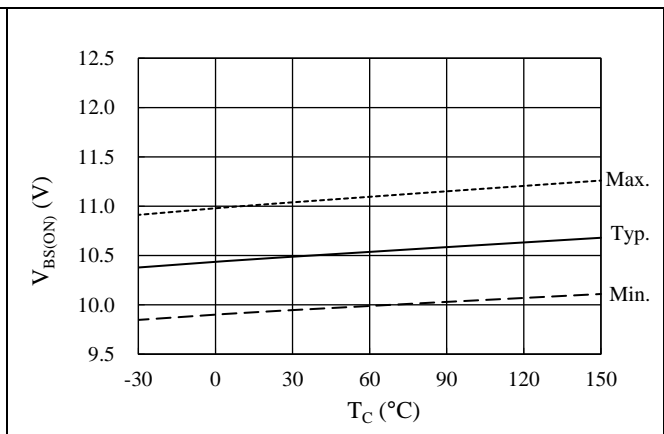


Figure 15-6. Logic Operation Start Voltage,  $V_{BS(ON)}$  vs.  $T_C$

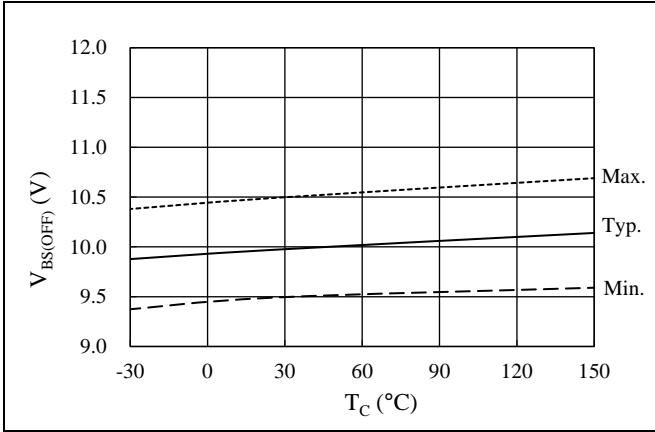


Figure 15-7. Logic Operation Stop Voltage,  $V_{BS(OFF)}$  vs.  $T_C$

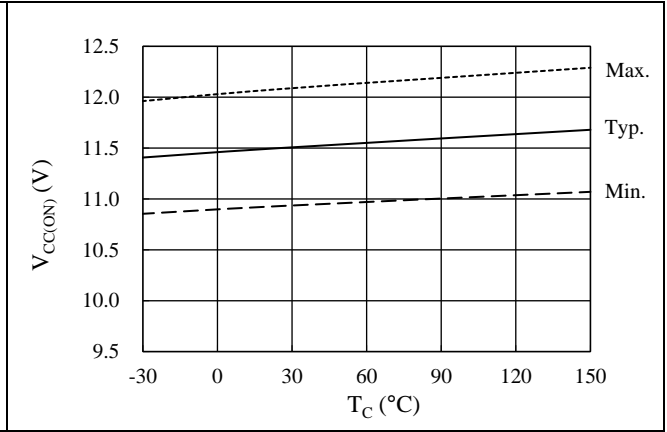


Figure 15-8. Logic Operation Start Voltage,  $V_{CC(ON)}$  vs.  $T_C$

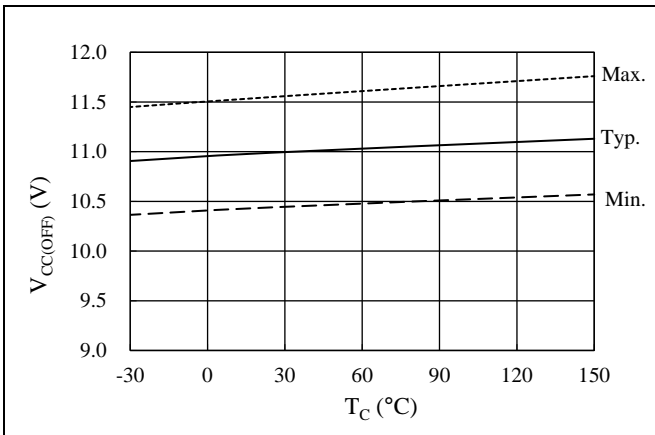


Figure 15-9. Logic Operation Stop Voltage,  $V_{CC(OFF)}$  vs.  $T_C$

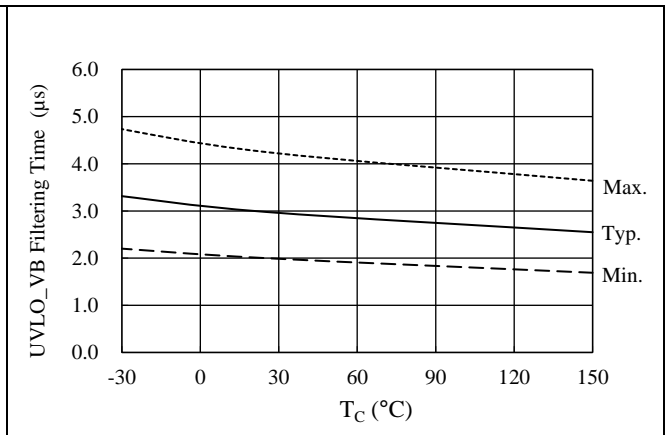


Figure 15-10. UVLO\_VB Filtering Time vs.  $T_C$

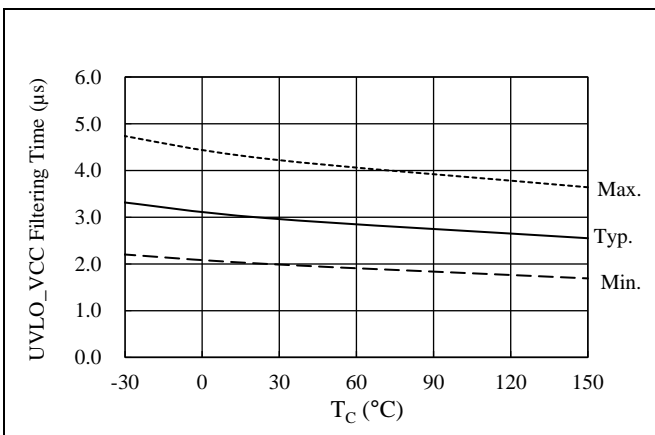


Figure 15-11. UVLO\_VCC Filtering Time vs.  $T_C$

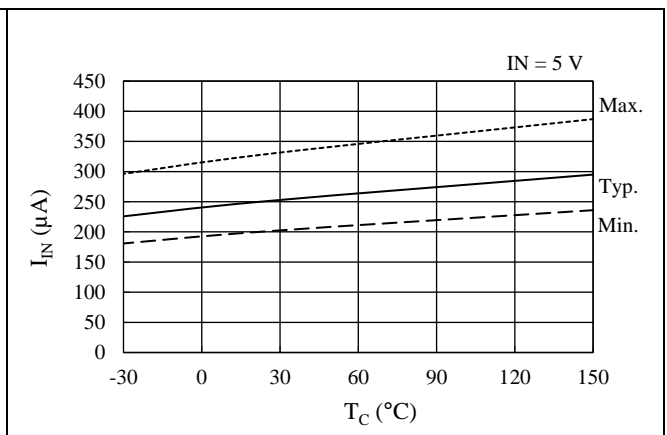


Figure 15-12. Input Current at High Level (HINx or LINx),  $I_{IN}$  vs.  $T_C$

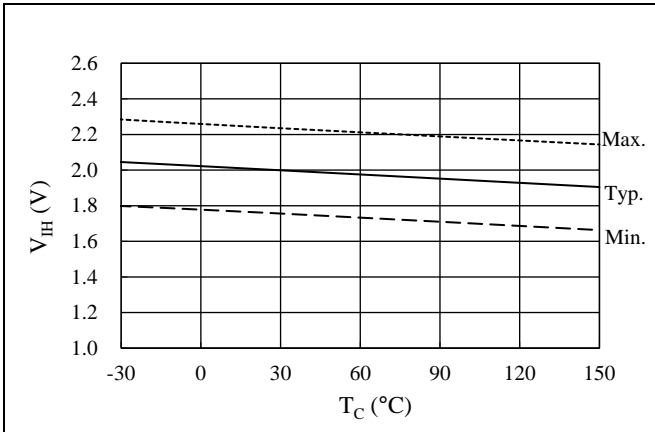


Figure 15-13. High Level Input Signal Threshold Voltage,  $V_{IH}$  vs.  $T_C$

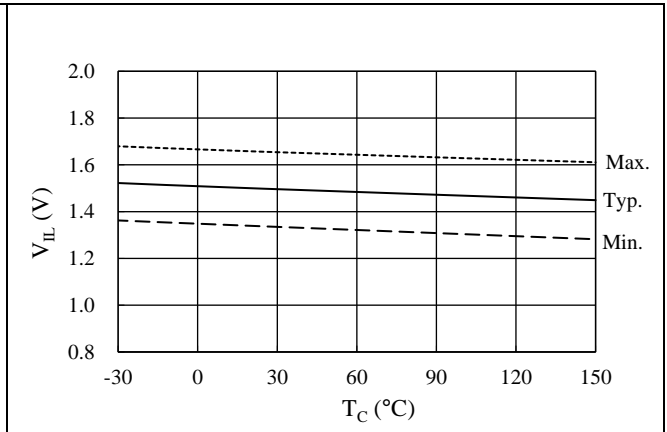


Figure 15-14. Low Level Input Signal Threshold Voltage,  $V_{IL}$  vs.  $T_C$

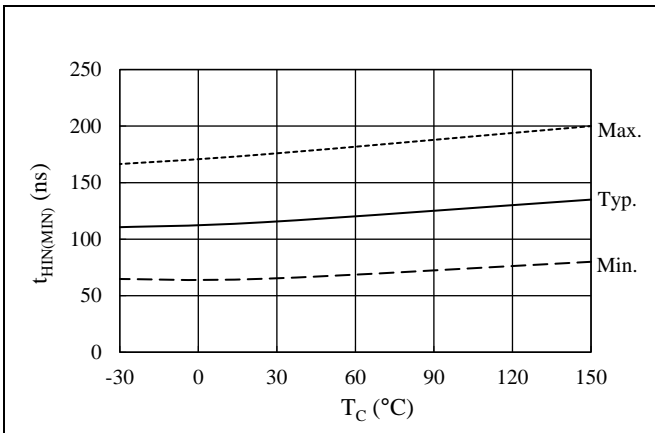


Figure 15-15. Minimum Transmittable Pulse Width for High-side Switching,  $t_{HI(MIN)}$  vs.  $T_C$

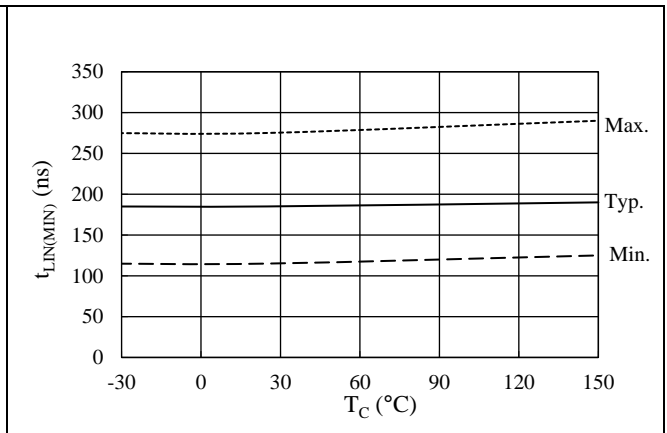


Figure 15-16. Minimum Transmittable Pulse Width for Low-side Switching,  $t_{LI(MIN)}$  vs.  $T_C$

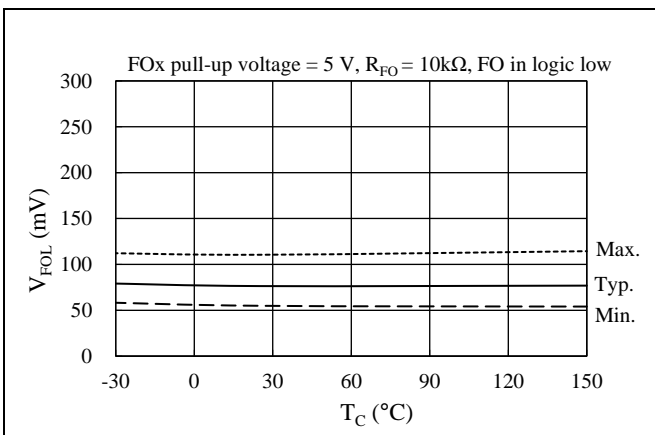


Figure 15-17. FO Pin Voltage in Normal Operation,  $V_{FOL}$  vs.  $T_C$

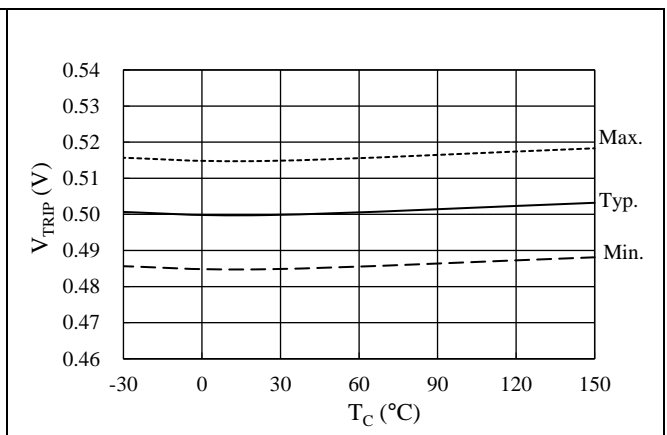


Figure 15-18. OCP Threshold Voltage,  $V_{TRIP}$  vs.  $T_C$

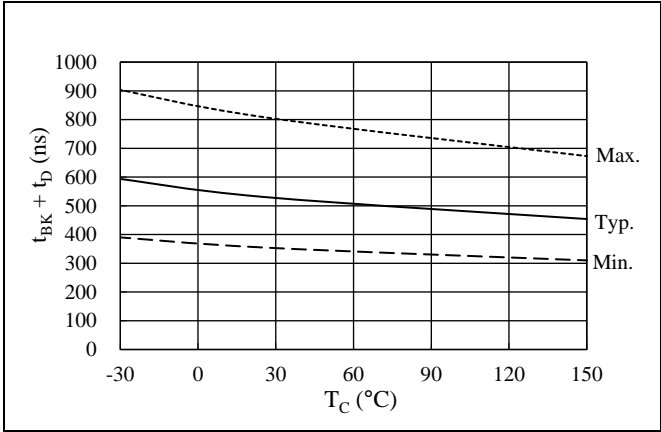


Figure 15-19. OCP Blanking Time,  $t_{BK(OCP)}$  + Propagation Delay,  $t_{D(OCP)}$  vs.  $T_C$

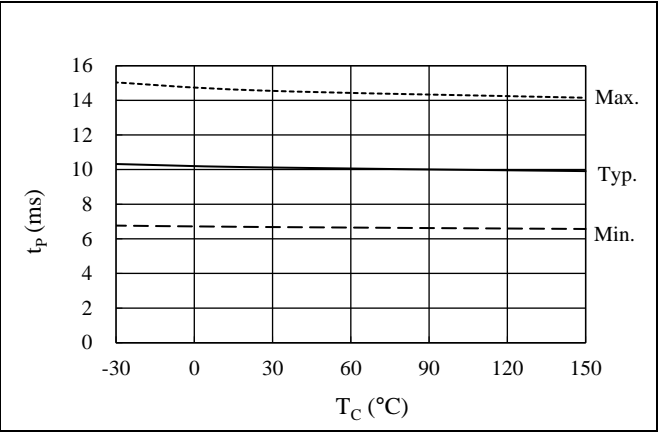


Figure 15-20. OCP Hold Time,  $t_P$  vs.  $T_C$



15.2. Performance Curves of Output Parts

15.2.1. Output Transistor Performance Curves

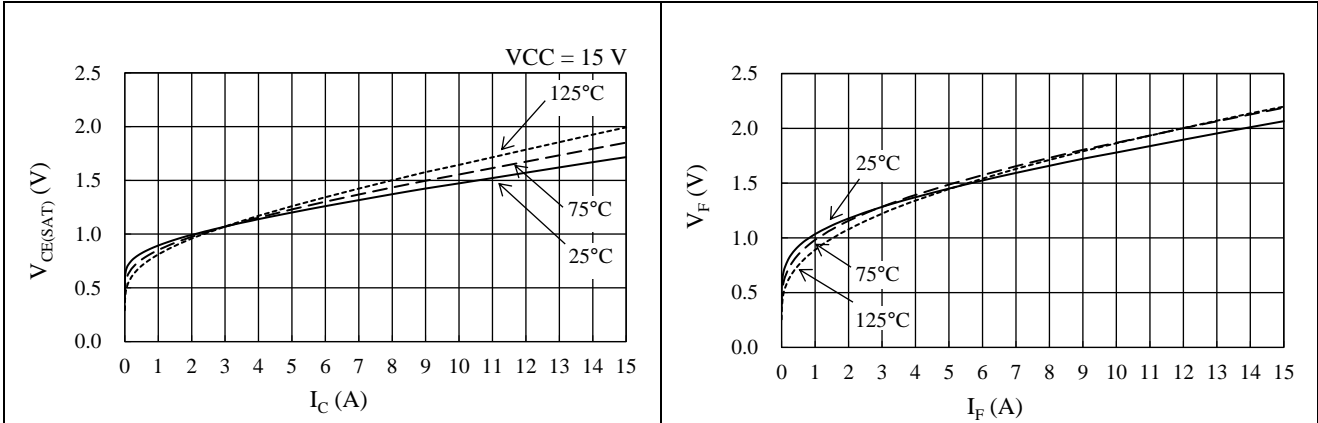


Figure 15-21. IGBT  $V_{CE(SAT)}$  vs.  $I_C$

Figure 15-22. Freewheeling Diode  $V_F$  vs.  $I_F$

15.2.2. Switching Loss Curves

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.  
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

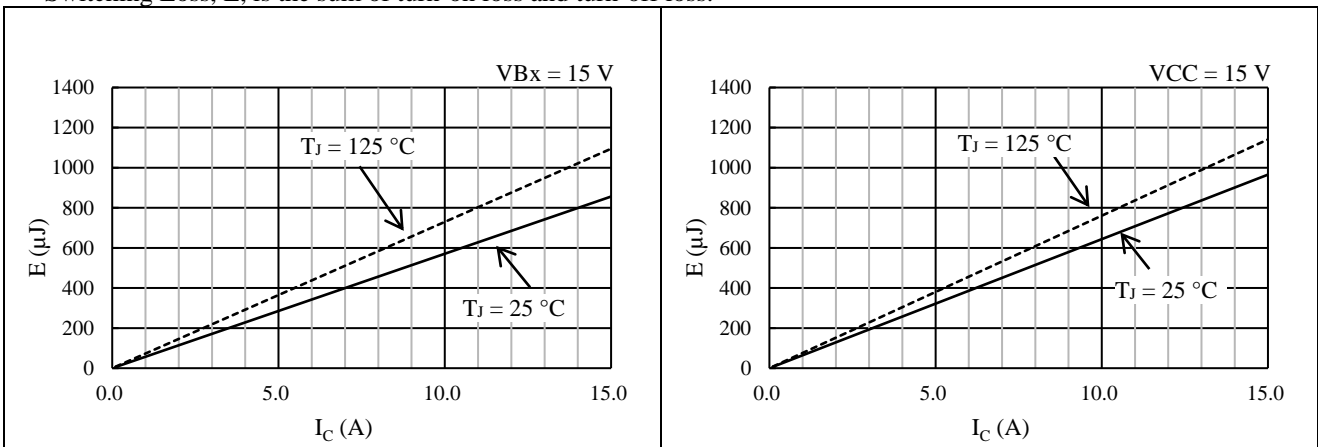


Figure 15-23. High-side Switching Loss

Figure 15-24. Low-side Switching Loss

### 15.3. Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical  $V_{CE(SAT)}$  and typical switching losses.

Operating conditions: VBB pin input voltage,  $V_{DC} = 300$  V; VCC pin input voltage,  $V_{CC} = 15$  V; modulation index,  $M = 0.9$ ; motor power factor,  $\cos\theta = 0.8$ ; junction temperature,  $T_J = 150$  °C.

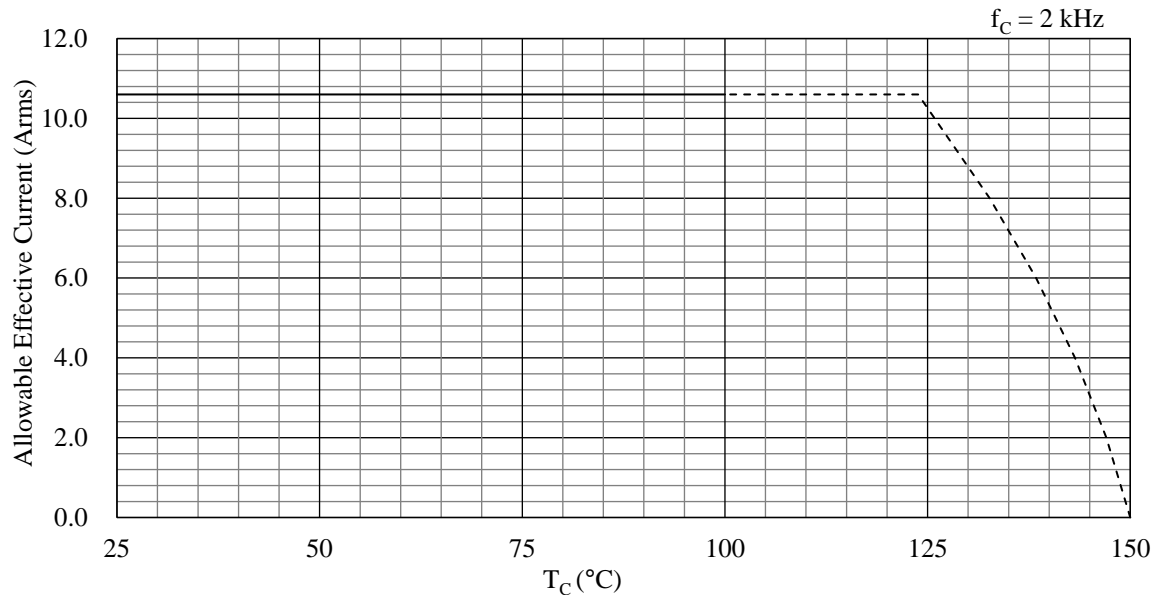


Figure 15-25. Allowable Effective Current ( $f_C = 2$  kHz)

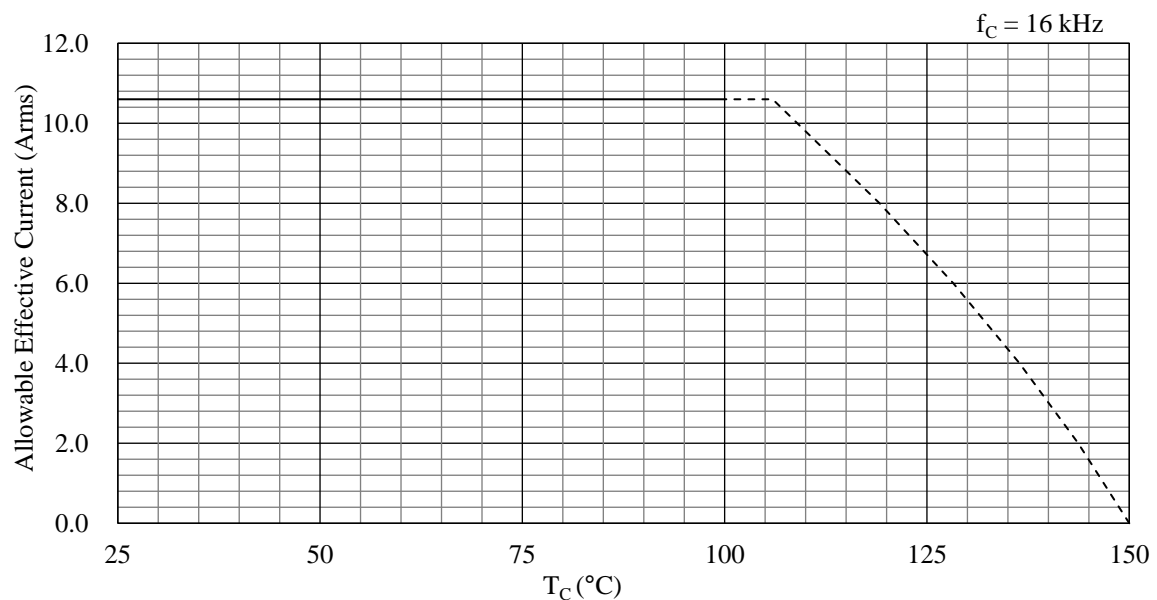


Figure 15-26. Allowable Effective Current ( $f_C = 16$  kHz)

### 15.4. Transient Thermal Resistance Curve

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state junction-to-case thermal resistance = 1. Note that the graph shows only IGBT characteristics; no freewheeling diode characteristics are included.

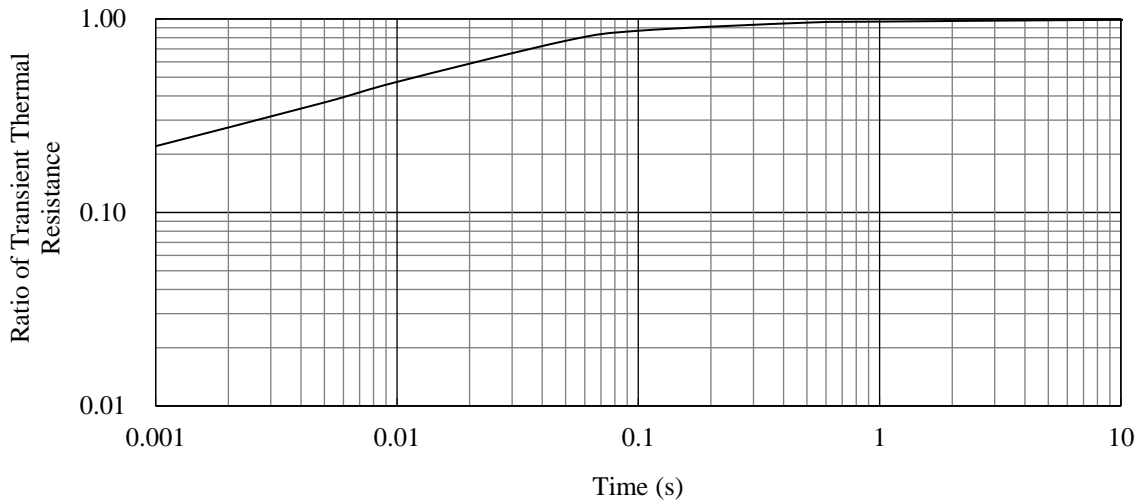


Figure 15-27. Transient Thermal Resistance

### 15.5. Short Circuit SOA (Safe Operating Area)

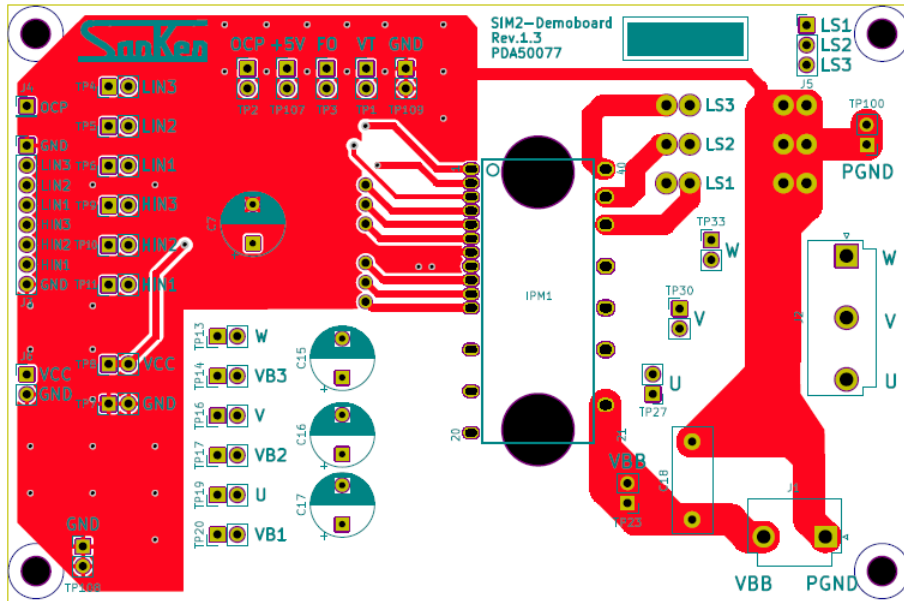
Conditions:  $V_{DC} \leq 400\text{ V}$ ,  $13.5\text{ V} \leq V_{CC} \leq 16.5\text{ V}$ ,  $T_J = 125\text{ }^\circ\text{C}$ , 1 pulse.



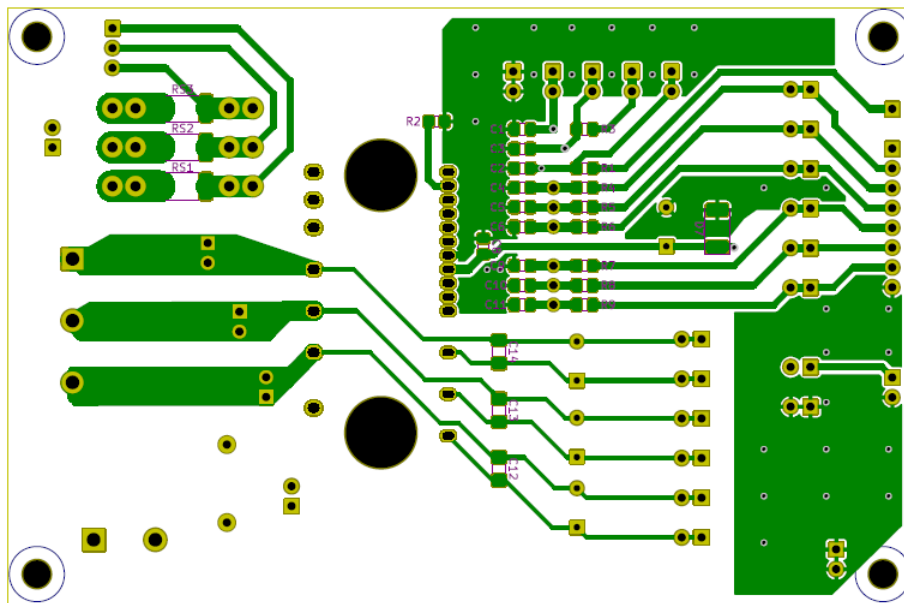
Figure 15-28. Short Circuit SOA

### 16. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SIM2-151A series device. Note that the pattern layout example only uses the parts illustrated in the circuit diagram below. For more details on through holes, see Section 10.



(Top View)



(Bottom View)

Figure 16-1. Pattern Layout Example

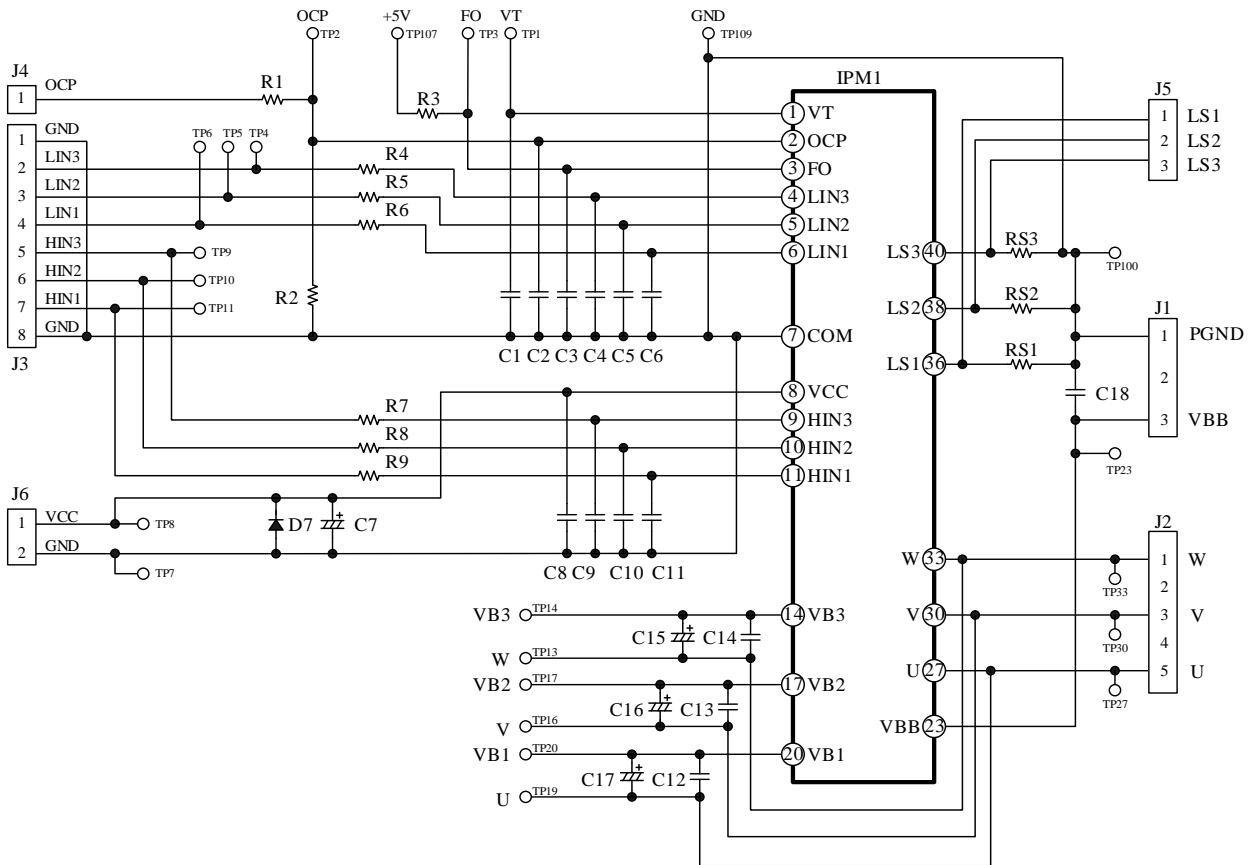


Figure 16-2. Circuit Diagram of PCB Pattern Layout Example

## SIM2-151A

### 17. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

#### • Motor Driver Specifications

|                                      |                |
|--------------------------------------|----------------|
| IC                                   | SIM2-151A      |
| Main Supply Voltage, V <sub>DC</sub> | 300 VDC (typ.) |
| Rated Output Power                   | 500 W          |

#### • Circuit Diagram

See Figure 16-2.

#### • Bill of Materials

| Symbol | Part Type              | Ratings               |
|--------|------------------------|-----------------------|
| C1     | Chip ceramic capacitor | 0.01 $\mu$ F, 50 V    |
| C2     | Chip ceramic capacitor | 10 nF, 50 V           |
| C3     | Chip ceramic capacitor | 0.01 $\mu$ F, 50 V    |
| C4     | Chip ceramic capacitor | 100 pF, 50 V          |
| C5     | Chip ceramic capacitor | 100 pF, 50 V          |
| C6     | Chip ceramic capacitor | 100 pF, 50 V          |
| C7     | Electrolytic capacitor | 47 $\mu$ F, 25 V      |
| C8     | Chip ceramic capacitor | 0.1 $\mu$ F, 50 V     |
| C9     | Chip ceramic capacitor | 100 pF, 50 V          |
| C10    | Chip ceramic capacitor | 100 pF, 50 V          |
| C11    | Chip ceramic capacitor | 100 pF, 50 V          |
| C12    | Chip ceramic capacitor | 0.1 $\mu$ F, 50 V     |
| C13    | Chip ceramic capacitor | 0.1 $\mu$ F, 50 V     |
| C14    | Chip ceramic capacitor | 0.1 $\mu$ F, 50 V     |
| C15    | Electrolytic capacitor | 10 $\mu$ F, 50 V      |
| C16    | Electrolytic capacitor | 10 $\mu$ F, 50 V      |
| C17    | Electrolytic capacitor | 10 $\mu$ F, 50 V      |
| C18    | Film capacitor         | 0.1 $\mu$ F, 450 V    |
| R1     | Chip resistor          | 100 $\Omega$ , 1/8 W  |
| R2     | Chip resistor          | Open                  |
| R3     | Chip resistor          | 10 k $\Omega$ , 1/8 W |
| R4     | Chip resistor          | 100 $\Omega$ , 1/8 W  |
| R5     | Chip resistor          | 100 $\Omega$ , 1/8 W  |
| R6     | Chip resistor          | 100 $\Omega$ , 1/8 W  |
| R7     | Chip resistor          | 100 $\Omega$ , 1/8 W  |
| R8     | Chip resistor          | 100 $\Omega$ , 1/8 W  |
| R9     | Chip resistor          | 100 $\Omega$ , 1/8 W  |
| RS1*   | Metal plate resistor   | 18 m $\Omega$ , 2 W   |
| RS2*   | Metal plate resistor   | 18 m $\Omega$ , 2 W   |
| RS3*   | Metal plate resistor   | 18 m $\Omega$ , 2 W   |
| D7     | Diode                  | Open                  |
| IPM1   | Motor Diver IC         | SIM2-151A             |
| J1     | Connector              | Equiv. to B2P3-VH     |
| J2     | Connector              | Equiv. to B3P5-VH     |
| J3     | Pin header             | Equiv. to MA08-1      |
| J4     | Pin header             | Equiv. to MA01-1      |
| J5     | Pin header             | Equiv. to MA03-1      |
| J6     | Pin header             | Equiv. to MA02-1      |

\* Refers to a part that requires adjustment based on operation performance in an actual application.

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