Sine-wave Driving, High Voltage 3-phase Motor Drivers with Built-in Hall Amplifiers

SIM262xM Series

Data Sheet

Description

The SIM262xM series are high voltage 3-phase motor drivers driven by a sinusoidal control, which can support Hall element and Hall IC inputs, thus offering high-efficient yet low-noise motor control. Supplied in a highly heat-dissipating DIP package, where a controller, a gate driver, the output transistors of three phases, and bootstrap diodes are highly integrated, the SIM262xM series requires only a few external components for building a motor driver. This also allows a motor driver to be highly reliable in performance and design-friendly with its compactness. You can select motor rotation directions, FG output pulses, and protections by setting input voltages applied to the ISx pin. The SIM262xM series supports both 8- and 10-pole motors with the function that outputs FG signals equivalent to 8-pole motor rotation signals even when a 10-pole motor is connected. These products can optimally control the inverter systems of low- to medium-capacity motors that require universal input standards.

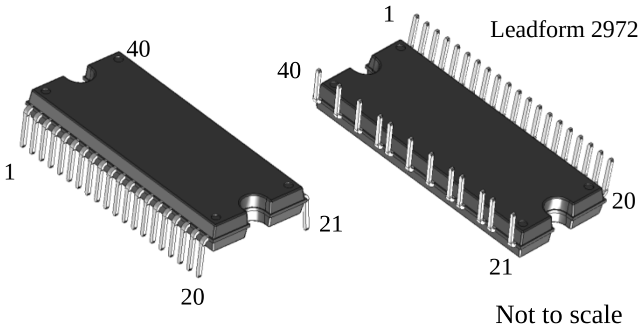
Features

- Pb-free (RoHS Compliant)
- Isolation Voltage: 1500 V (for 1 min) (UL Recognition Pending)
- Low Noise, High Efficiency (Sinusoidal Current Waveform)
- Reduced Number of Parts Achieved by Built-in Bootstrap Diodes
- Hall Element and Hall IC Inputs
- Application-specific Optimal Settings with External Signals:
  - Motor Speed
  - Phase Adavance Angle
  - Motor Direction
  - Number of Motor Poles
  - User-settable Motor Lock Detection (Enabled or Disabled)
- 5 V Reference Voltage Output (Used for Driving Hall Elements etc.)
- Protections Include:
  - VREG Pin Undervoltage Lockout (UVLO_REG)
  - Undervoltage Lockout for Power Supplies
    - VBx Pin (UVLO_VB)
    - VCC Pin (UVLO_VCC)
  - Overcurrent Limit (OCL)
  - Overcurrent Protection (OCP)
  - Overvoltage Protection (OVP)
  - Thermal Shutdown (TSD)
  - Motor Lock Protection (MLP)
  - Reverse Rotation Detection
  - Hall Signal Abnormality Detection

Package

DIP40

Mold Dimensions: 36.0 mm × 14.8 mm × 4.0 mm



Not to scale

Selection Guide

- Breakdown Voltage: 600 V

I_O	Part Number	Output Transistor
2.5 A	SIM2621M*	Power MOSFET
5.0 A	SIM2622M	IGBT + FRD

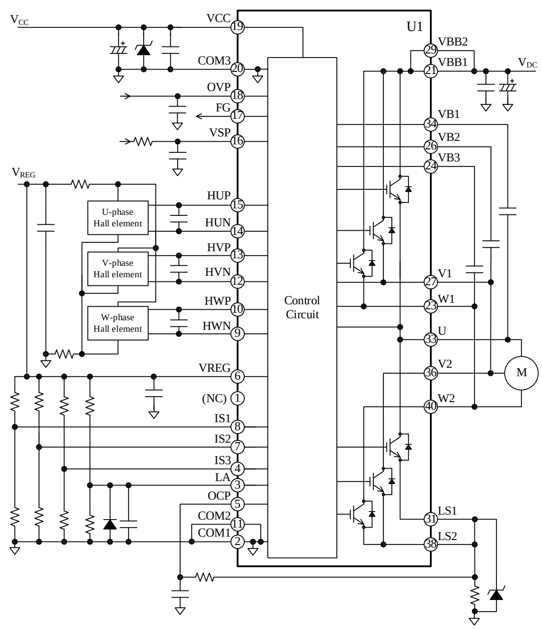
* Under development

Applications

For motor drives such as:

- Fan Motor and Pump Motor for Washer and Dryer
- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM3 = COM.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBBx–LSx	450	V	SIM2622M
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBBx–LSx	600	V	SIM2622M
Power MOSFET / IGBT Breakdown Voltage	V_{DSS}	I_D = 100 µA	600	V	SIM2621M
	V_{CES}	I_C = 1 mA	600	V	SIM2622M
Logic Supply Voltage	V_{CC}	VCC–COM	20	V	
	V_{BS}(1)	VB1–U, VB2–V1, VB3–W1	20	V	
Output Current (DC)(2)	I_O	T_C = 25 °C, T_J < 150 °C	2.5	A	SIM2621M
			5.0		SIM2622M
Output Current (Pulse)	I_{OP}	T_C = 25 °C, pulse width ≤ 100 µs	3.75	A	SIM2621M
			7.5		SIM2622M
VREG Pin Output Voltage	V_{REG}		5.5	V	
VREG Pin Current	I_{REG}		30	mA	
Input Voltage 1 (HUP, HUN, HVP, HVN, HWP, HWN, IS1, IS2, IS3, LA, OVP, OCP)	$V_{IN(1)}$		−0.5 to V_{REG}	V	
Input Voltage 2 (VSP)	$V_{IN(2)}$		−0.5 to 10	V	
Output Voltage (FG)	V_O		−0.5 to V_{REG}	V	
LSx Pin Voltage (DC)	$V_{LS(DC)}$	LSx–COM	−0.7 to 7	V	
LSx Pin Voltage (Surge)	$V_{LS(SURGE)}$	LSx–COM	−4 to 7	V	
Operating Case Temperature(3)	$T_{C(OP)}$		−30 to 100	°C	
Junction Temperature(4)	T_J		150	°C	
Storage Temperature	T_{STG}		−40 to 150	°C	

(1) Set the voltage between the VBx and the output (U, V1/V2, W1/W2) pins (VBx-HSx) so that VBx > HSx.
(2) Should be derated depending on an actual case temperature. See Section 17.4.
(3) Refers to a case temperature measured during IC operation.
(4) Refers to the junction temperature of each chip built in the IC, including the control stage, gate drive stage, and output transistors.

2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM3 = COM.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBBx–LSx	—	300	400	V	
Logic Supply Voltage	V_{CC}	VCC–COM	13.5	—	16.5	V	
	V_{BS}	VB1–U, VB2–V, VB3–W1	13.5	—	16.5	V	
Input Voltage 1 (HUP, HUN, HVP, HVN, HWP, HWN, IS1, IS2, IS3, LA, OVP, OCP)	$V_{IN(1)}$		0	—	5.0	V	
Input Voltage 2 (VSP)	$V_{IN(2)}$		0	—	5.4	V	
Bootstrap Capacitor	C_B		1	—	—	μF	
Shunt Resistor*	R_S	$I_{OP} \leq 3.75$ A	176	—	—	mΩ	SIM2621M
		$I_{OP} \leq 7.5$ A	88	—	—	mΩ	SIM2622M
RC Filter Resistor	R_O		—	—	100	Ω	
RC Filter Capacitor	C_O		100	—	2200	pF	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

* Should be a low-inductance resistor.

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM3 = COM.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Operation						
Low-side Logic Operation Start Voltage	$V_{CC(ON)}$	VCC–COM	10.5	11.5	12.5	V
Low-side Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC–COM	10.0	11.0	12.0	V
High-side Logic Operation Start Voltage	$V_{BS(ON)}$	VB1–U, VB2–V1, VB3–W1	9.5	10.5	11.5	V
High-side Logic Operation Stop Voltage	$V_{BS(OFF)}$	VB1–U, VB2–V1, VB3–W1	9.0	10.0	11.0	V
Logic Supply Current	I_{CC}	V_{SP} = 5.4 V, I_{REG} = 0 A	—	7.0	—	mA
Logic Supply Current	I_{BS}	V_{Bx} = 15 V, V_{SP} = 5.4 V; VBx pin current in 1-phase operation	40	140	350	μA
VREG Pin Output Voltage	V_{REG}	I_{REG} = 0 mA to 30 mA	4.5	5.0	5.5	V
Input Signal[1]						
High Level Input Current 1 (LA, VSP, IS1, IS2, IS3)	I_{IH1}	V_{IN} = V_{REG}	—	25	100	μA
Low Level Input Current 1 (LA, VSP, IS1, IS2, IS3)	I_{IL1}	V_{INL} = 0 V	—	—	2	μA
High Level Input Current 2 (OCP)	I_{IH2}	V_{IN} = V_{REG}	−5	—	5	μA
Low Level Input Current 2 (OCP)	I_{IL2}	V_{INL} = 0 V	—	23	90	μA
High Level Input Current 3 (HUP, HUN, HVP, HVN, HWP, HWN, OVP)	I_{IH3}	V_{IN} = V_{REG}	−5	—	5	μA
Low Level Input Current 3 (HUP, HUN, HVP, HVN, HWP, HWN, OVP)	I_{IL3}	V_{INL} = 0 V	−5	—	5	μA
High Level Output Voltage (FG)	V_{OH}		4.5	—	5.5	V
Low Level Output Voltage (FG)	V_{OL}		—	—	0.5	V

[1] Guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PWM Control						
PWM Carrier Frequency(2)	f_C		16	17	18	kHz
Internal Oscillator Frequency(2)	f_{OSC}		4.10	4.32	4.54	MHz
Dead Time(2)	t_D		—	1.0	—	µs
Control IC Output Pulse Duty Cycle(2)	D	V_{SP} = 2.0 V	—	0	3	%
		V_{SP} = 3.7 V	47	50	53	%
		V_{SP} = 5.0 V (driven by trapezoidal control)	88.0	—	91.8	%
		V_{SP} = 5.4 V (driven by sinusoidal control)	93.7	—	100	%
Protection						
OCL Threshold Voltage	V_{LIM}		0.25	0.30	0.35	V
OCL Blanking Time	$t_{BK(OCL)}$		—	2.6	4.6	µs
OCP Threshold Voltage	V_{TRIP}		0.54	0.60	0.66	V
OCP Blanking Time	$t_{BK(OCP)}$		—	0.8	1.7	µs
OCP Hold Time	t_P		14	15	16	ms
MLP Detection Time	t_{LD}		4.7	5	5.3	s
MLP Hold Time	t_{LH}		1.8	2.0	2.2	s
TSD Operating Temperature(3)	T_{DH}	I_{REG} = 0 mA; without heatsink	—	130	—	°C
TSD Releasing Temperature(3)	T_{DL}		—	100	—	°C
TSD Hysteresis Temperature(3)	$T_{D(HYS)}$		—	30	—	°C
VREG Pin Undervoltage Lockout Operating Voltage(2)	V_{UVRL}		3.24	3.60	3.96	V
VREG Pin Undervoltage Lockout Releasing Voltage(2)	V_{UVRH}		3.60	4.00	4.40	V
OVP Operating Voltage	V_{OVPH}		2.25	2.50	2.75	V
OVP Releasing Voltage	V_{OVPL}		2.05	2.30	2.55	V

(2) Refers to an internal signal; guaranteed by design.
(3) Refers to the junction temperature of the gate drive stage.

3.2 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	—	—	100	µA
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 10 mA; voltage drop in R_{BOOT} included	—	3.0	5.0	V

3.3 Transistor Characteristics

Figure 3-1 provides the definitions of switching characteristics described in this and the following sections. Internal signals, HINx and LINx, are defined as V_{IN} (see Section 6). The SIM2621M is an IC having built-in power MOSFETs; the SIM2622M is an IC incorporating IGBTs and freewheeling diodes.

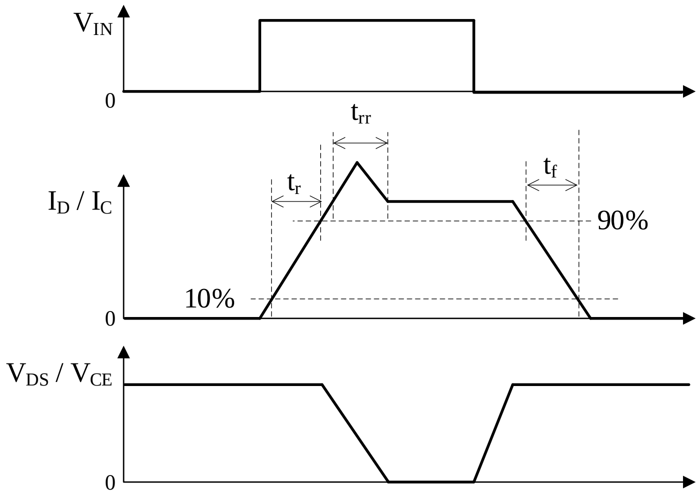


Figure 3-1. Switching Characteristics Definitions

3.3.1 SIM2621M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{IN} = 0 V	—	—	100	µA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1.25 A, V_{IN} = 5 V	—	2.0	2.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 1.25 A, V_{IN} = 0 V	—	1.0	1.6	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, I_D = 1.25 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	150	—	ns
Rise Time*	t_r		—	80	—	ns
Fall Time*	t_f		—	30	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, I_D = 1.25 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	175	—	ns
Rise Time*	t_r		—	95	—	ns
Fall Time*	t_f		—	25	—	ns

3.3.2 SIM2622M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 5.0 A, V_{IN} = 5 V	—	1.75	2.2	V
Diode Forward Voltage	V_F	I_F = 5.0 A, V_{IN} = 0 V	—	2.0	2.4	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, I_C = 5.0 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	80	—	ns
Rise Time*	t_r		—	70	—	ns
Fall Time*	t_f		—	100	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, I_C = 5.0 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	80	—	ns
Rise Time*	t_r		—	100	—	ns
Fall Time*	t_f		—	100	—	ns

* Guaranteed by design.

3.4 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance[1]	$R_{J\text{-}C}$	All power MOSFETs operating	—	—	3.6	°C/W	SIM2621M
	$R_{(J\text{-}C)Q}$[2]	All IGBTs operating	—	—	3.6	°C/W	SIM2622M
	$R_{(J\text{-}C)F}$[3]	All freewheeling diodes operating	—	—	4.2	°C/W	SIM2622M
Junction-to-Ambient Thermal Resistance	$R_{J\text{-}A}$	All power MOSFETs operating	—	—	25	°C/W	SIM2621M
	$R_{(J\text{-}A)Q}$	All IGBTs operating	—	—	25	°C/W	SIM2622M
	$R_{(J\text{-}A)F}$	All freewheeling diodes operating	—	—	29	°C/W	SIM2622M

(1) Refers to a case temperature at the measurement point described in Figure 3-2.
(2) Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 17.1.
(3) Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

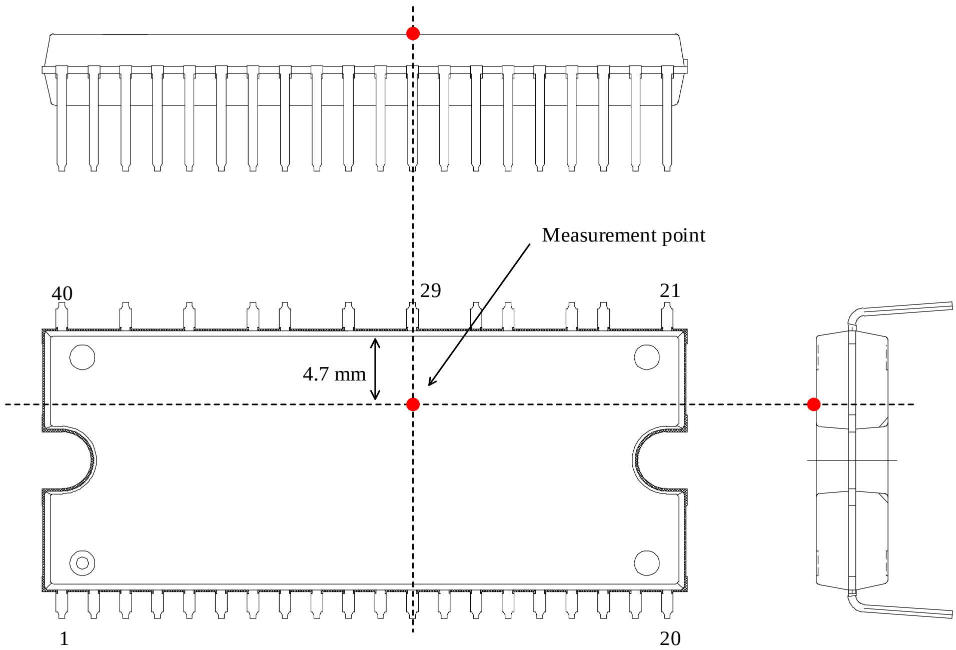


Figure 3-2. Case Temperature Measurement Point

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	*	0.294	—	0.441	N·m	
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	100	µm	
Package Weight		—	5.2	—	g	

* Requires using a metric screw of M2.5 and a plain washer of 6.0 mm (φ). For more on screw tightening, see Section 15.3.

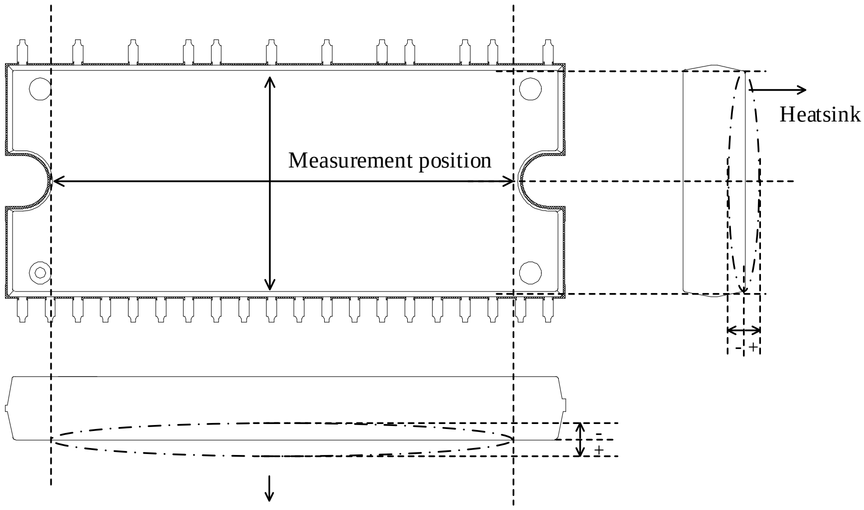


Figure 4-1. Flatness Measurement Position

5. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clearance	Between heatsink* and leads. See Figure 5-1.	1.5	—	2.1	mm	
Creepage		1.7	—	—	mm	

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

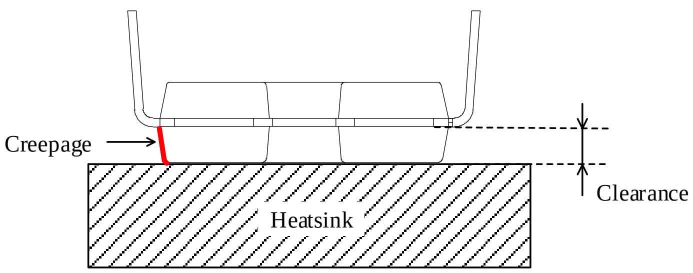


Figure 5-1. Insulation Distance Definitions

6. Block Diagrams

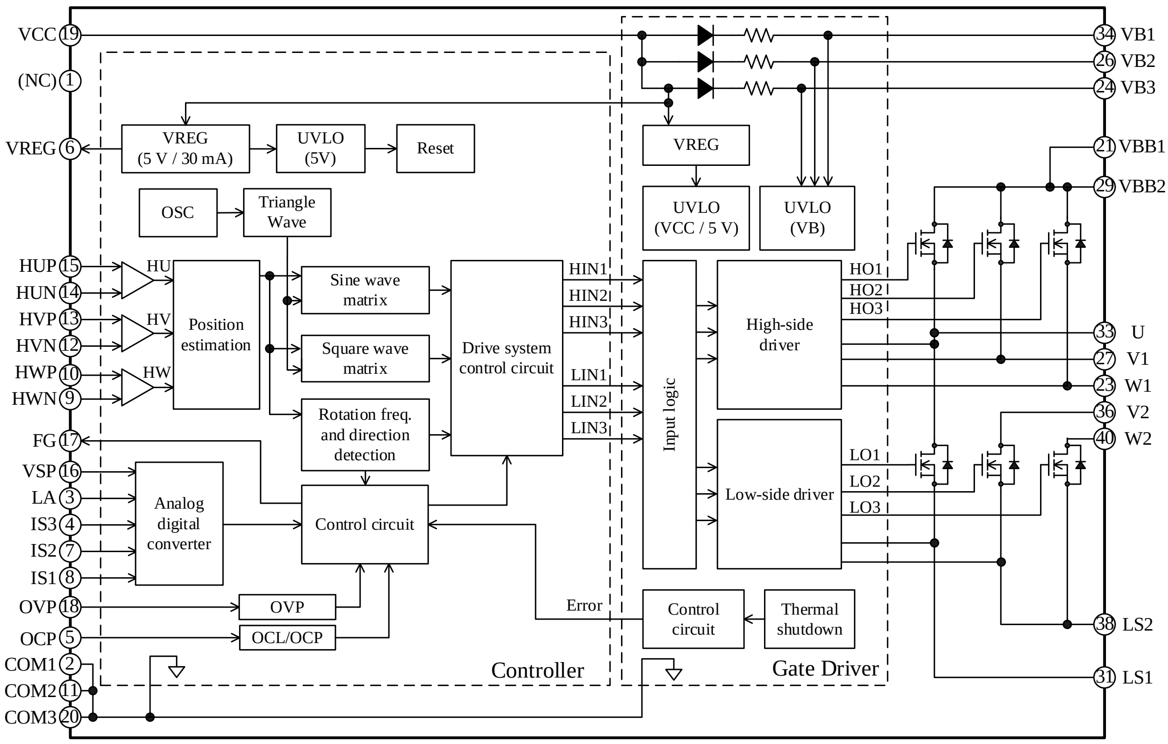


Figure 6-1. Block Diagram: SIM2621M

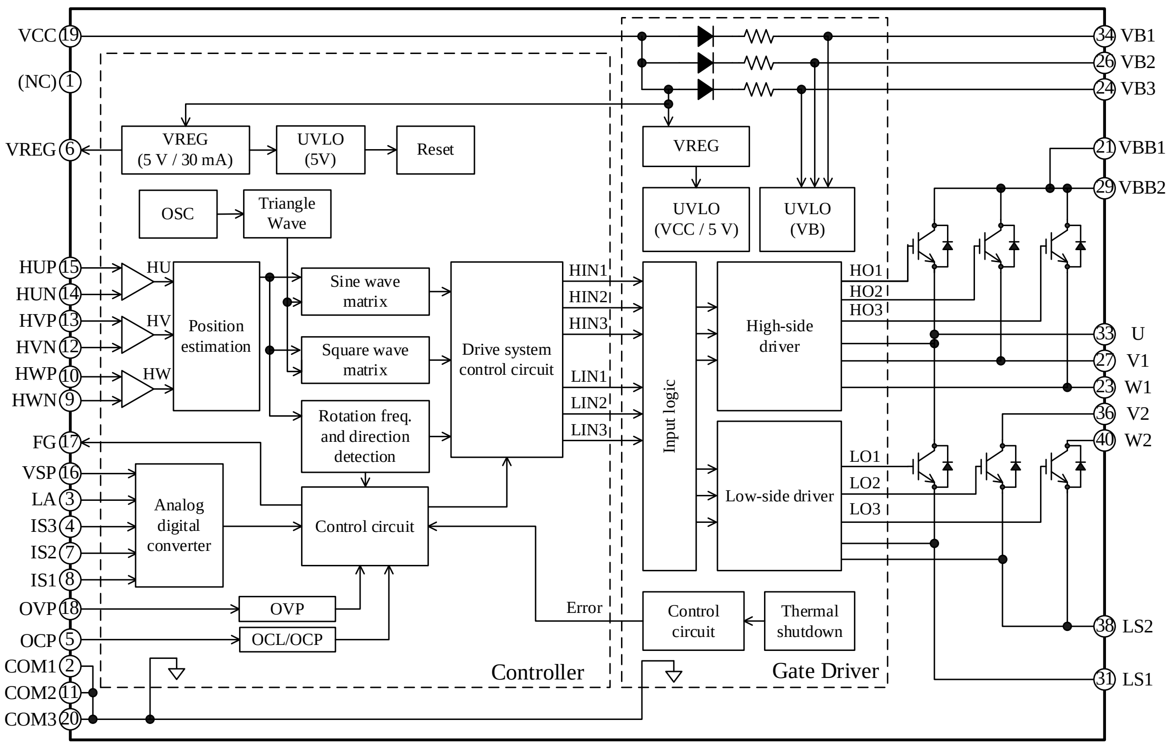
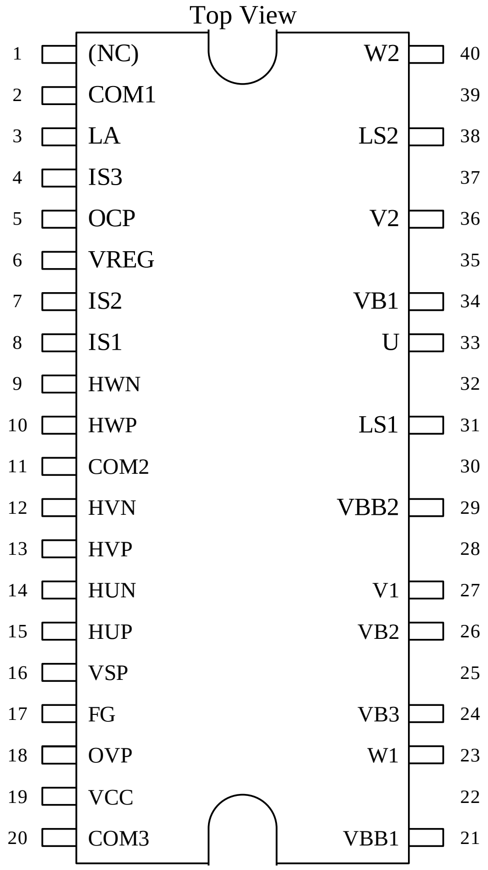


Figure 6-2. Block Diagram: SIM2622M

7. Pin Configuration Definitions



Pin Number	Pin Name	Description
1	NC	(No connection)
2	COM1	Logic ground
3	LA	Input for phase advance angle setting signal
4	IS3	Function setting pin 3 (rotation direction, motor lock protection, voltage range of output duty cycle control)
5	OCP	Input for overcurrent detection signal
6	VREG	Internal regulator output
7	IS2	Function setting pin 2 (phase advance setting)
8	IS1	Function setting pin 1 (the number of rotation pulses, the number of motor poles, protection recovery mode setting)
9	HWN	W-phase Hall element negative signal input (−)
10	HWP	W-phase Hall element positive signal input (+)
11	COM2	Logic ground
12	HVN	V-phase Hall element negative signal input (−)
13	HVP	V-phase Hall element positive signal input (+)
14	HUN	U-phase Hall element negative signal input (−)
15	HUP	U-phase Hall element positive signal input (+)
16	VSP	Input for motor speed control signal
17	FG	Rotation pulse signal output
18	OVP	Input for overvoltage detection signal
19	VCC	Input for logic supply voltage
20	COM3	Logic ground
21	VBB1	Positive DC bus supply voltage (+)
22	—	Pin removed
23	W1	W-phase output (connected to W2 externally)
24	VB3	W-phase high-side floating supply voltage input
25	—	Pin removed
26	VB2	V-phase high-side floating supply voltage input
27	V1	V-phase output (connected to V2 externally)
28	—	Pin removed
29	VBB2	Positive DC bus supply voltage (+)
30	—	Pin removed
31	LS1	U-phase low-side IGBT emitter (connected to L2 externally)
32	—	Pin removed
33	U	U-phase output
34	VB1	U-phase high-side floating supply voltage input
35	—	Pin removed
36	V2	V-phase output (connected to V1 externally)
37	—	Pin removed
38	LS2	V-/W- phases low-side IGBT emitter (connected to L1 externally)
39	—	Pin removed
40	W2	W-phase output (connected to W1 externally)

8. Typical Applications

Figure 8-1 is a typical application which uses signals input from the Hall elements; Figure 8-2 is a typical application which uses signals input from Hall ICs.

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

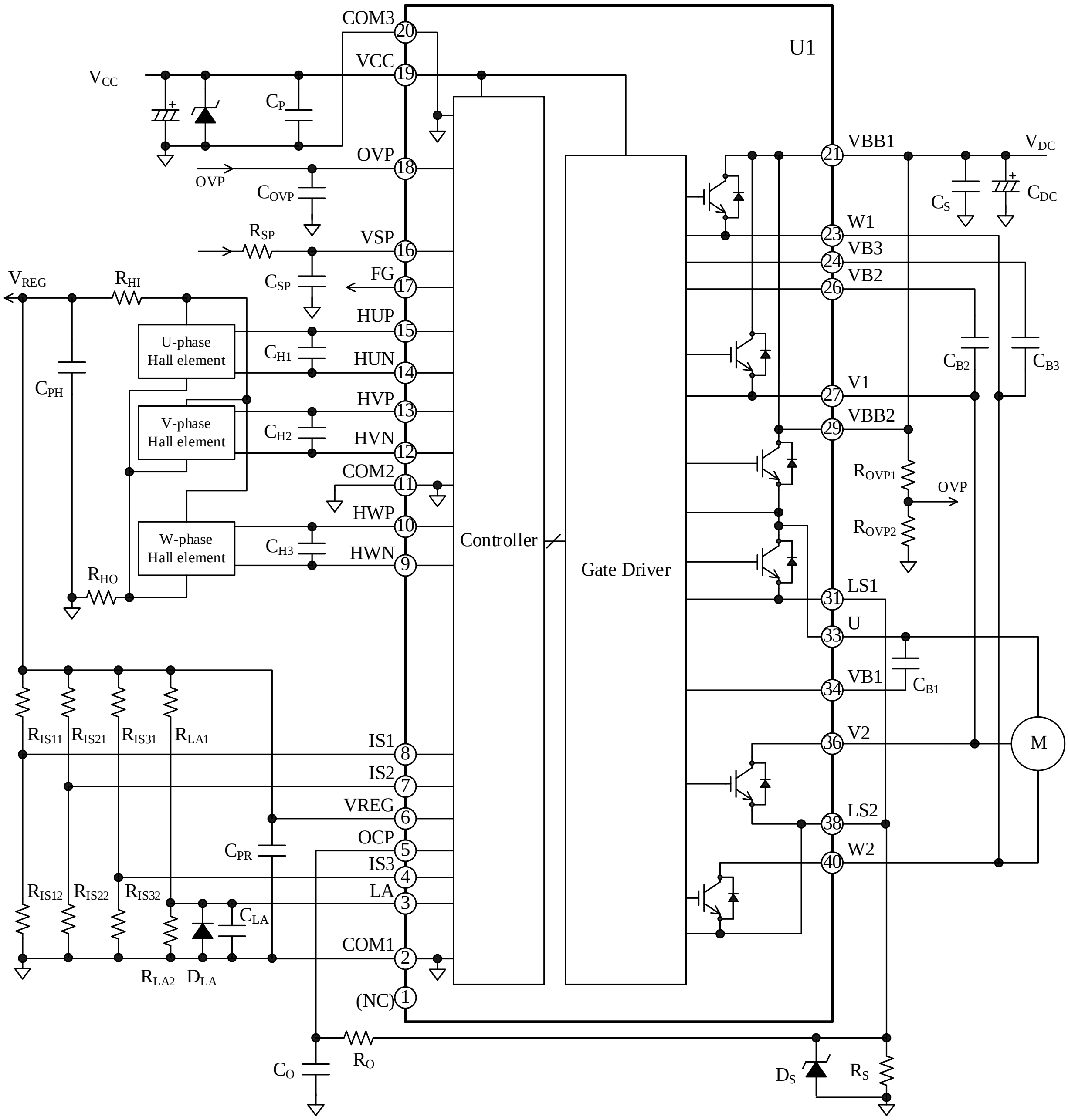


Figure 8-1. Application Using Signals Input from Hall Elements

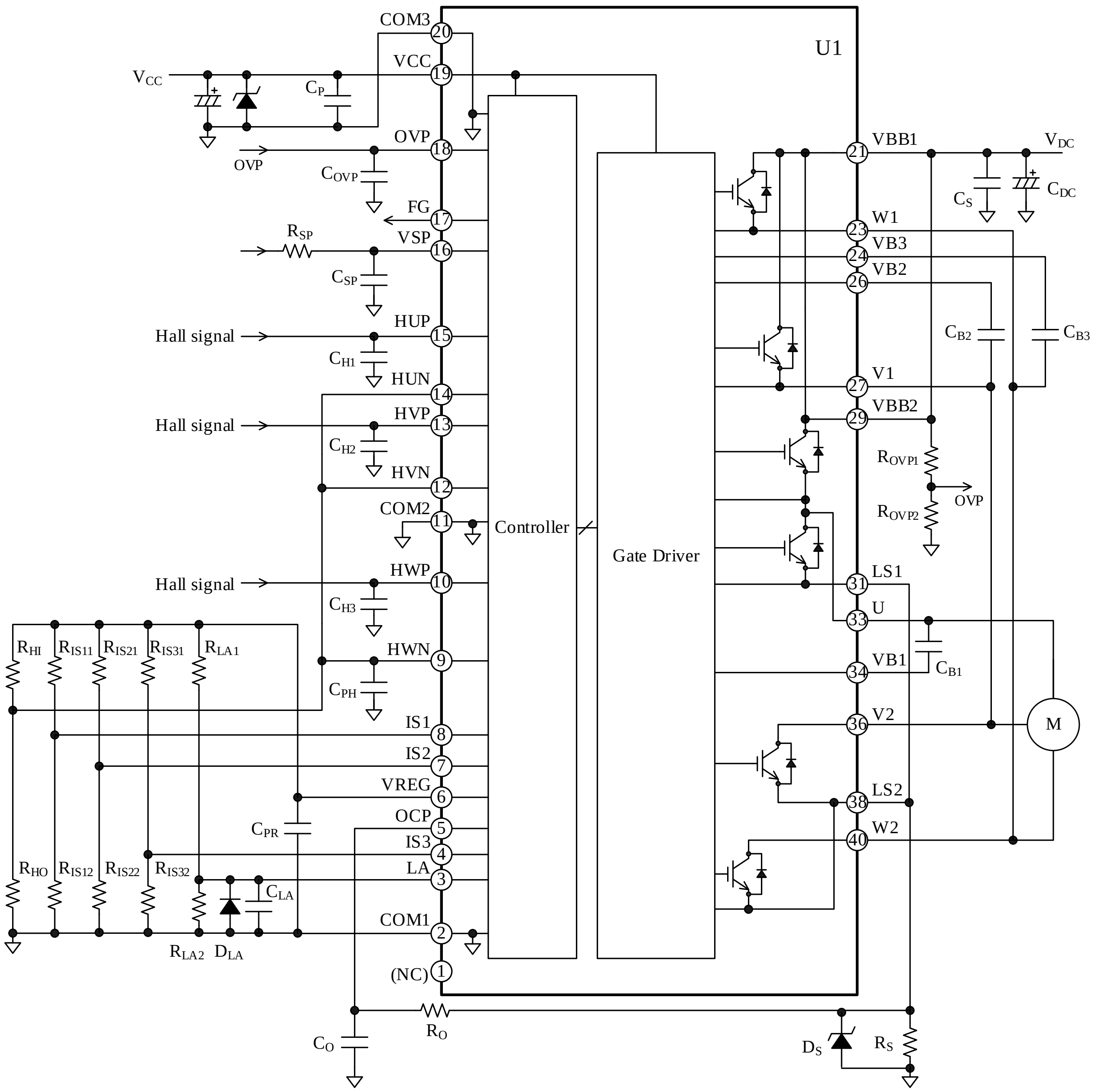
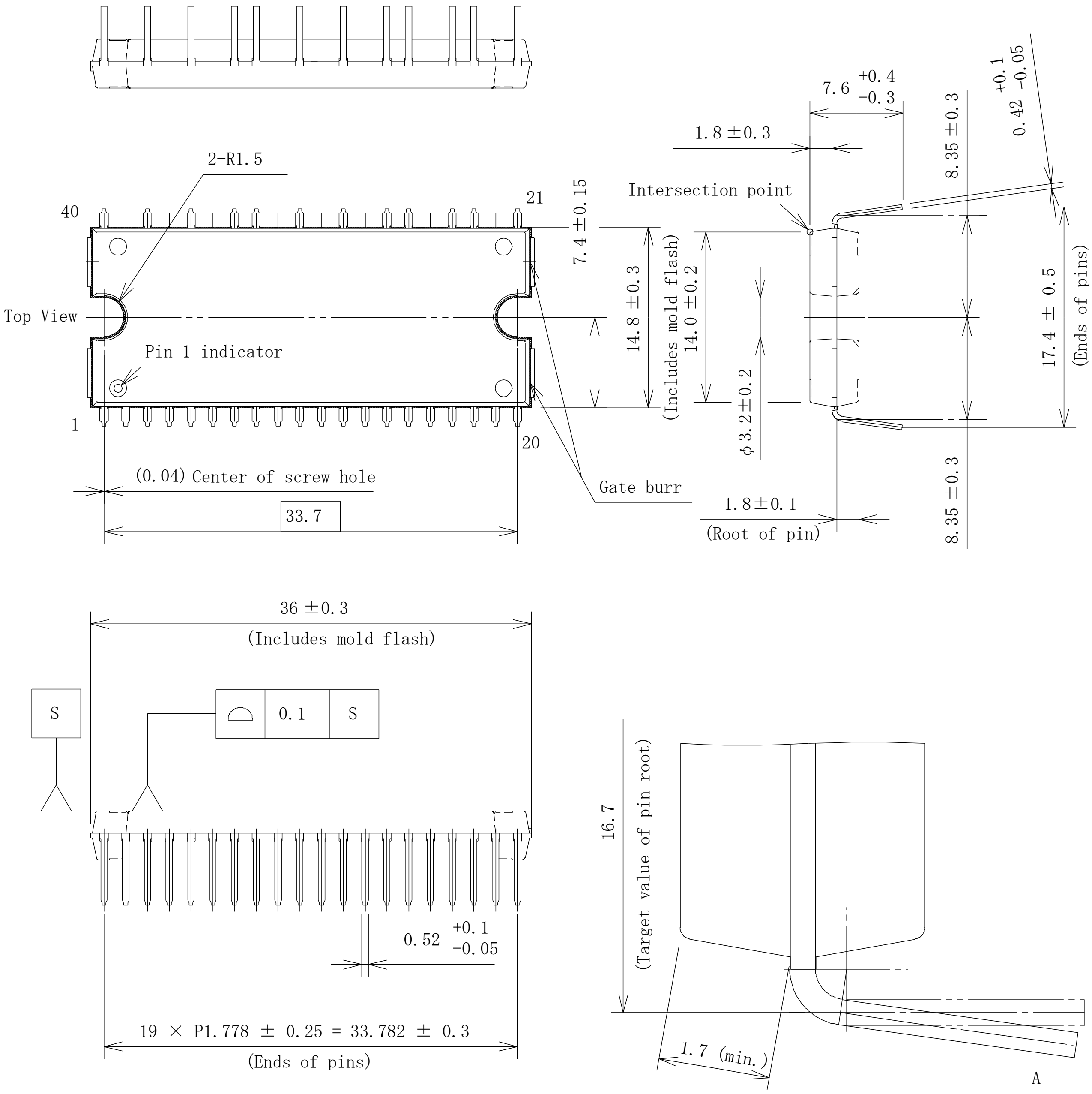


Figure 8-2. Application Using Signals Input from Hall ICs

9. Physical Dimensions

● **DIP40 Package**

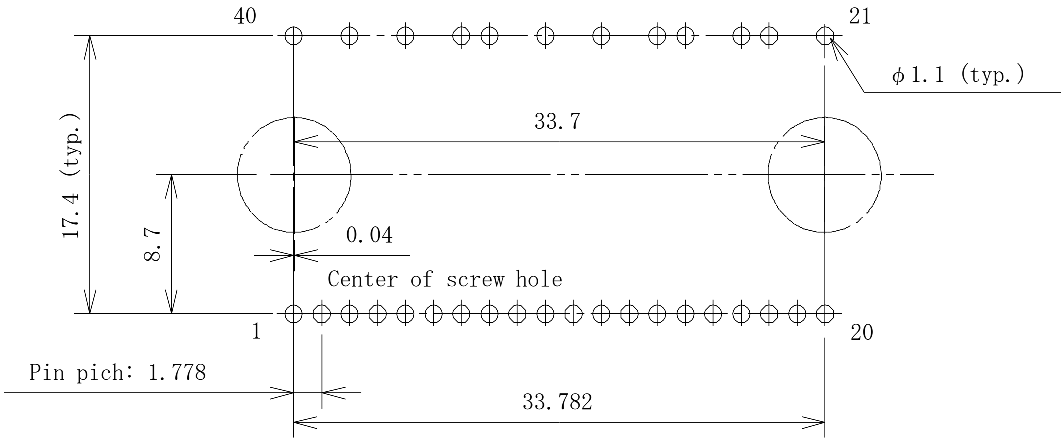


NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)
- "A" represents a pin illustrated for reference only, not the actual state of a bend.
- Maximum gate burr height is 0.3 mm.

- **Land Pattern Example**

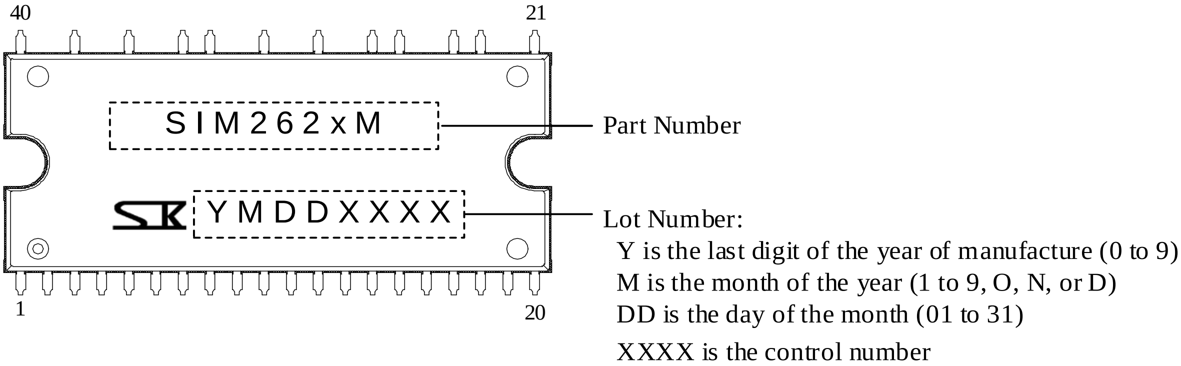
- **Reference Through Hole Size and Layout**



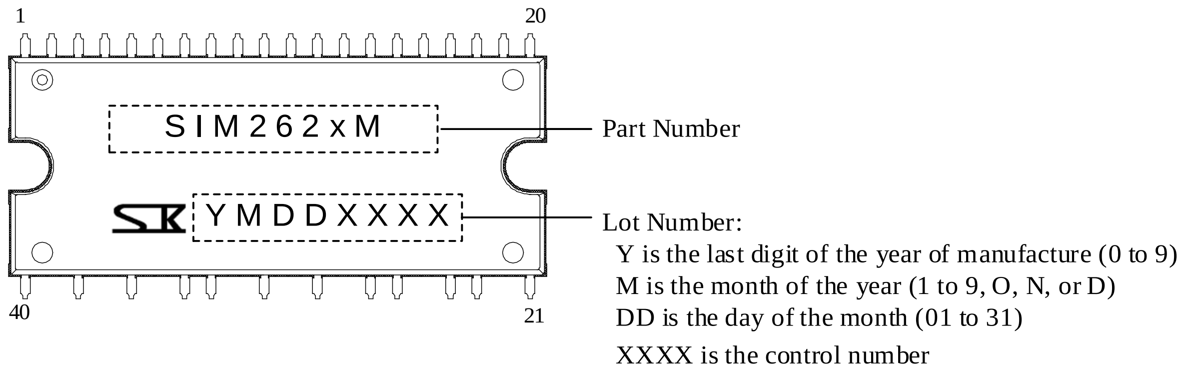
Unit: mm

10. Marking Diagram

- **Front-side Marking**



- **Back-side Marking**



11. Truth Tables

Table 11-1 and Table 11-2 are truth tables for motor driving at startup by the trapezoidal control in a forward or reverse rotation, respectively.

Table 11-1. Truth Table for Trapezoidal Control (Forward)

Position Sensing Signal			U-phase		V-phase		W-phase	
HU	HV	HW	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor
H	L	H	OFF	ON	ON	OFF	OFF	OFF
H	L	L	OFF	ON	OFF	OFF	ON	OFF
H	H	L	OFF	OFF	OFF	ON	ON	OFF
L	H	L	ON	OFF	OFF	ON	OFF	OFF
L	H	H	ON	OFF	OFF	OFF	OFF	ON
L	L	H	OFF	OFF	ON	OFF	OFF	ON
L	L	L	OFF	OFF	OFF	OFF	OFF	OFF
H	H	H	OFF	OFF	OFF	OFF	OFF	OFF

Table 11-2. Truth Table for Trapezoidal Control (Reverse)

Position Sensing Signal			U-phase		V-phase		W-phase	
HU	HV	HW	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor
L	H	L	OFF	ON	ON	OFF	OFF	OFF
L	H	H	OFF	ON	OFF	OFF	ON	OFF
L	L	H	OFF	OFF	OFF	ON	ON	OFF
H	L	H	ON	OFF	OFF	ON	OFF	OFF
H	L	L	ON	OFF	OFF	OFF	OFF	ON
H	H	L	OFF	OFF	ON	OFF	OFF	ON
H	H	H	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	OFF	OFF	OFF	OFF	OFF	OFF

12. Pin Settings: IS1, IS2, and IS3

Table 12-1 to Table 12-3 list the settings for the ISx pin. Setting the ISx pin voltages at startup enables the individual pin settings (e.g., the number of rotation pulse signals, phase advance angles, rotation directions).

Table 12-1. IS1 Pin Settings

IS1 Pin Voltage (Typ.)	Number of FG Output Pulses		Protection Recovery Mode
	Number of Motor Poles	Number of FG Output Pulses per Motor Rotation	
0 to 1/8 V_{REG}	8 poles	3 pulses	Automatic
1/8 V_{REG} to 2/8 V_{REG}	8 poles	3 pulses	Manual
2/8 V_{REG} to 3/8 V_{REG}	10 poles	3 pulses	Automatic
3/8 V_{REG} to 4/8 V_{REG}	10 poles	3 pulses	Manual
4/8 V_{REG} to 5/8 V_{REG}	10 poles	1 pulse	Manual
5/8 V_{REG} to 6/8 V_{REG}	10 poles	1 pulse	Automatic
6/8 V_{REG} to 7/8 V_{REG}	8 poles	1 pulse	Manual
7/8 V_{REG} to 8/8 V_{REG}	8 poles	1 pulse	Automatic

Table 12-2. IS2 Pin Settings

IS2 Pin Voltage (Typ.)	Phase Advance Function	Setting Range of Phase Advance Angle
0 to 1/8 V_{REG}	External phase advance	0° to 58°
1/8 V_{REG} to 2/8 V_{REG}	Cubic function operation	0° to 58°
2/8 V_{REG} to 3/8 V_{REG}	Quadratic function operation	0° to 29°
3/8 V_{REG} to 4/8 V_{REG}	Quadratic function operation	0° to 41°
4/8 V_{REG} to 5/8 V_{REG}	Quadratic function operation	0° to 58°
5/8 V_{REG} to 6/8 V_{REG}	Linear function operation	0° to 29°
6/8 V_{REG} to 7/8 V_{REG}	Linear function operation	0° to 41°
7/8 V_{REG} to 8/8 V_{REG}	Linear function operation	0° to 58°

Table 12-3. IS3 Pin Settings

IS3 Pin Voltage (Typ.)	Rotation Direction	Motor Lock Protection	Voltage Range of Output Duty Cycle Control
0 to 1/8 V_{REG}	Forward (CW)	Enabled	2.1 V to 5.4 V
1/8 V_{REG} to 2/8 V_{REG}	Forward (CW)	Disabled	2.1 V to 5.4 V
2/8 V_{REG} to 3/8 V_{REG}	Forward (CW)	Enabled	0.5 V to 5.4 V
3/8 V_{REG} to 4/8 V_{REG}	Forward (CW)	Disabled	0.5 V to 5.4 V
4/8 V_{REG} to 5/8 V_{REG}	Reverse (CCW)	Disabled	0.5 V to 5.4 V
5/8 V_{REG} to 6/8 V_{REG}	Reverse (CCW)	Enabled	0.5 V to 5.4 V
6/8 V_{REG} to 7/8 V_{REG}	Reverse (CCW)	Disabled	2.1 V to 5.4 V
7/8 V_{REG} to 8/8 V_{REG}	Reverse (CCW)	Enabled	2.1 V to 5.4 V

13. Timing Charts

The following symbols used in these figures represent the signals generated inside the IC: S_U, S_V, S_W, S_X, S_Y, S_Z.

Figure 13-1 shows the operational waveforms of each pin when an 8-pole motor rotates forward (no phase advance) in normal operation.

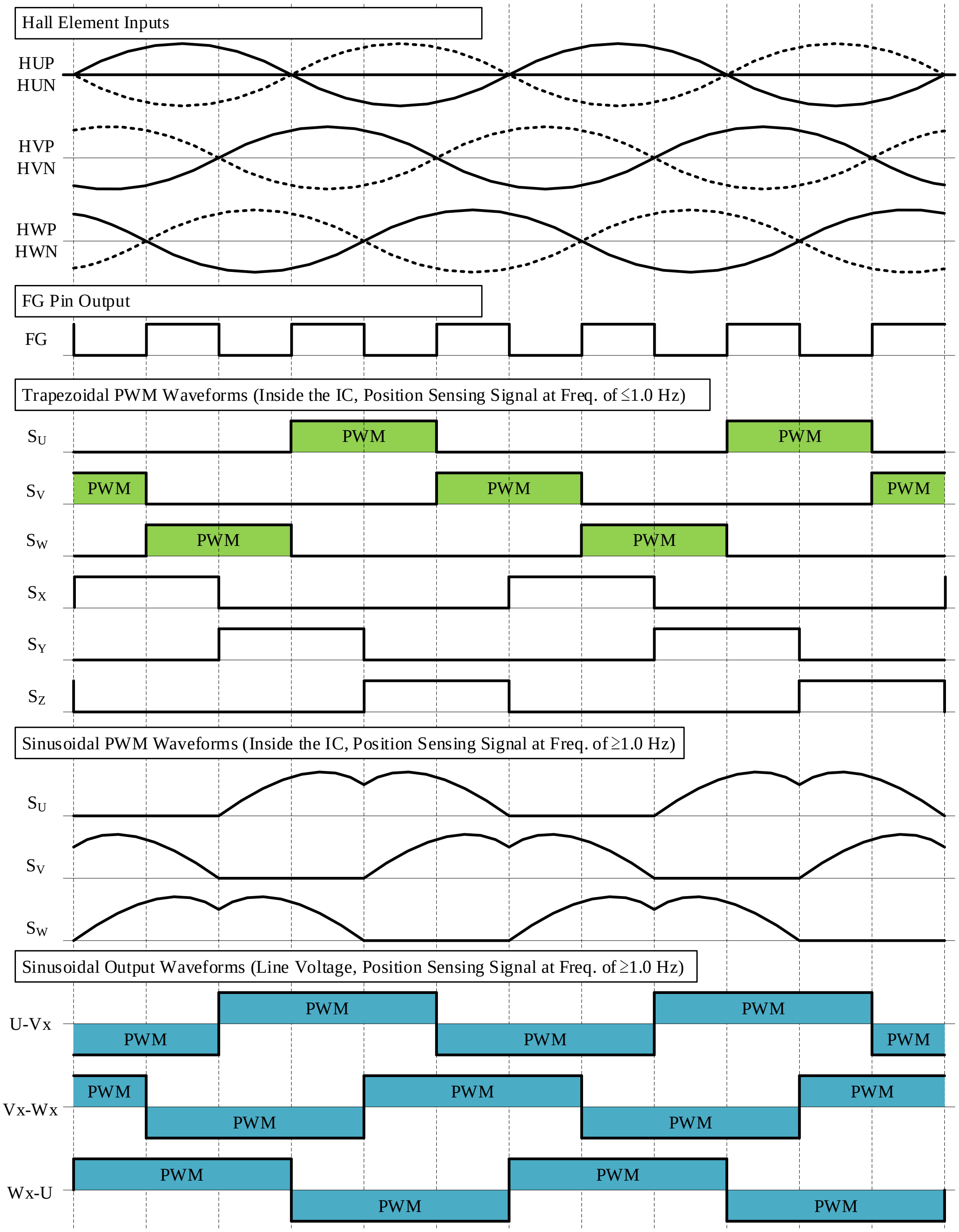


Figure 13-1. Operational Waveforms (Forward, No Phase Advance)

Figure 13-2 shows the operational waveforms of each pin when an 8-pole motor rotates forward (phase advance by 15°) in normal operation.

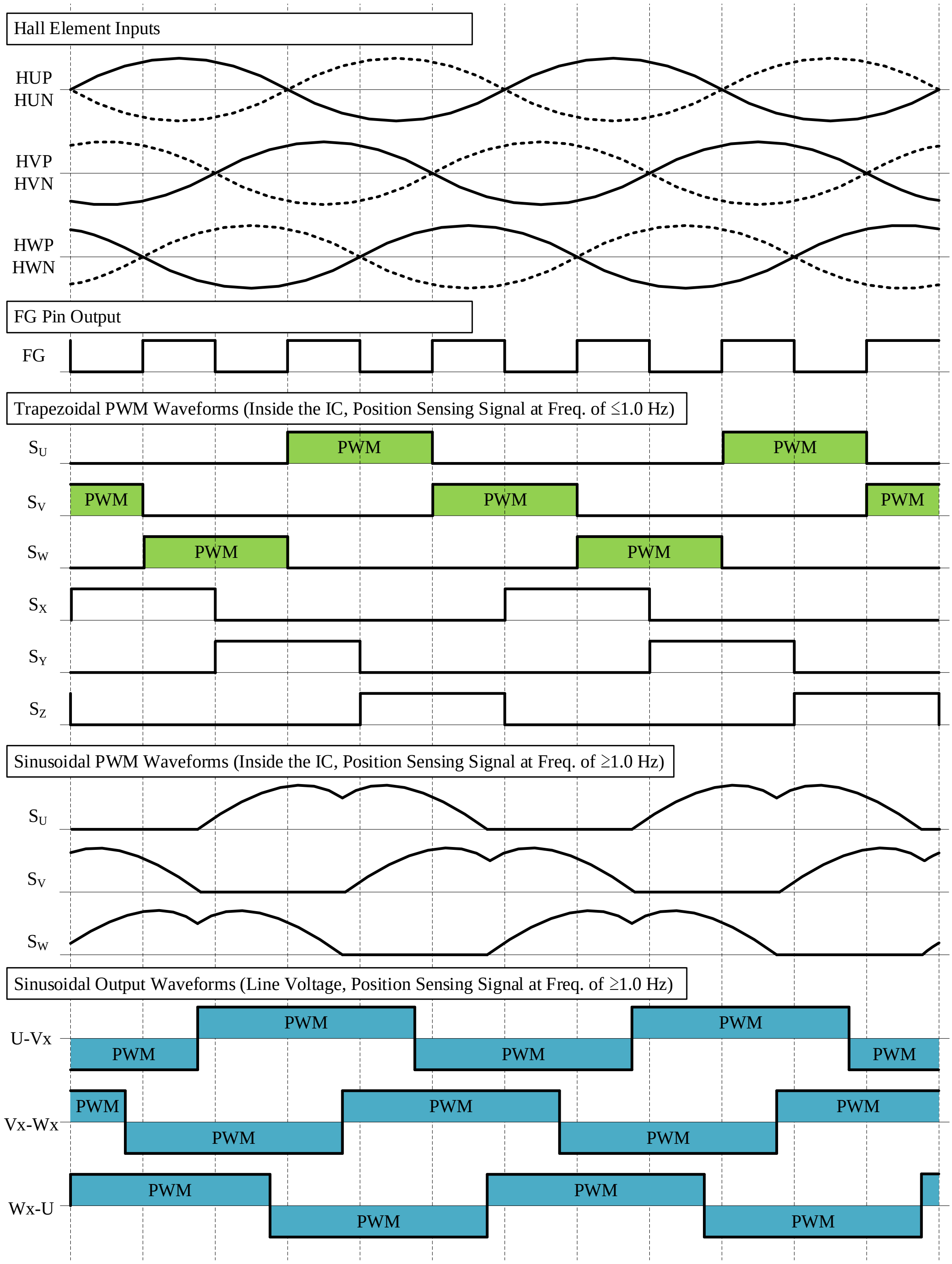


Figure 13-2. Operational Waveforms (Forward, Phase Advance by 15°)

In case the motor rotates in a direction opposite to the preset direction, the reverse rotation detection function starts operating. In the reverse rotation detection, the IC drives the motor with the trapezoidal control.

Figure 13-3 shows the operational waveforms of the motor at forward rotation (CW) when the preset direction is reverse (CCW).

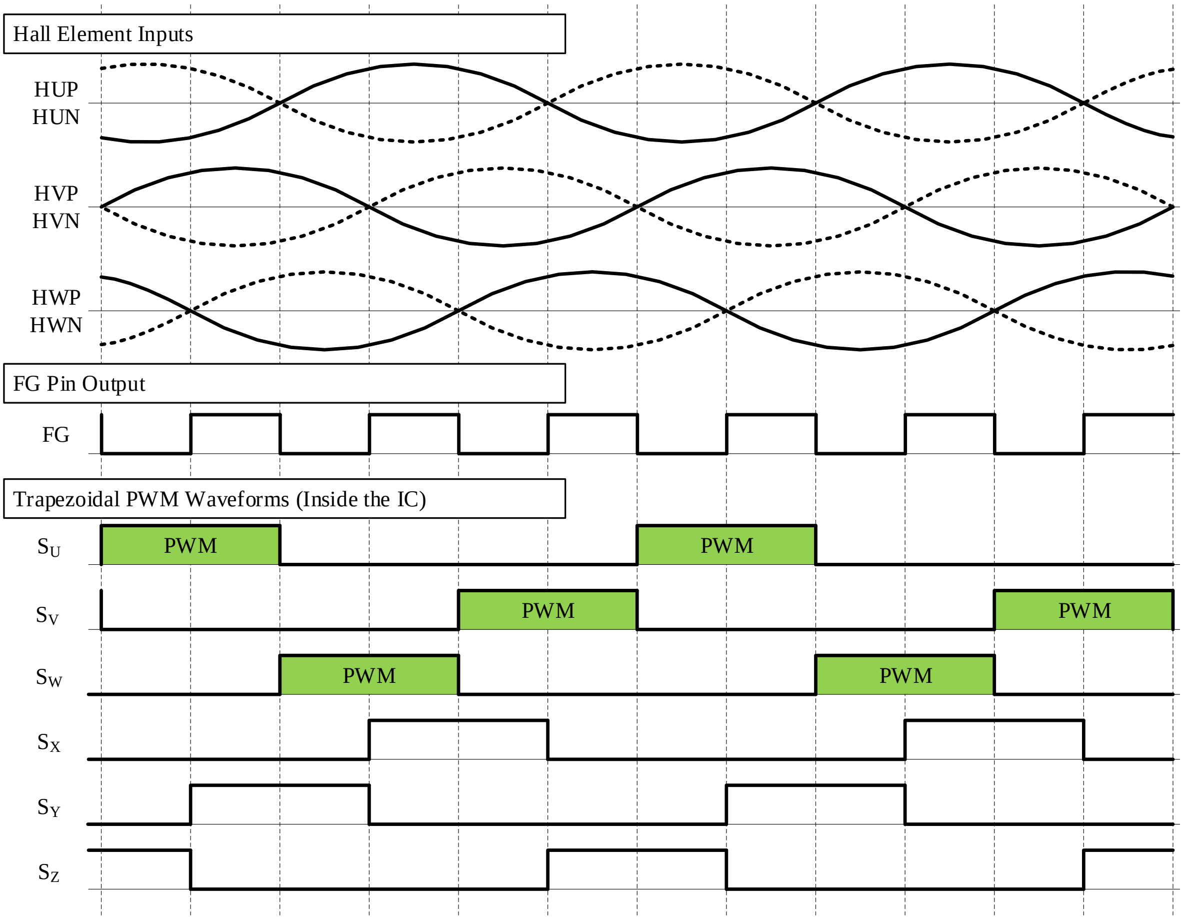


Figure 13-3. Operational Waveforms (in Reverse Rotation Detection)

Figure 13-4 shows the operational waveforms of each pin when an 8-pole motor rotates forward (no phase advance) at startup.

During startup, the IC generates a square-wave signal based on position sensing signals for driving the motor. After startup, the motor driving system is switched from the trapezoidal control to the sinusoidal control when the frequencies of input signals to the Hall elements increase to the predefined value or more. In the reverse rotation detection, the IC drives the motor with the trapezoidal control.

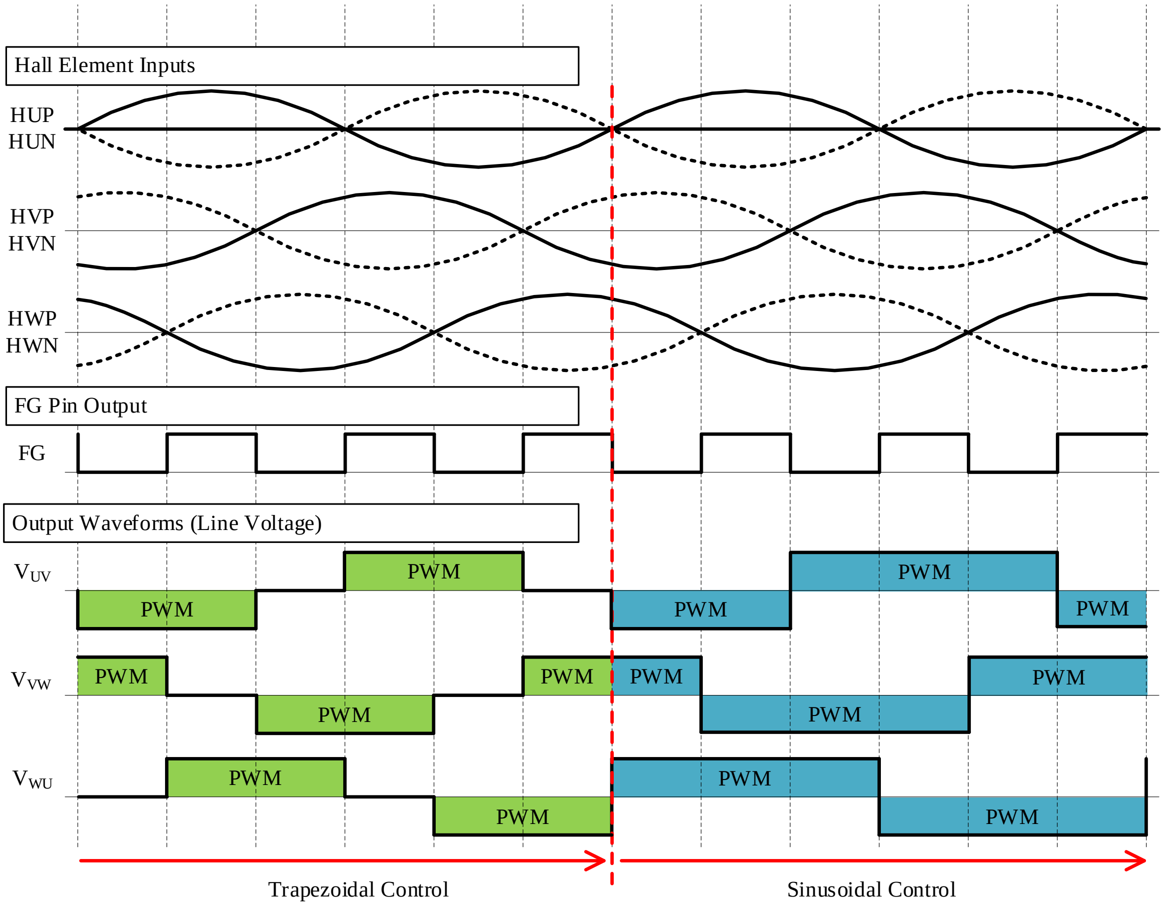


Figure 13-4. Operational Waveforms at Startup

14. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 3 and the electronic symbol names of the typical applications in Section 8. All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.
- All the circuit diagrams listed in this section represent the type of IC that incorporates IGBTs. All the functional descriptions in this section are also applicable to the type of IC that incorporates power MOSFETs.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name or an electronic symbol name with the arbitrary letter "x", representing the certain numbers and letters (1 to 3 and U to W). Thus, "the VBx pin" is used when referring to any or all of the VB1, VB2, and VB3 pins.

14.1 Pin Descriptions

14.1.1 COM1, COM2, and COM3

These are the logic ground pins for the built-in control ICs and are internally connected. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 14-1).

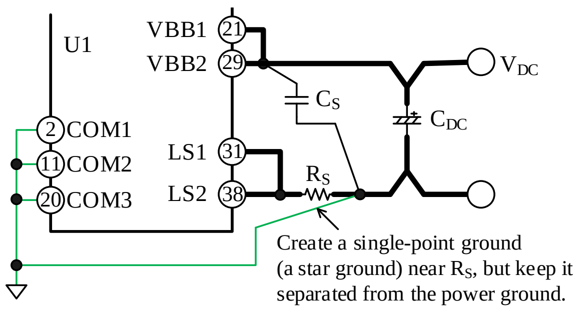


Figure 14-1. Connections to Logic Ground

14.1.2 LA

The IC features the phase advance function. The angle of phase advance is determined by an analog voltage applied to the LA pin. Section 14.5 gives detailed explanations on the LA pin settings and the phase advance function.

14.1.3 IS1

The IS1 pin sets the number of FG output pulses based on the number of motor poles connected and selects which protection recovery mode to enable. The IS1 pin is for changing pin voltages to be applied and setting the pin functions (see Table 12-1).

Table 14-1 shows the relation between the number of pulses of a rotation pulse signal per 360° electrical angle and the IS1 pin voltage. The IC detects the IS1 pin setting information during a startup period (i.e., when the VCC pin voltage is rising).

Table 14-1. Number of Pulses of Rotation Pulse Signal

IS1 Pin Voltage	Number of Signal Pulses
< 1/2 V_{REG}	3 pulses per 360° electrical angle
> 1/2 V_{REG}	1 pulse per 360° electrical angle

14.1.4 IS2

The IS2 pin determines the phase advance control. The IS2 pin is for changing pin voltages to be applied and setting the pin functions (see Table 12-2).

Section 14.5 gives detailed explanations on the phase advance function.

14.1.5 IS3

The IS3 pin selects the motor's rotation direction, enables and disables the motor lock protection, and sets the voltage range of output duty cycle control. The IS3 pin is for changing pin voltages to be applied and setting the pin functions (see Table 12-3).

Table 14-2 shows the relation between the motor direction and the IS3 pin voltage. The IC detects the IS3 pin setting information during a startup period (i.e., when the VCC pin voltage is rising).

Table 14-2. Motor Direction

IS3 Pin Voltage	Motor Direction
< 1/2 V_{REG}	Forward (CW)
> 1/2 V_{REG}	Reverse (CCW)

You can change the motor directions even after the IC startup (i.e., when the VCC pin voltage has risen). To change the motor direction, adjust the IS3 pin voltage under the following conditions:

- V_{SP} < 0.5 V
- Motor frequency < 1.0 Hz

Section 14.6.6 explains more details on the motor lock protection.

14.1.6 OCP

This pin serves as the input of the overcurrent protection (OCP) which monitors the currents flowing through the output transistors. The IC determines which of the overcurrent limit (OCL) and overcurrent protection (OCP) functions to activate according to the level of a voltage applied to the OCP pin. Section 14.6.3 provides further information about the OCP circuit configuration and its mechanism.

14.1.7 VREG

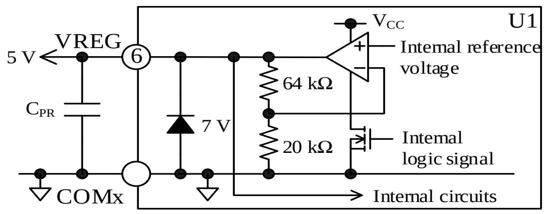


Figure 14-2. Internal Circuit Diagram of VREG Pin

This is the 5.0 V regulator output pin, which can be used for the power supply of the external Hall elements. A maximum output current of the VREG pin is 30 mA. To stabilize the VREG pin output, connect a capacitor, C_{PR}, of about 0.1 µF to the pin. The VREG pin also has the undervoltage lockout. For more details on this function, see Section 14.6.1.

14.1.8 HUP, HVP, and HWN; HUN, HVN, and HWP

These are the input pins for Hall element signals. The HxP pin is connected to the positive node of a Hall element, whereas the HxN pin is connected to the negative node of a Hall element. As Figure 14-3 illustrates, connect a noise filter capacitor, C_{Hx}, with a capacitance of about 0.1 µF, between the HxP and HxN pins. C_{Hx} must be placed near the IC with a minimal length of traces. The IC incorporates the protection circuit that detects abnormal signals from the external Hall elements (see Section 14.6.8).

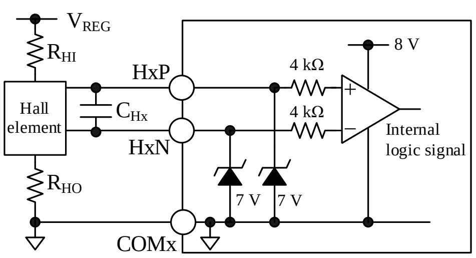


Figure 14-3. Internal Circuit Diagram of HxP and HxN Pins

14.1.9 VSP

The IC controls the speed of motor rotation with an analog voltage applied to the VSP pin. For more details on the motor speed control, see Section 14.4.

14.1.10 FG

The FG pin outputs a rotation pulse signal that is generated based on a position sensing signal. A rotation pulse signal is inverted at each edge of the Hall element signal assigned to the U-, V-, and W-phases. As shown in Figure 14-4, the FG pin is internally pulled down to the COMx pin.

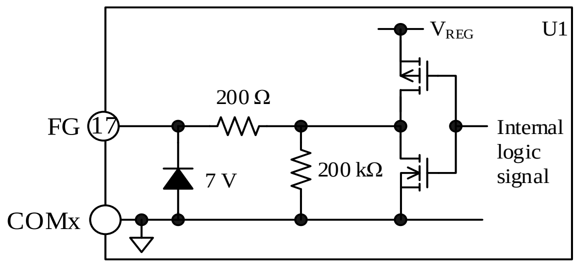


Figure 14-4. Internal Circuit Diagram of FG Pin

Use the IS1 pin to set the number of rotation pulses to be output from the FG pin (see Section 14.1.3).

14.1.11 OVP

The OVP pin serves as the input for the overvoltage protection which monitors voltages across the VBBx and COMx pins.

Section 14.6.4 provides details on the OVP pin peripheral circuit and the OVP operation.

14.1.12 VCC

This is the logic supply pin for the built-in control ICs. The VCC pin has the undervoltage lockout for power supply (see Section 14.6.2.2). To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_P, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCC and COMx pins. Voltages to be applied between the VCC and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

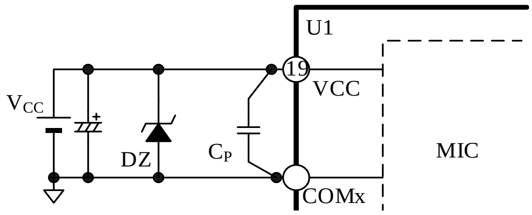


Figure 14-5. VCC Pin and Its Peripheral Circuit

14.1.13 VBB1 and VBB2

These are the input pins for the main supply voltage, i.e., the positive DC bus. All of the high-side collectors are connected to these pins. Voltages between the VBBx and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBBx pin and an electrolytic capacitor, C_{DC}, with a minimum length of PCB trace to the VBBx pin.

14.1.14 VB1, VB2, and VB3

The VB1, VB2, and VB3 pins are connected to bootstrap capacitors, C_{Bx}, for the high-side floating supply. For proper startup, turn on the low-side transistors first, then fully charge the bootstrap capacitors, C_{Bx}. Section 14.2 describes the startup sequences of the IC in detail; Section 14.3 explains the procedures to charge the bootstrap capacitors.

C_{Bx} ,with a capacitance of about 1 µF, must be placed near the IC, and connected between the VBx and output (U, V1, W1) pins with a minimum length of trance. The VBx pin also has the undervoltage lockout for power supply. For more details on this function, see Section 14.6.2.1.

14.1.15 U, V1, V2, W1, and W2

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The V1 and W1 pins must be connected to the V2 and W2 pins on a PCB, respectively. The U, V, and W1 pins are the grounds for the VB1, VB2, and VB3 pins. The U, V1, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{Bx}. Since high voltages are applied to these output pins (U, V1, V2, W1, W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

14.1.16 LS1 and LS2

The LS1 pin is connected to the low-side emitter of the U-phase; the LS2 pin is connected to the low-side emitters of the V- and W-phases. The LSx pin should be connected to an external shunt resistor, R_S, on a PCB. When connecting the shunt resistor, use the resistor with low inductance (required), and place it as near as possible to the IC with a minimum length of traces to the LSx and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

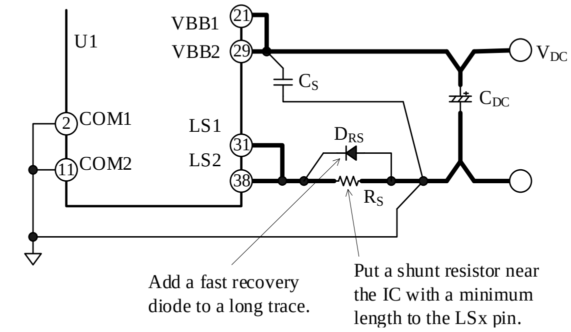


Figure 14-6. Connections to LSx Pin

14.2 Startup Operation

The IC drives the motor with the trapezoidal control at startup.

When the VCC pin voltage reaches $V_{CC(ON)}$ = 11.5 V, the IC starts operating. At this time, the IC detects all information about the IS1 to IS3 pin settings and reflects the information to the motor driving control. The IC identifies a motor rotation state from position sensing signals detected by the HxP and HxN pins. Then, according to the IS1 to IS3 pin settings, the IC generates a sine-wave signal to rotate the motor.

The IC then waits for the VSP pin voltage to reach a certain level at which output duty cycles are controllable. At startup, the IC operates according to the VSP pin voltage levels as follows:

When a voltage range of 2.1 V to 5.4 V for output duty cycle control is set by the IS3 pin:

- **V_{SP} < 1.0 V:**
  All the output signals are off.
- **1.0 V ≤ V_{SP} < 2.1 V:**
  The IC starts charging bootstrap capacitors. For more details, see Section 14.3.
- **2.1 V ≤ V_{SP} ≤ 5.4 V:**
  The IC controls its output duty cycles according to the

VSP pin voltage levels. The IC has a hysteresis for an output duty cycle control start voltage of 2.1 V. To restart the IC, decrease the VSP pin voltage to 1.9 V or less, and then turn on the IC again.

When a voltage range of 0.5 V to 5.4 V for output duty cycle control is set by the IS3 pin:

- **V_{SP} < 0.13 V:**
  All the output signals are off.
- **V_{SP} < 0.5 V:**
  The IC starts charging bootstrap capacitors. For more details, see Section 14.3.
- **2.1 V ≤ V_{SP} ≤ 5.4 V:**
  The IC controls its output duty cycles according to the VSP pin voltage levels. The IC has a hysteresis for an output duty cycle control start voltage of 0.5 V. To restart the IC, decrease the VSP pin voltage to 0.1 V or less, and then turn on the IC again.

Table 11-1 and Table 11-2 are truth tables for the motor driven by the trapezoidal control in a forward or reverse rotation. The following timing charts represent the operational waveforms in different motor operations: the motor in a forward rotation (no phase advance; Figure 13-1), the motor in a forward rotation (phase advance by 15°; Figure 13-2), and the motor during reverse rotation detection (Figure 13-3).

Then the IC detects a state in which the motor rotates inversely to the preset direction, the motor driving system is immediately switched to the trapezoidal control before a rotation of 60° electrical angle completes. For detailed descriptions on the reverse rotation detection, see Section 14.6.7.

The following are the important considerations for appropriate power startup and shutdown sequences.

- To turn on the IC, be sure to increase the VSP pin voltage last. To turn off the IC, be sure to decrease the VSP pin voltage first.
- When you have enabled the motor lock protection by the IS3 pin, be sure to apply a voltage to the VBBx pin at the timing described below. At startup, apply a voltage to the VCC pin and the VREG pin voltage, V_{REG}, increases. Then, apply a main supply voltage to the VBBx pin within the period from V_{REG} increase to an MLP detection time, t_{LD}. When a position sensing signal stays unchanged even after a lapse of t_{LD}, the IC determines this condition as a motor lockup state and activates the motor lock protection (see Section 14.6.6).

14.3 Charging of Bootstrap Capacitors

When setting a voltage range of 0.5 V to 5.4 V for output duty cycle control by the IS3 pin, apply the values in parentheses.

It is required to fully charge bootstrap capacitors, C_{Bx}, at startup. The charging sequence depends on the VSP pin voltage, V_{SP}. When 1.0 V ≤ V_{SP} < 2.1 V (0.13 V ≤ V_{SP} < 0.5 V) at startup, the IC turns on the low-side transistors at every PWM cycle in order to charge C_{Bx}. When V_{SP} ≥ 2.1 V (0.5 V), the IC controls the motor speed according to the VSP pin voltage levels (see Section 14.4). However, note that the IC does not charge C_{Bx} even when 1.0 V ≤ V_{SP} < 2.1 V (0.13 V ≤ V_{SP} < 0.5 V) along with the motor rotating inversely to the preset direction, or the motor coasting at a frequency of ≥1.0 Hz. If a sudden rise in the VSP pin voltage up to 2.1 V (0.5 V) or more occurs at startup, the IC starts the motor speed control after charging C_{Bx} for a period of 9 ms ± 5%.

14.4 Motor Speed Control

The IC controls the speed of motor rotation with an analog voltage applied to the VSP pin. Under the voltage ranges determined by the IS3 pin for output duty cycle control, the IC controls its output duty cycles depending on the VSP pin voltage levels. For the IC operations where the voltage ranges for output duty cycle control are not applicable (i.e., the startup sequence), see Section 14.2.

A duty cycle of an output signal is determined according to a digital signal that is generated by the built-in 7-bit AD converter from the VSP pin input voltage. The higher the VSP pin voltage increases, the higher the duty cycle becomes, thus causing the motor to rotate faster. Figure 14-7 and Figure 14-8 depict how duty cycles vary according to the VSP pin voltage, V_{SP}, respectively. While V_{SP} maintains at 5.4 V or more, the IC controls its output signals at duty cycle = 100%.

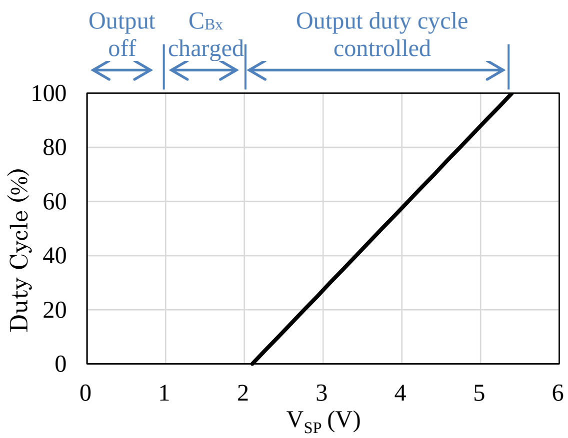


Figure 14-7. VSP Pin Voltage vs. Duty Cycle (Voltage Range: 2.1 V to 5.4 V)

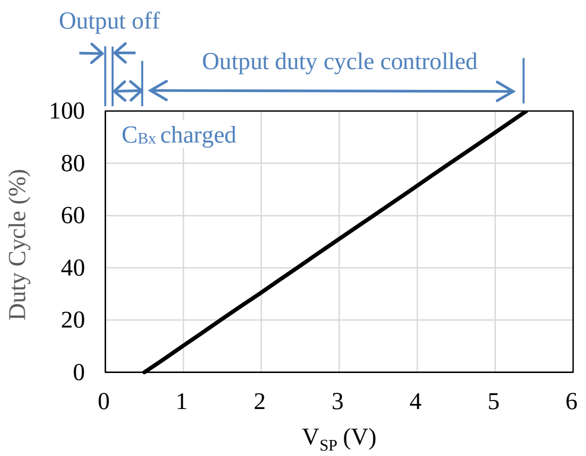


Figure 14-8. VSP Pin Voltage vs. Duty Cycle (Voltage Range: 0.5 V to 5.4 V)

Figure 14-9 is an internal circuit diagram describing the VSP pin and its peripheral circuit. A voltage to be applied on the VSP pin, V_{SPP}, must be set to <10 V, i.e., below the rated VSP pin input voltage. R_{SP} should have a resistance of about 100 Ω; C_{SP} should have a capacitance of about 0.1 μF.

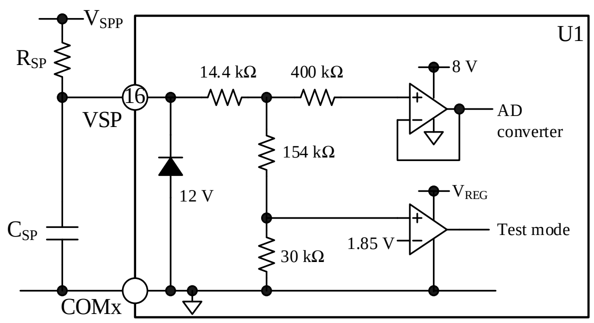


Figure 14-9. Internal Circuit Diagram of VSP Pin and Its Peripheral Circuit

The IC can also operate in test mode. In test mode, the IC disables the phase advance function (with phase advance angle fixed at 0°) and the TSD function. To start IC operations in test mode, turn on the IC after applying a voltage of ≥8.1 V on the VSP pin.

14.5 Phase Advance Function

The IC features the phase advance function. The phase advance function has options allowing motor-appropriate settings: the external phase advance and the internal phase advance (with linear to cubic function operations). Use the IS2 pin to set the phase advance function (see Table 12-2).

14.5.1 External Phase Advance

When the external phase advance is selected, an analog voltage applied to the LA pin determines the phase advance angle. As shown in Figure 14-10, the VREG pin voltage divided by two resistors, R_{LA1} and R_{LA2}, is applied to the LA pin. Figure 14-11 plots how a phase advance angle changes over the LA pin voltage. When the phase advance function is enabled, each phase shifts ±0.46875° every 4 cycles of a Hall signal to the preset angle. The phase advance angle should range from 0° to 58°

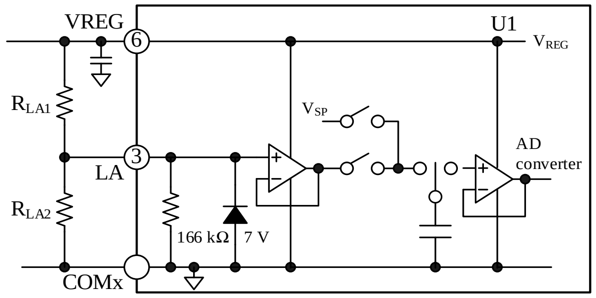


Figure 14-10. Internal Circuit Diagram of LA Pin and Its Peripheral Circuit

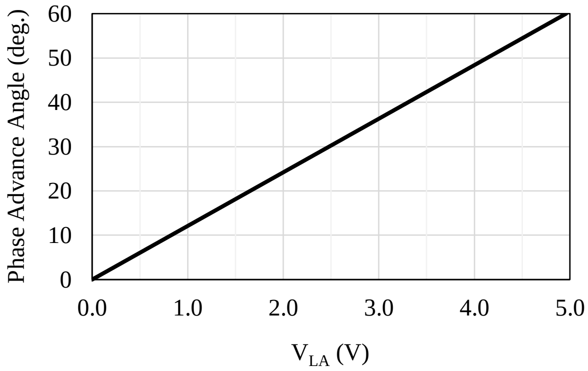


Figure 14-11. LA Pin Voltage vs. Phase Advance Angle

14.5.2 Internal Phase Advance

When the internal phase advance is selected, a phase advance angle is calculated based on the motor rotation speed (i.e., the VSP pin voltage, V_{SP}). The built-in AD converter reads the value of V_{SP} every 50 μs and calculates a value of the phase advance angle in each case. The calculated phase advance angle is stored in the internal register as a target value at the timing of the V_{SP} value reading. The IC then compares an actual phase advance angle with the stored target value every mechanical angle of 360°. And PWM signals shift through 0.9375° until the actual value reaches the target value.

There are three functions available to calculate values for the internal phase advance: linear function, quadratic function, and cubic function. For the linear and quadratic functions, you can select the upper limit of the phase advance angle. Additionally, coefficients applied to these calculations are adjustable with the angle corresponding to the LA pin voltage, LA_{IN}.

Below are the equations applied to individual function operations.

- **Cubic Function Operation**

Note that which equation to apply depends on the value of V_{SP}. The following equations determine the phase advance angle, LA. The phase advance angle should range from 0° to 58°.

When 2.1 V ≤ V_{SP} ≤ 3.75 V:

$$LA = a \times (V_{SP} - 2.1)^2 \quad . \tag{1}$$

When 3.75 V < V_{SP} ≤ 5.4 V:

$$LA = LA_{IN} - a \times \left(3.3 - (V_{SP} - 2.1)\right)^2 \quad . \tag{2}$$

Where:
LA is the phase advance angle (°),
V_{SP} is the VSP pin voltage (V),
LA_{IN} is the angle corresponding to the LA pin voltage (°), and
a is the coefficient (see the equation below).

$$a = \frac{LA_{IN}}{2 \times 1.65^2} . \tag{3}$$

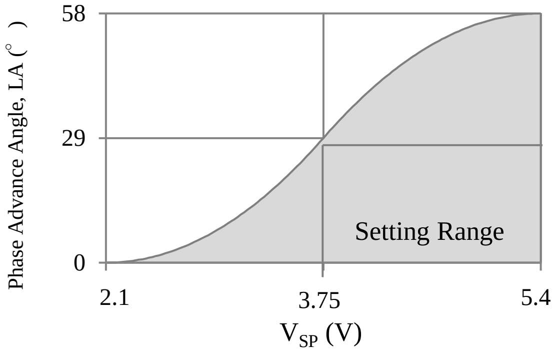


Figure 14-12. Cubic Function Characteristics

- **Quadratic Function Operation**

When 2.1 V ≤ V_{SP} ≤ 5.4 V, the phase advance angle, LA, is calculated by Equation (4):

$$LA = a \times (V_{SP} - 2.1)^2 \quad . \tag{4}$$

Where:
LA is the phase advance angle (°),
V_{SP} is the VSP pin voltage (V), and
a is the coefficient (see the equation below).

$$a = \frac{LA_{IN}}{1.65^2} , \tag{5}$$

letting LA_{IN} be the angle corresponding to the LA pin voltage (°).

When the quadratic function is applied to the internal phase advance, you can select the upper limit of the phase advance angle (29°, 41°, 58°) by setting the IS2 pin. The quadratic function operation uses the soft-clip function that allows the phase advance angle to reach the upper limit selected. Table 14-3 lists the upper limits of the phase advance angles mentioned above and the corresponding phase advance angles at which the soft-clip function starts operating.

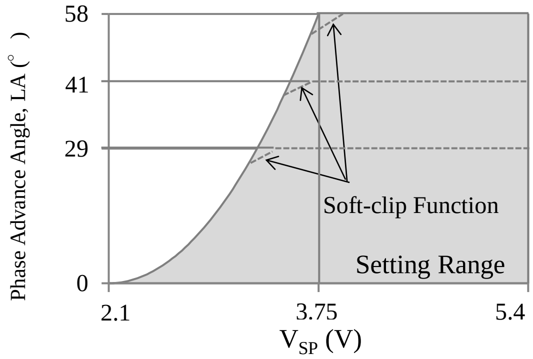


Figure 14-13. Quadratic Function Characteristics

Table 14-3. Soft-clip Function

Upper Limit of Phase Advance Angle	Phase Advance Angle at Which Soft-clip Function Starts
29°	24°
41°	35°
58°	49°

- **Linear Function Operation**

When 2.1 V ≤ V_{SP} ≤ 5.4 V, the phase advance angle, LA, is calculated by Equation (6):

$$LA = a \times (V_{SP} - 2.1) . \tag{6}$$

Where:
LA is the phase advance angle (°),
V_{SP} is the VSP pin voltage (V), and
a is the coefficient (see the equation below).

$$a = \frac{LA_{IN}}{1.65} , \tag{7}$$

letting LA_{IN} be the angle corresponding to the LA pin voltage (°).

When the linear function is applied to the internal phase advance, you can select the upper limit of the phase advance angle (29°, 41°, 58°) by setting the IS2 pin.

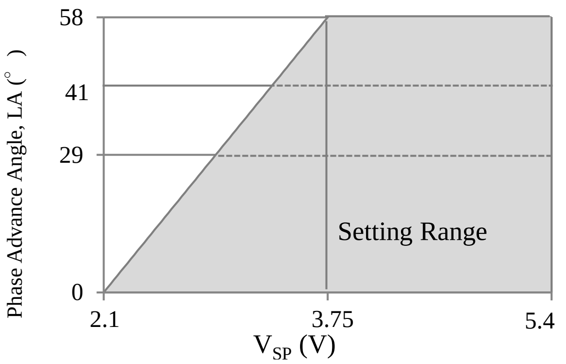


Figure 14-14. Linear Function Characteristics

14.6 Protection Functions

This section describes the various protection circuits provided in the SIM262xM series, such as those designed to detect a voltage drop across power supplies, an overcurrent condition, an abnormal motor state, and so on.

14.6.1 VREG Pin Undervoltage Lockout (UVLO_VREG)

When the VREG pin voltage decreases to V_{UVRL} = 3.60 V or less, the VREG pin undervoltage lockout (UVLO_VREG) circuit gets activated and turns off the high- and low-side transistors. When the VREG pin voltage increases to V_{UVRH} = 4.00 V or more, the IC releases the UVLO_VREG operation. Then, the high- and low-side transistors resume operating according to position sensing signals. During the UVLO_VREG operation, the FG pin does not transmit any rotation pulse signal.

14.6.2 Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SIM262xM series has the undervoltage lockout (UVLO) circuits for each of the high-side (the VBx pin) and the low-side (the VCC pin) power supplies.

14.6.2.1. VBx Pin (UVLO_VB)

When the voltage between the VBx and output (U, V1/V2, or W1/W2) pins (VBx–HSx) decreases to $V_{BS(OFF)}$ = 10.0 V or less, the UVLO_VB circuit gets activated and turns off the high-side transistors. When the voltage between the VBx and output pins increases to $V_{BS(ON)}$ = 10.5 V or more, the IC releases the UVLO_VB operation. Then, the high-side transistors resume operating according to position sensing signals.

Set the voltage between VBx and HSx pins so that VBx > HSx.

14.6.2.2. VCC Pin (UVLO_VCC)

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 11.0 V or less, the UVLO_VCC circuit gets activated and turns off the high- and low-side transistors. When the VCC pin voltage increases to $V_{CC(ON)}$ = 11.5 V or more, the IC releases the UVLO_VCC operation. Then, the high- and low-side transistors resume operating according to position sensing signals.

14.6.3 Overcurrent Limit (OCL) and Overcurrent Protection (OCP)

The IC has two different protections against overcurrent conditions: the overcurrent limit (OCL) and the overcurrent protection (OCP). Figure 14-15 is an internal circuit diagram describing the OCP pin and its peripheral circuit. The OCP pin detects overcurrents with voltage across an external shunt resistor, R_S. Because the OCP pin is internally pulled up, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S. When the shunt resistor, R_S, is open, the IC activates the OCP function.

Note that overcurrents are undetectable when one or more of the U, V1/V2, and W1/W2 pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

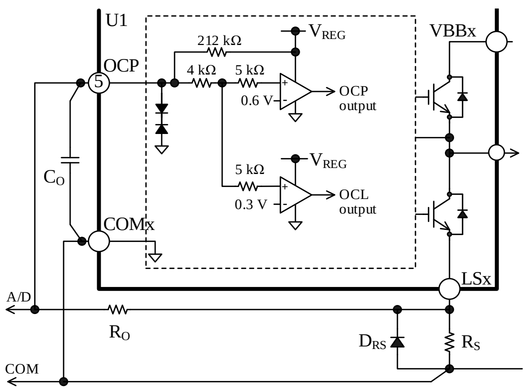


Figure 14-15. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

The overcurrent limit (OCL) is a protection against relatively low overcurrent conditions. When the OCP pin voltage increases to V_{LIM} = 0.30 V or more, and remains in this condition for a period of a blanking time ($t_{BK(OCL)}$ = 2.6 μs) or longer, the IC turns off the high- and low-side transistors. The OCL operation is automatically released at each PWM cycle.

The overcurrent protection (OCP) is a protection against large inrush currents. When the OCP pin voltage increases to V_{TRIP} = 0.60 V or more, and remains in this condition for a period of a blanking time ($t_{BK(OCP)}$ = 0.8 μs) or longer, the OCP circuit is activated. Then, the high- and low-side transistors are turned off for a certain period of time (t_P = 15 ms). After that, the high- and low-side transistors resume operating according to position sensing signals. During the OCP operation, the FG pin does not send any rotation pulse signal.

The OCL and OCP are used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. For this reason, motor operations must be controlled by the external microcontroller so that it can immediately stop the motor upon OCP detection. If you need to resume the IC operation thereafter, set the IC to be resumed after a lapse of ≥2 seconds.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Set the OCP pin input voltage to vary within the rated input voltages, $V_{IN(1)}$ (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

14.6.4 Overvoltage Protection (OVP)

Figure 14-16 is an internal circuit diagram describing the OVP pin and its peripheral circuit.

The VBBx pin voltage split by a resistive voltage divider, R_{OVP1} and R_{OVP2}, is applied to the OVP pin.

The higher the VBBx pin voltage, the higher the OVP pin voltage. When the OVP pin voltage increases to the OVP Operating Voltage, V_{OVPH} = 2.50 V or more, the OVP circuit is activated. The enabled OVP circuit turns off the high- and low-side output transistors. After that, when the OVP pin voltage decreases to the OVP Releasing Voltage, V_{OVPL} = 2.30 V or less, the IC releases the OVP operation. When not using the OVP, short the OVP and COMx pins.

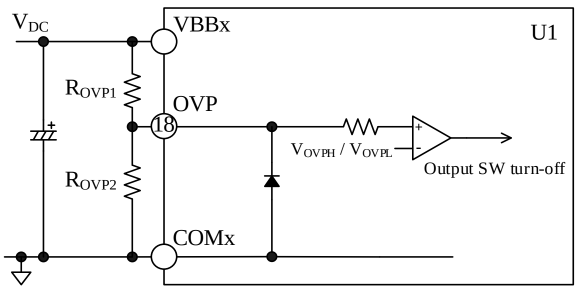


Figure 14-16. Internal Circuit Diagram of OVP Pin and Its Peripheral Circuit

14.6.5 Thermal Shutdown (TSD)

The SIM262xM series incorporates the thermal shutdown (TSD) circuit. In case of overheating (e.g., increased power dissipation due to overload, or elevated ambient temperature at the device), the IC shuts down the high- and low-side transistors.

The TSD circuit in the MIC for gate driver monitors temperatures (see Figure 6-1). When the junction temperature of the MIC for gate driver, $T_{J(DRV)}$, exceeds T_{DH} = 130 °C, the TSD circuit is activated. When $T_{J(DRV)}$ decreases to $T_{DH} - T_{D(HYS)}$ after the TSD activation, the shutdown condition is released. The output transistors then resume operating according to input signals. During the TSD operation, the FG pin does not transmit any rotation pulse signal.

Note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

14.6.6 Motor Lock Protection (MLP)

The IC determines to enable or disable the motor lock protection based on the IS3 pin settings (see Table 12-3). The IC detects the IS3 pin setting information during a startup period (i.e., when the VCC pin voltage is rising).

When the state in which a position sensing signal stays unchanged within a rotation of 60° electrical angle persists for a motor lock hold time (t_{LD} = 5 s) or longer, the motor lock protection (MLP) circuit gets activated. Then, the high- and low-side transistors stop operating for a certain period of time.

After that, the high- and low-side transistors resume operating according to position sensing signals. When the state in which a position sensing signal stays unchanged within a rotation of 60° electrical angle still persists at this time, the high- and low-side transistors repeat operating and stopping (MLP operations), as shown in Figure 14-17.

When the protection recovery mode is set to manual by the IS1 pin settings (see Table 12-1), the high- and low-side transistors remain stopped after the 10th MLP operation. When the protection recovery mode is set to automatic by the IS1 pin settings, the high- and low-side transistors repeat operating and stopping (MLP operations).

To release the MLP operation, set the VSP pin voltage according to the voltage range of output duty cycle control: ≤1.0 V (voltage range: 2.1 V to 5.4 V); ≤0.13 V (voltage range: 0.5 V to 5.4 V).

During the MLP operation, the FG pin does not transmit any rotation pulse signal. Moreover, direct currents through the output transistors cause an increase in the junction temperatures of the output transistors. Therefore, care must be taken not to allow the junction temperatures to exceed the absolute maximum rating.

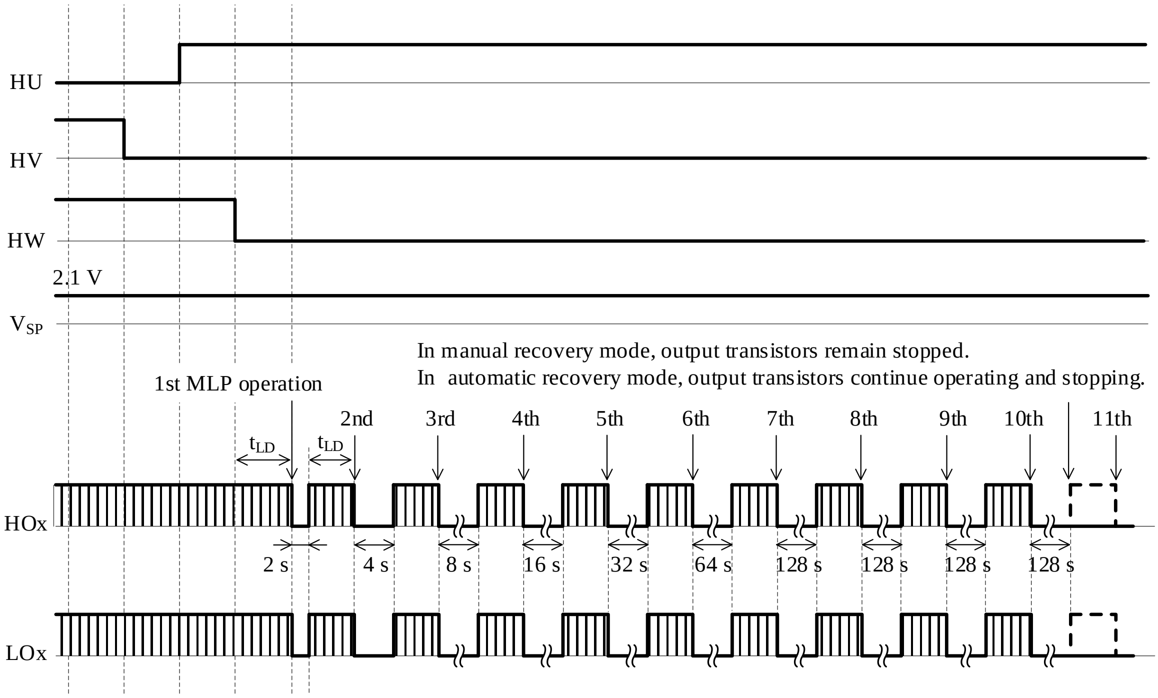


Figure 14-17. MLP Operational Waveforms

14.6.7 Reverse Rotation Detection

In case the motor actually rotates in a direction opposite to the preset direction, the reverse rotation detection function starts operating. When the IC detects that the motor rotation agrees with the preset direction, the motor driving system is immediately switched to the trapezoidal control before a rotation of 60° electrical angle completes. For the operational waveforms of each pin during the MLP operation, see Figure 13-3.

14.6.8 Hall Signal Abnormality Detection

As Figure 14-18 shows, signals from the external Hall elements are input into the corresponding comparators. The IC then receives the comparator outputs as the motor positional information, i.e., position sensing signals (HU, HV, HW). When the position sensing signals are in any of the following state, the Hall signal abnormality detection function gets activated and turns off the high- and low-side transistors. While the function is being enabled, the FG pin does not send any rotation pulse signal.

- When all the position sensing signals are in a high state
- When all the position sensing signals are in a low state
- When one cycle of the electrical angle of the position sensing signals is 700 Hz or more

When the IC detects input states other than those above, each of the high- and low-side transistors responds in accordance with the input logic levels of the position sensing signals. For the truth tables for the position sensing signals and the output transistors, see Table 11-1 and Table 11-2.

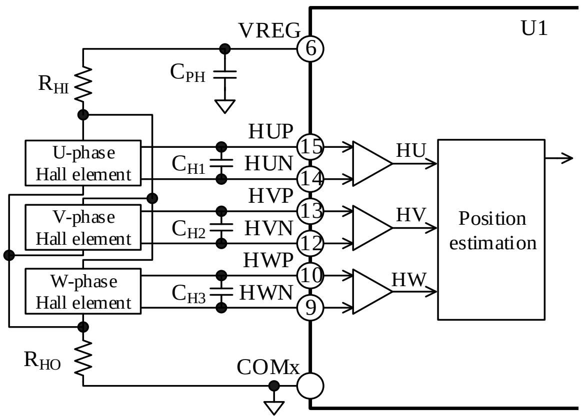


Figure 14-18. Internal Circuit Diagram of HxP and HxN Pins and Their Peripheral Circuit

15. Design Notes

15.1 PCB Pattern Layout

Figure 15-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

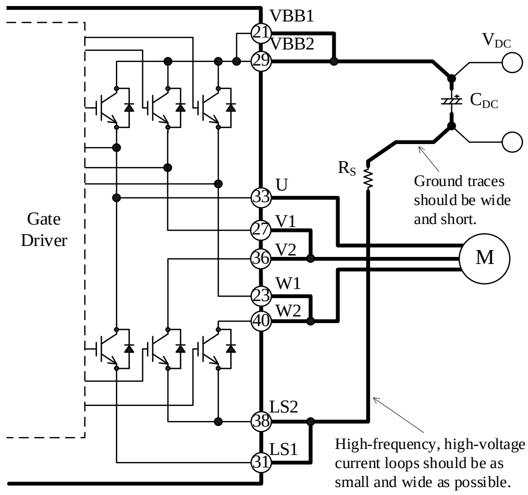


Figure 15-1. High-frequency, High-voltage Current Paths

15.2 Considerations in IC Characteristics Measurement

When measuring the leakage current of the output transistors incorporated in the IC, note that all of the output (U, V1, V2, W1, W2), VCC, LSx, and COMx pins must be appropriately connected. Otherwise, the output transistors may result in permanent damage. Also note that the gate and emitter of each output transistor should have the same potential during the leakage current measurement. Moreover, care should be taken during the measurement because each output transistor is connected as follows:

- All the high-side collectors are internally connected to the VBBx pin.
- In the U-phase, the high-side emitter and the low-side collector are internally connected to the U pin. (In the V- and W-phases, the high- and low-side transistors are unconnected inside the IC.)

- In the U-phase, the low-side emitters are internally connected to the LS1 pin.
- In the V- and W-phases, the low-side emitters are internally connected to the LS2 pin.
- The high-side gates are internally pulled down to the output pins.
- The low-side gates are internally pulled down to the COMx pin.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 15-2 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 15-3 shows the low-side transistor (Q_{1L}) in the U-phase. And all the pins that are not represented in these figures are open. When measuring the high-side transistors, leave all the non-measuring pins open. When measuring the low-side transistors, apply a voltage of 15 V between the VCC and COMx pins, connect only the measuring LSx pin to the COMx pin, and leave the other pins open.

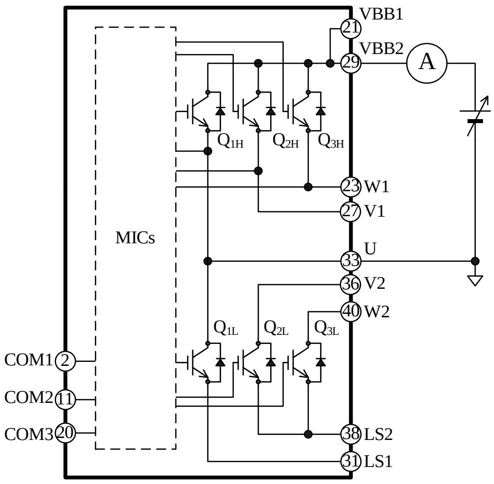


Figure 15-2. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

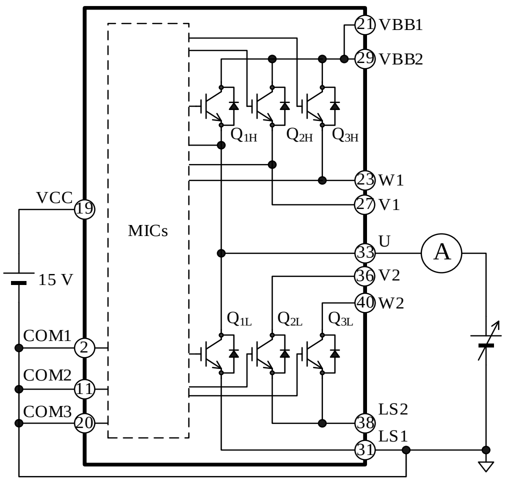


Figure 15-3. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

15.3 Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- A pair of a metric screw of M2.5 and a plain washer of 6.0 mm (φ) must be used. When tightening the screws, use a torque screwdriver and tighten them within the range of screw torque defined in Section 4. Be sure to avoid uneven tightening. Temporarily tighten the two screws first, then tighten them equally on both sides until the specified screw torque is reached.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  - Grease thickness: 100 µm
  - Heatsink flatness: ±100 µm
  - Apply a silicone grease within the area indicated in Figure 15-4, below.

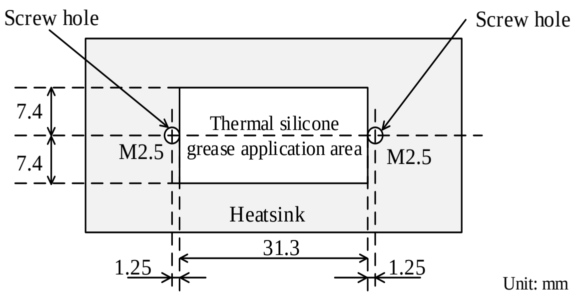


Figure 15-4. Reference Application Area for Thermal Silicone Grease

16. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in an output transistor, and to estimate a junction temperature (in all-element operation). Note that the descriptions listed here are applicable to the SIM262xM series, which is controlled by a 3-phase sine-wave PWM driving strategy.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0050: SIM2621M Calculation Tool
  https://www.semicon.sanken-ele.co.jp/en/calc-tool/mosfet_caltool_en.html

- DT0107: SIM2622M Calculation Tool
  https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbtall_caltool2_en.html

16.1 Power MOSFET

Total power loss in a power MOSFET can be obtained by taking the sum of the following losses: steady-state loss, P_{RON}; switching loss, P_{SW}; the steady-state loss of a body diode, P_{SD}. In the calculation procedure we offer, the recovery loss of a body diode, P_{RR}, is considered negligibly small compared with the ratios of other losses.

The following subsections contain the mathematical procedures to calculate these losses (P_{RON}, P_{SW}, and P_{SD}) and the junction temperature of all power MOSFETs operating.

16.1.1 Power MOSFET Steady-state Loss, P_{RON}

Steady-state loss in a power MOSFET can be computed by using the $R_{DS(ON)}$ vs. I_D curves, listed in Section 17.3.1. As expressed by the curves in Figure 16-1, a linear approximation at a range the I_D is actually used is obtained by: $R_{DS(ON)} = \alpha \times I_D + \beta$. The values gained by the above calculation are then applied as parameters in Equation (8), below. Hence, the equation to obtain the power MOSFET steady-state loss, P_{RON}, is:

$$P_{RON} = \frac{1}{2\pi}\int_0^{\pi} I_D\,(\varphi)^2 \times R_{DS(ON)}(\varphi) \times DT \times d\varphi$$

$$= 2\sqrt{2}\alpha\left(\frac{1}{3\pi} + \frac{3}{32}M \times \cos\theta\right) I_M{}^3 + 2\beta\left(\frac{1}{8} + \frac{1}{3\pi}M \times \cos\theta\right) I_M{}^2 . \qquad (8)$$

Where:

I_D is the drain current of the power MOSFET (A),

$R_{DS(ON)}$ is the drain-to-source on-resistance of the power MOSFET (Ω),

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current (A),

α is the slope of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve, and

β is the intercept of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve.

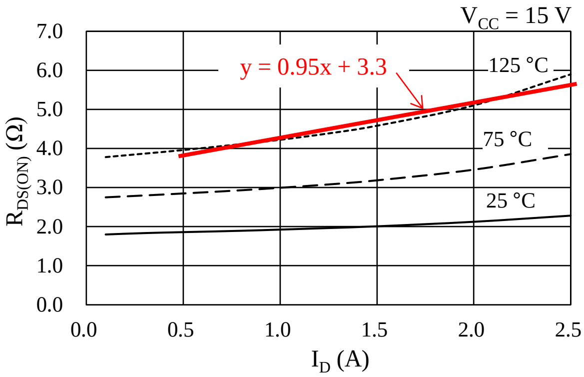


Figure 16-1. Linear Approximate Equation of $R_{DS(ON)}$ vs. I_D

16.1.2 Power MOSFET Switching Loss, P_{SW}

Switching loss in a power MOSFET can be calculated by Equation (9), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \qquad (9)$$

Where:

f_C is the PWM carrier frequency (Hz),

V_{DC} is the main power supply voltage (V), i.e., the VBBx pin input voltage, and

α_E is the slope on the switching loss curve (see Section 17.3.2.1).

16.1.3 Body Diode Steady-state Loss, P_{SD}

Steady-state loss in the body diode of a power MOSFET can be computed by using the V_{SD} vs. I_{SD} curves, listed in Section 17.3.1. As expressed by the curves in Figure 16-2, a linear approximation at a range the I_{SD} is actually used is obtained by: $V_{SD} = \alpha \times I_{SD} + \beta$. The values gained by the above calculation are then applied as parameters in Equation (10), below. Hence, the equation to obtain the body diode steady-state loss, P_{SD}, is:

$$P_{SD} = \frac{1}{2\pi}\int_0^{\pi} V_{SD}(\varphi) \times I_{SD}(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right) I_M{}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right) I_M . \qquad (10)$$

Where:

V_{SD} is the source-to-drain diode forward voltage of the power MOSFET (V),
I_{SD} is the source-to-drain diode forward current of the power MOSFET (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the V_{SD} vs. I_{SD} curve, and
β is the intercept of the linear approximation in the V_{SD} vs. I_{SD} curve.

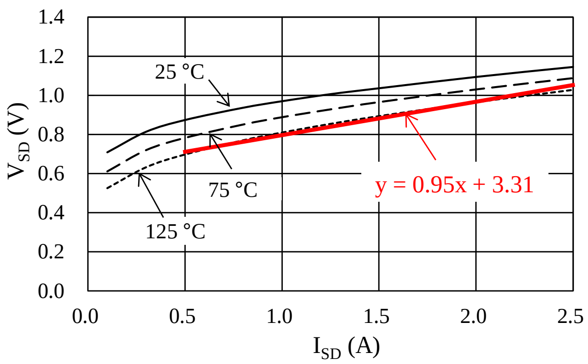


Figure 16-2. Linear Approximate Equation of V_{SD} vs. I_{SD}

16.1.4 Estimating Junction Temperature of Power MOSFET

The junction temperature of all power MOSFETs operating, T_J, can be estimated with Equation (11):

$$T_J = R_{J-C} \times \{(P_{ON} + P_{SW} + P_{SD}) \times 6\} + T_C . \qquad (11)$$

Where:

R_{J-C} is the junction-to-case thermal resistance (°C/W) of all the power MOSFETs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-2.

16.2 IGBT

Total power loss in an output transistor can be obtained by taking the sum of IGBT steady-state loss, P_{ON}, IGBT switching loss, P_{SW}, and freewheeling diode steady-state loss, P_F. The following subsections contain the mathematical procedures to calculate these losses (P_{ON}, P_{SW}, and P_F) and the junction temperature of all IGBTs and freewheeling diodes operating.

16.2.1 IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, listed in Section 17.3.1. As expressed by the curves in Figure 16-3, linear approximations at a range the I_C is actually used are obtained by: $V_{CE(SAT)} = \alpha \times I_C + \beta$. The values gained by the above calculation are then applied as parameters in Equation (12), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} + \frac{4}{3\pi}M \times \cos\theta\right) I_M{}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} + \frac{\pi}{8}M \times \cos\theta\right) I_M . \qquad (12)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT (V),
I_C is the collector current of the IGBT (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve, and
β is the intercept of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve.

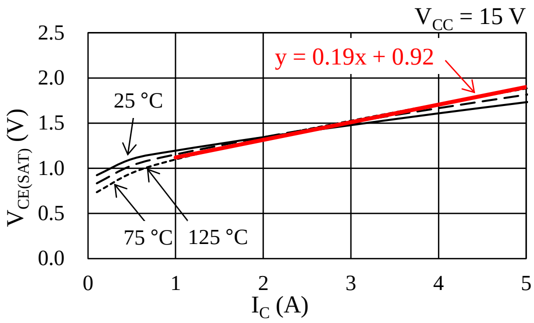


Figure 16-3. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C

16.2.2 IGBT Switching Loss, P_{SW}

Switching loss in an IGBT, P_{SW}, can be calculated by Equation (13), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300} . \tag{13}$$

Where:

f_C is the PWM carrier frequency (Hz),

V_{DC} is the main power supply voltage (V), i.e., the VBBx pin input voltage, and

α_E is the slope on the switching loss curve (see Section 17.3.2.2).

16.2.3 Estimating Junction Temperature of IGBT

The junction temperature of all IGBTs operating, T_J, can be estimated with Equation (14):

$$T_J = R_{(J-C)Q} \times \{(P_{ON} + P_{SW}) \times 6\} + T_C . \tag{14}$$

Where:

$R_{(J-C)Q}$ is the junction-to-case thermal resistance (°C/W) of all the IGBTs operating, and

T_C is the case temperature (°C), measured at the point defined in Figure 3-2.

16.2.4 Freewheeling Diode Steady-state Loss, P_F

Steady-state loss in a freewheeling diode can be computed by using the V_F vs. I_F curves, listed in Section 17.3.1. As expressed by the curves in Figure 16-4, a linear approximation at a range the I_F is actually used is obtained by: $V_F = \alpha \times I_F + \beta$.

The values gained by the above calculation are then applied as parameters in Equation (15), below. Hence, the equation to obtain the freewheeling diode steady-state loss, P_F, is:

$$P_F = \frac{1}{2\pi}\int_0^{\pi} V_F(\varphi) \times I_F(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right) I_M{}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right) I_M . \tag{15}$$

Where:

V_F is the forward voltage of the freewheeling diode (V),

I_F is the forward current of the freewheeling diode (A),

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2} ,$$

M is the modulation index (0 to 1),

$\cos\theta$ is the motor power factor (0 to 1),

I_M is the effective motor current (A),

α is the slope of the linear approximation in the V_F vs. I_F curve, and

β is the intercept of the linear approximation in the V_F vs. I_F curve.

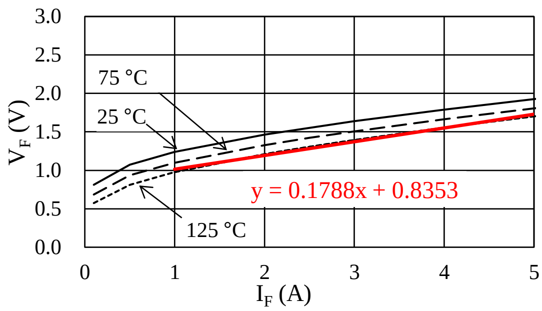


Figure 16-4. Linear Approximate Equation of V_F vs. I_F

16.2.5 Estimating Junction Temperature of Freewheeling Diode

The junction temperature of all freewheeling diodes operating, T_J, can be estimated with Equation (16):

$$T_J = R_{(J-C)F} \times (P_F \times 6) + T_C . \tag{16}$$

Where:

$R_{(J-C)F}$ is the junction-to-case thermal resistance (°C/W) of all the freewheeling diodes operating, and

T_C is the case temperature (°C), measured at the point defined in Figure 3-2.

17. Performance Curves

17.1 Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state junction-to-case thermal resistance = 1. Note that the graph representing that of the IGBT-embedded device shows only IGBT characteristics; no freewheeling diode characteristics are included.

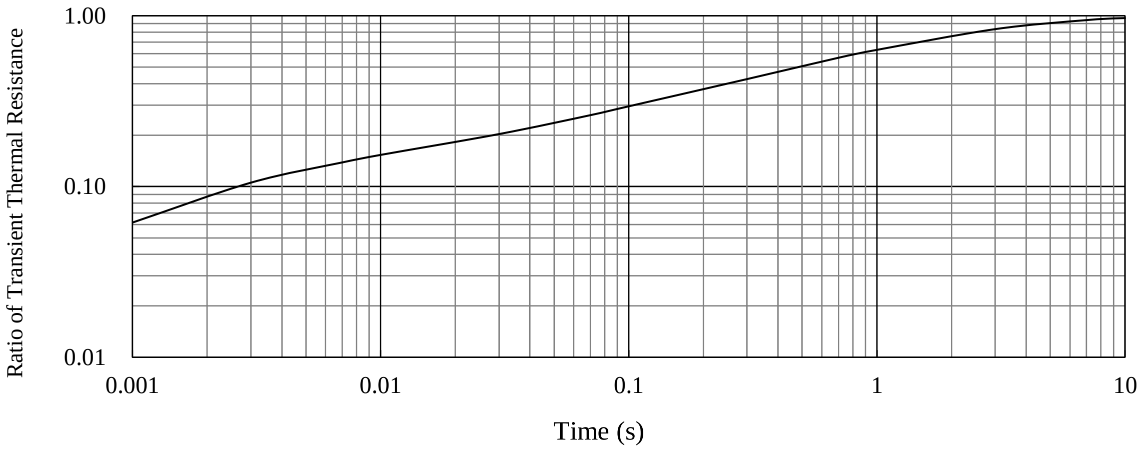


Figure 17-1. Transient Thermal Resistance: SIM2621M

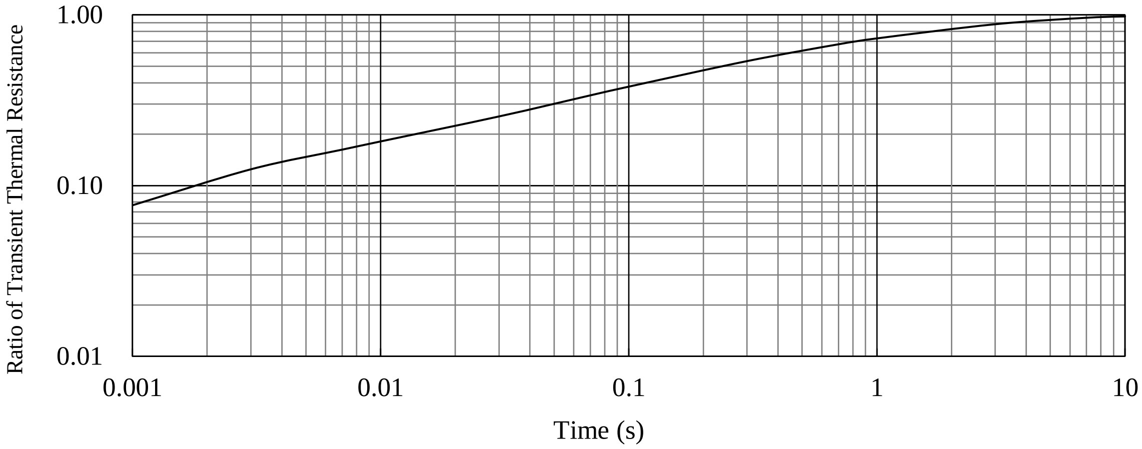


Figure 17-2. Transient Thermal Resistance: SIM2622M

17.2 Performance Curves of Control Parts

Figure 17-3 to Figure 17-19 provide performance curves of the control parts integrated in the SIM262xM series, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 17-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 17-3	Logic Supply Current, I_{CC} vs. T_C
Figure 17-4	Logic Supply Current, I_{CC} vs. VCC Pin Voltage, V_{CC}
Figure 17-5	Logic Supply Current in 1-phase Operation (V_{SP} = 0 V), I_{BS} vs. T_C
Figure 17-6	Logic Supply Current in 1-phase Operation (V_{SP} = 5.5 V), I_{BS} vs. T_C
Figure 17-7	High-side Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 17-8	High-side Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 17-9	Low-side Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 17-10	Low-side Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 17-11	UVLO_VB Filtering Time vs. T_C
Figure 17-12	UVLO_VCC Filtering Time vs. T_C
Figure 17-13	High Level Input Current 1 (LA, IS1, IS2, IS3, OVP, or VSP Pin), I_{IN1} vs. T_C
Figure 17-14	High Level Input Current 2 (OCP Pin), I_{IN2} vs. T_C
Figure 17-15	VREG Pin Voltage, V_{REG} vs. T_C
Figure 17-16	Current Limit Reference Voltage, V_{LIM} vs. T_C
Figure 17-17	OCL Blanking Time, $t_{BK(OCL)}$ + Propagation Delay, t_D vs. T_C
Figure 17-18	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 17-19	OCP Hold Time, t_P vs. T_C

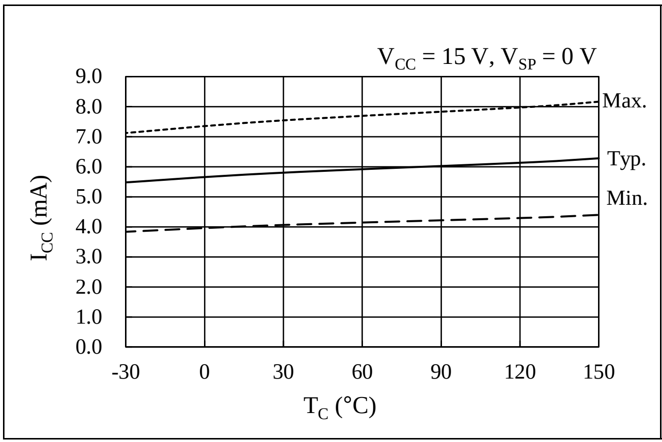


Figure 17-3. Logic Supply Current, I_{CC} vs. T_C

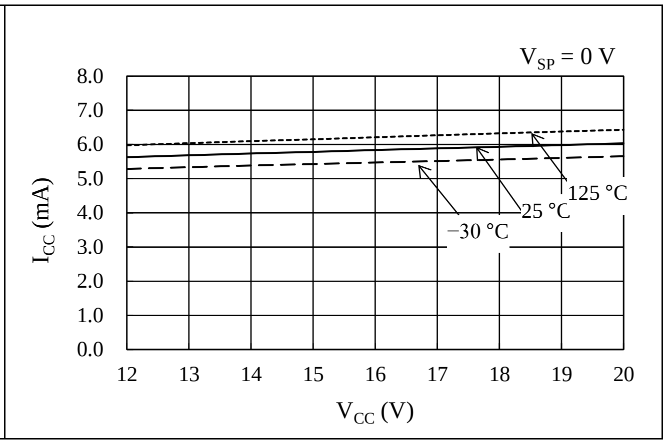


Figure 17-4. Logic Supply Current, I_{CC} vs. VCC Pin Voltage, V_{CC}

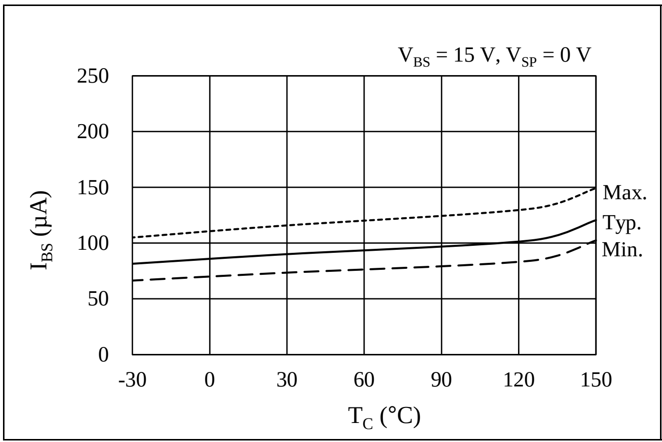


Figure 17-5. Logic Supply Current in 1-phase Operation (V_{SP} = 0 V), I_{BS} vs. T_C

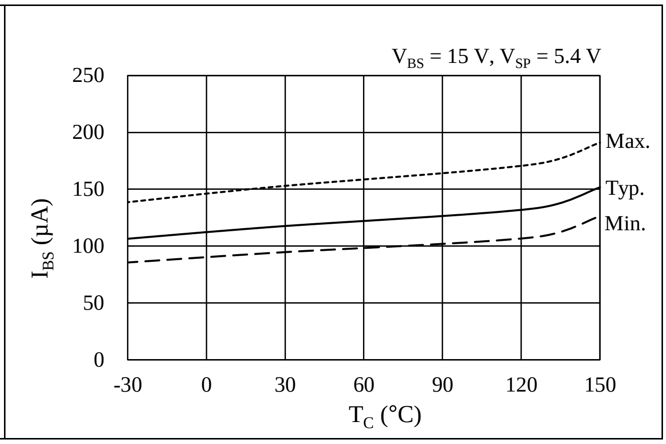


Figure 17-6. Logic Supply Current in 1-phase Operation (VSP = 5.5 V), I_{BS} vs. T_C

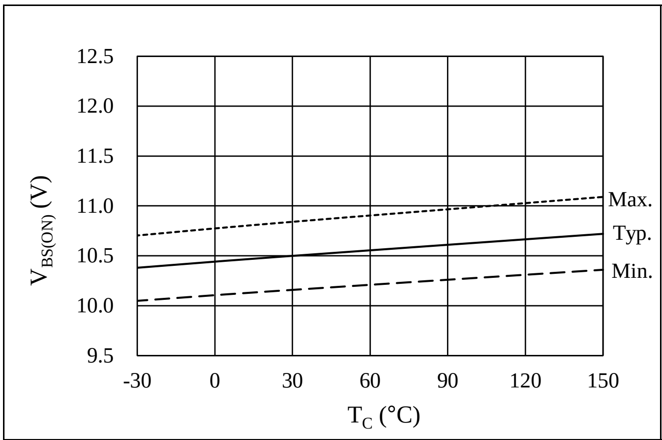


Figure 17-7. High-side Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

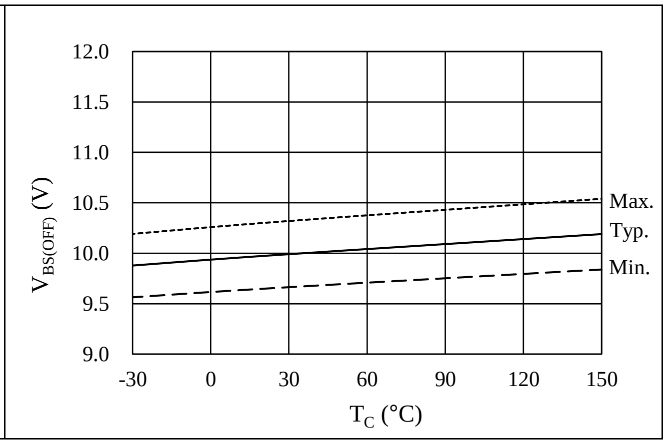


Figure 17-8. High-side Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

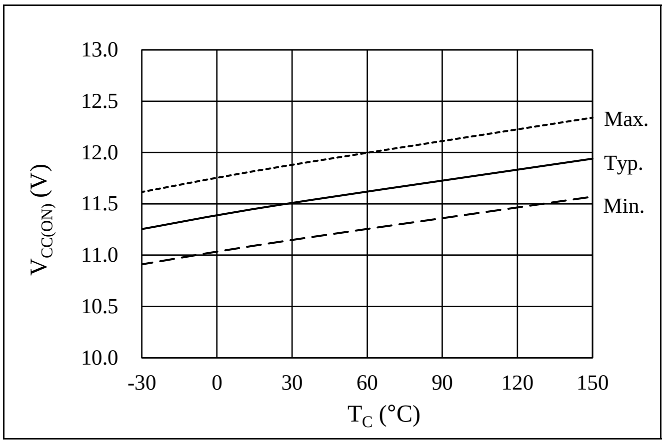


Figure 17-9. Low-side Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

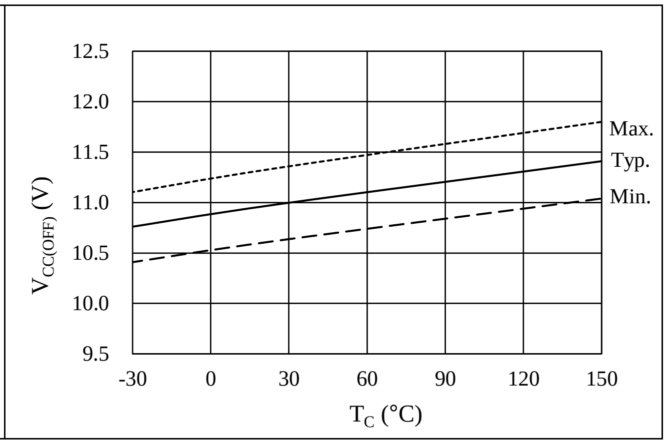


Figure 17-10. Low-side Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

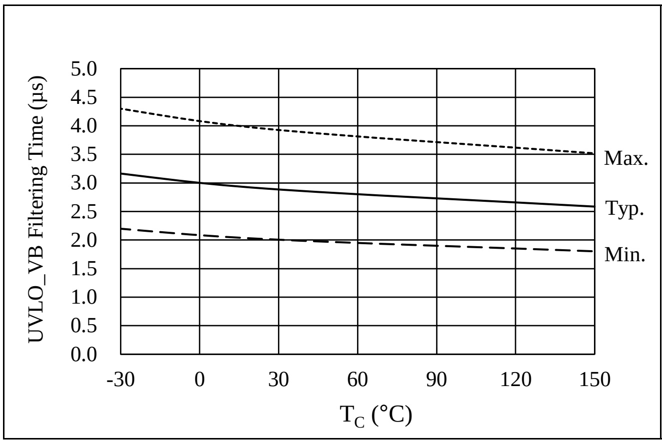


Figure 17-11. UVLO_VB Filtering Time vs. T_C

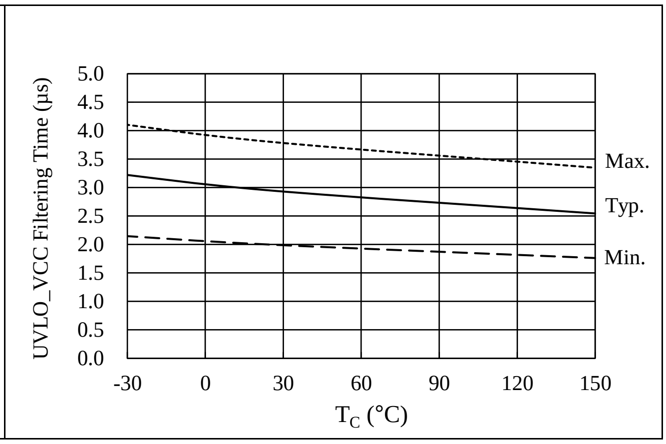


Figure 17-12. UVLO_VCC Filtering Time vs. T_C

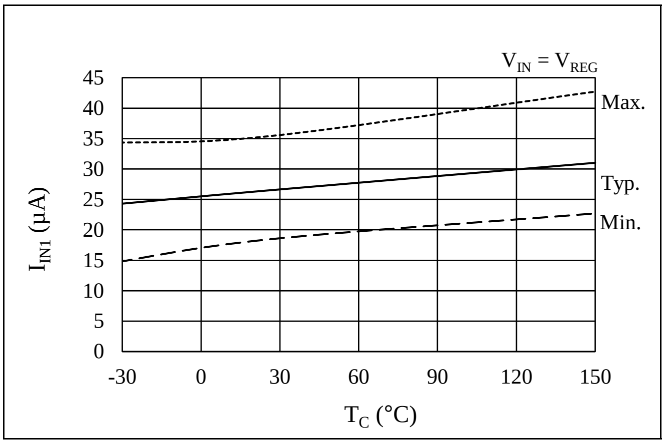


Figure 17-13. High Level Input Current 1 (LA, IS1, IS2, IS3, OVP, or VSP Pin), I_{IN1} vs. T_C

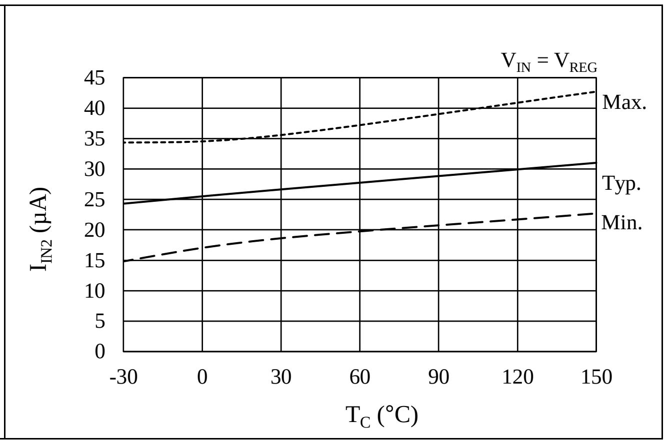


Figure 17-14. High Level Input Current 2 (OCP Pin), I_{IN2} vs. T_C

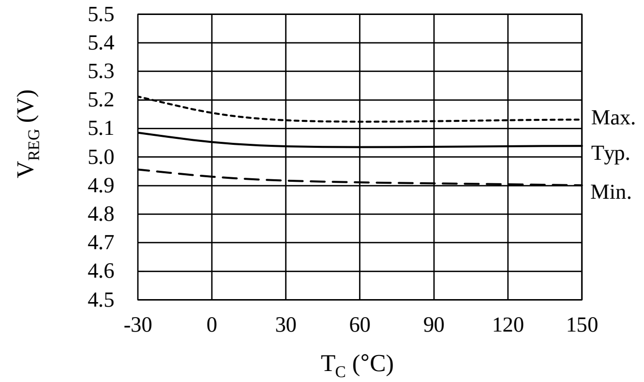


Figure 17-15. VREG Pin Voltage, V_{REG} vs. T_C

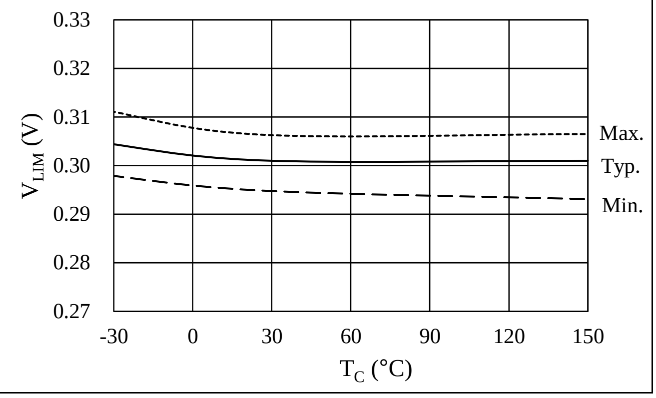


Figure 17-16. Current Limit Reference Voltage, V_{LIM} vs. T_C

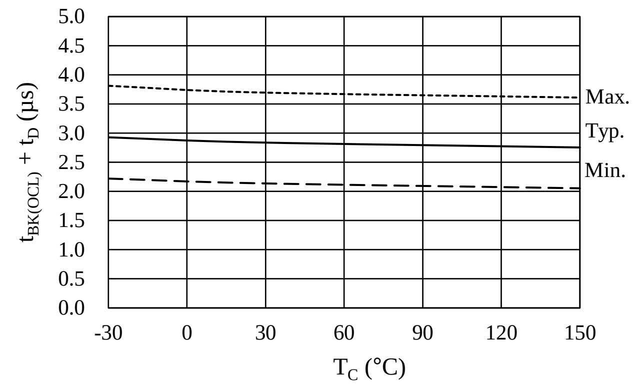


Figure 17-17. OCL Blanking Time, $t_{BK(OCL)}$ + Propagation Delay, t_D vs. T_C

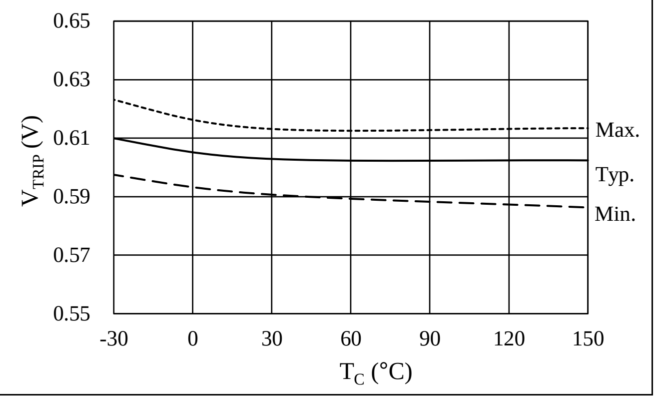


Figure 17-18. OCP Threshold Voltage, V_{TRIP} vs. T_C

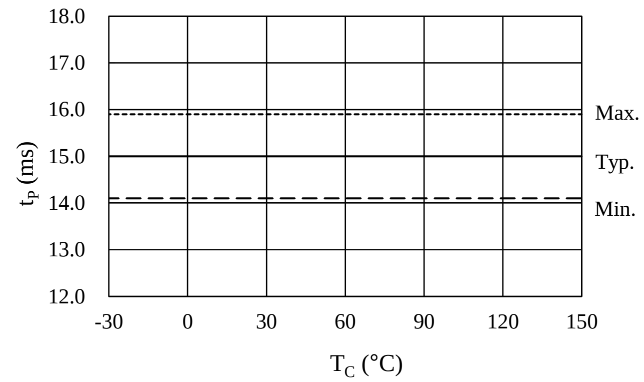
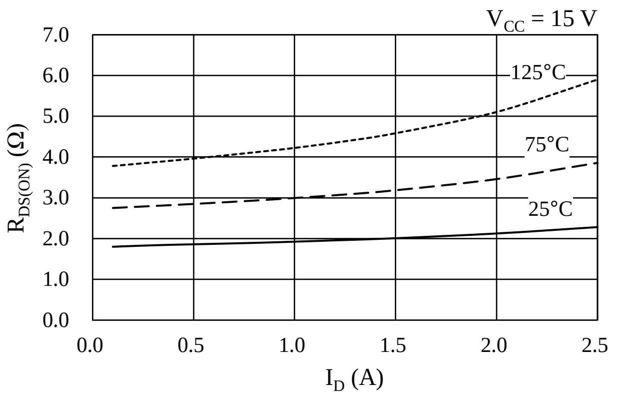


Figure 17-19. OCP Hold Time, t_P vs. T_C

17.3 Performance Curves of Output Parts

17.3.1 Transistor Characteristics

17.3.1.1. SIM2621M



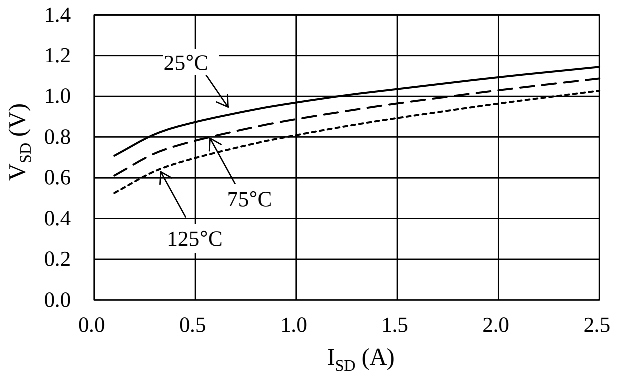
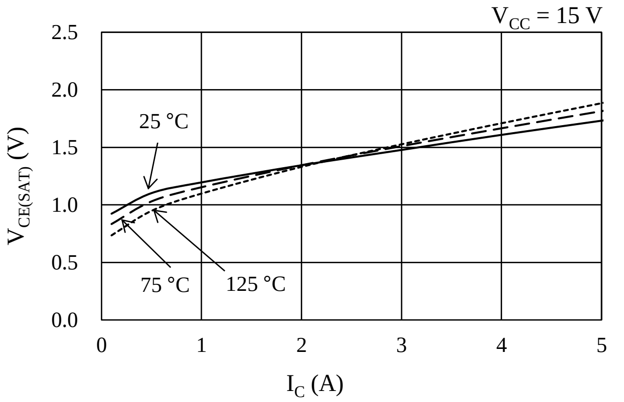


Figure 17-20. Power MOSFET $R_{DS(ON)}$ vs. I_D

Figure 17-21. Power MOSFET V_{SD} vs. I_{SD}

17.3.1.2. SIM2622M



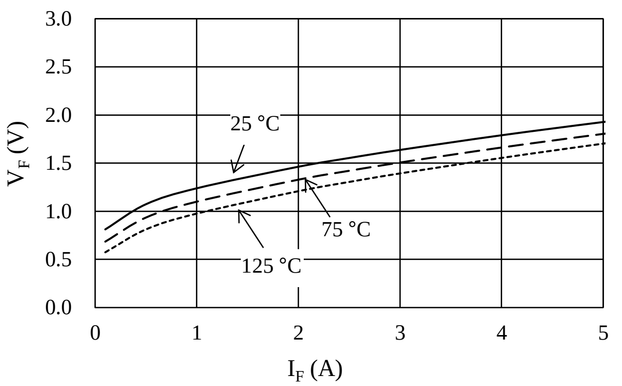


Figure 17-22. IGBT $V_{CE(SAT)}$ vs. I_C

Figure 17-23. Freewheeling Diode V_F vs. I_F

17.3.2 Switching Losses

Conditions: VBBx pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

17.3.2.1. SIM2621M

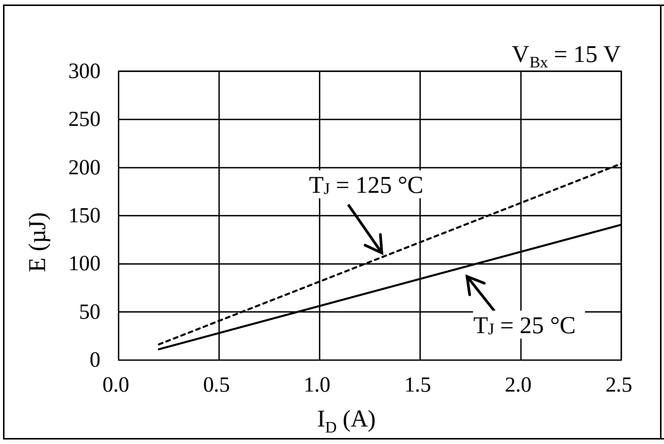


Figure 17-24. High-side Switching Loss

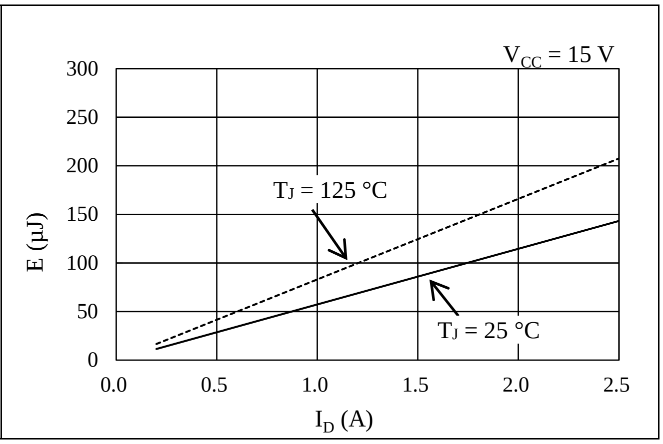


Figure 17-25. Low-side Switching Loss

17.3.2.2. SIM2622M

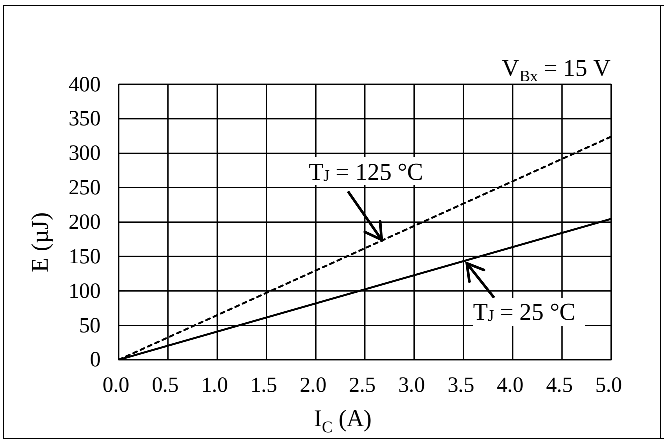


Figure 17-26. High-side Switching Loss

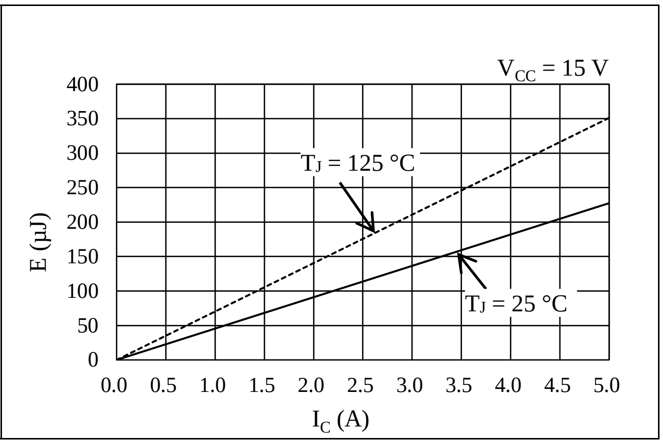


Figure 17-27. Low-side Switching Loss

17.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $R_{DS(ON)}$ or $V_{CE(SAT)}$, and typical switching losses.

Operating conditions: VBBx pin input voltage, V_{DC} = 300 V; VCC pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

17.4.1 SIM2621M

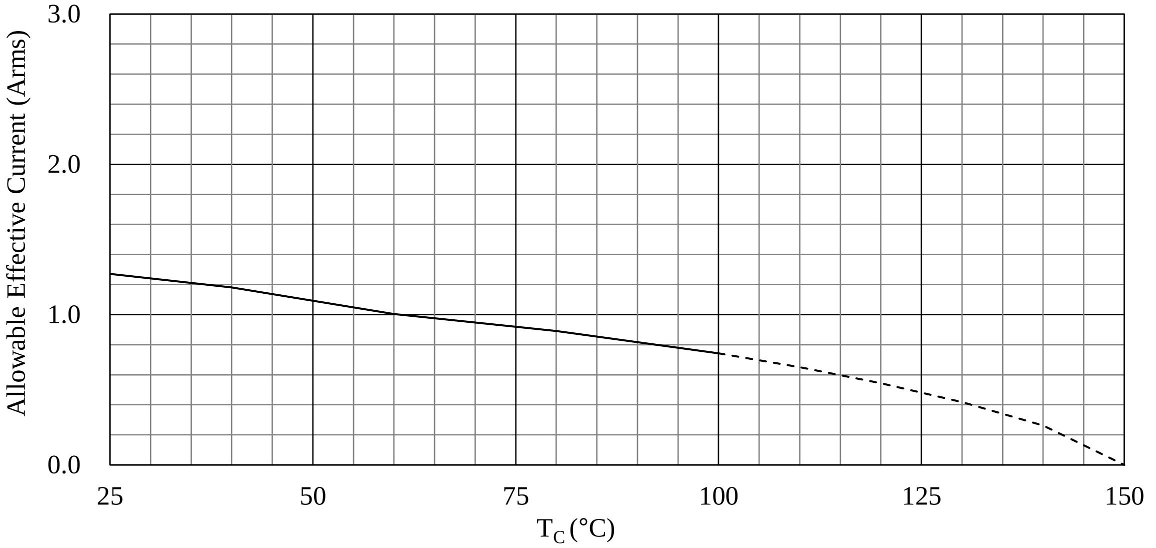


Figure 17-28. Allowable Effective Current (f_C = 17 kHz): SIM2621M

17.4.2 SIM2622M

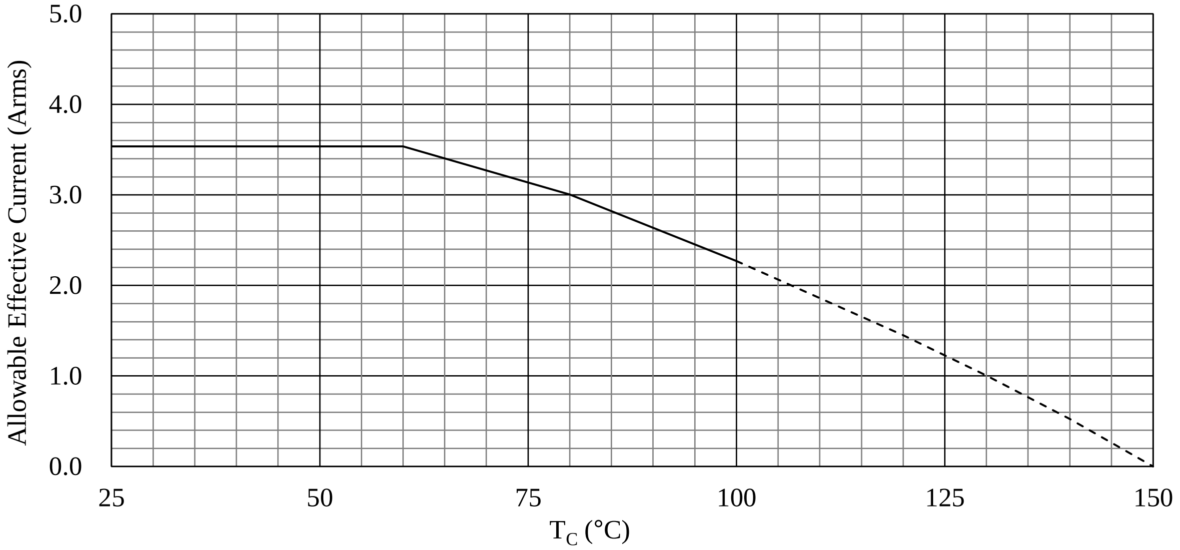


Figure 17-29. Allowable Effective Current (f_C = 17 kHz): SIM2622M

17.5 Short Circuit SOA (Safe Operating Area)

This section provides the graph illustrating the short circuit SOA of the SIM2622M device whose output transistors consist of built-in IGBTs.

Conditions: $V_{DC} \leq 400$ V, 13.5 V $\leq V_{CC} \leq 16.5$ V, $T_J = 125$ °C, 1 pulse.

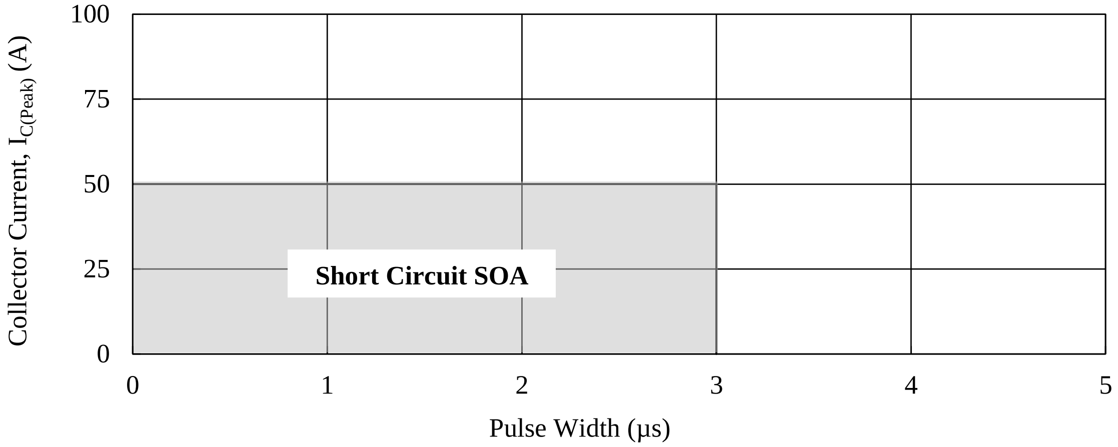
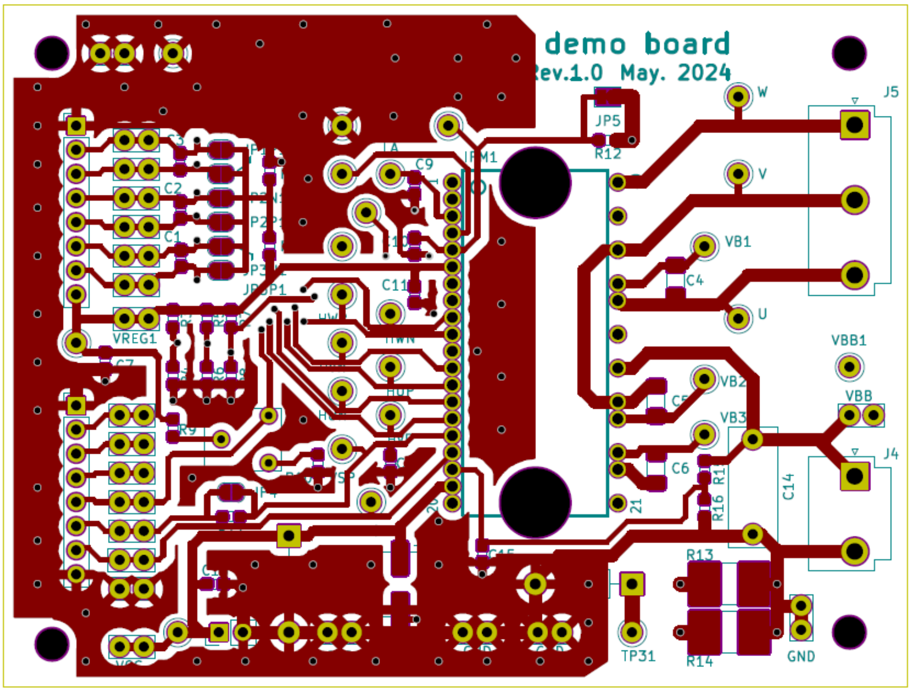


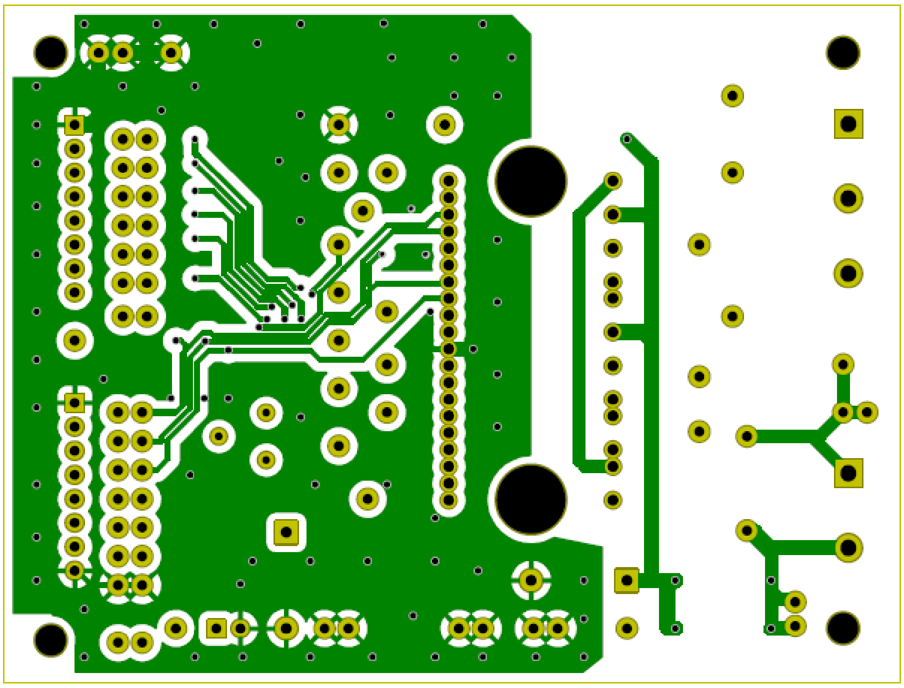
Figure 17-30. Short Circuit SOA: SIM2622M

18. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SIM262xM series device. For details on the land pattern example of the IC, see Section 9.



(Top View)



(Bottom View)

Figure 18-1. Pattern Layout Example

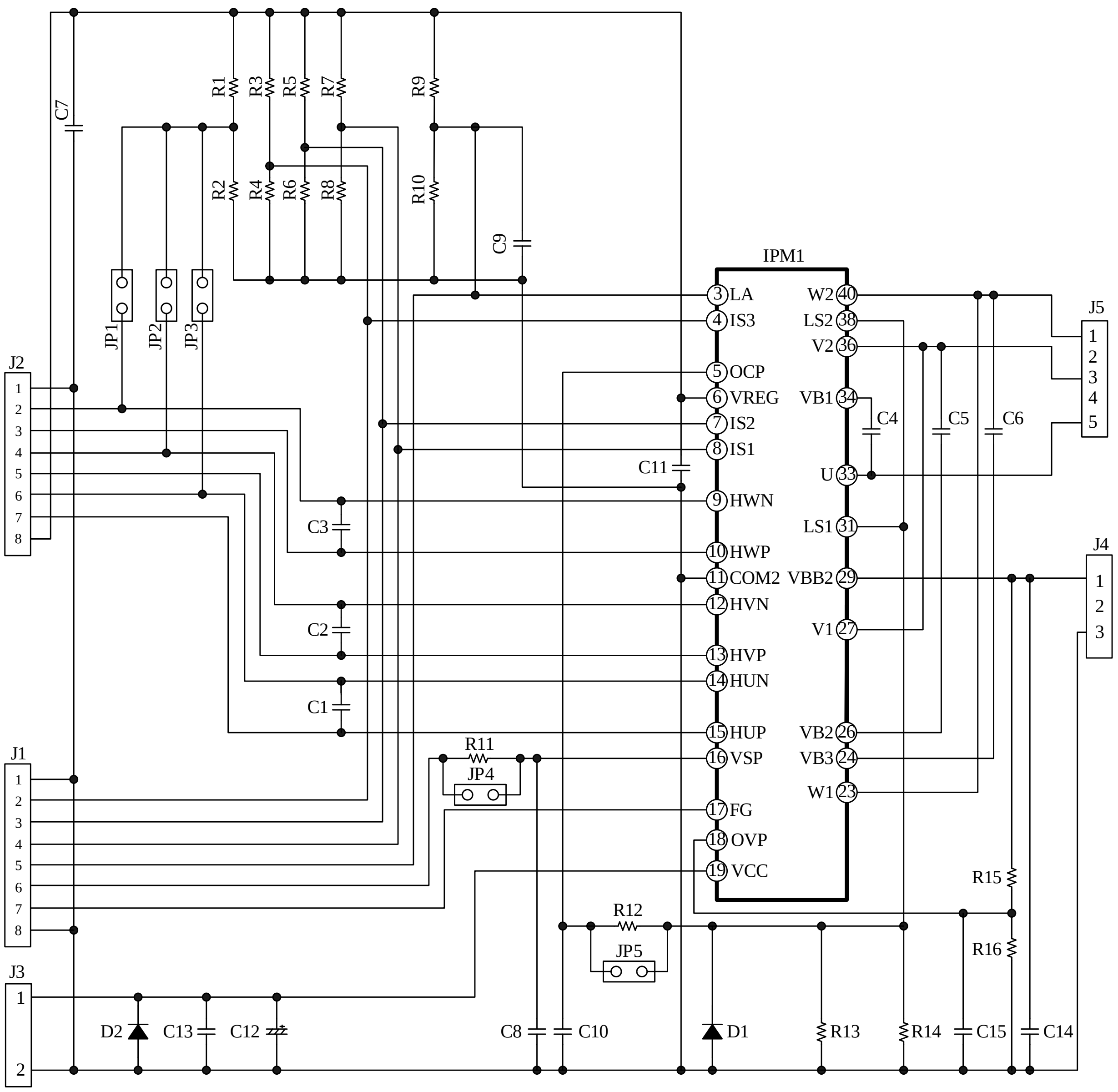


Figure 18-2. Circuit Diagram of PCB Pattern Layout Example

19. Typical Motor Driver Application

This section contains the information on the typical motor driver application (which uses signals input from the Hall elements) listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SIM2622M
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	150 W

- **Circuit Diagram**

See Figure 18-2.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1[1]	Ceramic	Open	R3	General	Short
C2[1]	Ceramic	Open	R4	General	Open
C3[1]	Ceramic	Open	R5	General	Short
C4	Ceramic	1 µF, 35 V	R6	General	Open
C5	Ceramic	1 µF, 35 V	R7	General	Short
C6	Ceramic	1 µF, 35 V	R8	General	Open
C7	Ceramic	0.1 µF, 35 V	R9	General	Short
C8	Ceramic	0.1 µF, 35 V	R10	General	1 kΩ, 0.25 W
C9	Ceramic	0.1 µF, 35 V	R11[2]	General	Open
C10	Ceramic	2200 pF, 35 V	R12	General	100 Ω, 0.25 W
C11	Ceramic	0.1 µF, 35 V	R13	Metal plate	0.33 Ω, 1 W
C12	Electrolytic	100 µF, 35 V	R14	Metal plate	Open
C13	Ceramic	0.1 µF, 35 V	R15	General	470 kΩ, 0.25 W
C14	Ceramic	0.1 µF, 630 V	R16	General	2.2 kΩ, 0.25 W
C15	Ceramic	0.01 µF, 35 V	JP1[3][4]	Jumper	Open
J1	Pin header	1 × 08	JP2[3][4]	Jumper	Open
J2	Pin header	1 × 08	JP3[3][4]	Jumper	Open
J3	Pin header	1 × 02	JP4[5]	Jumper	Short
J4	Pin header	Equiv. to B2P3-VH	JP5	Jumper	Open
J5	Pin header	Equiv. to B3P5-VH	D1	General	1 A, 50 V
R1	General	2.2 kΩ, 0.25 W	D2	Zener	V_Z = 20 V, 0.5 W
R2	General	2.2 kΩ, 0.25 W	IPM1	IC	SIM2622M

[1] Refers to a noise filter capacitor for Hall element signals; should be connected as needed.
[2] Refers to a noise filter resistor for a motor speed control signal input to the VSP pin; should be connected as needed.
[3] When inputting Hall IC signals for detecting a south pole: set JP1, JP3, JP5 = short.
[4] When inputting Hall IC signals for detecting a north pole: set JP1, JP3, JP5 = open.
[5] Should be opened when R11 is connected; should be shorted when R11 is not connected.

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