SLA7070MPRT Series Unipolar 2-Phase Stepper Motor Driver ICs

General Description

This document describes the SLA7070MPRT series, which are unipolar 2-phase stepping motor driver ICs. The SLA7070MPRT series employs a clock input method as a control signal input method, enabling full control of the device operation using only a few signal lines, instead of the conventional phase input method that requires about 10 signal lines. This allows simplification of the circuit design and a reduced workload on the control microprocessor.

In addition, the SLA7070MPRT series is improved in its reliability by preventing the IC from damage due to abnormal conditions. For example, it has a flag output terminal to signal that a protection circuit has operated. The series also has a built-in protection circuitry against motor coil opens/shorts and thermal shutdown protection as well.

All the SLA7070MPRT series ICs are compatible in their pin layouts and interface specifications, allowing customers the flexibility of choosing the IC that is optimal for the target equipment characteristics.

Figure 1. SLA7070MPRT packages are fully molded ZIPs with an exposed pad for heatsink mounting.

Features and Benefits

- Power supply voltages, V_{BB}: 46 V (max.), 10 to 44 V normal operating range
- Logic supply voltages, V_{DD}: 3.0 to 5.5 V
- Maximum output currents: 1 A, 1.5 A, 2 A, 3 A
- Built-in sequencer
- Full-, half-, and microstepping available (microstepping options are capable of full-, half-, quarter-, eighth-, and sixteenth-stepping
- Built-in sense resistor, R_{SInt}
- All variants are pin-compatible for enhanced design flexibility
- ZIP type 23-pin molded package (SLA package)
- Self-excitation PWM current control with fixed off-time (microstepping options off-time adjusted automatically by step reference current ratio; 3 levels)
- Built-in synchronous rectifying circuit reduces losses at PWM-off
- Synchronous PWM chopping function prevents motor noise in Hold mode
- Sleep mode for reducing the IC input current in stand-by state
- Built-in protection circuitry against motor coil opens/shorts and thermal shutdown protection options

Applications

- LBPs, PPCs, ATMs, industrial robots, and so forth

The SLA7070MMPR series product variants and optional features

Part Number	Stepping Rate	Output Current (I_{OUT}) (A)	Input Clock Edge Detection	Blanking Time (µs)
			Standard	Standard
SLA7070MPRT	Full and half step	1	Rising (positive) edge	3.2
SLA7071MPRT		1.5		
SLA7072MPRT		2		
SLA7073MPRT		3		
SLA7075MPRT	Microstep	1	Rising (positive) edge	1.7
SLA7076MPRT		1.5		
SLA7077MPRT		2		
SLA7078MPRT		3		

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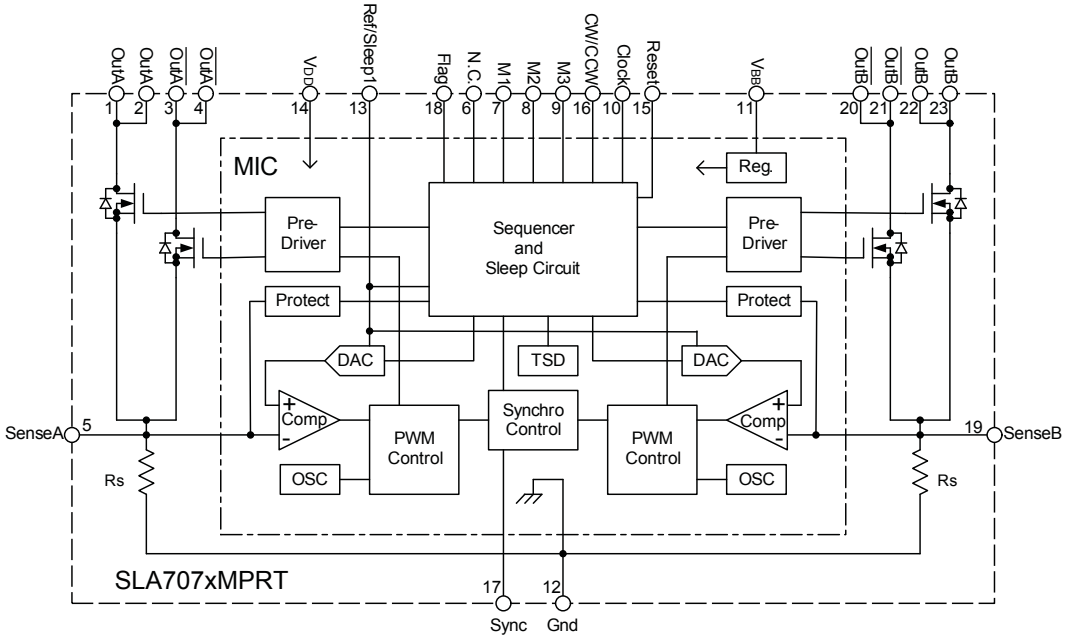
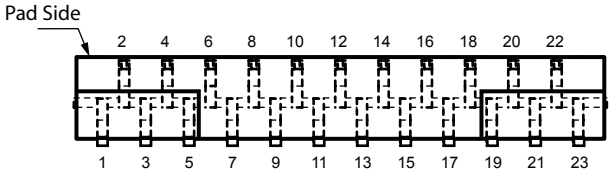
Table of Contents

Functional Block Diagrams

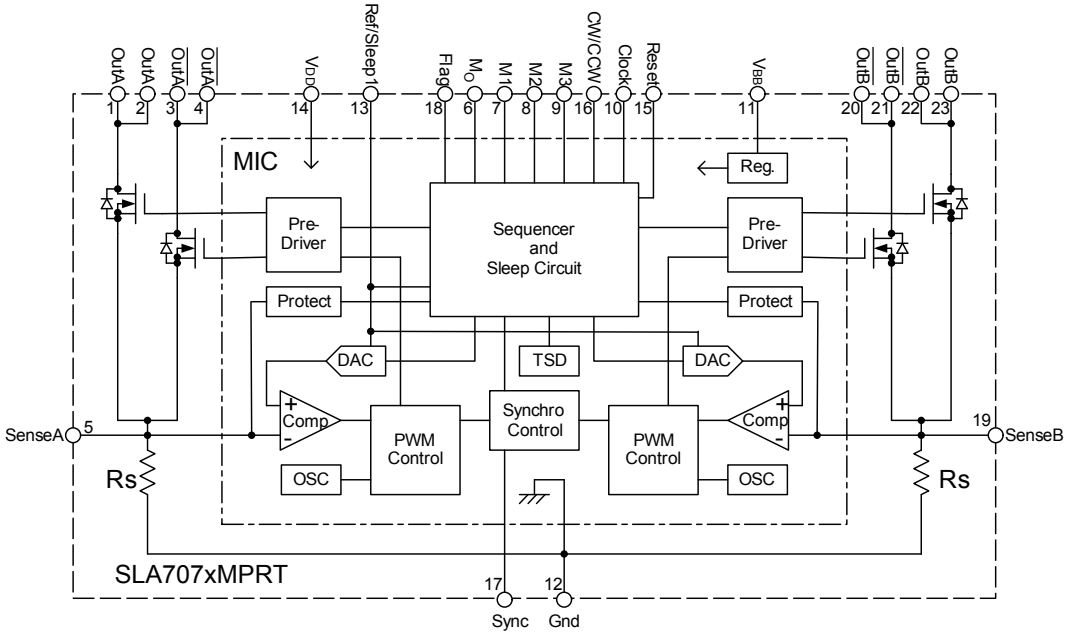
SLA7070MPRT to SLA7073MPRT: Full and Half step

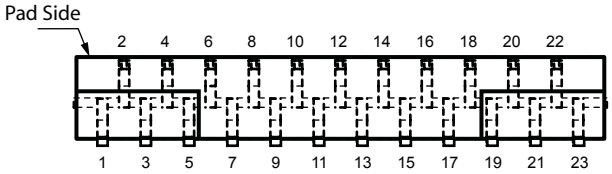




Pin Number.	Symbol	Function
1, 2	OutA	Output of phase A
3, 4	$\overline{\text{OutA}}$	Output of phase $\overline{\text{A}}$
5	SenseA	Phase A current sensing
6	N.C.	No connection
7	M1	Commutation and Sleep2 setting
8	M2	
9	M3	
10	Clock	Step clock input
11	VBB	Main power supply (for motor)
12	Gnd	Ground
13	Ref/Sleep1	Input for control current and Sleep1 setting
14	VDD	Power supply to logic
15	Reset	Reset for internal logic
16	CW/CCW	Forward/reverse switch input
17	Sync	Synchronous PWM control switch input
18	Flag	Output from protection circuits monitor
19	SenseB	Phase B current sensing
20, 21	$\overline{\text{OutB}}$	Output of phase $\overline{\text{B}}$
22, 23	OutB	Output of phase B

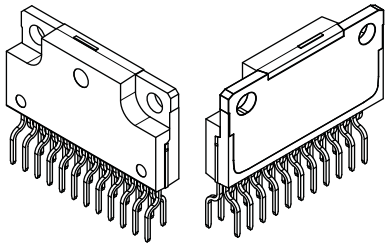
SLA7075MPRT to SLA7078MPRT: Microstep

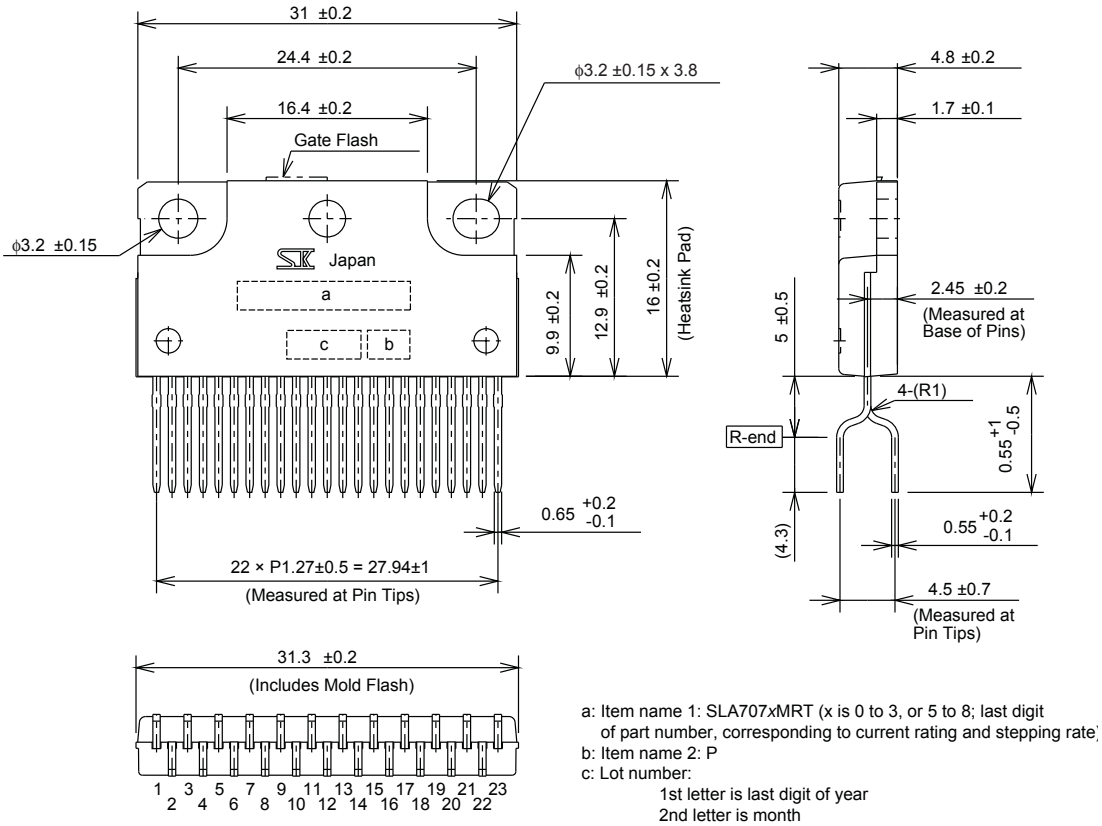




Pin Number.	Symbol	Function
1, 2	OutA	Output of phase A
3, 4	$\overline{\text{OutA}}$	Output of phase $\overline{A}$
5	SenseA	Phase A current sensing
6	M_O	2-phase commutation status monitor output
7	M1	Commutation and Sleep2 setting
8	M2	
9	M3	
10	Clock	Step clock input
11	VBB	Main power supply (for motor)
12	Gnd	Ground
13	Ref/Sleep1	Input for control current and Sleep1 setting
14	VDD	Power supply to logic
15	Reset	Reset for internal logic
16	CW/CCW	Forward/reverse switch input
17	Sync	Synchronous PWM control switch input
18	Flag	Output from protection circuits monitor
19	SenseB	Phase B current sensing
20, 21	$\overline{\text{OutB}}$	Output of phase $\overline{A}$
22, 23	OutB	Output of phase B

Package Outline Drawing, SLA 23-Pin





a: Item name 1: SLA707*x*MRT (x is 0 to 3, or 5 to 8; last digit of part number, corresponding to current rating and stepping rate)
b: Item name 2: P
c: Lot number:
1st letter is last digit of year
2nd letter is month
January to September: 1 to 9
October: O
November: N
December: D
3rd and 4th are date of manufacture (01 to 31)

Unit: mm
Pin material: Cu
Pin Plating: Solder plating (Pb free)

Leadframe plating Pb-free. Device composition includes high-temperature solder (Pb >85%), which is exempted from the RoHS directive.

Electrical Characteristics

• This section provides separate sets of electrical characteristic data for each product.

• The polarity value for current specifies a sink as "+ ," and a source as "−," referencing the IC.

• Please refer to the datasheet of each product for additional details.

Absolute Maximum Ratings Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Notes		Rating	Unit
Load (Motor Supply) Voltage	V_M			46	V
Main Power Supply Voltage	V_{BB}			46	V
Logic Supply Voltage	V_{DD}			6	V
		≤1 µs (5% duty)		7	V
Output Current	I_O	SLA7070MPRT SLA7075MPRT	Control current value	1.0	A
		SLA7071MPRT SLA7076MPRT		1.5	A
		SLA7072MPRT SLA7077MPRT		2.0	A
		SLA7073MPRT SLA7078MPRT		3.0	A
Logic Input Voltage	V_{IN}			−0.3 to V_{DD}+0.3	V
REF Input Voltage	V_{REF}			−0.3 to V_{DD}+0.3	V
Sense Voltage	V_{RS}			±1	V
Power Dissipation	P_D	Without heatsink		4.7	W
Junction Temperature	T_J			150	°C

Recommended Operating Conditions Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Load (Motor Supply) Voltage	V_M		–	–	44	V
Main Power Supply Voltage	V_{BB}		10	–	44	V
Logic Supply Voltage	V_{DD}	Surge voltage at VDD pin should be less than ±0.5 V to avoid malfunctioning in operation	3.0	–	5.5	V
Case Temperature	T_c	Measured at pin 12, without heatsink	–	–	90	°C

Electrical Characteristics Common to All Variants Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Main Power Supply Current	I_{BB}	Normal mode	–	–	15	mA
	I_{BBS}	Sleep1 and Sleep2 mode	–	–	100	µA
Logic Power Current	I_{DD}		–	–	5	mA
MOSFET Breakdown Voltage	V_{DSS}	V_{BB} = 44 V, I_D = 1 mA	100	–	–	V
Maximum Response Frequency	f_{clk}	Clock duty = 50%	250	–	–	KHz
Logic Supply Voltage	V_{IL}		–	–	$0.25 \times V_{DD}$	V
	V_{IH}		$0.75 \times V_{DD}$	–	–	V
Logic Supply Current	I_{IL}		–	±1	–	µA
	I_{IH}		–	±1	–	µA
REF Input Voltage[1]	V_{REF}	See figure 1	–	–	–	V
	V_{REFS}	Output off, Sleep1 mode	2.0	–	V_{DD}	V
REF Input Current	I_{REF}		–	±10	–	µA
SENSE Voltage	V_{SENSE}	V_{REF} = 0 to 1.5 V Step reference current ratio: 100%	V_{REF} – 0.03	–	V_{REF} – 0.03	V
Sleep to Enable Recovery Time	t_{SE}	Sleep1 and Sleep2	100	–	–	µs
Switching Time	t_{con}	Clock edge to output on	–	2.0	–	µs
	t_{coff}	Clock edge to output off	–	1.5	–	µs
Overcurrent Detection Voltage[2]	V_{OCP}	At motor coil short-circuit	0.65	0.7	0.75	V
Overcurrent Detection Current (V_{OCP} / R_S)	I_{OCP}	SLA7070MPRT, SLA7075MPRT, SLA7071MPRT, SLA7076MPRT	–	2.3	–	A
		SLA7072MPRT, SLA7077MPRT	–	3.5	–	A
		SLA7073MPRT, SLA7078MPRT	–	4.6	–	A
Load Disconnection Undetected Time	t_{opp}	From PWM off	–	2	–	µs
Overheat Protection Temperature	T_{tsd}	Measured at back of device case (after heat has saturated)	–	140	–	°C
Flag Output Voltage	V_{FlagL}	I_{FlagL} = 1.25 mA	–	–	1.25	V
	V_{FlagH}	I_{FlagH} = –1.25 mA	V_{DD} – 1.25	–	–	V
Flag Output Current	I_{FlagL}		–	–	1.25	mA
	I_{FlagH}		–1.25	–	–	mA

[1]In a state of: Sleep1, I_{BBS}, output off, and Sequencer enabled.
[2]In a condition of $V_{SENSE} \geq V_{OCP}$, the protection circuit will activate.

Electrical Characteristics Varying with Stepping Sequence Unless specifically noted, T_A is 25°C, V_{BB} = 24 V, V_{DD} = 5 V

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SLA7070MPRT, SLA7071MPRT, SLA7072MPRT, and SLA7073MPRT (Full- and Half-Stepping)						
Step Reference Current Ratio	Mode F	$V_{REF} \approx V_{SENSE}$ = 100 V, V_{REF} = 0 to 1.0 V	–	100	–	%
	Mode 8		–	70	–	%
PWM Minimum On-Time	$t_{on(min)}$		–	3.2	–	µs
PWM Off-Time	t_{off}		–	12	–	µs
SLA7075MPRT, SLA7076MPRT, SLA7077MPRT, and SLA7078MPRT (Microstepping)						
Step Reference Current Ratio	Mode F	$V_{REF} \approx V_{SENSE}$ = 100 V, V_{REF} = 0 to 1.0 V	–	100	–	%
	Mode E		–	98.1	–	%
	Mode D		–	95.7	–	%
	Mode C		–	92.4	–	%
	Mode B		–	88.2	–	%
	Mode A		–	83.1	–	%
	Mode 9		–	77.3	–	%
	Mode 8		–	70.7	–	%
	Mode 7		–	63.4	–	%
	Mode 6		–	55.5	–	%
	Mode 5		–	47.1	–	%
	Mode 4		–	38.2	–	%
	Mode 3		–	29	–	%
	Mode 2		–	19.5	–	%
	Mode 1		–	9.8	–	%
M_O (Load) Output Voltage	V_{MOL}	I_{MOL} = 1.25 mA	–	–	1.25	V
	V_{MOH}	I_{MOH} = –1.25 mA	V_{DD} – 1.25	–	–	V
M_O (Load) Output Current	I_{MOL}		–	–	1.25	mA
	I_{MOH}		–1.25	–	–	mA
PWM Minimum On-Time	$t_{on(min)}$		–	1.7	–	µs
PWM Off-Time	t_{off1}	Mode 8, 9, A, B, C, D, E, and F	–	12	–	µs
	t_{off2}	Mode 4, 5, 6, and 7	–	9	–	µs
	t_{off3}	Mode 1, 2, and 3	–	7	–	µs

Electrical Characteristics Varying with Output Current Range Unless specifically noted, T_A is 25°C, V_{BB} = 24 V, V_{DD} = 5 V

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SLA7070MPRT and SLA7075MPRT (I_O = 1.0 A)						
Output On-Resistance	$R_{DS(on)}$	I_D = 1 A	–	0.7	0.85	Ω
Body Diode Forward Voltage	V_f	I_f = 1 A	–	0.85	1.1	V
Sense Resistor*	R_S	±3% tolerance	0.296	0.305	0.314	Ω
REF Input Voltage	V_{REF}	Within specified current limit, I_O = 1.0 A	0.04	–	0.3	V
SLA7071MPRT and SLA7076MPRT (I_O = 1.5 A)						
Output On-Resistance	$R_{DS(on)}$	I_D = 1.5 A	–	0.45	0.6	Ω
Body Diode Forward Voltage	V_f	I_f = 1.5 A	–	1.0	1.25	V
Sense Resistor*	R_S	±3% tolerance	0.296	0.305	0.314	Ω
REF Input Voltage	V_{REF}	Within specified current limit, I_O = 1.5 A	0.04	–	0.45	V
SLA7072MPRT and SLA7077MPRT (I_O = 2.0 A) Electrical Characteristics						
Output On-Resistance	$R_{DS(on)}$	I_D = 2 A	–	0.25	0.4	Ω
Body Diode Forward Voltage	V_f	I_f = 2 A	–	0.95	1.2	V
Sense Resistor*	R_S	±3% tolerance	0.199	0.205	0.211	Ω
REF Input Voltage	V_{REF}	Within specified current limit, I_O = 2.0 A	0.04	–	0.4	V
SLA7073MPRT and SLA7078MPRT (I_O = 3.0 A) Electrical Characteristics						
Output On-Resistance	$R_{DS(on)}$	I_D = 3 A	–	0.18	0.24	Ω
Body Diode Forward Voltage	V_f	I_f = 3 A	–	0.95	2.1	V
Sense Resistor*	R_S	±3% tolerance	0.150	0.155	0.160	Ω
REF Input Voltage	V_{REF}	Within specified current limit, I_O = 3.0 A	0.04	–	0.45	V

*Includes the inherent bulk resistance (approximately 5 mΩ) of the resistor itself.

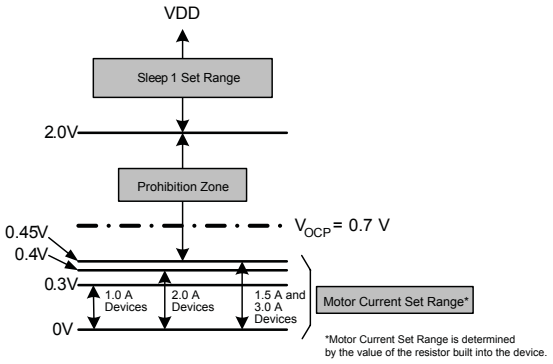


Figure 1. Reference Voltage Setting (V_{REF}, REF/SLEEP1 Pin). Please pay extra attention to the change-over between the motor current specification range, I_{MO}, and the Sleep1 Set Range. V_{OCP} falls on the "prohibition zone" threshold. If the change-over time is too slow, OCP operation will start when $V_{SInt} > V_{OCP}$.

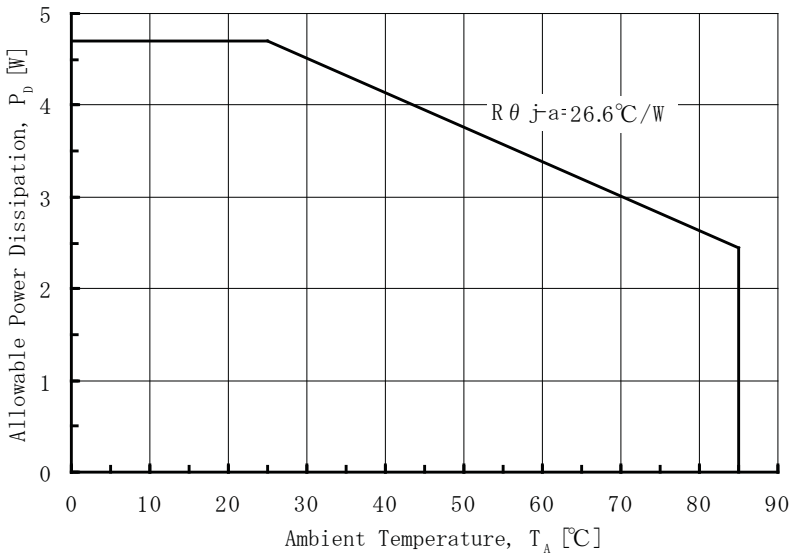


Figure 2. Allowable Power Dissipation

Typical Application
(Microstepper Variants)

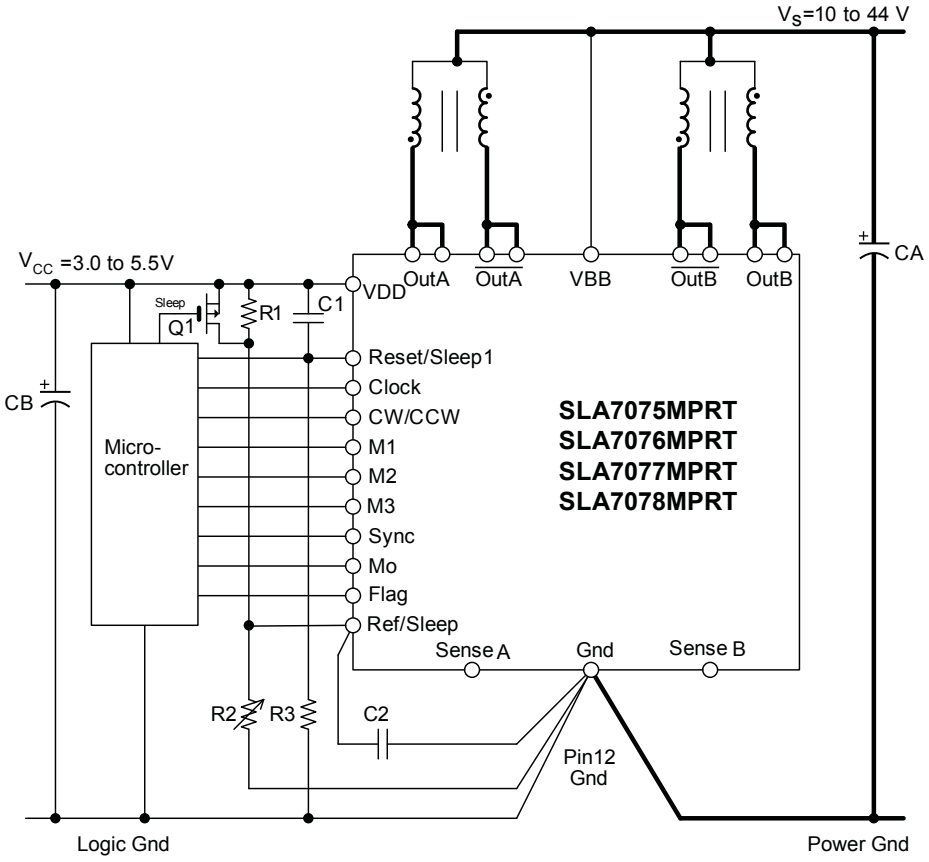


Figure 3. Typical Application Circuit

External Component Typical Values
(for reference use only):

Component	Value	Component	Value
R1	10 kΩ	CA	100 µF / 50 V
R2	1 kΩ (varistor)	CB	10 µF / 10 V
R3	10 kΩ	C1	0.1 µF

- Take precautions to avoid noise on the VDD line; noise levels greater than 0.5 V on the VDD line may cause device malfunction. Noise can be reduced by separating the logic ground and the power ground on a PCB from the GND pin (pin 12).
- Unused logic input pins (CW / CCW, M1, M2, M3, Reset, and SYNC) must be pulled up or down to VDD or ground. If those unused pins are left open, the device malfunctions.
- Unused logic output pins (Mo, Flag) must be kept open.

Truth Tables

Common Input Pins

Table 1 shows the truth table for input pins common to both half/full step and microstep variants of the SLA7070MPRT series.

• The Reset function is asynchronous. If the input on the Reset pin is high, the internal logic circuit is reset. At this point, if the Ref pin stays low, then the DMOS outputs turn on at the starting point of excitation. Note that the Disable control functions are not available with the Reset pin signal set high.

• Voltage at the Ref/Sleep1 pin controls the PWM current and the Sleep1 function. For normal operation, V_{REF} should be below 1.5 V (low level). Applying a voltage greater than 2.0 V (high level) to the Ref/Sleep1 pin disables the outputs and puts the motor in a free state (coast). This function is used to minimize power consumption when the device is not in use. Although it disables much of the internal circuitry, including the output MOSFETs and regulator, the sequencer/translator circuit remains active.

• The Sync function is active only for 2-phase excitation timing. If this function is used during other than 2-phase excitation timing, the overall stepping sequence might collapse because PWM off-time and set current are different in each phase A and phase B control scenario. (2-phase excitation timing is when the step reference current ratio of both phase A and phase B is Mode 8.)

Commutation/Sleep2 Function

Table 2 shows the logic of the pins (M1, M2, and M3) which set commutation. In the Sleep2 function, the outputs are disabled and the driver supply current (I_{BB}) is reduced. However, unlike the Sleep1 function, the logic circuitry is put into a standby state and therefore the sequencer/translator circuit is not active.

Note: When awakening from Sleep2 mode, a delay of 100 μs or longer before sending a Clock pulse is recommended.

Monitor Output Pin

The SLA7070MPRT series provides two device status monitor outputs:

• Flag pin – Protection feature operation

• Mo pin (microstep variants only) – Stepping sequence

Table 3 shows the logic for the monitor pins. The outputs turn off when the protection circuit starts operating. To release the protection state, cycle (set low, and then high) the logic supply voltage (V_{DD}).

Table 2. Commutation-Sleep2 Truth Table for Common Input Pins (Half/Full and Microstep)

Pin Name			Full/Half Step	Microstep
M1	M2	M3		
L	L	L	Full step (Mode 8 fixed)	Full step (Mode 8 fixed)
H	L	L	Full step (Mode F fixed)	Full step (Mode F fixed)
L	H	L	Half step	Half step
H	H	L	Half step (Mode F fixed)	Half step (Mode F fixed)
L	L	H	Sleep2 function	Quarter step
H	L	H		Eighth step
L	H	H		Sixteenth step
H	H	H		Sleep2 function

Table 3. Monitor Output Pins Logic

Pin Name	Low Level	High Level
Flag	Normal operation	Protection circuit operation
Mo	Other than 2-phase excitation timing	2-phase excitation timing

Table 1. Truth Table for Common Input Pins (Half/Full and Microstep)

Pin Name	Low Level	High Level	Clock
Reset	Normal operation	Logic reset	
CW/CCW	Forward (CW)	Reverse (CCW)	
M1, M2, M3	Commutation (Sleep2 is not included)		
Ref/Sleep1	Normal operation	Sleep1 function	
Sync	Non-sync PWM control	Sync PWM control	**(Positive Edge)**

Logic Input Pins

The low pass filter incorporated with the logic input pins (Reset, Clock, CW/CCW, M1, M2, M3, and Sync) improves noise rejection. The logic inputs are CMOS input compatible, and therefore they are in a high impedance state. Use the IC at a fixed input level, either low or high.

Input Logic Timing

Clock Signal

A low-to-high then high-to-low transition on the Clock input advances the sequencer / translator. The Clock pulse width should be set at 2 µs in both positive and negative polarities. Therefore, clock response frequency should be 250 kHz. Only the positive edge is used for timing, however, it is necessary to control the logic levels of the Clock signal both before and after each Clock signal edge sent to the sequencer logic circuit, in order to maintain proper stepping operation.

Clock Edge Timing

With regard to the input logic of the CW/CCW, M1, M2, and M3 pins, a 1 µs delay should occur both before and after the pulse edges and as setup and hold times. The sequencer logic circuitry might malfunction if the logic polarity is changed during these setup and hold times. (Refer to figure 4).

Reset Release and Clock Input Timing

The Reset pulse width is equivalent to the high pulse level hold time. It should be greater than the 2 µs Clock input pulse width.

When the timing of a Reset release (falling edge) and a Clock edge is simultaneous, the internal logic might cause an unexpected operation. Therefore, a greater than 5 µs delay is required between the falling edge of the Reset input and the next rising edge of the Clock input. (Refer to figure 4).

Logic Level Change

Logic level inputs on CW/CCW, M1, M2, and M3 set the translator step direction (CW/CCW) and step mode (M1, M2, and M3; refer to the Commutation Truth Table). Changes to these inputs do not take effect until the rising edge of the Clock input. However, depending on the type and state of a motor, there may be errors in motor operation. A thorough evaluation on the changes of sequence should be carried out.

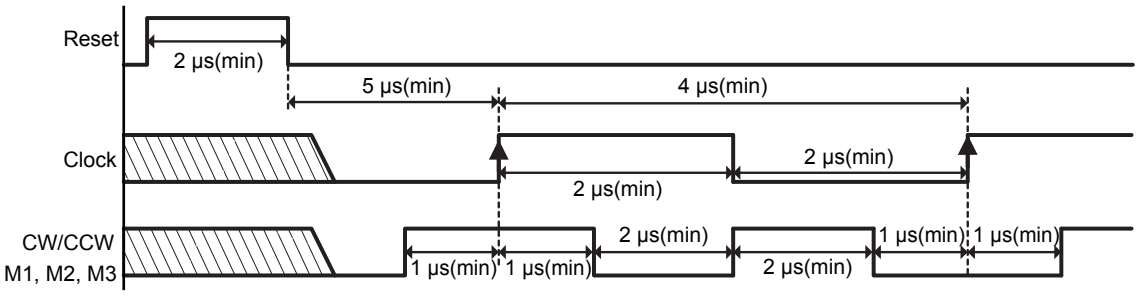


Figure 4. Input Signal Timing. When awakening from Sleep1 or Sleep2 mode, a delay of 100 µs or longer before sending a Clock pulse is recommended.

Stepping Sequence Diagrams

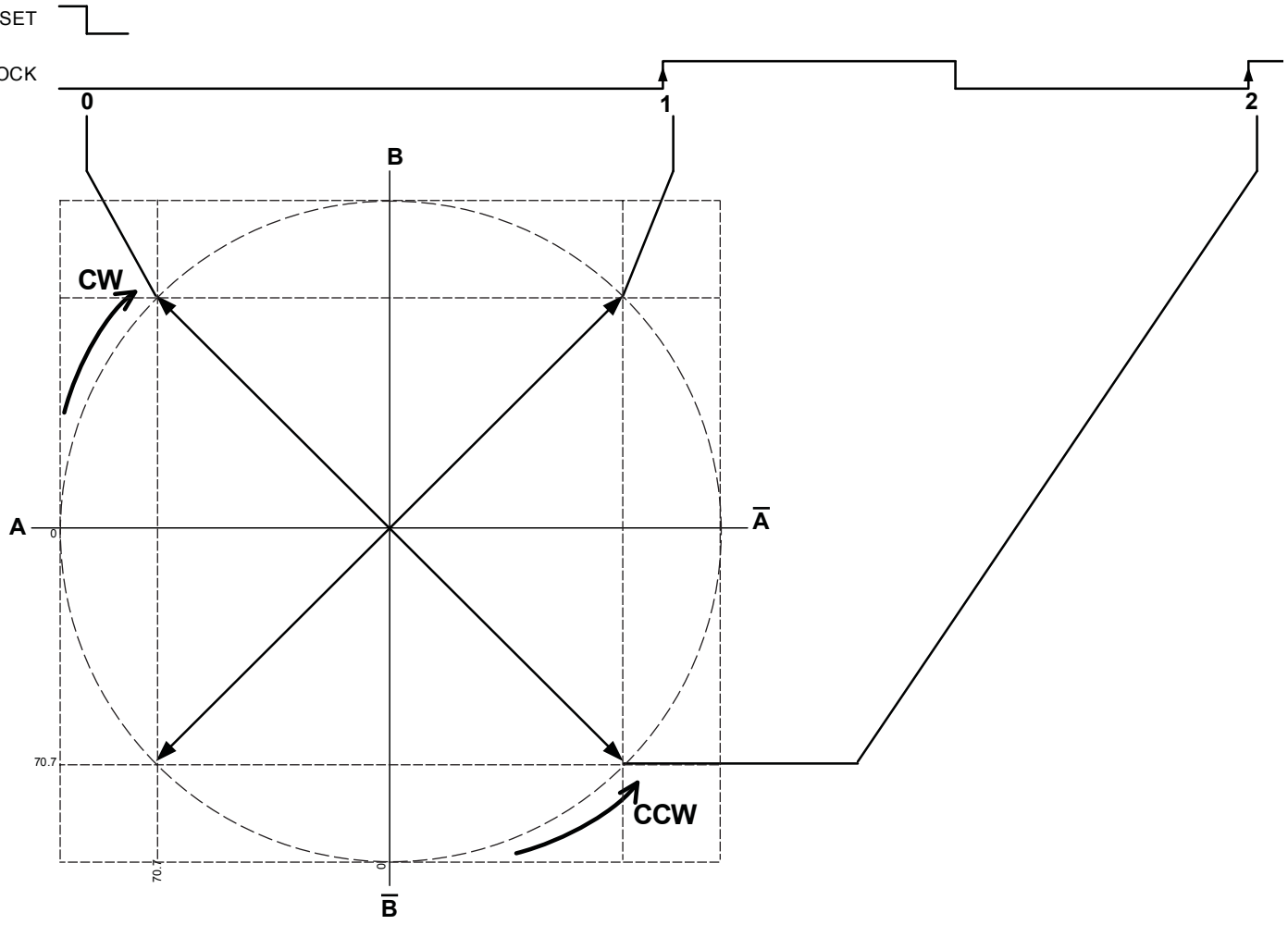


Figure 5. Full step; for microstep and full/half step products

Sequence Selection

Mode	Pin Logic		
	M1	M2	M3
Full Step 8	Low	Low	Low

Shows the state to which the stepping sequence progresses at the rising (positive) edge of the Clock input.

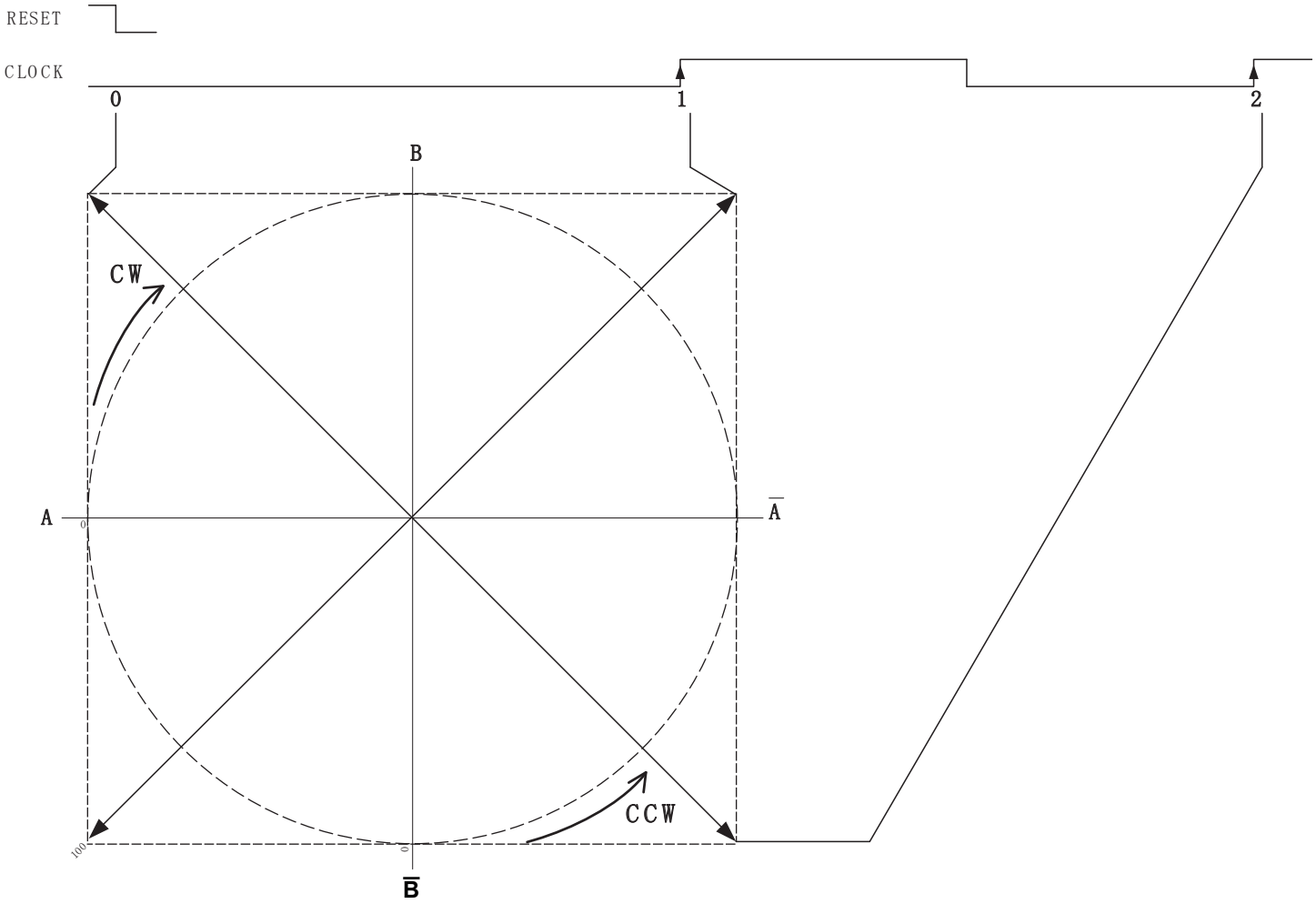


Figure 6. Full step; for microstep and full/half step products

Sequence Selection

Mode	Pin Logic		
	M1	M2	M3
Full Step F	High	Low	Low

Shows the state to which the stepping sequence progresses at the rising (positive) edge of the Clock input.

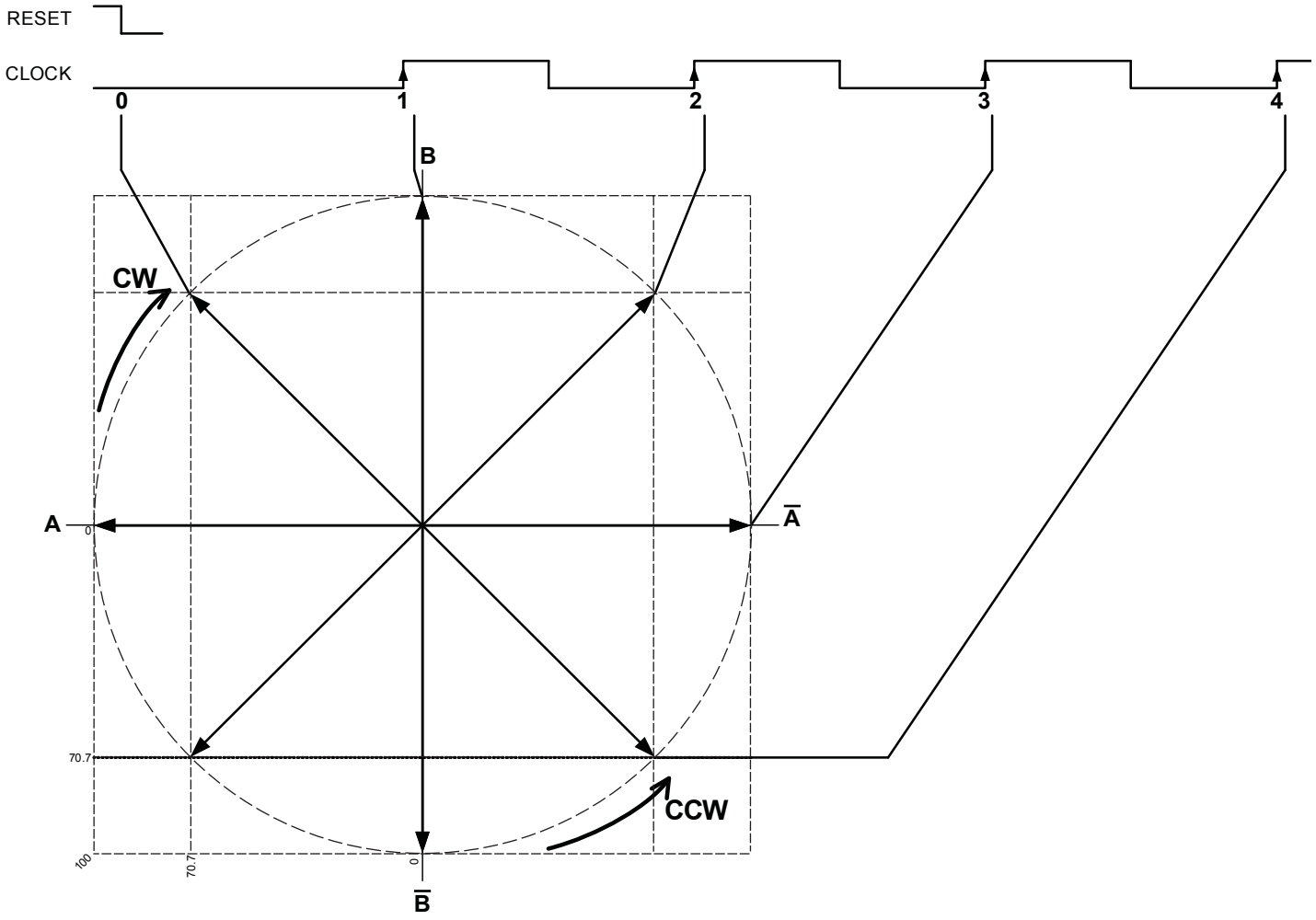


Figure 7. Half step; for microstep and full/half step products

Sequence Selection

Mode	Pin Logic		
	M1	M2	M3
Half Step 8, F	Low	High	Low

Shows the state to which the stepping sequence progresses at the rising (positive) edge of the Clock input.

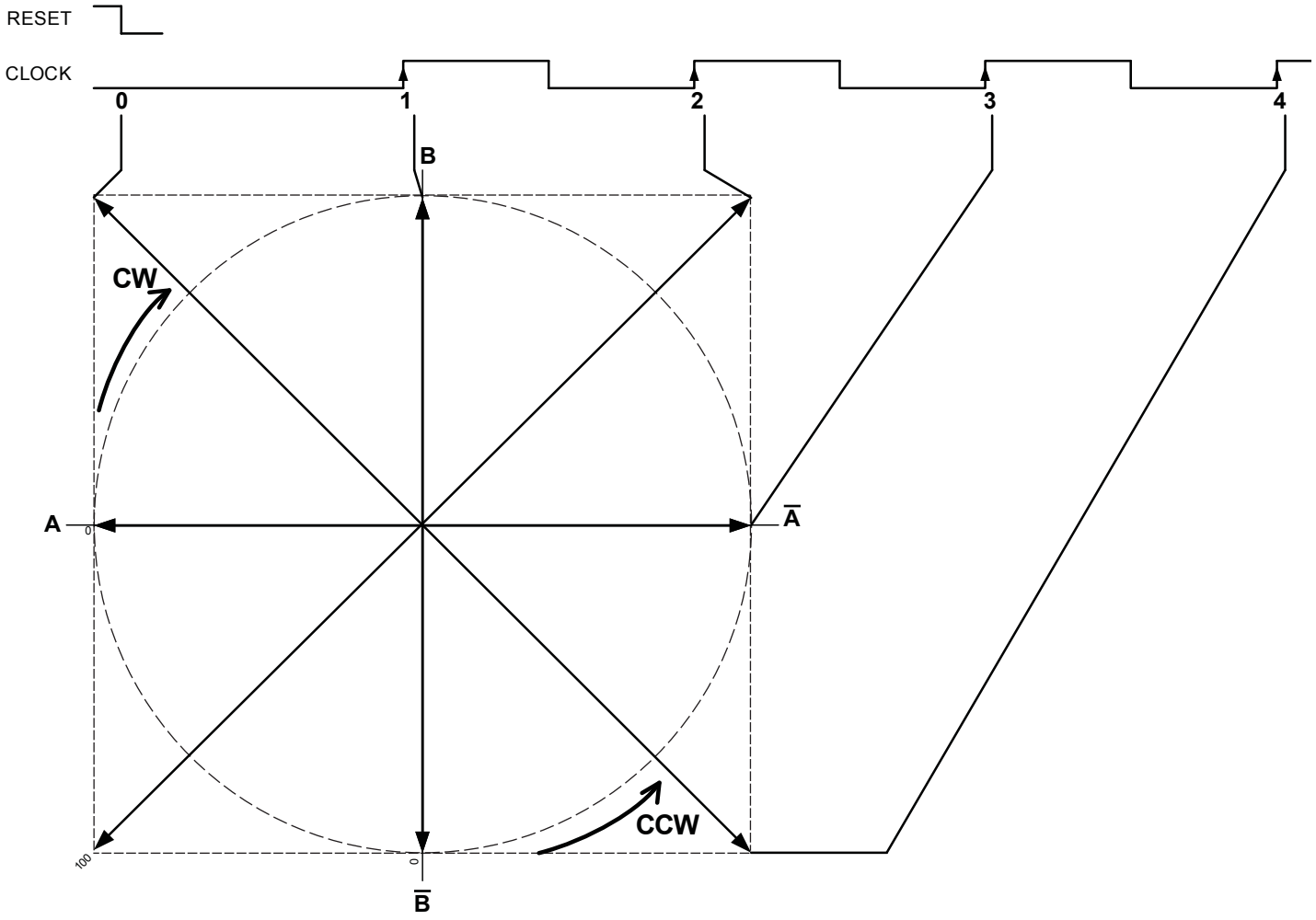


Figure 8. Half step; for microstep and full/half step products

Sequence Selection

Mode	Pin Logic		
	M1	M2	M3
Half Step F	High	High	Low

Shows the state to which the stepping sequence progresses at the rising (positive) edge of the Clock input.

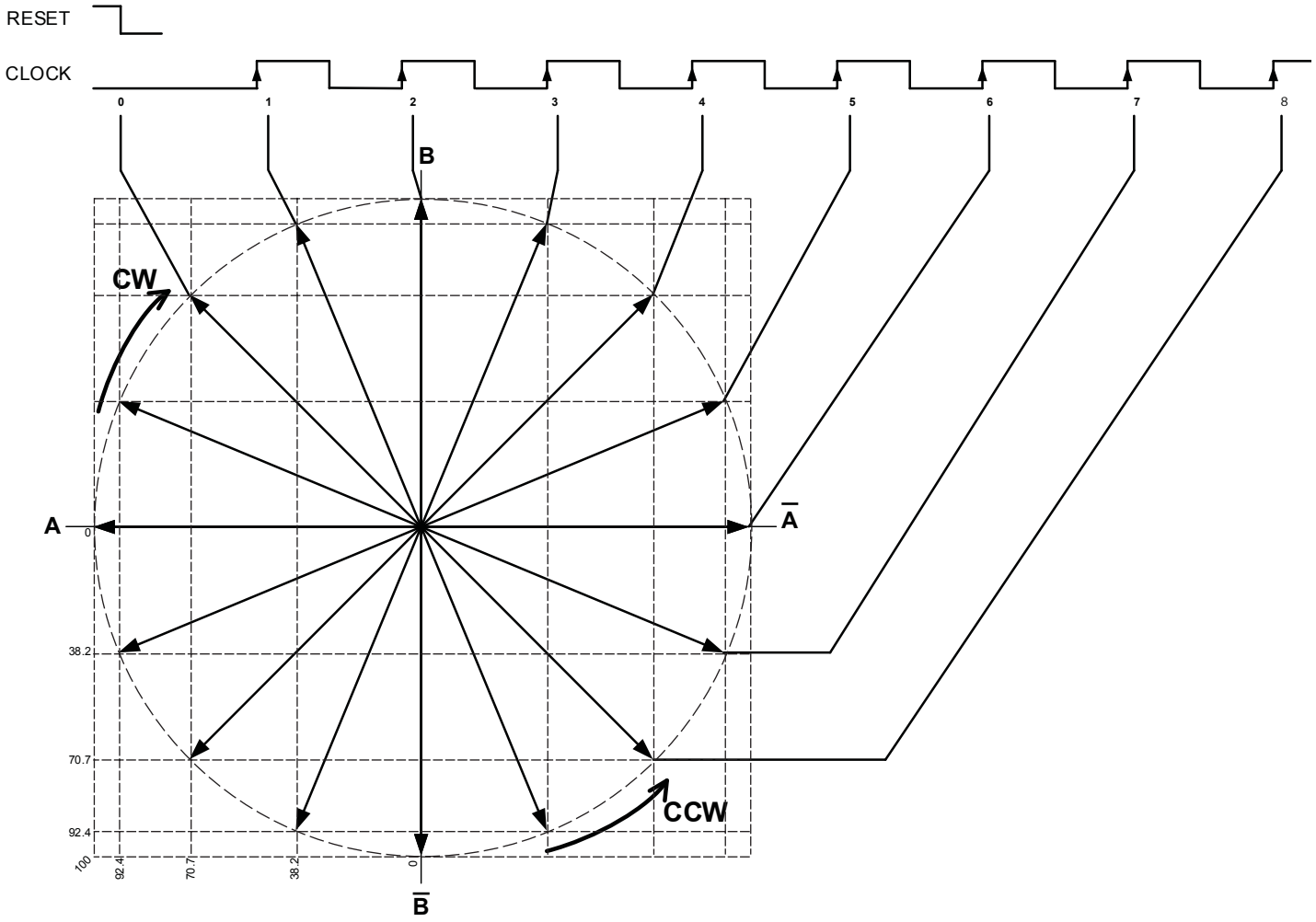


Figure 9. Quarter step; for microstep products

Sequence Selection

Mode	Pin Logic		
	M1	M2	M3
Quarter Step	Low	Low	High

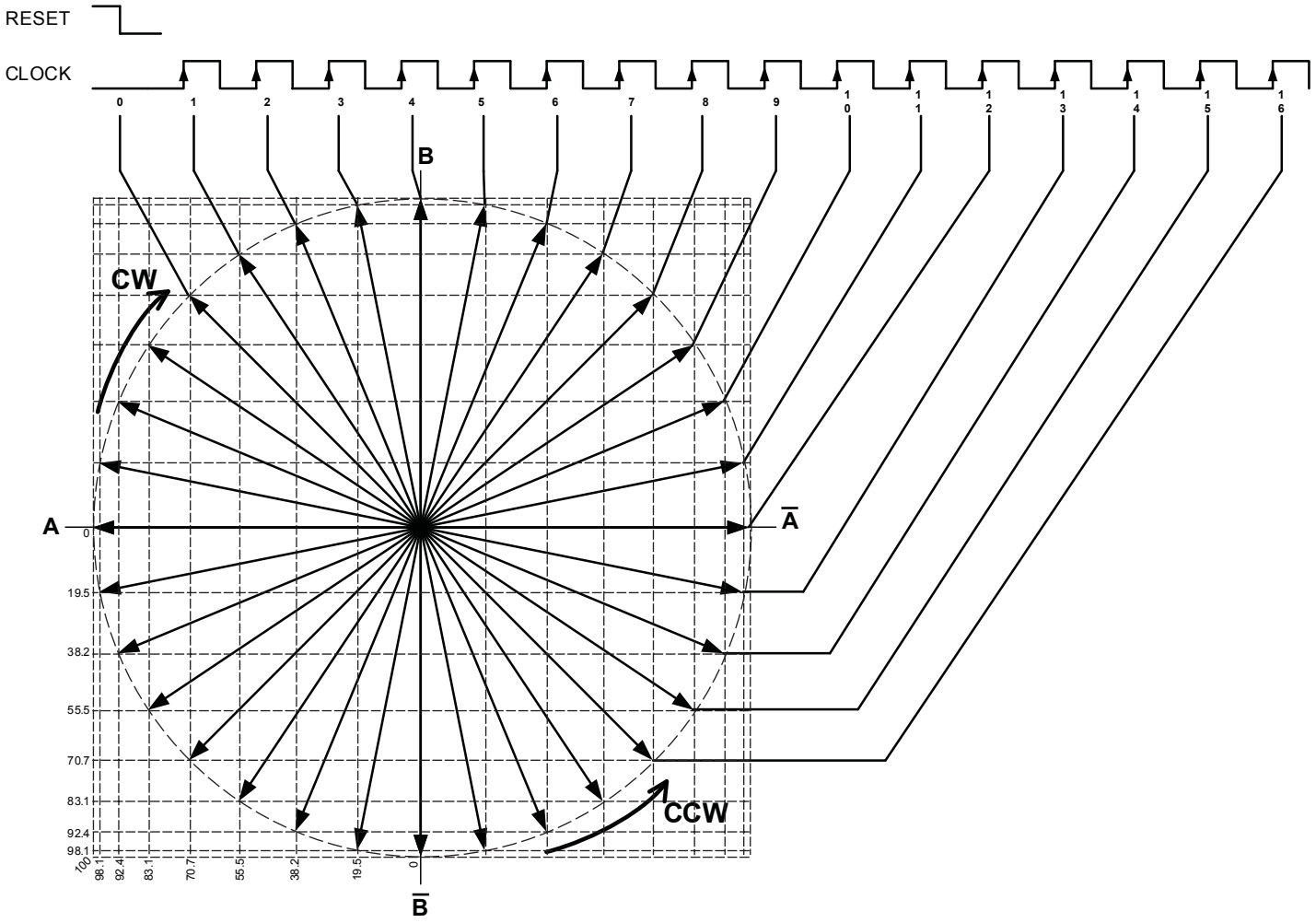


Figure 10. Eighth step; for microstep products

Sequence Selection

Mode	Pin Logic		
	M1	M2	M3
Eighth Step	High	Low	High

Shows the state to which the stepping sequence progresses at the rising (positive) edge of the Clock input.

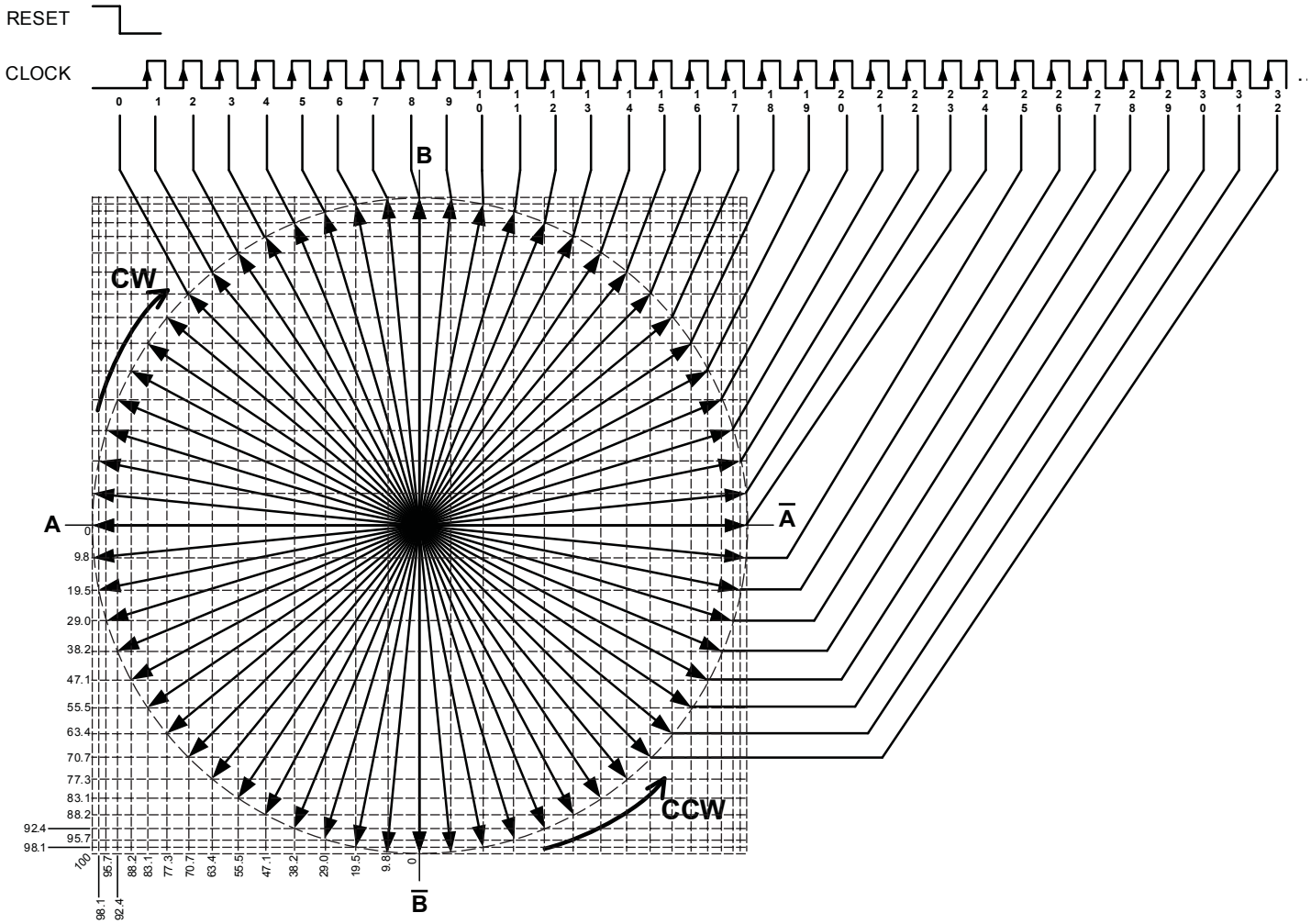


Figure 11. Sixteenth step; for microstep products

Sequence Selection

Mode	Pin Logic		
	M1	M2	M3
Sixteenth Step	Low	High	High

Shows the state to which the stepping sequence progresses at the rising (positive) edge of the Clock input.

Excitation Change Sequence

The change of excitation modes is determined by the settings of the excitation pins (M1, M2, and M3) before and after the step signal.Table 4 shows each excitation mode state setting.

Table 4. Excitation Mode States

Direction	Internal Sequence State				Step Sequencing						
	Phase A		Phase B		Full Step		Half Step		1/4 Step	1/8 Step	1/16 Step
	PWM	Mode	PWM	Mode	Mode 8	Mode F	Mode 8, F	Mode F			
Counter Clockwise	A	8	B	8	X	X*	X	X*	X	X	X
	A	7	B	9							X
	A	6	B	A						X	X
	A	5	B	B							X
	A	4	B	C					X	X	X
	A	3	B	D							X
	A	2	B	E						X	X
	A	1	B	F							X
	–	–	B	F			X	X	X	X	X
	$\overline{A}$	1	B	F							X
	$\overline{A}$	2	B	E						X	X
	$\overline{A}$	3	B	D							X
	$\overline{A}$	4	B	C					X	X	X
	$\overline{A}$	5	B	B							X
	$\overline{A}$	6	B	A						X	X
	$\overline{A}$	7	B	9							X
	$\overline{A}$	8	B	8	X	X*	X	X*	X	X	X
	$\overline{A}$	9	B	7							X
	$\overline{A}$	A	B	6						X	X
	$\overline{A}$	B	B	5							X
	$\overline{A}$	C	B	4					X	X	X
	$\overline{A}$	D	B	3							X
	$\overline{A}$	E	B	2						X	X
	$\overline{A}$	F	B	1							X
	$\overline{A}$	F	–	–			X	X	X	X	X
	$\overline{A}$	F	$\overline{B}$	1							X
	$\overline{A}$	E	$\overline{B}$	2						X	X
	$\overline{A}$	D	$\overline{B}$	3							X
	$\overline{A}$	C	$\overline{B}$	4					X	X	X
	$\overline{A}$	B	$\overline{B}$	5							X
	$\overline{A}$	A	$\overline{B}$	6						X	X
	$\overline{A}$	9	$\overline{B}$	7							X
	$\overline{A}$	8	$\overline{B}$	8	X	X*	X	X*	X	X	X
	$\overline{A}$	7	$\overline{B}$	9							X
	$\overline{A}$	6	$\overline{B}$	A						X	X
	$\overline{A}$	5	$\overline{B}$	B							X
	$\overline{A}$	4	$\overline{B}$	C					X	X	X
	$\overline{A}$	3	$\overline{B}$	D							X
	$\overline{A}$	2	$\overline{B}$	E						X	X
	$\overline{A}$	1	$\overline{B}$	F							X
	–	–	$\overline{B}$	F			X	X	X	X	X
	A	1	$\overline{B}$	F							X
	A	2	$\overline{B}$	E						X	X
	A	3	$\overline{B}$	D							X
	A	4	$\overline{B}$	C					X	X	X
	A	5	$\overline{B}$	B							X
	A	6	$\overline{B}$	A						X	X
	A	7	$\overline{B}$	9							X
	A	8	$\overline{B}$	8	X	X*	X	X*	X	X	X
	A	9	$\overline{B}$	7							X
	A	A	$\overline{B}$	6						X	X
	A	B	$\overline{B}$	5							X
	A	C	$\overline{B}$	4					X	X	X
	A	D	$\overline{B}$	3							X
	A	E	$\overline{B}$	2						X	X
	A	F	$\overline{B}$	1							X
	A	F	–	–			X	X	X	X	X
	A	F	B	1							X
	A	E	B	2						X	X
Clockwise	A	D	B	3							X
	A	C	B	4					X	X	X
	A	B	B	5							X
	A	A	B	6						X	X
	A	9	B	7							X

∗ Sequence state is Mode 8, but step reference current ratio is Mode F. Mode F has step reference current ratio of 100%, and PWM off-time of 12 µs.

Individual Circuit Descriptions

Monolithic IC (MIC)

• ***Sequencer Logic*** The single Clock input is used for step timing. Direction is controlled by the CW/CCW input. Commutation mode is controlled by the combination of the M1, M2, and M3 inputs logic levels. For details, refer to the Commutation Truth Table.

• ***PWM Control*** Each pair of outputs is controlled by a fixed off-time PWM current-control circuit. The internal oscillator (OSC) sets the off-time. Its operation mechanism is identical to that of the SLA7070M family. Refer to the PWM Current Control section for further details.

• ***Synchronous Control*** This function prevents occasional motor noise during Hold mode, which normally results from asynchronous PWM operation of both motor phases. A logic high at the Sync input sets synchronous operation. A logic low sets asynchronous operation. The use of synchronous operation during normal stepping is not recommended because it produces less motor torque and can cause motor vibration due to staircase current. The use of synchronous operation when the motor is not in operation is allowed only in full/half step sequence timing, due to the difference in the current controlled and PWM off-time at other step sequence timings.

• ***DAC (D-to-A Converter)*** In microstep sequencing, the current at each step is set by the value of a sense resistor (RSInt), a reference voltage (V_{REF}), and the output voltage of the DACs, controlled by the output of the sequencer / translator). Please refer the electric characteristic, Step Reference Current Ratio, page 8.

• ***Regulator Circuit*** The integrated regulator circuit is used in driving the output MOSFET gates and powering other internal linear circuits.

• ***Protect Circuit*** A built-in protection circuit against motor coil opens or shorts is provided. Protection is activated by sensing voltage on the internal RSInt resistors; therefore, an overcurrent condition cannot be detected which results from the the Outx pins or Sensex pins, or both, shorting to Gnd. Protection against motor coil opens is available only during PWM operation; therefore, it does not work at constant voltage driving, when the motor is rotating at high speed. Operation of the protection circuit disables all of the DMOS outputs. To come out of protection mode, cycle the logic supply, V_{DD}.

• ***TSD circuit*** This circuit protects a driver by shifting the output to Disable mode when the temperature of a product control IC (MIC) rises and becomes higher than threshold value. In order to reset, cycle the logic supply, V_{DD}.

Output MOSFET Chip

The value of the built-in output DMOS chip varies according to which of the four different output current ratings has been selected.

Sense Resistor

The resistance varies according to which of the four different output current ratings has been selected, as follows:

Output Current (A)	RSInt Resistance (Ω typ)
1	0.305
1.5	0.305
2	0.205
3	0.155

Each resistance shown above includes the inherent resistance (approximately 5 mΩ) in the resistor itself.

Functional Description

PWM Current Control

Blanking Time

The actual operating waveforms on the Sensex pins when driving a motor are shown in figure 12. The actual operating waveforms on the Sensex pins when driving a motor are shown in figure 13. Immediately after PWM turns OFF, ringing (or spike) noise on the Sensex pins isobserved for a few µs. Ringing noise can be generated by various causes, such as capacitance between motor coils and inappropriate motor wiring.

Each pair of outputs is controlled by a fixed off-time (7 to 12 µs, depending on stepping mode) PWM current-control circuit that limits the load current to a target value, I_{TRIP}. Initially, an output is enabled and current flows through the motor winding and the current-sense resistors. When the voltage across the current sense resistor equals the DAC output voltage, V_{TRIP}, the current sense comparator resets the PWM latch. This turns off the driver for the fixed off-time, during which the load inductance causes the current to recirculate for the off-time period. Therefore, if the ringing noise on the sense resistor equals and surpasses V_{TRIP}, PWM turns off.

To prevent this phenomenon, the blanking time is set to override signals from the current-sense comparator for a certain period immediately after PWM turns on.

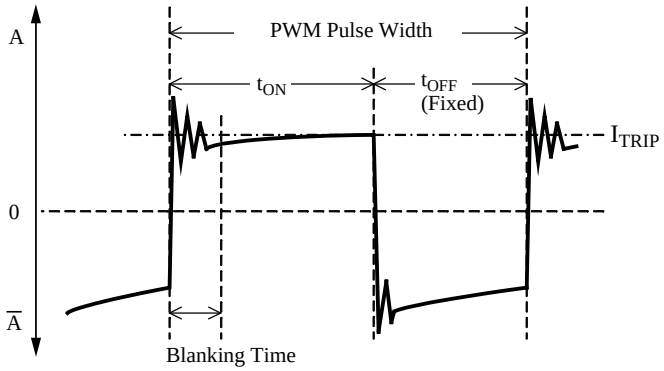


Figure 13. Sensex pin waveform during PWM control

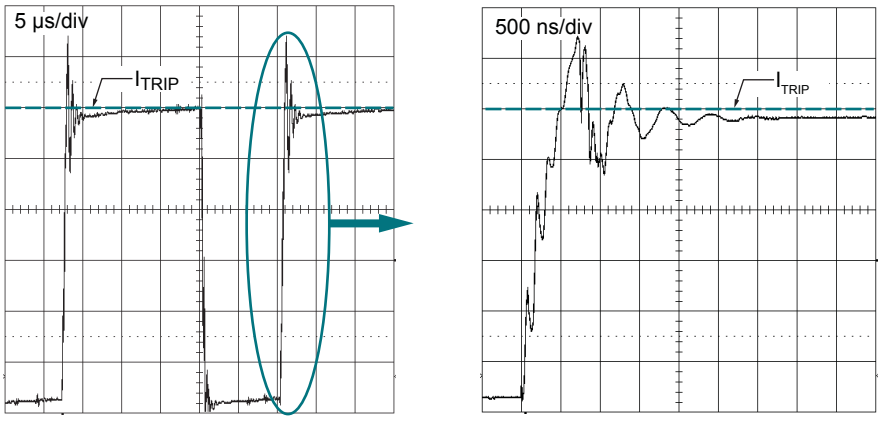


Figure 12. Operating waveforms on the Sensex pins during PWM chopping (circled area of left panel is shown in expanded scale in right panel)

• ***Blanking time and seeking phenomenon*** Although current control can be improved by shortening blanking time, the degree of margin to a ringing noise decreases simultaneously. For this reason, when a motor is driven by the device, a seeking phenomenon may occur. Figure 14 shows an example of the waveform when the phenomenon occurs.

• ***Blanking time difference*** The difference in blanking time is shown in table 5. This comparison is based on the case where drive conditions, such as a motor, motor power supply voltage, and Ref input voltage, and a circuit constant were kept the same while only the indicated parameter was changed.

▫ Minimum PWM On-time $t_{on(min)}$. The product blanking time is fixed by the PWM control. Thus, when the on-time is shortened in order to reduce the current, it would not go below the blanking time. Minimum PWM On-time refers to the time the output is on during this blanking period, that is, when the output MOSFET actually is turned on. In other words, the blanking time determines the minimum time (*small* in table 5).

▫ Minimum coil current. This refers to the coil current when PWM control is performed during PWM minimum on-time. In other words, when the coil current is reduced when the power is reduced, where blanking time is shorter can reduce current.

• ***Coil current waveform distortion during a high velocity revolution*** While a microstep drive is active, the I_{Trip} value changes with the Clock input, to the predetermined value. The I_{trip} value (internal reference voltage splitting ratio) is set up to be a sine wave. Because PWM control of the motor coil current is set according to the I_{trip} value, the coil current will be controlled to be sine wave-like. In fact, according the inductance characteristic of the coil, the device requires some time to bring the coil current completely to the targeted value.

Roughly, the relationship between the convergence time (t_{conv}) between the I_{trip} value of the coil current and the duty cycle (t_{clk}) of the input Clock pulse in any mode is:

$$t_{conv} < t_{clk} \quad (1)$$

where the coil current waveform amplitude serves as the limit for I_{trip}.

When the current attempts to increase, the full limits of t_{conv} are determined by the damping time constant of power supply voltage and the coil used. When the current attempts to decrease, the limits are determined by the power supply voltage, the damping time constant, and the minimum on-time.

When the frequency of the input clock is raised, because t_{clk} becomes small, it is normal that the case will occur in which the coil current cannot be raised to the I_{trip} value within a single clock period. In this situation, the waveform amplitude of the coil current degenerates from the sine wave, referred to as *waveform distortion*.

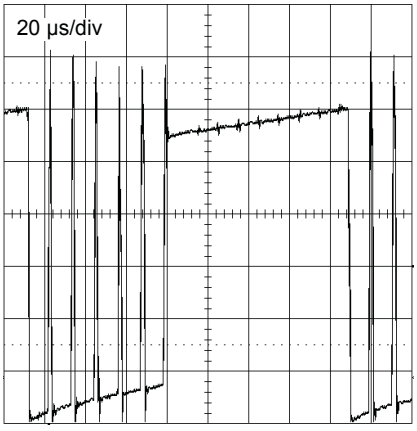


Figure 14. Example of a Sensex terminal waveform during hunching phenomenon

Table 5. Characteristic Comparison by the Difference in Blanking Time

Parameter	Better Performance		
Internal Blanking Time Setting	Short		Long
PWM minimum on-time	Short	←	
Maximize ringing noise suppression		→	Large
Minimum coil current	Small	←	
Coil current waveform distortion at a high rotation (mainly microstep)		→	Large

Figure 15 shows the compared result of the waveform distortion by observing the waveform of various devices for which the operating condition of power supply voltage, the current preset value, the motor, and so forth are kept the same. As shown in the places circled (blanking time) in the figure, while the amplitude envelope of the Sensex pin waveform, which is the same as the current waveform, in the 1.7 µs case has become sine wave-like, the blanking time in the 3.2 µs case has degenerated from an ideal sine wave.

The term *Large* in table 5 means that the wave distortion will be less where the blanking time is longer, assuming the same drive conditions, while the wave distortion will be larger where the blanking time is shorter, if the Clock frequency is the same. In addition, when such waveform distortion is confirmed, there is uncertainty if the motor characteristic will be affected. Therefore, please make a final judgment after evaluating very thoroughly.

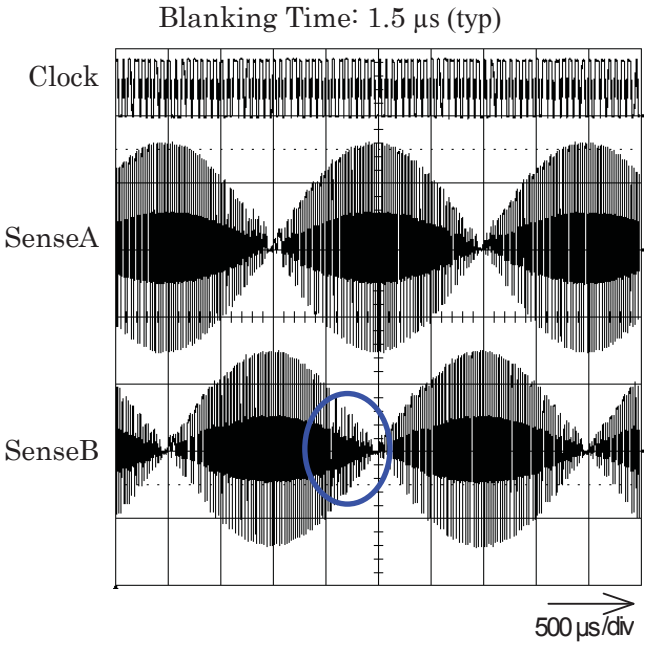


Figure 15. Comparison of a Sense terminal waveform during high speed revolution

PWM Off-Time

The PWM off-time for the SLA7070MPRT series is controlled at a fixed time by an internal oscillator. It also is switched in three levels by current proportion (see the Electrical Characteristics table). In addition, the SLA7070MPRT series provides a function that decreases losses occurring when the PWM turns off. This function dissipates back EMF stored in the motor coil at MOSFET turn-on, as well as at PWM turn-on (synchronous rectification operation).

Figure 16 shows the difference in back EMF generation between the SLA7060M series and SLA7070MPRT series. The SLA7060M series performs on–off operations using only the MOSFET on the PWM-on side, but the SLA7070MPRT series also performs on–off operations using only the MOSFET on the PWM-off side. To prevent simultaneous switching of the MOSFETs at synchronous rectification operation, the IC has a dead time of approximately 0.5 µs. During dead time, the back EMF flows through the body diode of the MOSFET.

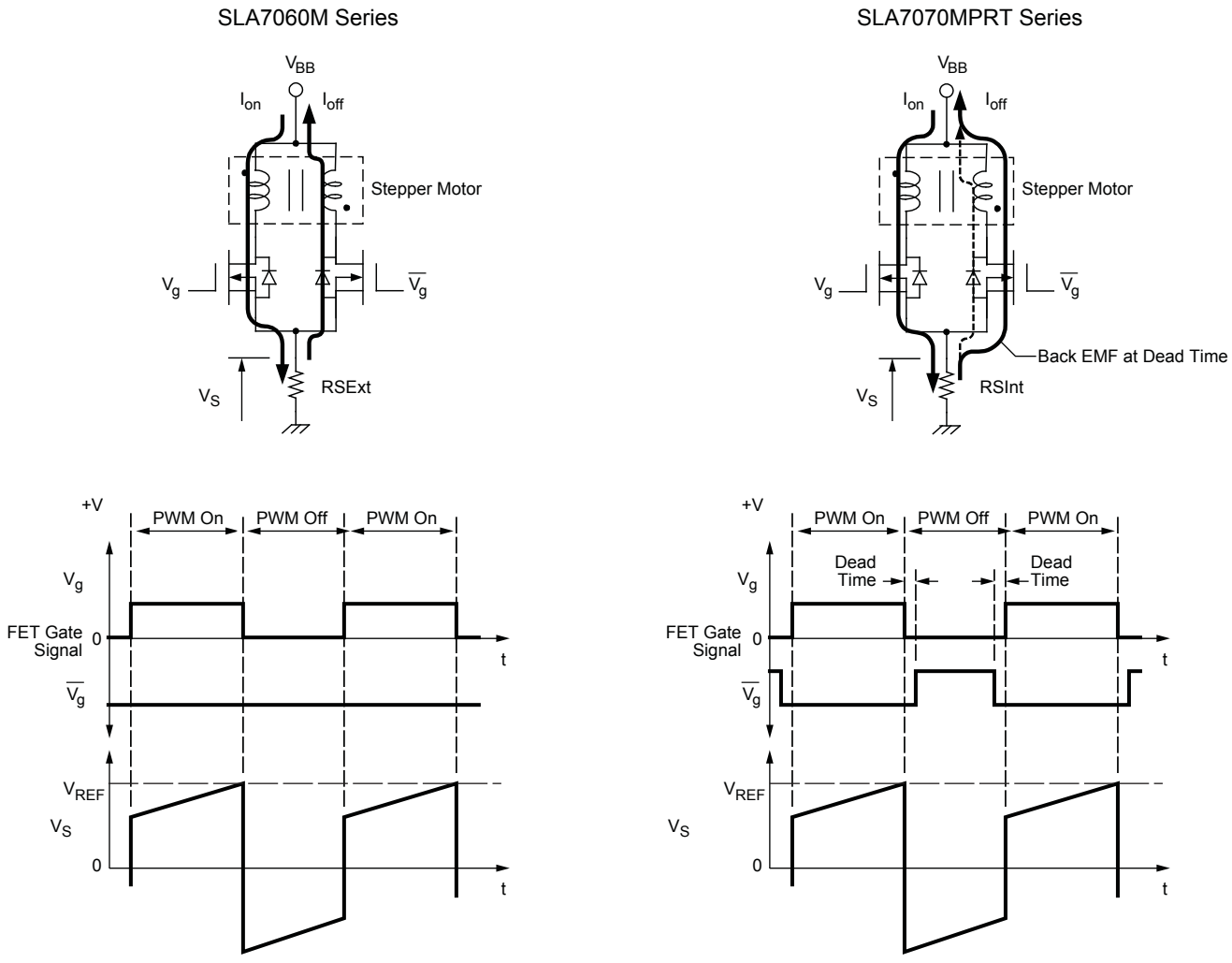


Figure 16. Synchronous rectification operation

Protection Functions

The SLA7070MPRT series includes a motor coil short-circuit protection circuit, a motor coil open protection circuit, and an overheating protection circuit. An explanation of each protection circuit is provided below.

• ***Motor Coil Short-Circuit Protection (Load Short) Circuit***. This protection circuit, embedded in the SLA7070MPRT series, begins to operate when the device detects an increase in the sense resistor voltage level, V_{RS}. The voltage at which motor coil short-circuit protection starts its operation, V_{OCP}, is set at approximately 0.7 V. The output is disabled at the time the protection circuit starts, where V_{RS} exceeds V_{OCP}. (See figure 17.)

• ***Motor Coil Open Protection*** (Patent acquired) Driver destruction can occur when one output pin (motor coil) is disconnected in a unipolar drive during operation. This is because a MOSFET connected after disconnection will be in the avalanche breakdown state, where very high energy is added with back EMF when PWM is off. With an avalanche state, an output cancels the energy stored in the motor coil where the resisting pressure between the drain and source of the MOSFET is reached (the condition which caused the breakdown).

Although MOSFETs with a certain amount of avalanche energy tolerance rating are used in the SLA7070MPRT series, avalanche energy tolerance falls as temperature increases.

Because high energy is added repeatedly whenever PWM operation disconnects the MOSFET, the temperature of the MOSFET rises, and when the applied energy exceeds the tolerance, the driver will be destroyed. Therefore, a circuit which detects this avalanche state and protects the driver was added in the SLA7070MPRT series. The operation is shown in figure 18.

As explained above, when the motor coil is disconnected, the accumulated voltage in the MOSFET causes a reverse current to flow during the PWM off-time. For this reason, V_{RS} that is negative during the PWM off-time in a normal operation becomes positive when the motor coil is disconnected. Thus, a disconnected motor is detectable by sensing that V_{RS} in the PWM off-time is positive.

In the SLA7070MPRT series, in order to avoid detection malfunctions, when a state of motor disconnection is detected 3 times continuously, the protection functions are enabled (figure 19).

Note: When the breakdown of an output is confirmed by the occurrence of surge noise after PWM turn-off, when a breakdown condition continues after an overload disconnection undetected time (t_{opp}) has elapsed, even if the load is not actually disconnected, a protection feature may operate. Please review the placement of the motor, wiring, and so forth to improve and to settle the breakdown time within the load disconnection undetected time (t_{opp}) (application variations also must be taken into consideration). When the breakdown is not confirmed, there will be no issue in operation. Moreover, the device may be made to operate normally by inserting a capacitor for surge noise suppression between the Out and Gnd pins as one possible corrective strategy.

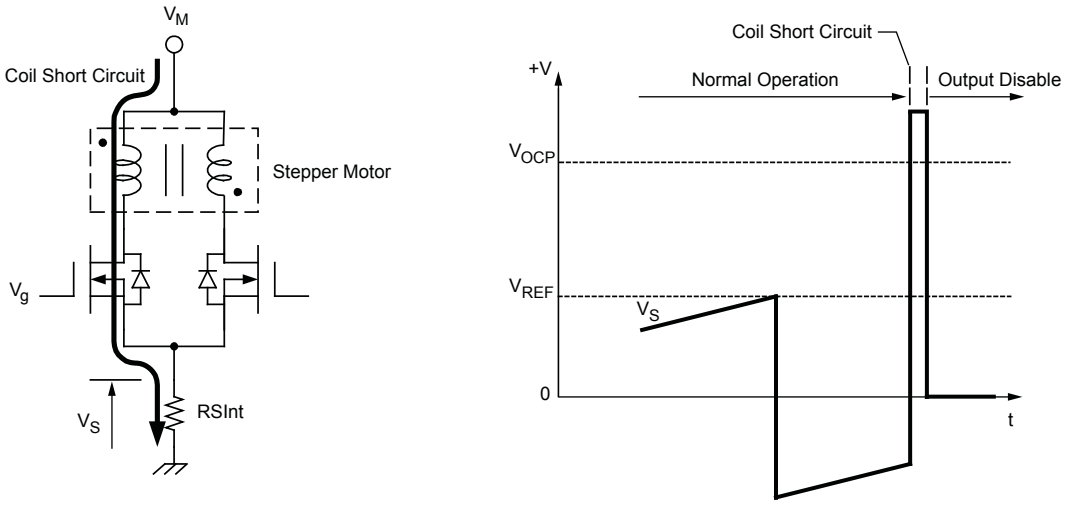


Figure 17. Motor coil short circuit protection circuit operation. Overcurrent that flows without passing the sense resistor is undetectable. To recover the circuit after protection operates, VDD must be cycled and started up again.

When the product temperature rises and exceeds T_{tsdk}, the protection circuit starts operating and all the outputs are set to Disable mode.

Note: This product has multichip composition (one IC for control, four MOSFETs, and two chip resistors). Although the location which actually detects temperature is the control IC (MIC), because the main heat sources are the MOSFET chips and the chip resistors, which are separated by a distance from the control IC, some delay will occur while the heat propagates to the control IC. For this reason, because a rapid temperature change cannot be detected, please perform worst-case thermal evaluations in the application design phase.

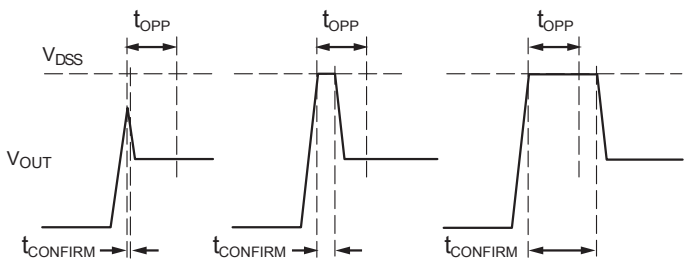


Figure 19. Coil Open Protection (Patent acquired)

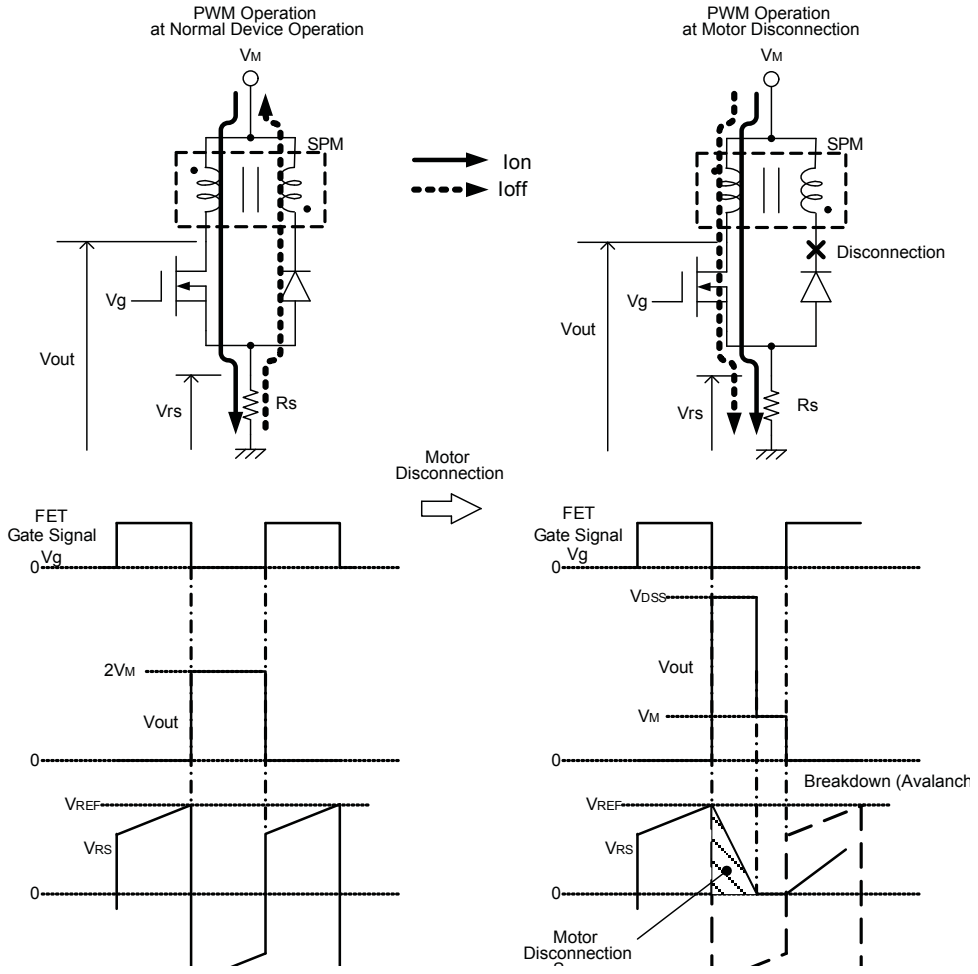


Figure 18. Motor coil short circuit protection circuit operation. Overcurrent that flows without passing the sense resistor is undetectable. To recover the circuit after protection operates, VDD must be cycled and started up again.

Application Information

Motor Current Ratio Setting (R1, R2, RS)

The setting calculation of motor current, I_{OUT}, for the SLA7070MPRT series is determined by the ratios of the external components R1, R2, and current sense resistor, RS. The following is a formula for calculating I_{OUT}:

$$I_{OUT} = \frac{R_2}{R_1 + R_2} \times V_{DD} / R_S \quad (2)$$

when V_{REF} is within specification. If V_{REF} is set less than 0.1 V, variation or impedance of the wiring pattern may influence the IC and the possibility of less accurate current sensing becomes high.

The standard voltage for current I_{Trip} that the SLA7070MPRT series controls is partially divided by the internal DAC:

$$I_{Trip} = \frac{V_{REF}}{R_S} \times \text{Mode Proportion} \quad (3)$$

Lower Limit of Control Current

The SLA7070MPRT series uses a self-oscillating PWM current control topology in which the off - time is fixed. As energy stored in motor coil is eliminated within the fixed PWM of -time, coil current flows intermittently, as shown in figure 20. Thus, average current decreases and motor torque also decreases.

The point at which current starts flowing to the coil is considered as the lower limit of the control current, $I_{OUT}(min)$, where I_{OUT} is the target current level. The lower limit of control current differs by conditions of the motor or other factors, but it is calculated from the following formula:

$$I_{O(min)} = \frac{V_M}{R}\left[\frac{1}{\exp\left(\frac{-t_{OFF}}{t_c}\right)} - 1\right] \quad (4)$$

where

V_M is the motor supply voltage,

$R_{DS(on)}$ is the MOSFET on-resistance,

I_O is the target current level,

R_m is the motor winding resistance,

L_m is the motor winding inductance,

t_{OFF} is the PWM of -time, and

t_C is calculated as:

$$t_c = L_m / R \ , \quad (5)$$

where

$$R = R_m + R_{DS(on)} + R_S \quad (6)$$

Even if the control cur ent value is set at less than the lower limit of the control current, there is no setting at which the IC fails to operate. However, control current will worsen against setting current.

Avalanche Energy

In the unipolar topology of the SLA7070MPRT series, a surge voltage (ringing noise) that exceeds the MOSFET capacity to withstand might be applied to the IC. To prevent damage, the SLA7070MPRT series is designed with a built-in MOSFET having sufficient avalanche resistance to withstand this surge voltage. Therefore, even if surge voltages occur, users will be able to use the IC without any problems. However, in cases in which the motor harness is long or the IC is used above its rated current or voltage, there is a possibility that an avalanche energy could be applied that exceeds Sanken design expectations. Thus, users must test the avalanche energy applied to the IC under actual application conditions.

The following procedure can be used to check the avalanche energy in an application.

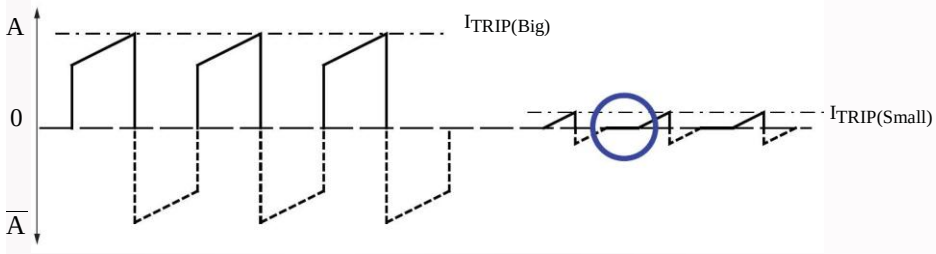


Figure 20. Control current lower limit model waveform

Given:

From the waveform test result (reference figure 22)

$V_{DS(AV)}$ = 140 V,

I_D = 1 A, and

t = 0.5 µs.

The avalanche energy, E_{AV} can be calculated using the following:

$$E_{AV} = V_{DS(AV)} \times {}^1/_2 \times I_D \times t \quad (7)$$

$$= 140\ (V) \times {}^1/_2 \times 1\ (A) \times 0.5 \times 10^{-6}\ (\mu s)$$

$$= 0.035\ (mJ)$$

By comparing the E_{AV} calculated with the graph shown in figure 23, the application can be evaluated if it is safe for the IC, by being within the avalanche energy-tolerated does range of the MOSFET.

On-Off Sequence of Power Supply (VBB and VDD)

There is no restriction of the on-off sequence between the main power supply, VBB, and the logic supply, VDD.

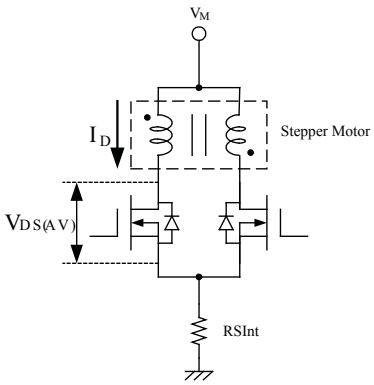


Figure 21. Test points

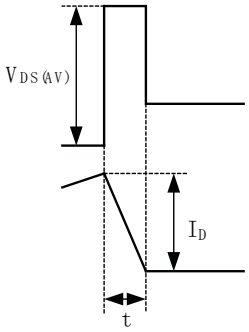


Figure 22. Waveform at avalanche breakdown

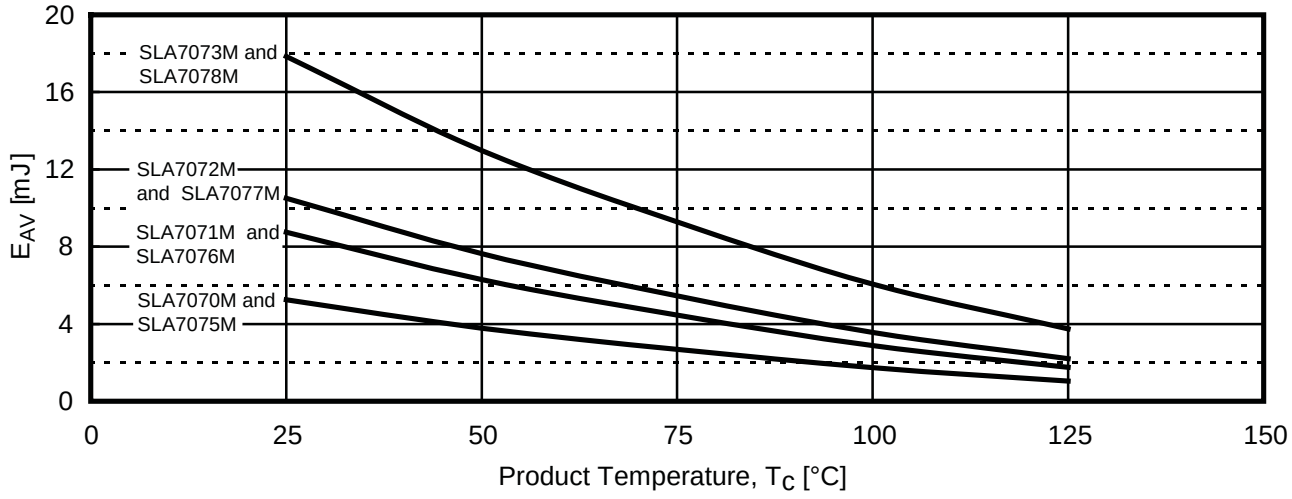


Figure 23. SLA7070MPRT iterated avalanche energy tolerated level, E_{AV}(max)

Motor Supply Voltage (V_M) and Main Power Supply Voltage (V_{BB})

Because the SLA7070MPRT series has a structure that separates the control IC (MIC) and the power MOSFETs as shown in the Functional Block diagrams, the motor supply and main power supply are separated. Therefore, it is possible to drive the IC using different power supplies and different voltages for motor supply and main power supply. However, extra caution is required because the supply voltage ranges differ among power supplies.

Internal Logic Circuits

Reset

The sequencer/translator circuit of this product is initialized after logic supply (VDD) is applied, and the power-on reset function operates. To initialize the sequencer/translator, the output immediately after power-on indicates the status that the power circuits are in the home state. In a case where the sequencer/translator must be reset after the motor has been operating, a reset signal must be input on the Reset pin. In a case in which external reset control is not necessary, and the Reset pin is not used, the Reset pin must be pulled to logic low on the application circuit board.

Clock Input

When the Clock input signal stops, excitation changes to the motor Hold state. At this time, there is no difference to the IC if the Clock input signal is at the low level or the high level. The SLA7070MPRT series is designed to move one sequence increment at a time, according to the current stepping mode, when a positive Clock pulse edge is detected.

Chopping Synchronous Circuit

The SLA7070MPRT series has a chopping synchronous function to protect from abnormal noises that may occasionally occur during the motor Hold state. This function can be operated by setting the Sync pin at high level. However, if this function is used during motor rotation, control current does not stabilize, and therefore this may cause reduction of motor torque or increased vibration. So, Sanken does not recommend using this function while the motor is rotating. In addition, the synchronous circuit should be disabled in order to control motor current properly in case it is used other than in dual excitation state (Modes 8 and F) or single excitation Hold state.

In normal operation, generally the input signal for switching can be sent from an external microcomputer. However, in applications where the input signal cannot be transmitted adequately due to limitations of the port, the following method can be taken to use the functions.

The schematic diagram in figure 24 shows how the IC is designed so that the Sync signal can be determined by the Clock input signal. When a logic high signal is received on the Clock pin, the internal capacitor, C, is charged, and the Sync signal is set to logic low level. However, if the Clock signal cannot rise above logic low level (such as when the circuit between the microcomputer and the IC is not adequate), the capacitor is discharged by the internal resistor, R, and the Sync signal is set to logic high, causing the IC to shift to synchronous mode.

The RC time constant in the circuit should be determined by the minimum clock frequency used. In the case of a sequence that keeps the Clock input signal at logic high, an inverter circuit must be added. In a case where the Clock signal is set at an undetermined level, an edge detection circuit (figure 25) can be used to prepare the signal for the Clock input, allowing correct processing by the circuit shown in figure 24.

Output Disable (Sleep1 and Sleep2) Circuits

There are two methods to set this IC at motor free-state (coast, with outputs disabled). One is to set the Ref/Sleep1 pin to more than 2 V (Sleep1), and the other (Sleep2) is to set the excitation signals (pins M1, M2, and M3). In either way, the IC will change to Sleep mode, stopping the main power supply at the same time, and decreasing circuit current. The difference between the two methods is that, in the first way, the internal sequencer remains in an enabled state, and in the latter method, the IC enters the

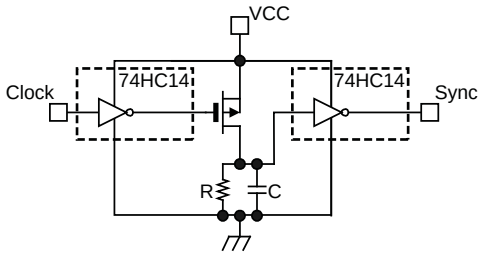


Figure 24. Clock signal shutoff detection circuit

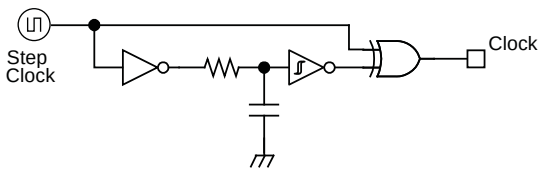


Figure 25. Clock signal edge detection circuit

Hold state. Moreover, in the method using the excitation signals (Sleep2), excitation timing remains in a standby state, even if a signal is input on the Clock pin during Sleep mode.

When awaking to normal operating mode (motor rotation) from Disable (Sleep1 or Sleep2) mode, set an appropriate delay time from cancellation of the Disable mode to the initial Clock input edge. In doing so, consider not only the rise time for the IC, but also the rise time for the motor excitation current, which is important (see figure 26).

Ref/Sleep1 Pin

The Ref/Sleep1 pin provides access to the following functions:

• Standard voltage setting for output current level setting

• Output Enable-Disable control input

These functions are further described in the Truth Table section, and in the discussion of output disabling, above.

Range A. In this range, control current value also varies in accordance with V_{REF}. Therefore, losses in the IC and the sense resistors must be given extra consideration.

Range B. In this range, the voltage that switches output enable and disable (Sleep mode) exists. At enable, the same cautions apply as in range A. In addition, for some cases, there are possibilities that the output status will become unstable as a result of iteration between enable and disable.

Logic Input Pins

If a logic input pin (Clock, Reset, CW/CCW, M1, M2, M3, or Sync) is not used (fixed logic level), the pin must be tied to VDD or Gnd. Please do not leave them floating, because there is possibility of undefined effects on IC performance when they are left open.

Output Pins (M_O and Flag). The M_O and Flag output pins are designed as monitor outputs, and inside of the IC is an output inverter (see figure 27). Therefore, let these pins float if they are not used.

Thermal Design Information

It is not practical to calculate the power dissipation of the SLA7070MPRT series accurately, because that would require factors that are variable during operation, such as time periods and excitation modes during motor rotation, input frequencies and sequences, and so forth. Given this situation, it is preferable to perform an approximate calculation at worst conditions. The following is a simplified formula for calculation of power dissipation:

$$P_D = I^2_{OUT} \times (R_{DS(on)} + R_S) \times 2 \quad (8)$$

where

P is the power dissipation in the IC,

I_{OUT} is the operating output current,

$R_{DS(on)}$ is the resistance of the output MOSFET, and

R_S is the current sense resistance.

Based on the PD calculated using the above formula, the expected increase in operating junction temperature, ΔT_J , of the IC can be estimated using figure 28. This result must be added to the worst case ambient temperature when operating, T_A(max). Based on the calculation, there is no problem unless T_A(max) plus ΔT_J exceeds 150°C.

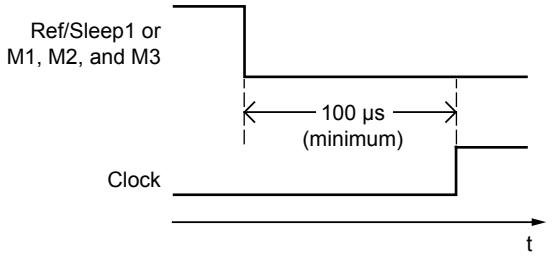


Figure 26. Timing delay between Disable mode cancellation and the next Clock input

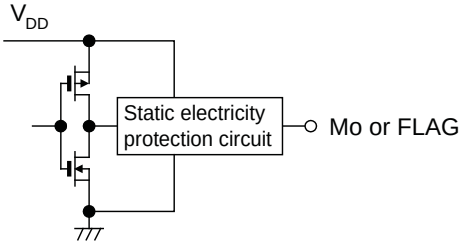


Figure 27. M_O pin and Flag pin general internal circuit layout

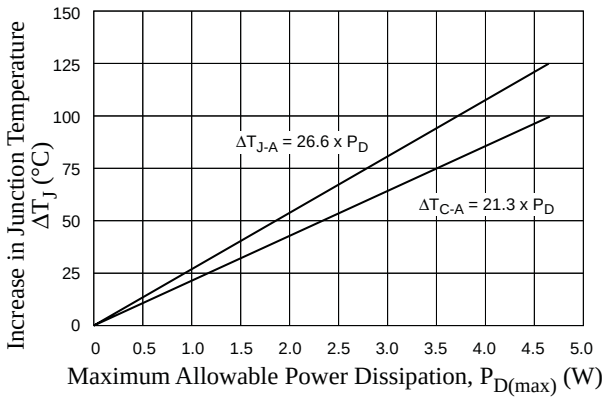


Figure 28. Temperature increase

When the IC is used with a heatsink attached, device package thermal resistance, $R_{\theta JA}$, is a variable used in calculating ΔT_{j-a}. The value of $R_{\theta FIN}$ is calculated from the following formula:

$$R_{\theta JA} \approx R_{\theta JC} + R_{\theta Fin} = R_{\theta JA} - R_{\theta CA} + R_{\theta Fin} \quad (9)$$

where $R_{\theta j-a}$ is the thermal resistance of the heatsink. ΔT_{j-a} can be calculated with using the value of $R_{\theta JA.}$

The following procedure should be used to measure product temperature and to estimate junction temperature in actual operation:

First, measure the temperature rise at pin 12 of the device (ΔT_{c-a}).

Second, estimate the loss (P) and junction temperature (T_j) from the temperature rise with reference to figure 28, temperature increase graph. At this point, the device temperature rise)(ΔT_{c-a}) and the junction temperature rise (T_j) are almost equivalent under the following formula:

$$\Delta T_J \approx \Delta T_{c-a} + P_D \times R_{\theta j-c} \quad (10)$$

CAUTION

The SLA7070MPRT series is designed as a multichip, with separate power elements (MOSFET), control IC (MIC), and sense resistance. Consequently, because the control IC cannot accurately detect the temperature of the power elements (which are the primary sources of heat), the ICs do not provide a protection function against overheating. For thermal protection, users must conduct sufficient thermal evaluations to be able to ensure that the junction temperature does not exceed the warranty level (150°C).

This thermal design information is provided for preliminary design estimations only. The thermal performance of the IC will be significantly determined by the conditions of the application, in particular the state of the mounting PCB, heatsink, and the ambient air. Before operating the IC in an application, the user must experimentally determine the actual thermal performance.

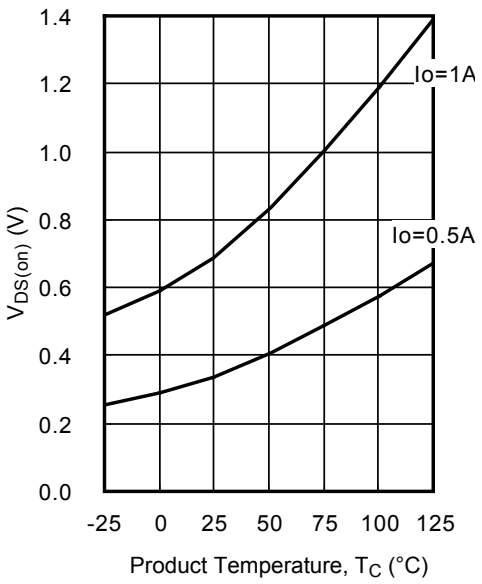
The maximum recommended case temperatures (at the center, pin 12) for the IC are:

- With no external heatsink connection: 90°C
- With external heatsink connection: 80°

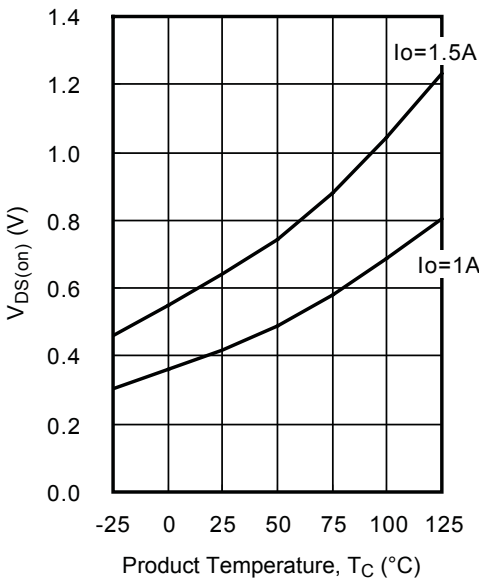
Characteristic Data

Output MOSFET On-Voltage, $V_{DS(on)}$

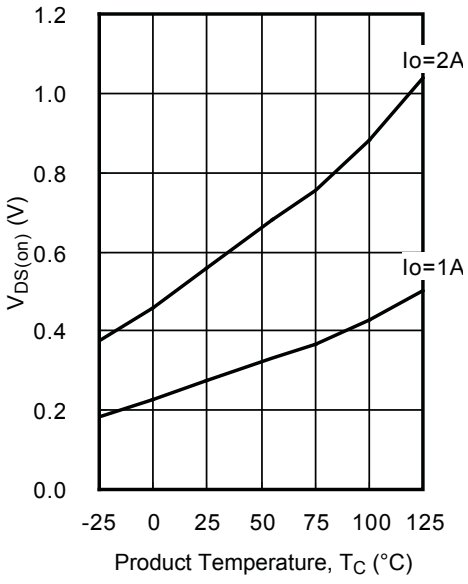
SLA7070MPRT/SLA7075MPRT



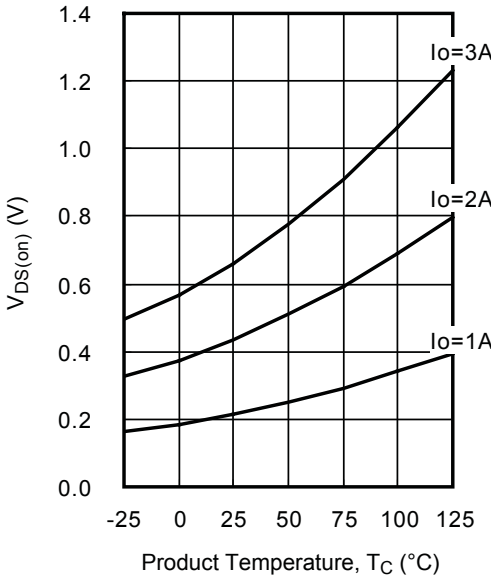
SLA7071MPRT/SLA7076MPRT



SLA7072MPRT/SLA7077MPRT

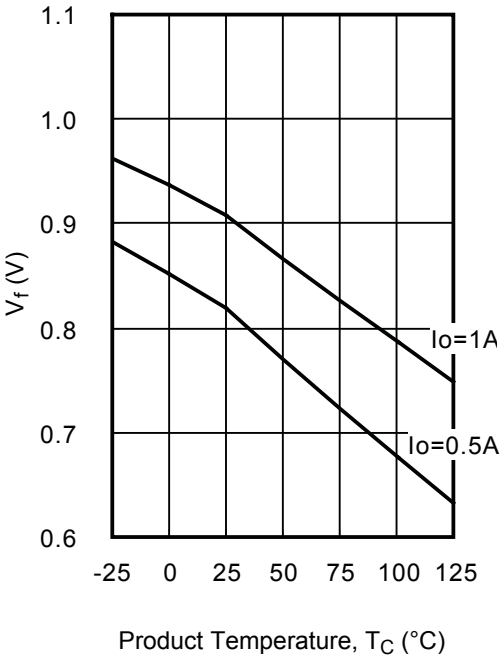


SLA7073MPRT/SLA7078MPRT

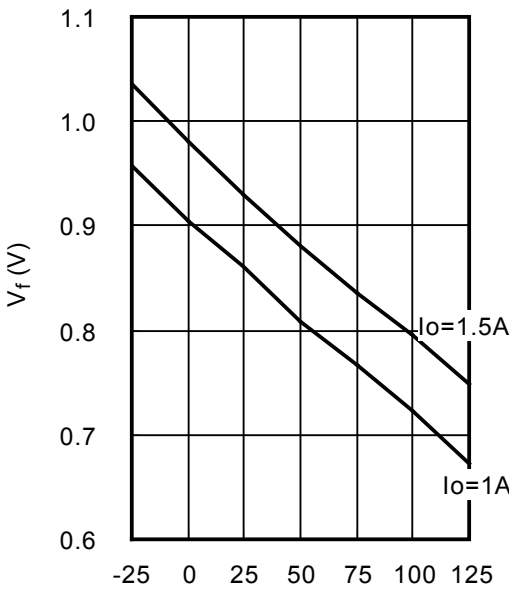


Output MOSFET Body Diode Forward Voltage, V_f

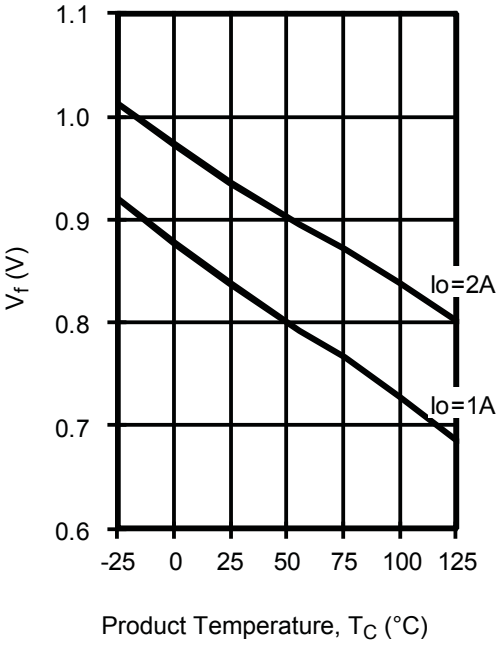
SLA7070MPRT/SLA7075MPRT



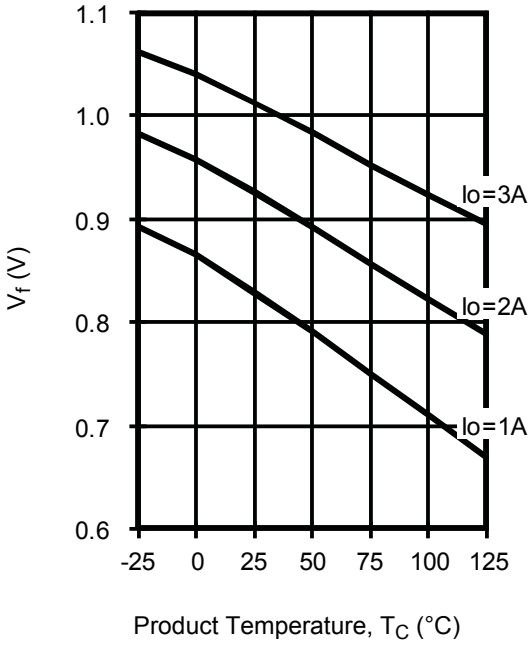
SLA7071MPRT/SLA7076MPRT



SLA7072MPRT/SLA7077MPRT



SLA7073MPRT/SLA7078MPRT



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