

150V breakdown voltage half bridge pre-driver IC SPF6001 (Auxiliary power mounted)

Features

150V breakdown voltage bootstrap circuit drive system
Charge pump circuit/ Auxiliary power mounted
Sanken original power surface mount

Absolute maximum ratings

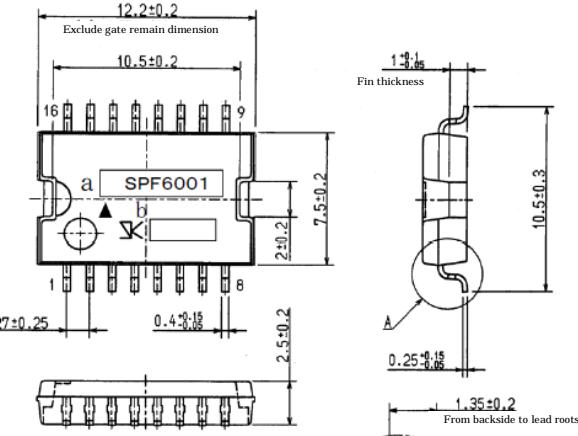
Item	Symbol	Ratings	Unit	Remark
DC input voltage	VBB	-0.6 ~ 35	V	40V T=400ms
VREG Power supply voltage for gate pin control	VREG	-0.6 ~ 18	V	
Power supply voltage for logic circuit	VDD	-0.3 ~ 6	V	
Input pin control voltage	HLO,EN	-0.3 ~ 6	V	
L/S LS pin breakdown voltage	LS	-4 ~ 4	V	
L/S GL pin breakdown voltage	GL	-4 ~ 18	V	
H/S S pin breakdown voltage	S	-4 ~ 132	V	
H/S GH pin breakdown voltage	GH	-4 ~ 150	V	
H/S C pin breakdown voltage	C	-0.3 ~ 150	V	
FLT pin breakdown voltage	VFLT	-0.3 ~ 6	V	
CPI pin breakdown voltage	CPI	-0.3 ~ 18	V	
CP2 pin breakdown voltage	CP2	-0.3 ~ 18	V	
Power dissipation	PD1	18.6	W	With infinite heat sink
	PD2	2.97	W	*1
Junction temperature	Tj	-40 ~ 150		
Operating ambient temperature	Top	-40 ~ 105		
Storage temperature	Tstg	-40 ~ 150		
Thermal resistance (Junction to Case)	θj-c	6.7	/W	
Thermal resistance (Junction to Ambient)	θj-a	42	/W	

*1 When use glass epoxy + copper foil board (Size: 5.0×7.4cm, t: glass epoxy=1.6mm, copper foil=18μm)

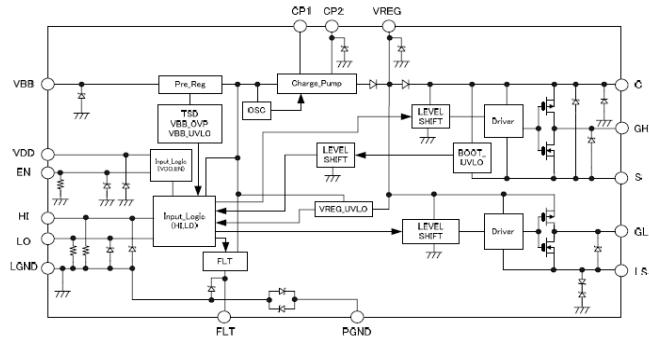
Electrical characteristics (Tj=25 °C)

Tj=30~125°C, VBB=14V,VDD=EN=5V,Creg=10pF,f PWM=22.5KHz,CP=0.1pF,CBOOT=0.1pF, unless otherwise specified						
Characteristic	Symbol	Limits			Unit	Test Conditions
		MIN	Typ	MAX		
Input power supply voltage	VBB	7	14	18	V	-
	VDD	4.5	5	5.5	V	-
VBB input current	IBB1	-	3	-	mA	VDD=EN=0V, HI=LO=0V with steady state (No load)
	IBB2	-	4	-	mA	HI=LO=0V with steady state (No load)
VDD input current	IDD	-	1.0	5.0	mA	HI=LO=0V with steady state (No load)
C,GH,S,LGND current	ICL	-	100	100	μA	C=GH=S=0V
VREG output voltage	VREG1	6	12	18	V	7V≤VBB<8V
	VREG2	12	15	18	V	8V≤VBB
EN pin · Input control voltage	VENH	2.0	-	V	-	-
	VENL	-	0.8	V	-	HI=5V, LS=S=LGND After input E, LO=0V→5V (GL monitor)
	AVEN	-	0.15	V	-	-
HI,LO pin · Input control voltage	VhH	2.0	-	V	-	-
	VhL	-	0.8	V	-	LO=5V, LS=S=LGND After input EN, HI=0V→5V (GH monitor)
	Avh	-	0.15	V	-	-
	VlH	2.0	-	V	-	-
	VlL	-	0.8	V	-	HI=5V, LS=S=LGND After input EN, HI=0V→5V (GL monitor)
EN pin · Input control current	IENH	-	100	500	μA	EN=5V
	IENL	-100	-	-	μA	EN=0V
	ihuH	-	100	500	μA	HI=5V
	ihuL	-100	-	-	μA	HI=0V
HI,LO pin · Input control current	ihH	-	100	500	μA	LO=5V
	ihL	-100	-	-	μA	LO=0V
FLT pin · Output saturation voltage	VFLT	-	-	0.4	V	IGTL=1mA
Boot Strap Di Vth	BDiVth	0.4	1.2	1.7	V	-
GH pin · Source RDS(ON) H	RDSsG_H	6	9	15	Ω	HI=5V, LO=0V, LS=S=LGND, C>10V, VREG>10V
GH pin · Sink RDS(ON) H	RDSsG_H	4	6	10	Ω	HI=5V, LO=0V, LS=S=LGND, C>10V, VREG>10V
GH pin · start-up time	t _{rGH}	10	50	100	nS	VGH=20%→80%, Ciss=3300pF
GH pin · falling time	t _{fGH}	10	50	100	nS	VGH=80%→20%, Ciss=3300pF
GL pin · Source RDS(ON) L	RDSsG_L	6	9	15	Ω	HI=0V, LO=5V, LS=S=LGND, C>10V, VREG>10V
GL pin · Sink RDS(ON) L	RDSsG_L	4	6	10	Ω	HI=0V, LO=5V, LS=S=LGND, C>10V, VREG>10V
GL pin · start-up time	t _{rGL}	10	50	100	nS	VGL=20%→80%, Ciss=3300pF
GL pin · falling time	t _{fGL}	10	50	100	nS	VGL=80%→20%, Ciss=3300pF
Output delay time	t _{onH}	150	250	420	nS	VhiH=VGH=10%, Ciss=3300pF
	t _{offH}	150	250	410	nS	VhiH=VGH=80%, Ciss=3300pF
	t _{onL}	150	250	420	nS	Viol=VGH=10%, Ciss=3300pF
	t _{offL}	150	250	410	nS	Viol=VGH=90%, Ciss=3300pF
VDD UVLO releasing voltage	VuvddH	3.5	4.0	4.5	V	(GH,GL,FLT monitor)
VDD UVLO activating voltage	VuvddL	3.3	3.8	4.3	V	(GH,GL,FLT monitor)
VDD UVLO hysteresis	ΔVuvdd	-	200	-	mV	
VBB OVP releasing voltage	VovbbH	24	28	32	V	(GH,GL,FLT monitor)
VBB OVF activating voltage	VovbbL	22	25	31	V	
VBB UVLO releasing voltage	Vurbbh	6.0	6.5	7.0	V	(GH,GL,FLT monitor)
VBB UVLO activating voltage	Vurbbl	5.5	6.1	6.6	V	(GH,GL,FLT monitor)
VBB UVLO hysteresis	ΔVurbb	-	400	-	mV	

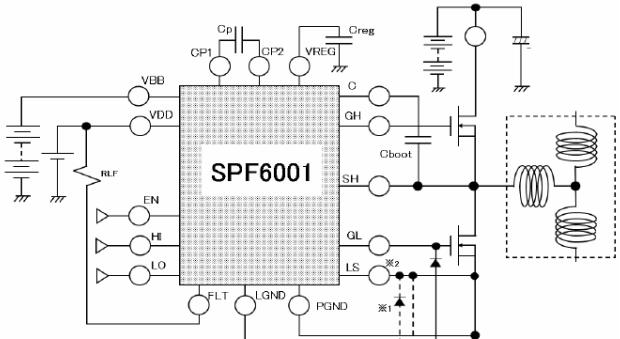
Package



Circuit block diagram



Typical connection diagram



Timing chart

