Description

The SSC3S900 series is a controller with SMZ* method for LLC current resonant switching power supplies, incorporating a floating drive circuit for a high-side power MOSFET.

The product includes useful functions such as Standby mode change, Overload Protection with input voltage compensation, Automatic Dead Time Adjustment, and Capacitive Mode Detection. The product realizes high performance-to-cost power supply system, downsized by high efficiency and low noise.

*SMZ: Soft-switched Multi-resonant Zero Current switch, achieved soft switching operation during all switching periods

Features

- Standby Mode Change Function
  - Output Power at Light Load: $P_O = 100 \text{ mW}$
    ($P_{IN} = 0.27 \text{ W}$, as a reference with discharge resistor of $1\Omega$ for across the line capacitor)
  - Burst operation in standby mode
  - Soft-on/Soft-off function: reduces audible noise
- Realizing power supply with universal mains input voltage
- Floating Drive Circuit: drives a high-side power MOSFET directly
- Soft-start Function
- Capacitive Mode Detection Function
- Reset Detection Function
- Automatic Dead Time Adjustment Function
- Built-in Startup Circuit
- Input Electrolytic Capacitor Discharge Function
- Protections
  - Brown-In and Brown-Out Function
  - High-side Driver UVLO
  - Overcurrent Protection (OCP): Peak drain current detection, 2-step detection
  - Overload Protection (OLP) with Input Voltage Compensation
  - Overvoltage Protection (OVP)
  - Thermal Shutdown (TSD)

Typical Application

Application

Switching power supplies for electronic devices such as:

- Digital appliances: LCD television and so forth
- Office automation (OA) equipment: server, multi-function printer, and so forth
- Industrial apparatus
- Communication facilities
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### 1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, $T_A$ is 25°C.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Pins</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSEN Pin Sink Current</td>
<td>$I_{SEN}$</td>
<td>1 – 10</td>
<td>1.0</td>
<td>mA</td>
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<tr>
<td>Control Part Input Voltage</td>
<td>$V_{CC}$</td>
<td>2 – 10</td>
<td>−0.3 to 35</td>
<td>V</td>
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<tr>
<td>FB Pin Voltage</td>
<td>$V_{FB}$</td>
<td>3 – 10</td>
<td>−0.3 to 6</td>
<td>V</td>
</tr>
<tr>
<td>VSPL Pin Sink Current</td>
<td>$I_{SPL}$</td>
<td>4 – 10</td>
<td>1.0</td>
<td>mA</td>
</tr>
<tr>
<td>CSS Pin Voltage</td>
<td>$V_{CSS}$</td>
<td>5 – 10</td>
<td>−0.3 to 6</td>
<td>V</td>
</tr>
<tr>
<td>CL Pin Voltage</td>
<td>$V_{CL}$</td>
<td>6 – 10</td>
<td>−0.3 to 6</td>
<td>V</td>
</tr>
<tr>
<td>RC Pin Voltage</td>
<td>$V_{RC}$</td>
<td>7 – 10</td>
<td>−6 to 6</td>
<td>V</td>
</tr>
<tr>
<td>PL Pin Voltage</td>
<td>$V_{PL}$</td>
<td>8 – 10</td>
<td>−0.3 to 6</td>
<td>V</td>
</tr>
<tr>
<td>SB Pin Sink Current</td>
<td>$I_{SB}$</td>
<td>9 – 10</td>
<td>100</td>
<td>µA</td>
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<tr>
<td>VGL pin Voltage</td>
<td>$V_{GL}$</td>
<td>11 – 10</td>
<td>−0.3 to $V_{REG} + 0.3$</td>
<td>V</td>
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<tr>
<td>REG pin Source Current</td>
<td>$I_{REG}$</td>
<td>12 – 10</td>
<td>−10.0</td>
<td>mA</td>
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<tr>
<td>Voltage Between VB Pin and VS Pin</td>
<td>$V_{B} - V_{S}$</td>
<td>14 – 15</td>
<td>−0.3 to 19.2</td>
<td>V</td>
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<td>VS Pin Voltage</td>
<td>$V_{S}$</td>
<td>15 – 10</td>
<td>−1 to 600</td>
<td>V</td>
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<td>VGH Pin Voltage</td>
<td>$V_{GH}$</td>
<td>16 – 10</td>
<td>$V_{S} - 0.3$ to $V_{B} + 0.3$</td>
<td>V</td>
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<td>ST Pin Voltage</td>
<td>$V_{ST}$</td>
<td>18 – 10</td>
<td>−0.3 to 600</td>
<td>V</td>
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<tr>
<td>Operating Ambient Temperature</td>
<td>$T_{OP}$</td>
<td>—</td>
<td>−40 to 85</td>
<td>°C</td>
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<tr>
<td>Storage Temperature</td>
<td>$T_{stg}$</td>
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<td>−40 to 125</td>
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<td>Junction Temperature</td>
<td>$T_{J}$</td>
<td>—</td>
<td>150</td>
<td>°C</td>
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* Surge voltage withstand (Human body model) of No.14, 15, 16 and 18 is guaranteed 1000V. Other pins are guaranteed 2000V.
2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, $T_A$ is 25°C, and $V_{CC}$ is 19 V.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Pins</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Notes</th>
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<tr>
<td>Start Circuit and Circuit Current</td>
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<tr>
<td>Operation Start Voltage</td>
<td>$V_{CC(ON)}$</td>
<td>2 – 10</td>
<td>12.9</td>
<td>14.0</td>
<td>15.1</td>
<td>V</td>
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<tr>
<td>Operation Stop Voltage</td>
<td>$V_{CC(OFF)}$</td>
<td>2 – 10</td>
<td>9.0</td>
<td>9.8</td>
<td>10.6</td>
<td>V</td>
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<tr>
<td>Startup Current Biasing Threshold Voltage*</td>
<td>$V_{CC(BIAS)}$</td>
<td>2 – 10</td>
<td>10.1</td>
<td>11.0</td>
<td>11.9</td>
<td>V</td>
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<tr>
<td>Circuit Current in Operation</td>
<td>$I_{CC(ON)}$</td>
<td>2 – 10</td>
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<tr>
<td>Circuit Current in Non-Operation</td>
<td>$I_{CC(OFF)}$</td>
<td>$V_{CC}=9V$</td>
<td>2 – 10</td>
<td></td>
<td>1.0</td>
<td>2.0</td>
<td>mA</td>
<td></td>
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<tr>
<td>Startup Current</td>
<td>$I_{CSS(T)}$</td>
<td>18 – 10</td>
<td>3.0</td>
<td>6.0</td>
<td>9.0</td>
<td>mA</td>
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<tr>
<td>VCC Pin Protection Circuit Release Threshold Voltage</td>
<td>$V_{CC(P.OFF)}$</td>
<td>2 – 10</td>
<td>9.0</td>
<td>9.8</td>
<td>10.6</td>
<td>V</td>
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<td>VCC Pin Latch Protection Circuit Release Threshold Voltage</td>
<td>$V_{CC(L.OFF)}$</td>
<td>2 – 10</td>
<td>6.5</td>
<td>7.8</td>
<td>9.0</td>
<td>V</td>
<td>SSC3S902</td>
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<tr>
<td>Circuit Current in Protection</td>
<td>$I_{CC(P)}$</td>
<td>$V_{CC}=11V$</td>
<td>2 – 10</td>
<td></td>
<td>1.0</td>
<td>2.0</td>
<td>mA</td>
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<td>Oscillator</td>
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<tr>
<td>Minimum Frequency</td>
<td>$I_{(MIN)}$</td>
<td>11 – 10</td>
<td>16 – 15</td>
<td>28.5</td>
<td>32.0</td>
<td>35.5</td>
<td>kHz</td>
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<tr>
<td>Maximum Frequency</td>
<td>$I_{(MAX)}$</td>
<td>11 – 10</td>
<td>16 – 15</td>
<td>230</td>
<td>300</td>
<td>380</td>
<td>kHz</td>
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<tr>
<td>Minimum Dead-Time</td>
<td>$I_{(MIN)}$</td>
<td>11 – 10</td>
<td>16 – 15</td>
<td>0.20</td>
<td>0.35</td>
<td>0.50</td>
<td>µs</td>
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<tr>
<td>Maximum Dead-Time</td>
<td>$I_{(MAX)}$</td>
<td>11 – 10</td>
<td>16 – 15</td>
<td>1.20</td>
<td>1.65</td>
<td>2.10</td>
<td>µs</td>
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<tr>
<td>Externally Adjusted Minimum Frequency</td>
<td>$I_{(MIN)ADJ}$</td>
<td>R$_{CSS}=30kΩ$</td>
<td>11 – 10</td>
<td>16 – 15</td>
<td>70.0</td>
<td>74.0</td>
<td>78.0</td>
<td>kHz</td>
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<td>Feedback Control</td>
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<tr>
<td>FB Pin Oscillation Start Threshold Voltage</td>
<td>$V_{FB(ON)}$</td>
<td>3 – 10</td>
<td>0.15</td>
<td>0.30</td>
<td>0.45</td>
<td>V</td>
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<td>FB Pin Oscillation Stop Threshold Voltage</td>
<td>$V_{FB(OFF)}$</td>
<td>3 – 10</td>
<td>0.05</td>
<td>0.20</td>
<td>0.35</td>
<td>V</td>
<td></td>
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<td>FB Pin Maximum Source Current</td>
<td>$I_{FB(MAX)}$</td>
<td>$V_{FB}=0V$</td>
<td>3 – 10</td>
<td></td>
<td>−300</td>
<td>−195</td>
<td>−100</td>
<td>µA</td>
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<tr>
<td>Soft-start</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>CSS Pin Charging Current</td>
<td>$I_{CSS(C)}$</td>
<td>5 – 10</td>
<td>−120</td>
<td>−105</td>
<td>−90</td>
<td>µA</td>
<td></td>
<td></td>
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<tr>
<td>CSS Pin Reset Current</td>
<td>$I_{CSS(R)}$</td>
<td>$V_{CC}=9V$</td>
<td>5 – 10</td>
<td></td>
<td>1.2</td>
<td>1.8</td>
<td>2.4</td>
<td>mA</td>
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<tr>
<td>Maximum Frequency in Soft-start</td>
<td>$I_{(MAX)SS}$</td>
<td>11 – 10</td>
<td>16 – 15</td>
<td>400</td>
<td>500</td>
<td>600</td>
<td>kHz</td>
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<td>Standby</td>
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<tr>
<td>SB Pin Standby Threshold Voltage</td>
<td>$V_{SB(STB)}$</td>
<td>9 – 10</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SB Pin Oscillation Start Threshold Voltage</td>
<td>$V_{SB(ON)}$</td>
<td>9 – 10</td>
<td>0.5</td>
<td>0.6</td>
<td>0.7</td>
<td>V</td>
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</tbody>
</table>

(1) $V_{CC(P.OFF)} = V_{CC(OFF)} < V_{CC(BIAS)}$ always.
(2) $V_{CC(L.OFF)} < V_{CC(OFF)} < V_{CC(BIAS)}$ always.
### SSC3S900 Series

#### Characteristic Symbol Conditions Pins Min. Typ. Max. Unit Notes

| SB Pin Oscillation Stop Threshold Voltage | V_{SB(OFF)} | 9 – 10 | 0.4 | 0.5 | 0.6 | V |
| SB Pin Clamp Voltage | V_{SB(CLAMP)} | 9 – 10 | 6.1 | 6.7 | 7.4 | V |
| SB Pin Source Current | I_{SB(SRC)} | 9 – 10 | −20 | −10 | −4 | µA |
| SB Pin Sink Current | I_{SB(SNK)} | 9 – 10 | 4 | 10 | 20 | µA |

#### Overload Protection (OLP) with Input Voltage Compensation

| CL Pin Threshold Voltage (1) | V_{CL1} | V_{SPL} = 1V | 6 – 10 | 4.40 | 4.69 | 4.88 | V |
| CL Pin Threshold Voltage (2) | V_{CL2} | V_{SPL} = 2V | 6 – 10 | 3.05 | 3.43 | 3.65 | V |
| CL Pin Threshold Voltage (3) | V_{CL3} | V_{SPL} = 4V | 6 – 10 | 1.60 | 1.83 | 2.05 | V |
| CL Pin Threshold Voltage (4) | V_{CL4} | V_{SPL} = 5V | 6 – 10 | 1.05 | 1.29 | 1.55 | V |
| CL Pin Source Current | I_{CL} | 6 – 10 | −29 | −17 | −5 | µA |

#### Brown-In and Brown-Out

| VSEN Pin Threshold Voltage (On) | V_{SEN(ON)} | 1 – 10 | 1.248 | 1.300 | 1.352 | V |
| VSEN Pin Threshold Voltage (Off) | V_{SEN(OFF)} | 1 – 10 | 1.070 | 1.115 | 1.160 | V |
| VSEN Pin Clamp Voltage | V_{SEN (CLAMP)} | 1 – 10 | 10.0 | — | — | V |
| VSPL Pin Clamp Voltage | V_{SPL (CLAMP)} | 4 – 10 | 10.0 | — | — | V |

#### Reset Detection

| Maximum Reset Time | t_{RST(MAX)} | 11 – 10 | 4.0 | 5.0 | 6.0 | µs |

#### Driver Circuit Power Supply

| VREG Pin Output Voltage | V_{REG} | 12 – 10 | 9.6 | 10.4 | 11.2 | V |

#### High-side Driver

| High-side Driver Operation Start Voltage | V_{BUV(ON)} | 14 – 15 | 6.3 | 7.3 | 8.3 | V |
| High-side Driver Operation Stop Voltage | V_{BUV(OFF)} | 14 – 15 | 5.5 | 6.4 | 7.2 | V |

#### Driver Circuit

| VGL, VGH Pin Source Current 1 | I_{GL(SRC1)} | I_{GH(SRC1)} | V_{REG} = 10.5V | V_{B} = 10.5V | V_{CL} = 0V | V_{GH} = 0V | 11 – 10 | 16 – 15 | — | 540 | — | A |
| VGL, VGH Pin Source Current 2 | I_{GL(SRC2)} | I_{GH(SRC2)} | V_{REG} = 12V | V_{B} = 12V | V_{CL} = 1.5V | V_{GH} = 1.5V | 11 – 10 | 16 – 15 | — | 140 | −90 | −40 | mA |
| VGL, VGH Pin Sink Current 1 | I_{GL(SNK1)} | I_{GH(SNK1)} | V_{REG} = 10.5V | V_{B} = 10.5V | V_{CL} = 0V | V_{GH} = 0V | 11 – 10 | 16 – 15 | — | 1.50 | — | A |
| VGL, VGH Pin Sink Current 2 | I_{GL(SNK2)} | I_{GH(SNK2)} | V_{REG} = 12V | V_{B} = 12V | V_{CL} = 1.5V | V_{GH} = 1.5V | 11 – 10 | 16 – 15 | — | 140 | 250 | 360 | mA |

#### Current Resonant and Overcurrent Protection (OCP)

| Capacitive Mode Detection Voltage 1 | V_{RC1} | 7 – 10 | 0.02 | 0.10 | 0.18 | V |
| — | — | — | −0.18 | −0.10 | −0.02 | V |
## SSC3S900 Series

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Pins</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Notes</th>
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<td>Capacitive Mode Detection Voltage 2</td>
<td>$V_{RC2}$</td>
<td>5 – 10</td>
<td>0.35</td>
<td>0.50</td>
<td>0.65</td>
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<td></td>
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<td>−0.65</td>
<td>−0.50</td>
<td>−0.35</td>
<td>V</td>
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<tr>
<td>RC Pin Threshold Voltage (Low)</td>
<td>$V_{RC(L)}$</td>
<td>7 – 10</td>
<td>1.42</td>
<td>1.50</td>
<td>1.58</td>
<td>V</td>
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<td>V</td>
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<tr>
<td>RC Pin Threshold Voltage (High speed)</td>
<td>$V_{RC(S)}$</td>
<td>7 – 10</td>
<td>2.15</td>
<td>2.30</td>
<td>2.45</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>−2.45</td>
<td>−2.30</td>
<td>−2.15</td>
<td>V</td>
<td></td>
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</tr>
<tr>
<td>CSS Pin Sink Current (Low)</td>
<td>$I_{CSS(L)}$</td>
<td>5 – 10</td>
<td>1.2</td>
<td>1.8</td>
<td>2.4</td>
<td>mA</td>
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<tr>
<td>CSS Pin Sink Current (High speed)</td>
<td>$I_{CSS(S)}$</td>
<td>5 – 10</td>
<td>13.0</td>
<td>20.5</td>
<td>28.0</td>
<td>mA</td>
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**Overvoltage Protection (OVP)**

| VCC Pin OVP Threshold Voltage                       | $V_{CC(OVP)}$ | 2 – 10     | 29.5  | 32.0  | 34.5  | V     |      |       |

**Thermal Shutdown (TSD)**

| Thermal Shutdown Temperature                        | $T_{j(TSD)}$ | —         | 140   | —     | —     | °C    |      |       |

**Thermal Resistance**

| Junction to Ambient Thermal Resistance               | $\theta_{j-A}$ | —         | —     | —     | —     | 95 °C/W |      |       |
3. Block Diagram

![Block Diagram]

4. Pin Configuration Definitions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Name</th>
<th>Function</th>
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<tbody>
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<td>1</td>
<td>VSEN</td>
<td>ST</td>
<td>18</td>
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<tr>
<td>2</td>
<td>VCC</td>
<td>VCC</td>
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</table>
5. Typical Application
6. Physical Dimensions

- SOP18

NOTES:
- Dimension is in millimeters
- Pb-free

7. Marking Diagram

Part Number
Lot Number:
- Y is the last digit of the year of manufacture (0 to 9)
- M is the month of the year (1 to 9, O, N, or D)
- D is the period of days represented by:
  1: the first 10 days of the month (1st to 10th)
  2: the second 10 days of the month (11th to 20th)
  3: the last 10–11 days of the month (21st to 31st)
Control Number
8. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−). Q(H) and Q(L) indicate a high-side power MOSFET and a low-side power MOSFET respectively. C_i and C_V indicate a current resonant capacitor and a voltage resonant capacitor, respectively.

8.1 Resonant Circuit Operation

Figure 8-1 shows a basic RLC series resonant circuit. The impedance of the circuit, $\hat{Z}$, is as the following Equation.

$$\hat{Z} = R + j \left( \omega L - \frac{1}{\omega C} \right), \quad (1)$$

where $\omega$ is angular frequency; and $\omega = 2\pi f$.

Thus,

$$\hat{Z} = R + j \left( 2\pi fL - \frac{1}{2\pi fC} \right). \quad (2)$$

When the frequency, $f$, changes, the impedance of resonant circuit will change as shown in Figure 8-2.

The frequency in which $\hat{Z}$ becomes minimum value is called a resonant frequency, $f_0$. The higher frequency area than $f_0$ is an inductance area. The lower frequency area than $f_0$ is a capacitance area.

From Equation (3), $f_0$ is as follows:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (4)$$

Figure 8-3 shows the circuit of a current resonant power supply. The basic configuration of the current resonant power supply is a half-bridge converter. The switching devices, Q(H) and Q(L), are connected in series with V_IN. The series resonant circuit and the voltage resonant capacitor, C_V, are connected in parallel with Q(L). The series resonant circuit is consisted of the following components: the resonant inductor, L_R; the primary winding, P, of a transformer, T1; and the current resonant capacitor, C_i. The coupling between the primary and secondary windings of T1 is designed to be poor so that the leakage inductance increases. This leakage inductance is used for L_R. This results in a down sized of the series resonant circuit. The dotted mark with T1 describes the winding polarity, the secondary windings, S1 and S2, are connected so that the polarities are set to the same position as shown in Figure 8-3. In addition, the winding numbers of each other should be equal. From Equation (1), the impedance of a current resonant power supply is calculated by Equation (5). From Equation (4), the resonant frequency, $f_0$, is calculated by Equation (6).

$$\hat{Z} = R + j \left( \omega (L_R + L_P) - \frac{1}{\omega C_i} \right), \quad (5)$$

$$f_0 = \frac{1}{2\pi\sqrt{(L_R + L_P) \times C_i}}. \quad (6)$$

where:
- R is the equivalent resistance of load,
- L_R is the inductance of the resonant inductor,
- L_P is the inductance of the primary winding P, and
- C_i is the capacitance of current resonant capacitor.
In the current resonant power supply, Q(H) and Q(L) are alternatively turned on and off. The on and off times of them are equal. There is a dead time between the on periods of Q(H) and Q(L). During the dead time, Q(H) and Q(L) are in off status.

In the current resonant power supply, the frequency is controlled. When the output voltage decreases, the IC decreases the switching frequency so that the output power is increased to keep a constant output voltage. This must be controlled in the inductance area \((f_{SW} < f_0)\). Since the winding current is delayed from the winding voltage in the inductance area, the turn-on operates in a ZCS (Zero Current Switching); and the turn-off operates in a ZVS (Zero Voltage Switching). Thus, the switching losses of Q(H) and Q(L) are nearly zero. In the capacitance area \((f_{SW} < f_0)\), the current resonant power supply operates as follows: When the output voltage decreases, the switching frequency is decreased; and then, the output power is more decreased. Therefore, the output voltage cannot be kept constant. Since the winding current goes ahead of the winding voltage in the capacitance area, Q(H) and Q(L) operate in the hard switching. This results in the increases of a power loss. This operation in the capacitance area is called the capacitive mode operation. The current resonant power supply must be operated without the capacitive mode operation (for more details, see Section 8.12).

Figure 8-4 describes the basic operation waveform of current resonant power supply (see Figure 8-3 about the symbol in Figure 8-4). For the description of current resonant waveforms in normal operation, the operation is separated into a period A to F. In the following description:

- \(I_{D(H)}\) is the current of Q(H),
- \(I_{D(L)}\) is the current of Q(L),
- \(V_{F(H)}\) is the forward voltage of Q(H),
- \(V_{F(L)}\) is the forward voltage of Q(L),
- \(I_s\) is the current of \(L_s\),
- \(V_{IN}\) is an input voltage,
- \(V_{Ci}\) is \(C_i\) voltage, and
- \(V_{CV}\) is \(C_v\) voltage.

The current resonant power supply operations in period A to F are as follows:

1) Period A
   When Q(H) is on, an energy is stored into the series resonant circuit by \(I_{D(H)}\) that flows through the resonant circuit and the transformer (see Figure 8-5). At the same time, the energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmission to the secondary circuit is stopped.

2) Period B
   After the secondary side current becomes zero, the resonant current flows to the primary side only to charge \(C_i\) (see Figure 8-6).
3) Period C

C is the dead-time period. Q(H) and Q(L) are in off status. When Q(H) turns off, CV is discharged by IL that is supplied by the energy stored in the series resonant circuit applies (see Figure 8-7). When CV decreases to $V_{F(L)} - I_{D(L)}$ flows through the body diode of Q(L), and CV is clamped to $V_{F(L)}$. After that, Q(L) turns on. Since $V_{DS(L)}$ is nearly zero at the point, Q(L) operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

4) Period D

When Q(L) turns on, $I_{D(L)}$ flows as shown in Figure 8-8; and CV is applied the primary winding voltage of the transformer. At the same time, energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

5) Period E

After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 8-9).

6) Period F

F is the dead-time period. Q(H) and Q(L) are in off status. When Q(L) turns off, CV is charged by $-I_{L}$ that is supplied by the energy stored in the series resonant circuit applies (see Figure 8-10). When CV decreases to $V_{IN} + V_{F(H)} - I_{D(H)}$ flows through body diode of Q(H), and CV is clamped to $V_{IN} + V_{F(H)}$. After that, Q(H) turns on. Since $V_{DS(H)}$ is nearly zero at the point, Q(H) operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

After the period F, $I_{D(H)}$ flows again; and the operation returns to the period A. The above operation is repeated to transfer energy to the secondary side from the resonant circuit.
8.2 Startup Operation

Figure 8-11 shows the VCC pin peripheral circuit. When the following all conditions are fulfilled, the IC starts the startup operation:

- The mains input voltage is provided, and the VSEN pin voltage increases to the on-threshold voltage, \( V_{SEN(ON)} = 1.300 \, \text{V} \), or more.
- The startup current, \( I_{COST} \), which is a constant current of 6.0 mA, is provided from the IC to capacitor C2 connected to the VCC pin, C2 is charged, and the VCC pin voltage increases to the operation start voltage, \( V_{CC(ON)} = 14.0 \, \text{V} \), or more.
- The FB pin voltage increases to the oscillation start threshold voltage, \( V_{FB(ON)} = 0.30 \, \text{V} \), or more.

After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

![Figure 8-11. VCC pin peripheral circuit](image)

During the IC operation, the rectified voltage from the auxiliary winding voltage, \( V_D \), of Figure 8-11 is a power source to the VCC pin.

The winding turns of the winding D should be adjusted so that the VCC pin voltage is applied to equation (7) within the specification of the mains input voltage range and output load range of the power supply. The target voltage of the winding D is about 19 V.

\[
V_{CC(BIAS)} < V_{CC} < V_{CC(OVF)}
\]

\[\Rightarrow 11.0 \, \text{V} < V_{CC} < 32.0 \, \text{V} \quad (7)\]

The startup time, \( t_{START} \), is determined by the value of C2 and C6 connected to the CSS pin. Since the startup time for C6 is much smaller than that for C2, the startup time is approximately given as below:

\[
t_{START} \approx C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{I_{CC(STR)}} \quad (8)
\]

where:
- \( t_{START} \) is the startup time in s,
- \( V_{CC(INT)} \) is the initial voltage of the VCC pin in V, and
- \( I_{CC(STR)} \) is the startup current, 6.0 mA

8.3 Undervoltage Lockout (UVLO)

Figure 8-12 shows the relationship of \( V_{CC} \) and \( I_{CC} \).

After the IC starts operation, when the VCC pin voltage decreases to \( V_{CC(OFF)} = 9.8 \, \text{V} \), the IC stops switching operation by the Undervoltage Lockout (UVLO) Function and reverts to the state before startup again.

![Figure 8-12. \( V_{CC} \) versus \( I_{CC} \)](image)

8.4 Bias Assist Function

Figure 8-13 shows the VCC pin voltage behavior during the startup period.

When the conditions of Section 8.2 are fulfilled, the IC starts operation. Thus, the circuit current, \( I_{CC} \), increases, and the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, \( V_D \), increases in proportion to the output voltage rise. Thus, the VCC pin voltage is set by the balance between dropping due to the increase of \( I_{CC} \) and rising due to the increase of the auxiliary winding voltage, \( V_D \). When the VCC pin voltage decreases to \( V_{CC(OFF)} = 9.8 \, \text{V} \), the IC stops switching operation and a startup failure occurs.

In order to prevent this, when the VCC pin voltage decreases to the startup current threshold biasing voltage, \( V_{CC(BIAS)} = 11.0 \, \text{V} \), the Bias Assist Function is activated.
While the Bias Assist Function is activated, any decrease of the VCC pin voltage is counteracted by providing the startup current, \( I_{CC(ST)} \), from the startup circuit. It is necessary to check the startup process based on actual operation in the application, and adjust the VCC pin voltage, so that the startup failure does not occur. If VCC pin voltage decreases to \( V_{CC(BIAS)} \) and the Bias Assist Function is activated, the power loss increases.

Thus, VCC pin voltage in normal operation should be set more than \( V_{CC(BIAS)} \) by the following adjustments.

- The turns ratio of the auxiliary winding to the secondary-side winding is increased.
- The value of \( C_2 \) in Figure 8-11 is increased and/or the value of \( R_1 \) is reduced.

During all protection operation, the Bias Assist Function is disabled.

### 8.5 Soft Start Function

Figure 8-14 shows the Soft-start operation waveforms.

The IC has Soft Start Function to reduce stress of peripheral component and prevent the capacitive mode operation. During the soft start operation, \( C_6 \) connected to the CSS pin is charged by the CSS Pin Charge Current, \( I_{CSS(C)} \). The oscillation frequency is varied by the CSS pin voltage. The switching frequency gradually decreases from \( f_{MAX} \) * = 500 kHz at most, according to the CSS pin voltage rise. At same time, output power increases. When the output voltage increases, the IC is operated with an oscillation frequency controlled by feedback.

When the IC becomes any of the following conditions, \( C_6 \) is discharged by the CSS Pin Reset Current, \( I_{CSS(R)} \), 1.8 mA.

- The VCC pin voltage decreases to the operation stop voltage, \( V_{CC(OFF)} = 9.8 \) V, or less.
- The VSEN pin voltage decreases to the off-threshold voltage, \( V_{SEN(OFF)} = 1.115 \) V, or less.
- Any of protection operations in protection mode (OVP, OLP or TSD) is activated.

### 8.6 Minimum and Maximum Switching Frequency Setting

The minimum switching frequency is adjustable by the value of \( R_5 \) (\( R_{CSS} \)) connected to the CSS pin. The relationship of \( R_5 \) (\( R_{CSS} \)) and the externally adjusted minimum frequency, \( f_{(MIN)ADJ} \), is shown in Figure 8-15.

The \( f_{(MIN)ADJ} \) should be adjusted to more than the resonant frequency, \( f_0 \) under the condition of the minimum mains input voltage and the maximum output power. The maximum switching frequency, \( f_{MAX} \), is determined by the inductance and the capacitance of the resonant circuit. The \( f_{MAX} \) should be adjusted to less than the maximum frequency, \( f_{(MAX)} = 300 \) kHz.

### 8.7 High-side Driver

Figure 8-16 shows a bootstrap circuit. The bootstrap circuit is for driving to \( Q(H) \) and is made by \( D_3 \), \( R_{12} \) and \( C_{12} \) between the REG pin and the VS pin. When \( Q(H) \) is OFF state and \( Q(L) \) is ON state, the VS pin voltage becomes about ground level and \( C_{12} \) is charged from the REG pin.

When the voltage of between the VB pin and the VS pin, \( V_{BUV} \), increases to \( V_{BUV(ON)} = 7.3 \) V or more, an internal high-side drive circuit starts operation. When \( V_{BUV} \) decreases to \( V_{BUV(OFF)} = 6.4 \) V or less, its drive circuit stops operation. In case the both ends of \( C_{12} \) and...
D4 are short, the IC is protected by \( V_{B(UV)(OFF)} \), D4 for protection against negative voltage of the VS pin

- **D3**
  D3 should be an ultrafast recovery diode of short recovery time and low reverse current. When the maximum mains input voltage of the application is 265VAC, it is recommended to use ultrafast recovery diode of \( V_{RM} = 600 \) V

- **C11, C12, and R12**
  The values of C11, C12, and R12 are determined by total gate charge, \( Q_g \), of external MOSFET and voltage dip amount between the VB pin and the VS pin in the burst mode of the standby mode change. C11, C12, and R12 should be adjusted so that the voltage between the VB pin and the VS is more than \( V_{B(UV)(ON)} = 7.3 \) V by measuring the voltage with a high-voltage differential probe.
  The reference value of C11 is 0.47 \( \mu \)F to 1 \( \mu \)F.
  The time constant of C12 and R12 should be less than 500 ns. The values of C12 and R22 are 0.047 \( \mu \)F to 0.1 \( \mu \)F, and 2.2 \( \Omega \) to 10 \( \Omega \).
  C11 and C12 should be a film type or ceramic capacitor of low ESR and low leakage current.

- **D4**
  D4 should be a Schottky diode of low forward voltage, \( V_f \), so that the voltage between the VB pin and the VS pin must not decrease to the absolute maximum ratings of \(-0.3 \) V or less.

The feedback current increases under slight load condition, and thus the FB pin voltage decreases. While the FB pin voltage decreases to the oscillation stop threshold voltage, \( V_{FB(OFF)} = 0.20 \) V, or less, the IC stops switching operation. This operation reduces switching loss, and prevents the increasing of the secondary output voltage.

In Figure 8-17, R8 and C9 are for phase compensation adjustment, and C5 is for high frequency noise rejection. The secondary-side circuit should be designed so that the collector current of PC1 is more than 195 \( \mu \)A which is the absolute value of the maximum source current, \( I_{FB(MAX)} \). Especially the current transfer ratio, CTR, of the photo coupler should be taken aging degradation into consideration.

![Figure 8-17. FB pin peripheral circuit](image)

### 8.9 Standby Function

The IC has the Standby Function in order to increase circuit efficiency in light load.

When the Standby Function is activated, the IC operates in the burst oscillation mode as shown in Figure 8-18. The burst oscillation has periodic non-switching intervals. Thus, the burst mode reduces switching losses.

Generally, to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. In addition, the IC has the Soft-on and the Soft-off Function in order to suppress rapid and sharp fluctuation of the drain current during the burst mode. thus, the audible noises can be reduced (see Section 8.9.2).

The operation of the IC changes to the standby operation by the external signal (see Section 8.9.1).

![Figure 8-18. Standby waveform](image)
8.9.1 Standby Mode Changed by External Signal

Figure 8-19 shows the standby mode change circuit with external signal. Figure 8-20 shows the standby change operation waveforms. When the standby terminal of Figure 8-19 is provided with the L signal, Q1 turns off, C10 connected to the SB pin is discharged by the sink current, ISB(SNK) = 10 µA, and the SB pin voltage decreases. When the SB pin voltage decrease to the SB Pin Oscillation Stop Threshold Voltage, VSB(OFF) = 0.5 V, the operation of the IC is changed to the standby mode. When SB pin voltage is VSB(OFF) = 0.5 V or less and FB pin voltage is Oscillation Stop Threshold Voltage VFB(OFF) = 0.20 V or less, the IC stops switching operation.

When the standby terminal is provided with the H signal and the SB pin voltage increases to Standby Threshold Voltage VSB(STB) = 5.0 V or more, the IC returns to normal operation.

8.9.2 Burst Oscillation Operation

In standby operation, the IC operates burst oscillation where the peak drain current is suppressed by Soft-on/Soft-off Function in order to reduce audible noise from transformer. During burst oscillation operation, the switching oscillation is controlled by SB pin voltage.

Figure 8-21 shows the burst oscillation operation waveforms.

When the SB pin voltage decreases to VSB(OFF) = 0.5 V or less and the FB pin voltage decreases to VFB(OFF) = 0.20 V or less, the IC stops switching operation and the output voltage decreases. Since the output voltage decreases, the FB pin voltage increases. When the FB pin voltage increases to the oscillation start threshold voltage, VFB(ON) = 0.30 V, C10 is charged by ISB(SRC) = −10 µA, and the SB pin voltage gradually increases.

When the SB pin voltage increases to the oscillation start threshold voltage, VSB(ON) = 0.6 V, the IC resumes switching operation, controlling the frequency control by the SB pin voltage. Thus, the output voltage increases (Soft-on). After that, when FB pin voltage decrease to oscillation stop threshold voltage, VFB(OFF) = 0.20 V, C10 is discharged by ISB(SNK) = 10 µA and SB pin voltage decreases. When the SB pin voltage decreases to VSB(OFF) again, the IC stops switching operation. Thus, the output voltage decreases (Soft-off).

The SB pin discharge time in the Soft-on and Soft-off Function depends on C10. When the value of C10 increases, the Soft-on/Soft-off Function makes the peak drain current suppressed, and makes the burst period longer. Thus, the output ripple voltage may increase and/or the VCC pin voltage may decrease.
If the VCC pin voltage decreases to $V_{CC(BIAS)} = 11.0 \text{ V}$, the Bias Assist Function is always activated, and it results in the increase of power loss (see Section 8.4).

Thus, it is necessary to adjust the value of C10 while checking the input power, the output ripple voltage, and the VCC pin voltage. The reference value of C10 is about 0.001 $\mu\text{F}$ to 0.1 $\mu\text{F}$.

### 8.10 Automatic Dead Time Adjustment Function

The dead time is the period when both the high-side and the low-side power MOSFETs are off.

As shown in Figure 8-22, if the dead time is shorter than the voltage resonant period, the power MOSFET is turned on and off during the voltage resonant operation. In this case, the power MOSFET turned on and off in hard switching operation, and the switching loss increases. The Automatic Dead Time Adjustment Function is the function that the ZVS (Zero Voltage Switching) operation of $Q(H)$ and $Q(L)$ is controlled automatically by the voltage resonant period detection of IC. The voltage resonant period is varied by the power supply specifications (input voltage and output power, etc.). However, the power supply with this function is unnecessary to adjust the dead time for each power supply specification.

![Figure 8-22. ZVS failure operation waveform](image)

As shown in Figure 8-23, the VS pin detects the $dv/dt$ period of rising and falling of the voltage between drain and source of the low-side power MOSFET, $V_{DS(L)}$, and the IC sets its dead time to that period. This function controls so that the high-side and the low-side power MOSFETs are automatically switched to Zero Voltage Switching (ZVS) operation. This function operates in the period from $t_{D(MIN)} = 0.35 \mu\text{s}$ to $t_{D(MAX)} = 1.65 \mu\text{s}$.

In minimum output power at maximum input voltage and maximum output power at minimum input voltage, the ZCS (Zero Current Switching) operation of IC (the drain current flows through the body diode is about 1 $\mu\text{s}$ as shown in Figure 8-24), should be checked based on actual operation in the application.

![Figure 8-23. VS pin and dead time period](image)

### 8.11 Brown-In and Brown-Out Function

Figure 8-25 shows the VSEN pin peripheral circuit. This function detects the mains input voltage, and stops switching operation during low mains input voltage, to prevent exceeding input current and overheating.

R2 to R4 set the detection voltage of this function. When the VCC pin voltage is higher than $V_{CC(ON)}$, this function operates depending on the VSEN pin voltage as follows:

- When the VSEN pin voltage is more than $V_{SEN(ON)} = 1.300 \text{ V}$, the IC starts.
- When the VSEN pin voltage is less than $V_{SEN(OFF)} = 1.115 \text{ V}$, the IC stops switching operation.

![Figure 8-25. VSEN pin peripheral circuit](image)

Given, the DC input voltage when the IC starts as
The DC input voltage when the switching operation of the IC stops as \( V_{\text{IN(OFF)}} \). \( V_{\text{IN(OFF)}} \) is calculated by Equation (10). Thus, the relationship between \( V_{\text{IN(ON)}} \) and \( V_{\text{IN(OFF)}} \) is Equation (11).

\[
V_{\text{IN(ON)}} \approx V_{\text{SEN(ON)}} \times \frac{R_2 + R_3 + R_4}{R_4} \tag{9}
\]

\[
V_{\text{IN(OFF)}} \approx V_{\text{SEN(OFF)}} \times \frac{R_2 + R_3 + R_4}{R_4} \tag{10}
\]

\[
V_{\text{IN(OFF)}} \approx \frac{V_{\text{SEN(OFF)}}}{V_{\text{SEN(ON)}}} \times V_{\text{IN(ON)}} \tag{11}
\]

The detection resistance is calculated from Equation (9) as follows:

\[
R_2 + R_3 \approx \frac{V_{\text{IN(ON)}} - V_{\text{SEN(ON)}}}{V_{\text{SEN(ON)}}} \times R_4 \tag{12}
\]

Because \( R_2 \) and \( R_3 \) are applied high DC voltage and are high resistance, the following should be considered:

- Select a resistor designed against electromigration according to the requirement of the application, or
- Use a combination of resistors in series for that to reduce each applied voltage

The reference value of \( R_2 \) is about 10 \( \text{M}\Omega \).

\( C_4 \) shown in Figure 8-25 is for reducing ripple voltage of detection voltage and making delay time. The value is 0.1 \( \mu \text{F} \) or more, and the reference value is about 0.47 \( \mu \text{F} \).

The value of \( R_2, R_3 \) and \( R_4 \) and \( C_4 \) should be selected based on actual operation in the application.

### 8.12 Capacitive Mode Detection Function

The resonant power supply is operated in the inductance area shown in Figure 8-26. In the capacitance area, the power supply becomes the capacitive mode operation (see Section 8.1). In order to prevent the operation, the minimum oscillation frequency is needed to be set higher than \( f_0 \) on each power supply specification.

However, the IC has the capacitive mode operation Detection Function kept the frequency higher than \( f_0 \). Thus, the minimum oscillation frequency setting is unnecessary and the power supply design is easier. In addition, the ability of transformer is improved because the operating frequency can operate close to the resonant frequency, \( f_0 \).

The resonant current is detected by the RC pin, and the IC prevents the capacitive mode operation. When the capacitive mode is detected, the \( C_7 \) connected to CL pin is charged by \( I_{\text{CL(SRC)}} = -17 \mu A \). When the CL pin voltage increases to \( V_{\text{CL(OLP)}} \), the OLP is activated and the switching operation stops. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 8.17). The detection voltage is changed to \( V_{\text{RC1}} = \pm 0.10 \text{V} \) or \( V_{\text{RC2}} = \pm 0.50 \text{V} \) depending on the load as shown in Figure 8-28 and Figure 8-29. The Capacitive Mode Operation Detection Function operations as follows:

- **Period in which the \( Q(\text{H}) \) is ON**
  - Figure 8-27 shows the RC pin waveform in the inductance area, and Figure 8-28 and Figure 8-29 shows the RC pin waveform in the capacitance area.
  - In the inductance area, the RC pin voltage doesn’t cross the plus side detection voltage in the downward direction during the on period of \( Q(\text{H}) \) as shown in Figure 8-27.
  - On the contrary, in the capacitance area, the RC pin voltage crosses the plus side detection voltage in the downward direction. At this point, the capacitive mode operation is detected. Thus, \( Q(\text{H}) \) is turned off, and \( Q(\text{L}) \) is turned on, as shown in Figure 8-28 and Figure 8-29.

- **Period in which the \( Q(\text{L}) \) is on**
  - Contrary to the above of \( Q(\text{H}) \), in the capacitance area, the RC pin voltage crosses the minus side detection voltage in the upward direction during the on period of \( Q(\text{L}) \). At this point, the capacitive mode operation is detected. Thus, \( Q(\text{L}) \) is turned off and \( Q(\text{H}) \) is turned on.

As above, since the capacitive mode operation is detected by pulse-by-pulse and the operating frequency is synchronized with the frequency of the capacitive...
mode operation, and the capacitive mode operation is prevented. In addition to the adjusting method of $R_{OCP}$, $C3$, and $R6$ in Section 8.16, $R_{OCP}$, $C3$, and $R6$ should be adjusted so that the absolute value of the RC pin voltage increases to more than $|V_{RC2}| = 0.50 \, V$ under the condition caused the capacitive mode operation easily, such as startup, turning off the mains input voltage, or output shorted. The RC pin voltage must be within the absolute maximum ratings of $-6 \, V$ to $6 \, V$.

### Figure 8-27. RC pin voltage in inductance area

![RC pin voltage in inductance area](image)

### Figure 8-28. High side capacitive mode detection in light load

![High side capacitive mode detection in light load](image)

### Figure 8-29. High side capacitive mode detection in heavy load

![High side capacitive mode detection in heavy load](image)

#### 8.13 Input Electrolytic Capacitor Discharge Function

Figure 8-30 shows an application that residual voltage of the input capacitor, $C1$, is reduced after turning off the mains input voltage. R2 is connected to the AC input lines through D7 and D8. Just after turning off the mains input voltage, the VSEN pin voltage decreases to $V_{SEN(OFF)} = 1.115 \, V$ according to a short time of the time constant with R2 to R4 and C4, and C1 is discharged by the equivalent to $I_{CC(ST)} = 6.0 \, mA$.

![Input capacitor discharge](image)

#### 8.14 Reset Detection Function

In the startup period, the feedback control for the output voltage is inactive. If a magnetizing current may not be reset in the on-period because of unbalanced operation, a negative current may flow just before a power MOSFET turns off. This causes a hard switching operation, increases the stresses of the power MOSFET. Where the magnetizing current means the circulating current applied for resonant operation, and flows only into the primary-side circuit. To prevent the hard switching, the IC has the reset detection function.

Figure 8-32 shows the high-side operation and the reference drain current waveforms in a normal resonant operation and a reset failure operation. To prevent the hard switching operation, the reset detection function operates such as an on period is extended until the absolute value of a RC pin voltage, $|V_{RC1}|$, increases to 0.10 $V$ or more. When the on period reaches the maximum reset time, $t_{RST(MAX)} = 5.0 \, \mu s$, the on-period expires at that moment, i.e., the power MOSFET turns off (see Figure 8-31).

![Reset Detection Operation Example at High-side On Period](image)
Turning on at $V_{DS(L)} = 0V$ results in soft-switching

Turning on at $V_{DS(L)} >> 0V$ results in hard-switching

Figure 8-32. Reference High-side Operation and Drain Current Waveforms in Normal Resonant Operation and in Reset Failure Operation
### 8.15 Overvoltage Protection (OVP)

When the voltage between the VCC pin and the GND pin is applied to the OVP threshold voltage, $V_{	ext{CC(OVP)}} = 32.0 \, \text{V}$, or more, the Overvoltage Protection (OVP) is activated.

The IC has two operation types of OVP. One is the auto restart. The other is latched shutdown.

When the auxiliary winding supplies the VCC pin voltage, the OVP is able to detect an excessive output voltage, such as when the detection circuit for output control is open in the secondary-side circuit because the VCC pin voltage is proportional to the output voltage.

The output voltage of the secondary-side circuit at OVP operation, $V_{\text{OUT(OVP)}}$, is approximately given as below:

$$V_{\text{OUT(OVP)}} = \frac{V_{\text{OUT(NORMAL)}}}{V_{\text{CC(NORMAL)}}} \times 32 \, (\text{V}) \quad (13)$$

where,

- $V_{\text{OUT(NORMAL)}}$: Output voltage in normal operation
- $V_{\text{CC(NORMAL)}}$: VCC pin voltage in normal operation

#### Auto Restart Type: SSC3S901

Figure 8-33 shows the OVP operation waveforms of auto restart type.

When the OVP is activated, the IC stops switching operation and VCC pin voltage decreases. When VCC pin voltage decreases to $V_{\text{CC(OFF)}} = 9.8 \, \text{V}$, the OVP operation is released and the startup circuit is activated. When VCC pin voltage is increased to $V_{\text{CC(ON)}} = 14.0 \, \text{V}$ by startup current, the IC starts the switching operation. During the OVP operation, the intermittent operation by UVLO is repeated.

When the fault condition is removed, the IC returns to normal operation automatically.

#### Latched Shutdown Type: SSC3S902

Figure 8-34 shows the OVP operation waveforms of latched shutdown type.

When the OVP is activated, the IC stops switching operation at the latched state and VCC pin voltage decreases.

When VCC pin voltage decreases to $V_{\text{CC(OFF)}} = 9.8 \, \text{V}$, the startup circuit is activated. When VCC pin voltage is increased to $V_{\text{CC(ON)}} = 14.0 \, \text{V}$ by startup current, the startup circuit is turned off and VCC pin voltage decreases. During the OVP operation, the latch state is kept by turning on/off of the startup circuit.

The latched state is released by the following condition: VCC pin voltage is decreased to $V_{\text{CC(L.OFF)}} = 7.8 \, \text{V}$ or less by turning off the input voltage, or VSEN pin voltage is decreased to $V_{\text{SEN(OFF)}} = 1.115 \, \text{V}$ or less.

### 8.16 Overcurrent Protection (OCP)

The Overcurrent Protection (OCP) detects the drain current, $I_D$, on pulse-by-pulse basis, and limits output power. In Figure 8-35, this circuit enables the value of C3 for shunt capacitor to be smaller than the value of Ci for current resonant capacitor, and the detection current through C3 is small. Thus, the loss of the detection resistor, $R_{\text{OCP}}$, is reduced, and $R_{\text{OCP}}$ is a small-sized one available. There is no convenient method to calculate the accurate resonant current value according to the mains input and output conditions, and others. Thus, $R_{\text{OCP}}$, C3, and C6 should be adjusted based on actual operation in the application. The following is a reference adjusting method of $R_{\text{OCP}}$, C3, R6, and C8:

- C3 and $R_{\text{OCP}}$ C3 is 100pF to 330pF (around 1% of Ci value). $R_{\text{OCP}}$ is around 100 $\Omega$.

Given the current of the high side power MOSFET at ON state as $I_{\text{D(H)}}$, $R_{\text{OCP}}$ is calculated Equation (14).

The detection voltage of $R_{\text{OCP}}$ is used the detection of the capacitive mode operation (see Section 8.12). Therefore, setting of $R_{\text{OCP}}$ and C3 should be taken account of both OCP and the capacitive mode operation.

$$R_{\text{OCP}} \approx \frac{V_{\text{OC(L)}}}{I_{\text{D(H)}}} \times \left( \frac{C3 + Ci}{C3} \right) \quad (14)$$
● R6 and C8 are for high frequency noise reduction. R6 is 100 Ω to 470 Ω. C6 is 100 pF to 1000 pF.

The OCP operation has two-step threshold voltage as follows:

- **Step I, RC pin threshold voltage (Low), V_{RC(L)}:**
  This step is active first. When the absolute value of the RC pin voltage increases to more than |V_{DCL(L)}| = 1.50 V, C6 connected to the CSS pin is discharged by I_{CSS(L)} = 1.8 mA. Thus, the switching frequency increases, and the output power is limited. During discharging C6, when the absolute value of the RC pin voltage decreases to |V_{RC(L)}| or less, the discharge stops.

- **Step II, RC pin threshold voltage (High-speed), V_{RC(S)}:**
  This step is active second. When the absolute value of the RC pin voltage increases to more than |V_{DCL(S)}| = 2.30 V, the high-speed OCP is activated, and power MOSFETs reverse on and off. At the same time, C6 is discharged by I_{CSS(S)} = 20.5 mA. Thus, the switching frequency quickly increases, and the output power is quickly limited. This step operates as protections for exceeding overcurrent, such as the output shorted. When the absolute value of the RC pin voltage decreases to |V_{RC(S)}| or less, the operation is changed to the above Step I.

When OLP Input Voltage Compensation is used, CL pin voltage is needed to reach the threshold voltage of Overload Protection (OLP), V_{CL(OLP)}, in the state that RC pin voltage is less than V_{RC(L)}. Therefore, when output power increases, the OLP is activated. When the input voltage is constant like PFC output, OLP Input Voltage Compensation is unnecessary. Therefore, when output power increases, the above OCP operation (Step I and Step II) is activated.

### 8.17 Overload Protection (OLP) with Input Voltage Compensation

#### 8.17.1 Overload Protection (OLP)

When CL pin voltage becomes the threshold voltage of Overload Protection (OLP), V_{CL(OLP)}, the OLP is activated and the switching operation stops. V_{CL(OLP)} is dependent on the input voltage by OLP Input Voltage Compensation Function as shown in Section 8.17.2.

The trigger of OLP is different according to the case with OLP Input Voltage Compensation Function or without it.

- **Without OLP Input Voltage Compensation Function**

  Figure 8-36 shows the OLP operation waveforms. When the absolute value of RC pin voltage increases to |V_{DCL(L)}| = 1.50 V by increasing of output power, the overcurrent protection (OCP) is activated. After that, the C7 connected to CL pin is charged by I_{CL} = −17 μA. When the OCP state continues and CL pin voltage increases to V_{CL(OLP)}, the OLP is activated.

- **With OLP Input Voltage Compensation Function**

  CL pin voltage is needed to reach V_{CL(OLP)} in the state that RC pin voltage is less than V_{RC(L)}. When CL pin voltage reaches V_{CL(OLP)} in one of the following condition, the OLP is activated as shown in Figure 8-37.

  1) The output power increases, CL pin voltage increases to V_{CL(OLP)}, which is constant.

  2) The input voltage increases, V_{CL(OLP)} depending on OLP Input Voltage Compensation decreases to CL pin voltage.

  Figure 8-36. OLP operation waveform without OLP Input Voltage Compensation Function
The IC series has two operation types of OLP. One is the auto restart. The other is latched shutdown.

- **Auto Restart Type: SSC3S901**
  Figure 8-38 shows the auto restart type OLP operation waveforms in the case without OLP Input Voltage Compensation Function.
  When the OLP is activated, the IC stops switching operation. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 8.15). When the fault condition is removed, the IC returns to normal operation automatically.

- **Latched Shutdown Type: SSC3S902**
  Figure 8-39 shows the latched shutdown type OLP operation waveforms in the case without OLP Input Voltage Compensation Function.
  When the OLP is activated, the IC stops switching operation at the latched state. During the OLP operation, the latch state is kept by turning on/off of the startup circuit (see Section 8.15). The latched state is released by following condition: VCC pin voltage is decreased to \( V_{CC(OFF)} = 7.8 \) V or less by turning off the input voltage, or VSEN pin voltage is decreased to \( V_{SEN(OFF)} = 1.115 \) V or less.
8.17.2 OLP Input Voltage Compensation Function

In the case without OLP Input Voltage Compensation Function, when the absolute value of RC pin voltage increases to \(|V_{OLP}| = 1.50\, \text{V}\), the capacitor connected to CS pin is charged. When CS pin voltage increases to \(V_{CL(OLP)}\), the OLP is activated (see Figure 8-36).

In the constant voltage control of current resonant topology, when the input voltage increases, the resonant frequency increases, and the peak drain current decreases. Since \(|V_{OLP}|\) is a fixed value, when output power increases at the constant rate, there are the output power difference at OLP operation in high and low input voltages as shown in Figure 8-40. In the universal mains input voltage, the output power at OLP operation is very large in the maximum input voltage, and component stresses are increased by heating.

Therefore, the IC has OLP Input Voltage Compensation Function that the output power difference at OLP operation is limited in input voltages, and can realize power supply of universal mains input voltage (85 VAC to 265VAC).

As shown in Figure 8-41, this function compensates the OLP threshold voltage, \(V_{CL(OLP)}\), depending on input voltage, and is used so that CL pin voltage reaches \(V_{CL(OLP)}\) in the state that RC pin voltage is less than \(V_{RCOLP}\).

![Figure 8-40. OLP operation waveforms according to input voltage (without OLP Input Voltage Compensation)](image)

![Figure 8-41. OLP operation waveforms according to input voltage (with OLP Input Voltage Compensation)](image)

- **PL Pin and CL Pin Setup:**
  The primary-side winding current as shown in Figure 8-42 includes the magnetizing current not transferred to the secondary-side circuit, and the load current proportional to the output current. The current separated from the primary-side winding current by \(C3\) flows to the PL pin. As shown in Figure 8-43, the primary-side winding current flows to the \(C7\) connected to CL pin during the high side power MOSFET turning on. The magnetizing current becomes zero by charging and discharging. Only the load current is charged to \(C7\). As a result, the CL pin voltage is proportional to the output current.

On actual operation of the application, \(C7\) connected to the CL pin should be adjusted so that ripple voltage of the CL pin reduces. R7 connected to the PL pin should be adjusted so that the OLP at the minimum mains input voltage is activated before the OCP limited by the low threshold voltage of OCP, \(V_{RCOLP}\). The PL pin voltage and the CL pin voltage must be within the absolute maximum ratings of \(-0.3\) to 6 V, by adjusting R7, in the OCP operation point at the minimum mains input voltage.

- **VSPL Pin Setup:**
  The VSPL pin detects the mains input voltage. Both \(V_{SP}\) and the setting voltage in Section 8.11 Brown-In and Brown-Out Function are determined by R2, R3, and R4. Both of them should be adjusted based on actual operation in the application.
8.18 Thermal Shutdown (TSD)

When the junction temperature of the IC reach to the Thermal Shutdown Temperature $T_{j(TSD)} = 140 \, ^\circ C$ (min.), Thermal Shutdown (TSD) is activated.

- **Auto Restart Type: SSC3S901**
  - When the TSD is activated, the IC stops switching operation. When the VCC pin voltage is decreased to $V_{CC(P.OFF)} = 9.8 \, V$ or less and the junction temperature of the IC is decreased to less than $T_{j(TSD)}$, the IC restarts. During the protection mode, restart and stop are repeated. When the fault condition is removed, the IC returns to normal operation automatically.

- **Latched Shutdown Type: SSC3S902**
  - When the TSD is activated, the IC stops switching operation at the latched state. During the TSD operation, the latch state is kept by turning on/off of the startup circuit (see Section 8.15).
  - The latched state is released by following condition: VCC pin voltage is decreased to $V_{CC(L.OFF)} = 7.8 \, V$ or less by turning off the input voltage, or VSEN pin voltage is decreased to $V_{SEN(OFF)} = 1.115 \, V$ or less.
9. Design Notes

9.1 External Components

Take care to use the proper rating and proper type of components.

9.1.1 Input and output electrolytic capacitors

Applying proper derating to a ripple current, a voltage, and a temperature rise. It is required to use the high ripple current and low impedance type electrolytic capacitor that is designed for switch mode power supplies.

9.1.2 Resonant transformer

The resonant power supply uses the leakage inductance of a transformer. Therefore, to reduce the effect of the eddy current and the skin effect, the wire of transformer should be used a bundle of fine litz wires.

9.1.3 Current detection resistor, $R_{OCP}$

To reduce the effect of the high frequency switching current flowing through $R_{OCP}$, choose the resistor of a low internal inductance type. In addition, its allowable dissipation should be chosen suitable.

9.1.4 Current resonant capacitor, $C_i$

Since a large resonant current flows through $C_i$, $C_i$ should be used a low loss and a high current capability capacitor such as a polypropylene film capacitor. In addition, $C_i$ must be taken into account its frequency characteristic because a high frequency current flows.

9.1.5 Gate Pin Peripheral Circuit

The VGH and VGL pins are gate drive outputs for external power MOSFETs. These peak source and sink currents are – 540 mA and 1.50 A, respectively.

To make a turn-off speed faster, connect the diode, $D_s$, as shown in Figure 9-1. When $R_A$, $R_B$ and $D_s$ is adjusted, the following contents should be taken into account: the power losses of power MOSFETs, gate waveforms (for a ringing reduction caused by a pattern layout, etc.), and EMI noises. $R_A$ is 33 $\Omega$ to 330 $\Omega$. $R_B$ is about 10 $\Omega$.

To prevent the malfunctions caused by steep $dv/dt$ at turn-off of power MOSFETs, connect $R_{GS}$ of 10 k$\Omega$ to 100 k$\Omega$ between the Gate and Source pins of the power MOSFET with a minimal length of PCB traces. When these gate resistances are adjusted, the gate waveforms should be checked that the dead time is ensured as shown in Figure 9-2.

![Figure 9-1. Power MOSFET Peripheral Circuit](image)

![Figure 9-2. Dead Time Confirmation](image)

9.2 PCB Trace Layout and Component Placement

The PCB circuit design and the component layout significantly affect a power supply operation, EMI noises, and power dissipation. Thus, to reduce the impedance of the high frequency traces on a PCB (see Figure 9-3), they should be designed as wide trace and small loop as possible. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

![Figure 9-3. High frequency current loops (hatched areas)](image)
Figure 9-4 shows the circuit design example. The PCB trace design should be also taken into account as follows:

1) Main Circuit Trace
   The main traces that switching current flows should be designed as wide trace and small loop as possible.

2) Control Ground Trace
   If the large current flows through a control ground, it may cause varying electric potential of the control ground; and this may result in the malfunctions of the IC. Therefore, connect the control ground as close and short as possible to the GND pin at a single-point ground (or star ground) that is separated from the power ground.

3) VCC Trace
   The trace for supplying power to the IC should be as small loop as possible. If C3 and the IC are distant from each other, a film capacitor $C_f$ (about 0.1 μF to 1.0 μF) should be connected between the VCC and GND pins with a minimal length of PCB traces.

4) Trace of Peripheral Components for the IC Control
   These components should be placed close to the IC, and be connected to the corresponding pin of the IC with as short trace as possible.

5) Trace of Bootstrap Circuit Components
   These components should be connected to the IC pin with as short trace as possible. In addition, the loop for these should be as small as possible.

6) Secondary Side Rectifier Smoothing Circuit Trace
   The traces of the rectifier smoothing loops carry the switching current. Thus it should be designed as wide trace and small loop as possible.

Figure 9-4. Peripheral circuit trace example around the IC
10. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of circuit using SSC3S900. The circuit symbols correspond to these of Figure 10-1.

(1) Main trace should be wide and short

(2) GND trace for IC should be connected at a single point

(3) Loop of VCC and C2 should be short

(4) Peripheral components for IC control should placed near IC

(5) Boot strap trace should be small loop

(6) Main trace of secondary side should be wide and short

Figure 10-1. PCB circuit trace layout example

Figure 10-2. Circuit schematic for PCB circuit trace layout
11. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification. The values in bill of materials are reference design. They are necessary to be adjusted based on actual operation in the application.

- Power supply specification

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<th>Part type</th>
<th>Rating</th>
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- Circuit schematic

- Bill of materials

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### SSC3S900 Series

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<td>$V_{REF} = 2.50$ V (TL431 or equiv)</td>
<td></td>
</tr>
<tr>
<td>Q601</td>
<td>PNP transistor</td>
<td>0.6 A, –60V, SOT23</td>
<td></td>
</tr>
<tr>
<td>Q602</td>
<td>NPN transistor</td>
<td>0.6 A, 40 V, SOT23</td>
<td></td>
</tr>
<tr>
<td>Q606</td>
<td>NPN transistor</td>
<td>0.8 A, 60 V SOT-23/TO-92</td>
<td></td>
</tr>
<tr>
<td>R200</td>
<td>Chip</td>
<td>47 kΩ ± 5 %, 1/4 W, 3216</td>
<td></td>
</tr>
<tr>
<td>R201</td>
<td>Chip</td>
<td>1.0 MΩ ± 5 %, 1/4 W, 3216</td>
<td></td>
</tr>
<tr>
<td>R202</td>
<td>Chip</td>
<td>1.0 MΩ ± 5 %, 1/4 W, 3216</td>
<td></td>
</tr>
<tr>
<td>R203</td>
<td>Chip</td>
<td>1.0 MΩ ± 5 %, 1/4 W, 3216</td>
<td></td>
</tr>
<tr>
<td>R204</td>
<td>Chip</td>
<td>910 kΩ + 47 kΩ ± 5 %, 1/4 W, 3216</td>
<td></td>
</tr>
<tr>
<td>R205</td>
<td>Chip</td>
<td>680 Ω ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R206</td>
<td>Chip</td>
<td>0 Ω ± 5 %, 1/4 W, 3216</td>
<td></td>
</tr>
<tr>
<td>R208</td>
<td>Chip</td>
<td>22 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R209</td>
<td>Chip</td>
<td>47 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R210</td>
<td>Chip</td>
<td>100 Ω ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R211</td>
<td>Chip</td>
<td>10 Ω ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R212</td>
<td>Chip</td>
<td>33 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R213</td>
<td>Chip</td>
<td>100 Ω ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R214</td>
<td>Chip</td>
<td>10 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R215</td>
<td>Chip</td>
<td>2.2 Ω ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R216</td>
<td>Chip</td>
<td>47 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R217</td>
<td>Chip</td>
<td>22 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R218</td>
<td>Chip</td>
<td>100 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R219</td>
<td>Chip</td>
<td>10 Ω ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R220</td>
<td>Chip</td>
<td>10 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R221</td>
<td>Chip</td>
<td>100 kΩ ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R225</td>
<td>Chip</td>
<td>150 Ω ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
<tr>
<td>R230</td>
<td>Chip</td>
<td>100 Ω ± 5 %, 1/8 W, 2012</td>
<td></td>
</tr>
</tbody>
</table>

* Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
Symbol | Part type | Rating | Recommended Sanken Parts
--- | --- | --- | ---
R301 | Chip | 5.6 kΩ ± 5 %, 1/8 W, 2012 | |
R302 | Chip | 4.7 kΩ ± 5 %, 1/8 W, 2012 | |
R303 | Chip | 10 kΩ ± 5 %, 1/8 W, 2012 | |
R304 | Chip | 2.2 kΩ ± 5 %, 1/8 W, 2012 | |
R305 | Chip | Open | |
R306 | Chip | 22 kΩ ± 5 %, 1/8 W, 2012 | |
R307 | Chip | 20 kΩ ± 5 %, 1/8 W, 2012 | |
R308* | Chip | Open | |
R309* | Chip | Open | |
R310 | Chip | 15 kΩ ± 5 %, 1/8 W, 2012 | |
R601 | Chip | 1 kΩ ± 5 %, 1/10 W, 2012 | |
R602 | Chip | 2.2 kΩ ± 5 %, 1/8 W, 2012 | |
R604 | Chip | 4.7 kΩ ± 5 %, 1/8 W, 2012 | |
R609 | Chip | Open | |
R610 | Chip | Open | |
R613* | Chip | Open | |
R614 | Chip | 22 kΩ+4.7 kΩ ± 5 %, 1/8 W, 2012 | |
R615 | Chip | Open | |
R616 | Chip | 0 Ω ± 5 %, 1/8 W, 2012 | |
T1 | See the specification | |

* Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

- Transformer specification
  
  Primary inductance, \( L_p \) : 250 μH  
  Leakage inductance, \( L_r \) : 80 μH  
  Core size : EER-42

- Winding specification

<table>
<thead>
<tr>
<th>Winding</th>
<th>Symbol</th>
<th>Number of turns (T)</th>
<th>Wire diameter (mm)</th>
<th>Construction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary winding</td>
<td>Lp</td>
<td>33</td>
<td>Litz φ0.1 mm 30 strands</td>
<td>Solenoid winding</td>
</tr>
<tr>
<td>Auxiliary winding</td>
<td>D</td>
<td>3</td>
<td>TIW φ0.2 mm</td>
<td>Space winding</td>
</tr>
<tr>
<td>Output winding 1-1</td>
<td>S1-1</td>
<td>2</td>
<td>Litz φ0.1 mm 70 strands</td>
<td>Bifilar winding</td>
</tr>
<tr>
<td>Output winding 1-2</td>
<td>S1-2</td>
<td>2</td>
<td>Litz φ0.1 mm 70 strands</td>
<td>Bifilar winding</td>
</tr>
<tr>
<td>Output winding 2-1</td>
<td>S2-1</td>
<td>15</td>
<td>Litz φ0.1 mm 30 strands</td>
<td>Bifilar winding</td>
</tr>
<tr>
<td>Output winding 2-2</td>
<td>S2-2</td>
<td>15</td>
<td>Litz φ0.1 mm 30 strands</td>
<td>Bifilar winding</td>
</tr>
</tbody>
</table>

Cross-section view
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