LLC Current-Resonant Off-Line Switching Controller

SSC3S927L

Data Sheet

Description

The SSC3S927L is a controller with SMZ* method for LLC current resonant switching power supplies, incorporating a floating drive circuit for a high-side power MOSFET. The IC includes useful functions such as Standby Function, Automatic Dead Time Adjustment, and Capacitive Mode Detection. The IC achieves high efficiency, low noise and high cost-effective power supply systems with few external components.

*SMZ: Soft-switched Multi-resonant Zero Current switch, achieved soft switching operation during all switching periods.

Package

SOP18

Not to scale

Features

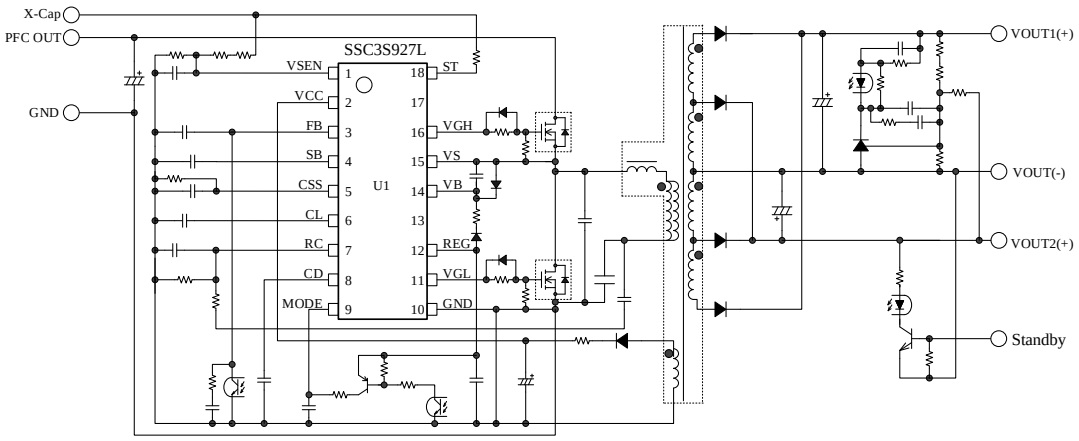
- Standby Mode Change Function
  - Output Power at Light Load:
    P_O = 150 mW (P_{IN} = 0.27 W)
  - Burst Operation in Standby Mode
  - Soft-on/Soft-off Function: Reduces Audible Noise
- Soft-start Function
- Capacitive Mode Detection Function
- Reset Detection Function
- Automatic Dead Time Adjustment Function
- Built-in Startup Circuit
- X-capacitor Discharge Function
- Protections
  - Input Voltage Detection Function
    Input Overvoltage Protection (HVP): Auto-restart
    Input Undervoltage Protection (UVP): Auto-restart
  - High-side Driver UVLO: Auto-restart
  - Overcurrent Protection (OCP): Auto-restart, Peak Drain Current Detection, 2-step Detection
  - Overload Protection (OLP): Auto-restart
  - Overvoltage Protection (OVP): Auto-restart
  - REG Overvoltage Protection (REG_OVP): Auto-restart
  - Thermal Shutdown (TSD): Auto-restart

Applications

Switching power supplies for electronic devices such as:

- Digital Appliances (e.g., Television)
- Office Automation (OA) Equipment (e.g., Server, MultiFunction Printer)
- Industrial Apparatus
- Communication Facilities

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25°C.

Parameter	Symbol	Pins	Rating	Unit
VSEN Pin Sink Current	I_{SEN}	1 − 10	1.0	mA
Control Part Input Voltage	V_{CC}	2 − 10	−0.3 to 35	V
FB Pin Voltage	V_{FB}	3 − 10	−0.3 to 6	V
SB Pin Voltage	V_{SB}	4 − 10	−0.3 to 6	V
CSS Pin Voltage	V_{CSS}	5 − 10	−0.3 to 6	V
CL Pin Voltage	V_{CL}	6 − 10	−0.3 to 6	V
RC Pin Voltage	V_{RC}	7 − 10	−6 to 6	V
CD Pin Voltage	V_{CD}	8 − 10	−0.3 to 6	V
MODE Pin Sink Current	I_{MODE}	9 − 10	100	μA
VGL pin Voltage	V_{GL}	11 − 10	−0.3 to V_{REG} + 0.3	V
REG pin Source Current	I_{REG}	12 − 10	−10.0	mA
Voltage Between VB Pin and VS Pin	V_B−V_S	14 − 15	−0.3 to 20.0	V
VS Pin Voltage	V_S	15 − 10	−1 to 600	V
VGH Pin Voltage	V_{GH}	16 − 10	V_S − 0.3 to V_B + 0.3	V
ST Pin Voltage	V_{ST}	18 − 10	−0.3 to 600	V
Operating Ambient Temperature	T_{OP}	−	−40 to 85	°C
Storage Temperature	T_{STG}	−	−40 to 125	°C
Junction Temperature	T_J	−	150	°C

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25 °C, V_{CC} is 19 V.

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Start Circuit and Circuit Current							
Operation Start Voltage	$V_{CC(ON)}$		2 − 10	15.8	17.0	18.2	V
Operation Stop Voltage (1)	$V_{CC(OFF)}$		2 − 10	7.8	8.9	9.8	V
Startup Current Biasing Threshold Voltage(1)	$V_{CC(BIAS)}$		2 − 10	9.0	9.8	10.6	V
Circuit Current in Operation	$I_{CC(ON)}$		2 − 10	—	—	10.0	mA
Circuit Current in Non-Operation (2)	$I_{CC(OFF)}$	V_{CC} = 11 V	2 − 10	—	0.7	1.5	mA
Startup Current (2)	I_{ST}		18 − 10	3.0	6.0	9.0	mA
Protection Operation Release Threshold Voltage(1)	$V_{CC(P.OFF)}$		2 − 10	7.8	8.9	9.8	V
Circuit Current in Protection	$I_{CC(P)}$	V_{CC} = 10 V	2 − 10	—	0.7	1.5	mA
Oscillator							
Minimum Frequency	$f_{(MIN)}$		11 – 10 16 – 15	27.5	31.5	35.5	kHz
Maximum Frequency	$f_{(MAX)}$		11 – 10 16 – 15	230	300	380	kHz
Minimum Dead-Time	$t_{d(MIN)}$		11 – 10 16 – 15	0.04	0.24	0.44	µs
Maximum Dead-Time	$t_{d(MAX)}$		11 – 10 16 – 15	1.20	1.65	2.20	µs
Externally Adjusted Minimum Frequency 1	$f_{(MIN)ADJ1}$	R_{CSS} = 30 kΩ	11 – 10 16 – 15	69	73	77	kHz
Externally Adjusted Minimum Frequency 2	$f_{(MIN)ADJ2}$	R_{CSS} = 77 kΩ	11 – 10 16 – 15	42.4	45.4	48.4	kHz
Feedback Control							
FB Pin Oscillation Start Threshold Voltage	$V_{FB(ON)}$		3 – 10	0.15	0.30	0.45	V
FB Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		3 – 10	0.05	0.20	0.35	V
FB Pin Maximum Source Current	$I_{FB(MAX)}$	V_{FB} = 0 V	3 – 10	−300	−195	−100	µA
FB Pin Reset Current	$I_{FB(R)}$		3 – 10	2.5	5.0	7.5	mA
Soft-start							
CSS Pin Charging Current	$I_{CSS(C)}$		5 – 10	−120	−105	−90	µA
CSS Pin Reset Current	$I_{CSS(R)}$	V_{CC} = 11V	5 – 10	1.1	1.8	2.5	mA
Maximum Frequency in Soft-start	$f_{(MAX)SS}$		11 – 10 16 – 15	400	500	600	kHz
Standby							
MODE Pin Standby Release Threshold Voltage	$V_{MODE(NRM)}$		9 – 10	4.5	5.0	5.5	V
MODE Pin Standby Threshold Voltage	$V_{MODE(STB)}$		9 – 10	1.35	1.5	1.65	V
MODE Pin Sink Current	$I_{MODE(SNK)}$		9 – 10	3	10	17	µA

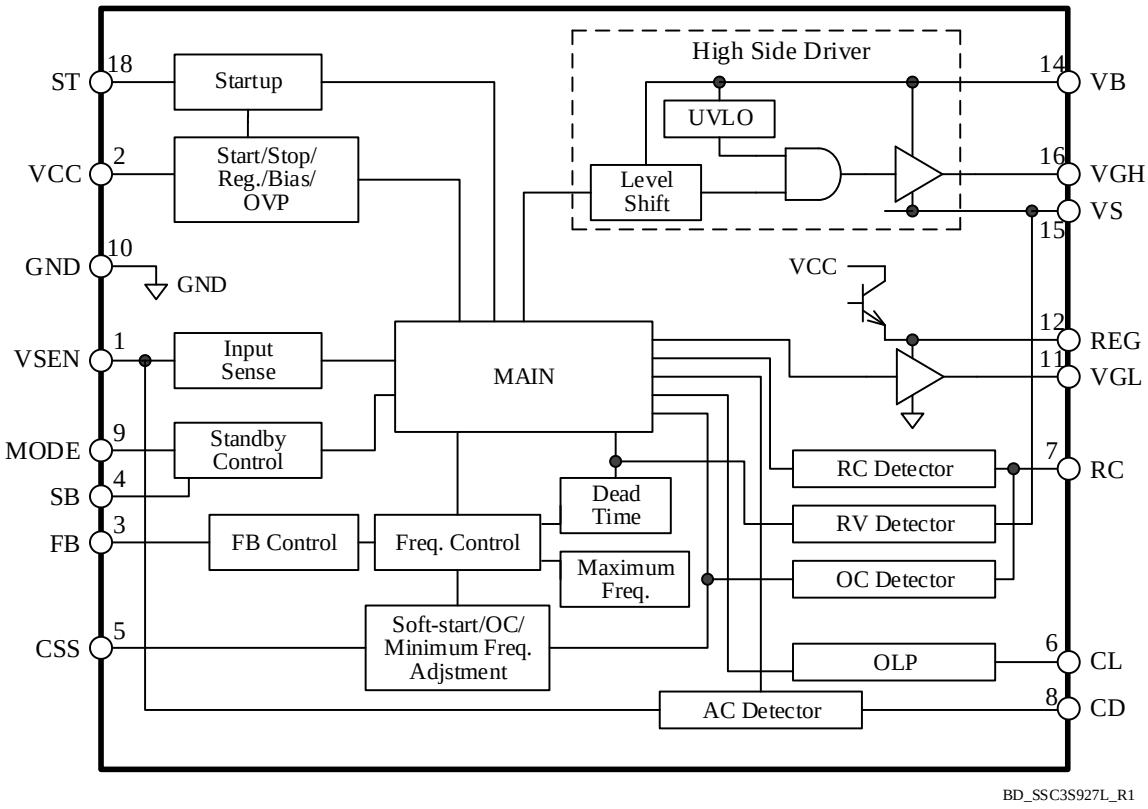
(1) $V_{CC(OFF)} = V_{CC(P.OFF)} < V_{CC(BIAS)}$ always.

(2) $I_{START} = I_{ST} - I_{CC(OFF)}$, where, I_{START} is VCC pin sink current in startup.

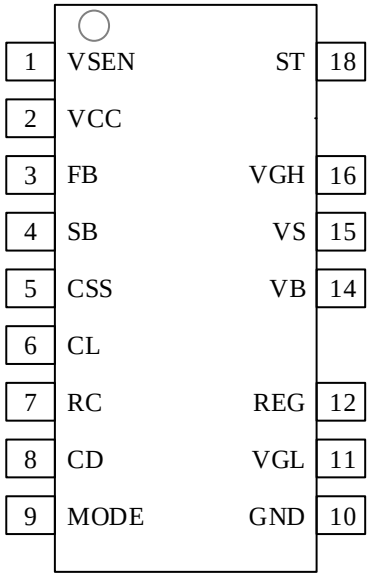
Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
MODE Pin Clamp Voltage	$V_{MODE(CLAMP)}$		9 – 10	7.0	8.5	10.0	V
SB Pin Oscillation Start Threshold Voltage	$V_{SB(ON)}$		4 – 10	0.5	0.6	0.7	V
SB Pin Oscillation Stop Threshold Voltage	$V_{SB(OFF)}$		4 – 10	0.4	0.5	0.6	V
SB Pin Source Current	$I_{SB(SRC)}$		4 – 10	−17	−10	−3	µA
SB Pin Sink Current	$I_{SB(SNK)}$		4 – 10	3	10	17	µA
Overload Protection (OLP)							
CL pin OLP Threshold Voltage	$V_{CL(OLP)}$		6 – 10	3.9	4.2	4.5	V
CL Pin Source Current 1	$I_{CL(SRC)1}$		6 – 10	−29	−17	−5	µA
CL Pin Source Current 2	$I_{CL(SRC)2}$		6 – 10	−180	−135	−90	µA
CL Pin Sink Current	$I_{CL(SNK)}$		6 – 10	10	30	50	µA
Input Undervoltage Protection (UVP)							
VSEN Pin Threshold Voltage (On)	$V_{SEN(ON)}$		1 – 10	1.150	1.200	1.250	V
VSEN Pin Threshold Voltage (Off) 1	$V_{SEN(OFF)1}$		1 – 10	0.955	1.000	1.045	V
VSEN Pin Threshold Voltage (Off) 2	$V_{SEN(OFF)2}$		1 – 10	—	0.8	—	V
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$		1 – 10	5.3	5.6	5.9	V
VSEN Pin Clamp Voltage	$V_{SEN\ (CLAMP)}$		1 – 10	10.0	—	—	V
VSEN pin Threshold Voltage for AC Line Detection 1	$V_{SEN(AC)1}$		1 – 10	2.56	2.70	2.84	V
VSEN Pin Threshold Voltage for AC Line Detection 2	$V_{SEN(AC)2}$		1 – 10	—	2.4	—	V
CD Pin Threshold Voltage 1	V_{CD1}		8 – 10	2.8	3.0	3.2	V
CD Pin Source Current	$I_{CD(SRC)}$	V_{CD} = 0 V	8 – 10	–12.0	–10.2	–8.5	µA
CD Pin Reset Current	$I_{CD(R)}$	V_{CD} = 2 V	8 – 10	1.0	2.5	4.0	mA
Reset Detection							
Maximum Reset Time	$t_{RST(MAX)}$		11 – 10 16 – 15	4	5	6	µs
Driver Circuit Power Supply							
VREG Pin Output Voltage	V_{REG}		12 – 10	9.6	10.0	10.8	V
High-side Driver							
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		14 – 15	5.7	6.8	7.9	V
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		14 – 15	5.5	6.4	7.3	V
Driver Circuit							
VGL,VGH Pin Source Current 1	$I_{GL(SRC)1}$ $I_{GH(SRC)1}$	V_{REG} = 10.5V V_B = 10.5V V_{GL} = 0V V_{GH} = 0V	11 – 10 16 – 15	—	–540	—	mA
VGL,VGH Pin Sink Current 1	$I_{GL(SNK)1}$ $I_{GH(SNK)1}$	V_{REG} = 10.5V V_B = 10.5V V_{GL} = 10.5V V_{GH} = 10.5V	11 – 10 16 – 15	—	1.50	—	A
VGL,VGH Pin Source Current 2	$I_{GL(SRC)2}$ $I_{GH(SRC)2}$	V_{REG} = 11.5V V_B = 11.5V V_{GL} = 10V V_{GH} = 10V	11 – 10 16 – 15	−140	−90	−40	mA

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
VGL,VGH Pin Sink Current 2	$I_{GL(SNK)2}$ $I_{GH(SNK)2}$	V_{REG} = 12V V_B = 12V V_{GL} = 1.5V V_{GH} = 1.5V	11 – 10 16 – 15	140	230	360	mA
Current Resonant and Overcurrent Protection(OCP)							
Capacitive Mode Detection Voltage 1	V_{RC1}		7 – 10	0.02	0.10	0.18	V
				−0.18	−0.10	−0.02	V
Capacitive Mode Detection Voltage 2	V_{RC2}		7 – 10	0.20	0.30	0.40	V
				−0.40	−0.30	−0.20	V
RC Pin Threshold Voltage (Low)	$V_{RC(L)}$		7 – 10	1.80	1.90	2.00	V
				−2.00	−1.90	−1.80	V
RC Pin Threshold Voltage (High speed)	$V_{RC(S)}$		7 – 10	2.62	2.80	2.98	V
				−2.98	−2.80	−2.62	V
CSS Pin Sink Current (Low)	$I_{CSS(L)}$		5 – 10	1.1	1.8	2.5	mA
CSS Pin Sink Current (High speed)	$I_{CSS(S)}$		5 – 10	13.0	20.5	28.0	mA
Overvoltage Protection (OVP)							
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 10	30.0	32.0	34.0	V
REG Pin OVP Threshold Voltage	$V_{CC(REG)}$		12 – 10	11.5	12.4	13.5	V
Thermal Shutdown (TSD)							
Thermal Shutdown Temperature	$T_{J(TSD)}$		—	140	—	—	°C
Thermal Resistance							
Junction to Ambient Thermal Resistance	θ_{J-A}		—	—	—	95	°C/W

3. Block Diagram



4. Pin Configuration Definitions



Number	Name	Function
1	VSEN	The mains input voltage detection signal input
2	VCC	Supply voltage input for the IC, and Overvoltage Protection (OVP) signal input
3	FB	Feedback signal input for constant voltage control
4	SB	Standby control capacitor connection
5	CSS	Soft-start capacitor connection
6	CL	Overload detection capacitor connection
7	RC	Resonant current detection signal input, and Overcurrent Protection (OCP) signal input
8	CD	Delay time setting capacitor connection
9	MODE	Standby mode change signal input
10	GND	Ground
11	VGL	Low-side gate drive output
12	REG	Supply voltage output for gate drive circuit
13	—	(Pin removed)
14	VB	Supply voltage input for high-side driver
15	VS	Floating ground for high-side driver
16	VGH	High-side gate drive output
17	—	(Pin removed)
18	ST	Startup current input

5. Typical Application

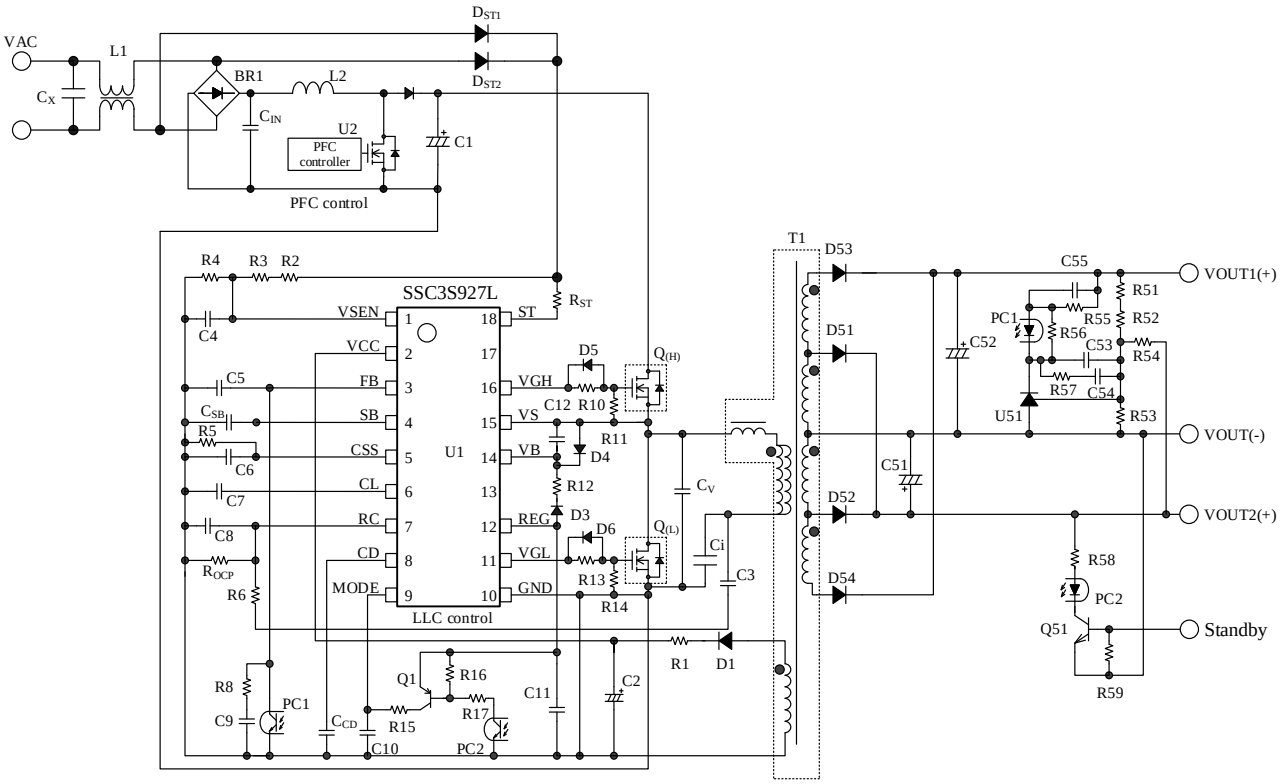
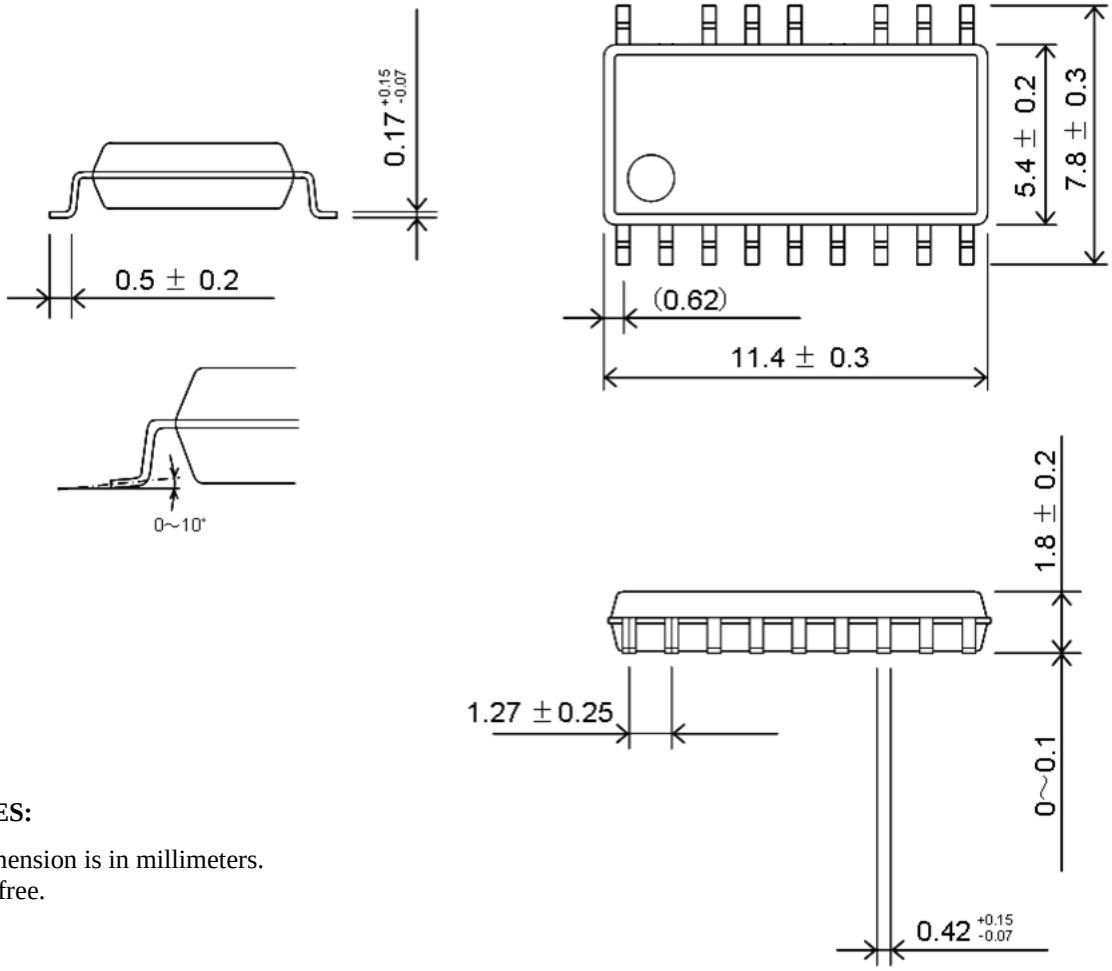


Figure 5-1. Typical Application

6. Physical Dimensions

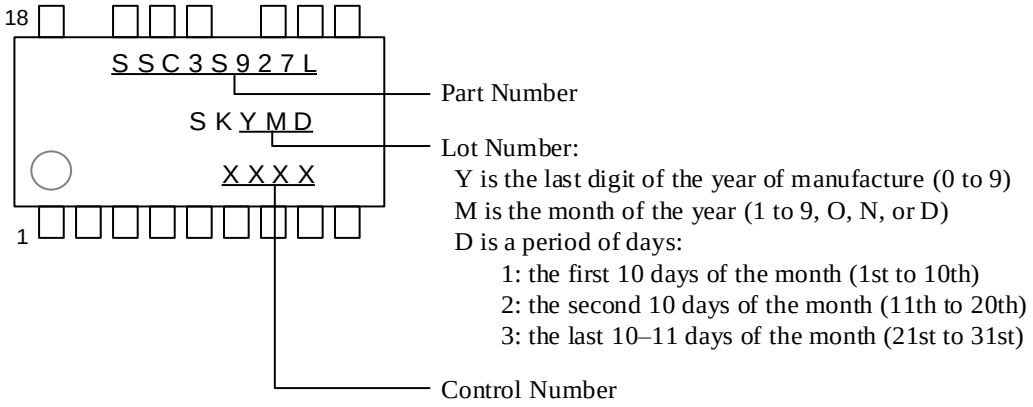
● SOP18



NOTES:

- Dimension is in millimeters.
- Pb-free.

7. Marking Diagram



8. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−). $Q_{(H)}$ and $Q_{(L)}$ indicate a high-side power MOSFET and a low-side power MOSFET respectively. Ci and C_V indicate a current resonant capacitor and a voltage resonant capacitor, respectively.

8.1 Resonant Circuit Operation

Figure 8-1 shows a basic RLC series resonant circuit.

The impedance of the circuit, $\dot{Z}$, is as the following Equation.

$$\dot{Z} = R + j\left(\omega L - \frac{1}{\omega C}\right), \quad (1)$$

where ω is angular frequency; and ω = 2πf.

Thus,

$$\dot{Z} = R + j\left(2\pi fL - \frac{1}{2\pi fC}\right). \quad (2)$$

When the frequency, f, changes, the impedance of resonant circuit will change as shown in Figure 8-2.

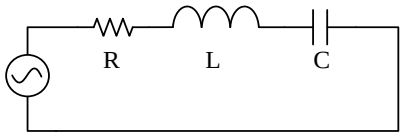


Figure 8-1. RLC Series Resonant Circuit

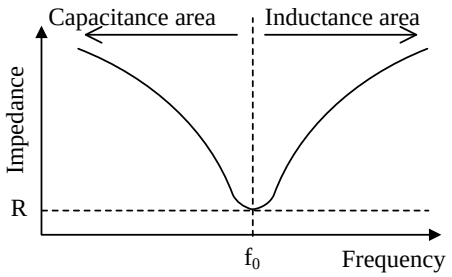


Figure 8-2. Impedance of Resonant Circuit

When 2πfL = 1/2πfC, $\dot{Z}$ of Equation (2) becomes the minimum value, R (see Figure 8-2). In the case, ω is calculated by Equation (3).

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}} \quad (3)$$

The frequency in which $\dot{Z}$ becomes minimum value is called a resonant frequency, f_0. The higher frequency area than f_0 is an inductance area. The lower frequency area than f_0 is a capacitance area.

From Equation (3), f_0 is as follows:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (4)$$

Figure 8-3 shows the circuit of a current resonant power supply. The basic configuration of the current resonant power supply is a half-bridge converter. The switching devices, $Q_{(H)}$ and $Q_{(L)}$, are connected in series with V_{IN}. The series resonant circuit and the voltage resonant capacitor, C_V, are connected in parallel with $Q_{(L)}$. The series resonant circuit is consisted of the following components: the resonant inductor, L_R; the primary winding, P, of a transformer, T1; and the current resonant capacitor, C_i. The coupling between the primary and secondary windings of T1 is designed to be poor so that the leakage inductance increases. This leakage inductance is used for L_R. This results in a down sized of the series resonant circuit. The dotted mark with T1 describes the winding polarity, the secondary windings, S1 and S2, are connected so that the polarities are set to the same position as shown in Figure 8-3. In addition, the winding numbers of each other should be equal. From Equation (1), the impedance of a current resonant power supply is calculated by Equation (5). From Equation (4), the resonant frequency, f_0, is calculated by Equation (6).

$$\dot{Z} = R + j\left\{\omega(L_R + L_P) - \frac{1}{\omega Ci}\right\}, \quad (5)$$

$$f_0 = \frac{1}{2\pi\sqrt{(L_R + L_P) \times Ci}}, \quad (6)$$

where:
R is the equivalent resistance of load,
L_R is the inductance of the resonant inductor,
L_P is the inductance of the primary winding P, and
Ci is the capacitance of current resonant capacitor.

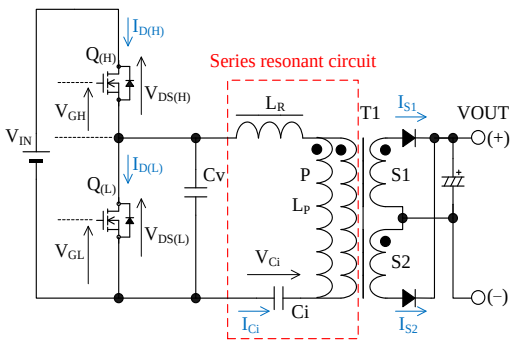


Figure 8-3. Current Resonant Power Supply Circuit

In the current resonant power supply, $Q_{(H)}$ and $Q_{(L)}$ are alternatively turned on and off. The on and off times of them are equal. There is a dead time between the on periods of $Q_{(H)}$ and $Q_{(L)}$. During the dead time, $Q_{(H)}$ and $Q_{(L)}$ are in off status.

In the current resonant power supply, the frequency is controlled. When the output voltage decreases, the IC decreases the switching frequency so that the output power is increased to keep a constant output voltage. This must be controlled in the inductance area ($f_{SW} < f_0$). Since the winding current is delayed from the winding voltage in the inductance area, the turn-on operates in a ZCS (Zero Current Switching); and the turn-off operates in a ZVS (Zero Voltage Switching). Thus, the switching losses of $Q_{(H)}$ and $Q_{(L)}$ are nearly zero. In the capacitance area ($f_{SW} < f_0$), the current resonant power supply operates as follows: When the output voltage decreases, the switching frequency is decreased; and then, the output power is more decreased. Therefore, the output voltage cannot be kept constant. Since the winding current goes ahead of the winding voltage in the capacitance area, $Q_{(H)}$ and $Q_{(L)}$ operate in the hard switching. This results in the increases of a power loss. This operation in the capacitance area is called the capacitive mode operation. The current resonant power supply must be operated without the capacitive mode operation (for more details, see Section 8.11).

Figure 8-4 describes the basic operation waveform of current resonant power supply (see Figure 8-3 about the symbol in Figure 8-4). For the description of current resonant waveforms in normal operation, the operation is separated into a period A to F. In the following description:

$I_{D(H)}$ is the current of $Q_{(H)}$,
$I_{D(L)}$ is the current of $Q_{(L)}$,
$V_{F(H)}$ is the forwerd voltage of $Q_{(H)}$,
$V_{F(L)}$ is the forwerd voltage of $Q_{(L)}$,
I_L is the current of L_R,
V_{IN} is an input voltage,
V_{Ci} is Ci voltage, and
V_{CV} is C_V voltage.

The current resonant power supply operations in period A to F are as follows:

1) Period A
When $Q_{(H)}$ is on, an energy is stored into the series resonant circuit by $I_{D(H)}$ that flows through the resonant circuit and the transformer (see Figure 8-5). At the same time, the energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

2) Period B
After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 8-6).

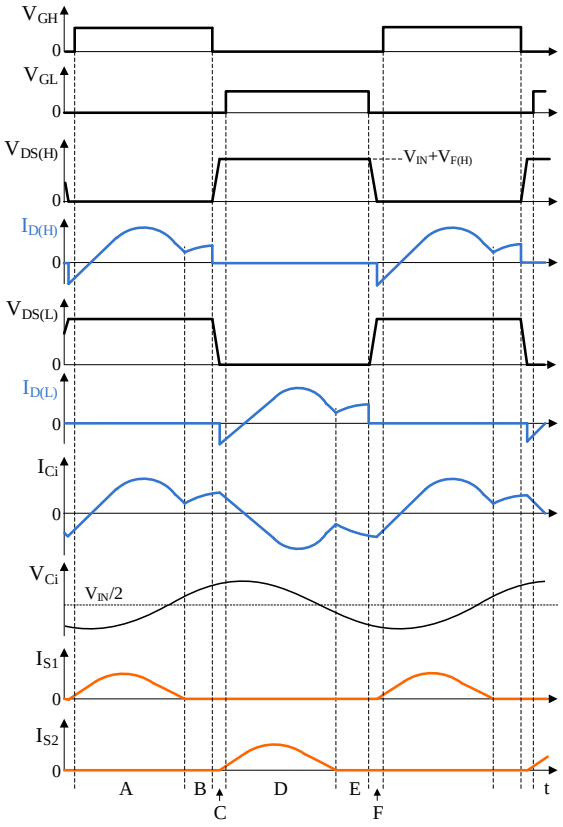


Figure 8-4. The Basic Operation Waveforms of Current Resonant Power Supply

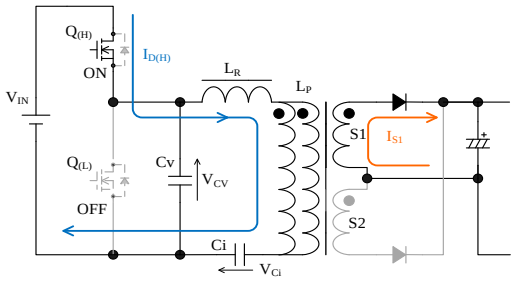


Figure 8-5. Operation in period A

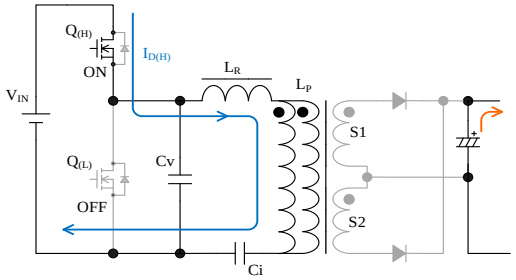


Figure 8-6. Operation in Period B

3) Period C

C is the dead-time period. $Q_{(H)}$ and $Q_{(L)}$ are in off status. When $Q_{(H)}$ turns off, C_V is discharged by I_L that is supplied by the energy stored in the series resonant circuit applies (see Figure 8-7). When V_{CV} decreases to $V_{F(L)}$, $-I_{D(L)}$ flows through the body diode of $Q_{(L)}$; and V_{CV} is clamped to $V_{F(L)}$. After that, $Q_{(L)}$ turns on. Since $V_{DS(L)}$ is nearly zero at the point, $Q_{(L)}$ operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

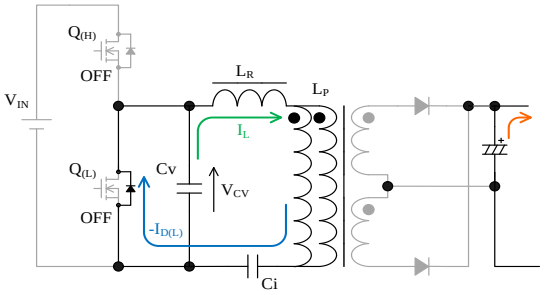


Figure 8-7. Operation in Period C

4) Period D

Immidiately after $Q_{(L)}$ turns on, $-I_{D(L)}$, which was flowing in Period C, continues to flow through $Q_{(L)}$ for a while. Then, $I_{D(L)}$ flows as shown in Figure 8-8; and V_{Ci} is applied the primary winding voltage of the transformer. At the same time, energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

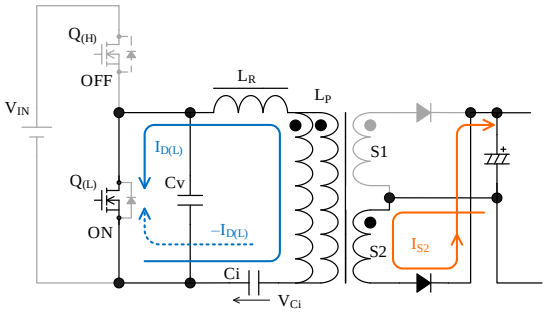


Figure 8-8. Operation in Period D

5) Period E

After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 8-9).

6) Period F

F is the dead-time period. $Q_{(H)}$ and $Q_{(L)}$ are in off status.

When $Q_{(L)}$ turns off, C_V is charged by $-I_L$ that is supplied by the energy stored in the series resonant circuit applies (see Figure 8-10). When V_{CV} decreases to $V_{IN} + V_{F(H)}$, $-I_{D(H)}$ flows through body diode of $Q_{(H)}$; and V_{CV} is clamped to $V_{IN} + V_{F(H)}$. After that, $Q_{(H)}$ turns on. Since $V_{DS(H)}$ is nearly zero at the point, $Q_{(H)}$ operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

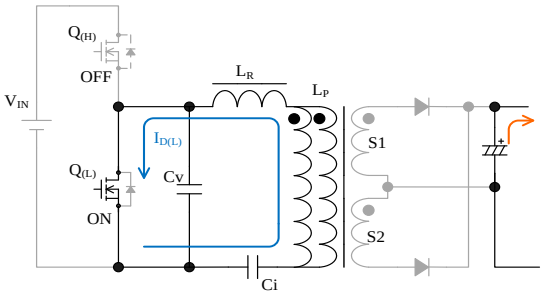


Figure 8-9. Operation in Period E

7) After the period F

Immidiately after $Q_{(H)}$ turns on, $-I_{D(H)}$, which was flowing in Period F, continues to flow through $Q_{(H)}$ for a while. Then, $I_{D(H)}$ flows again; and the operation returns to the period A. The above operation is repeated to transfer energy to the secondary side from the resonant circuit.

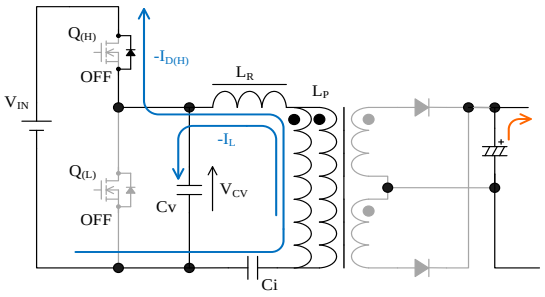


Figure 8-10. Operation in Period F

8.2 Startup Operation

The waveform at startup is shown in Figure 8-12.

When a mains input voltage is provided, and then the VSEN pin voltage increases to the on-threshold voltage, $V_{SEN(ON)}$ = 1.200 V, or more, C2 connected to the VCC pin is charged by the constant startup current, I_{ST} of 6.0 mA. When the VCC pin voltage increases to the operation start voltage, $V_{CC(ON)}$ = 17.0 V, the control circuit of the IC is activated. After that, when the VSEN pin voltage reaches $V_{SEN(ON)}$ = 1.200 V at the first-up edge of half-sinewave, REG pin voltage is output. Then, the capacitor C9 connected to FB pin starts to be charged. When the FB pin voltage increases to the oscillation start threshold voltage, $V_{FB(ON)}$ = 0.30 V, or more, the switching operation starts.

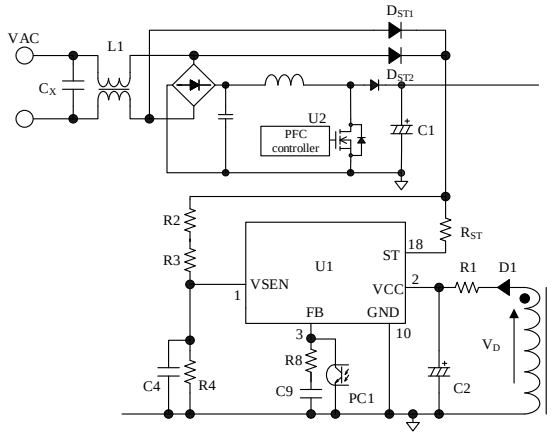


Figure 8-11. VCC Pin Peripheral Circuit

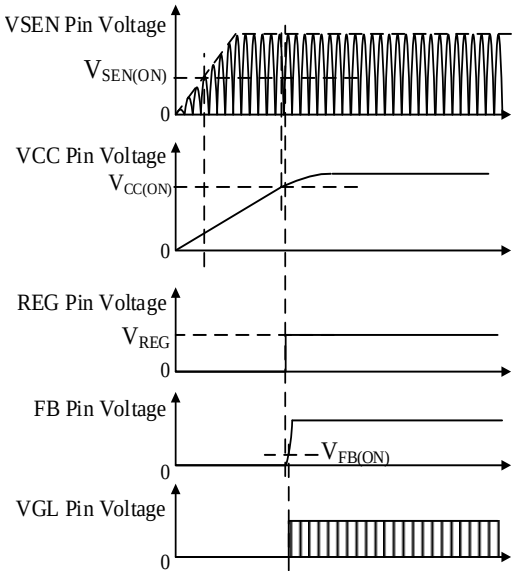


Figure 8-12. The Startup Operational Waveforms

8.3 Undervoltage Lockout (UVLO)

Figure 8-13 shows the relationship of V_{CC} and I_{CC}.

After the IC starts operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the IC stops switching operation by the Undervoltage Lockout (UVLO) Function and reverts to the state before startup again.

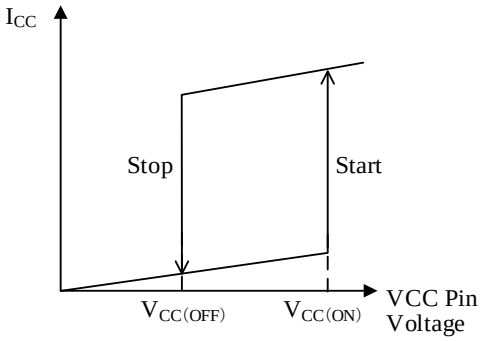


Figure 8-13. V_{CC} vs. I_{CC}

8.4 Bias Assist Function

Figure 8-14 shows the VCC pin voltage behavior during the startup period.

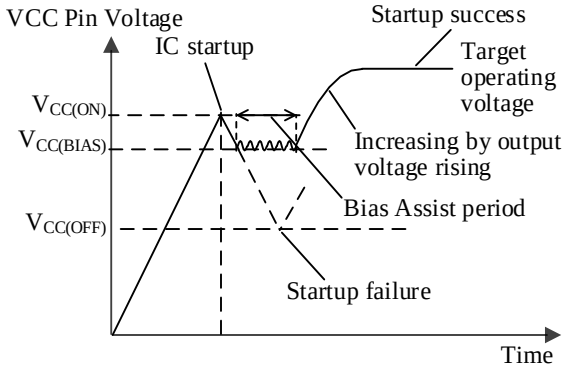


Figure 8-14. VCC Pin Voltage during Startup Period

When the conditions of Section 8.2 are fulfilled, the IC starts operation. Thus, the circuit current, I_{CC}, increases, and the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, V_D, increases in proportion to the output voltage rise. Thus, the VCC pin voltage is set by the balance between dropping due to the increase of I_{CC} and rising due to the increase of the auxiliary winding voltage, V_D.

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the IC stops switching operation and a startup failure occurs.

In order to prevent this, when the VCC pin voltage decreases to the startup current threshold biasing voltage, $V_{CC(BIAS)}$ = 9.8 V, the Bias Assist Function is activated.

While the Bias Assist Function is activated, any decrease of the VCC pin voltage is counteracted by providing the startup current, I_{ST}, from the startup circuit.

It is necessary to check the startup process based on actual operation in the application, and adjust the VCC pin voltage, so that the startup failure does not occur.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ and the Bias Assist Function is activated, the power loss increases.

Thus, the VCC pin voltage in operation should be set more than $V_{CC(BIAS)}$ by the following adjustments.

- The turns ratio of the auxiliary winding to the secondary-side winding is increased.
- The value of C2 in Figure 5-1 is increased and/or the value of R1 is reduced.

During all protection operation, the Bias Assist Function is disabled.

8.5 Soft Start Function

Figure 8-15 shows the Soft-start operation waveforms.

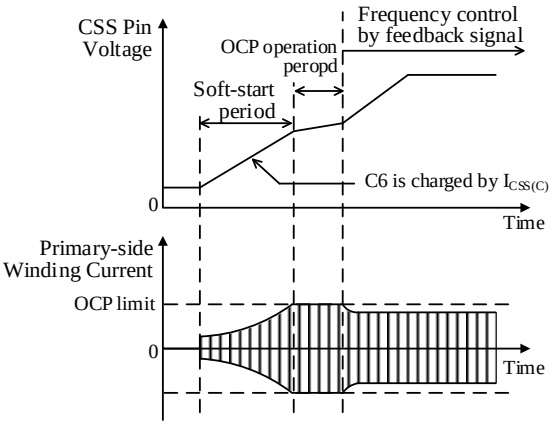


Figure 8-15. Soft-start Operation

The IC has Soft Start Function to reduce stress of peripheral component and prevent the capacitive mode operation.

During the soft start operation, C6 connected to the CSS pin is charged by the CSS Pin Charge Current, $I_{CSS(C)} = -105$ µA. The oscillation frequency is varied by the CSS pin voltage. The switching frequency gradually decreases from $f_{(MAX)SS}$* = 500 kHz at most, according to the CSS pin voltage rise. At same time, output power increases. When the output voltage increases, the IC is operated with an oscillation frequency controlled by feedback.

When the IC becomes any of the following conditions, C6 is discharged by the CSS Pin Reset Current, $I_{CSS(R)} = 1.8$ mA.

- The VCC pin voltage decreases to the operation stop voltage, $V_{CC(OFF)} = 8.9$ V, or less.
- After AC input voltage turns off, thr CD pin voltage increases to $V_{CD1} = 3.0$ V or more.
- Any of protection operations in protection mode (OVP, HVP, OLP or TSD) is activated.

8.6 Minimum and Maximum Switching Frequency Setting

The minimum switching frequency is adjustable by the value of R5 (R_{CSS}) connected to the CSS pin. The relationship of R5 (R_{CSS}) and the externally adjusted minimum frequency, $f_{(MIN)ADJ}$, is shown in Figure 8-16.

The $f_{(MIN)ADJ}$ should be adjusted to more than the resonant frequency, f_O, under the condition of the minimum mains input voltage and the maximum output power. The maximum switching frequency, f_{MAX}, is determined by the inductance and the capacitance of the resonant circuit. The f_{MAX} should be adjusted to less than the maximum frequency, $f_{(MAX)} = 300$ kHz.

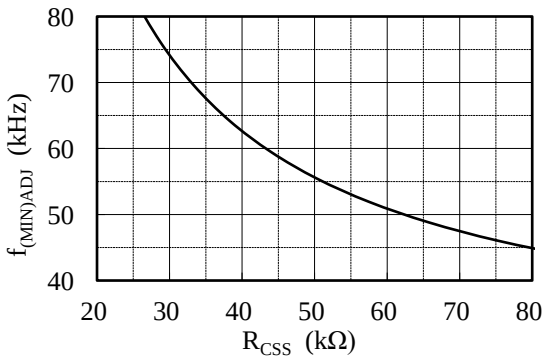


Figure 8-16. R5 (R_{CSS}) vs. $f_{(MIN)ADJ}$

8.7 High-side Driver

Figure 8-17 shows a bootstrap circuit. The bootstrap circuit is for driving to $Q_{(H)}$ and is made by D3, R12 and C12 between the REG pin and the VS pin.

When $Q_{(H)}$ is OFF state and $Q_{(L)}$ is ON state, the VS pin voltage becomes about ground level and C12 is charged from the REG pin.

When the voltage of between the VB pin and the VS pin, V_{B-S}, increases to $V_{BUV(ON)} = 6.8$ V or more, an internal high-side drive circuit starts operation. When V_{B-S} decreases to $V_{BUV(OFF)} = 6.4$ V or less, its drive circuit stops operation. In case the both ends of C12 and D4 are short, the IC is protected by $V_{BUV(OFF)}$. D4 for

* The maximum frequency during normal operation is $f_{(MAX)} = 300$ kHz.

protection against negative voltage of the VS pin

- D3
  D3 should be an ultrafast recovery diode of short recovery time and low reverse current. When the maximum mains input voltage of the apprication is 265VAC, it is recommended to use ultrafast recovery diode of V_{RM} = 600 V.

- C11, C12, and R12
  The values of C11, C12, and R12 are determined by total gate charge, Qg, of external MOSFET and voltage dip amount between the VB pin and the VS pin in the burst oscillation mode of the standby mode change.
  C11, C12, and R12 should be adjusted so that the voltage between the VB pin and the VS is more than $V_{BUV(ON)}$ = 6.8 V by measuring the voltage with a high-voltage differential probe.
  The reference value of C11 is 0.47μF to 1 μF.
  The time constant of C12 and R12 should be less than 500 ns. The values of C12 and R22 are 0.047μF to 0.1 μF, and 2.2 Ω to 10 Ω.
  C11 and C12 should be a film type or ceramic capacitor of low ESR and low leakage current.

- D4
  D4 should be a Schottky diode of low forward voltage, V_F, so that the voltage between the VB pin and the VS pin must not decrease to the absolute maximum ratings of −0.3 V or less.

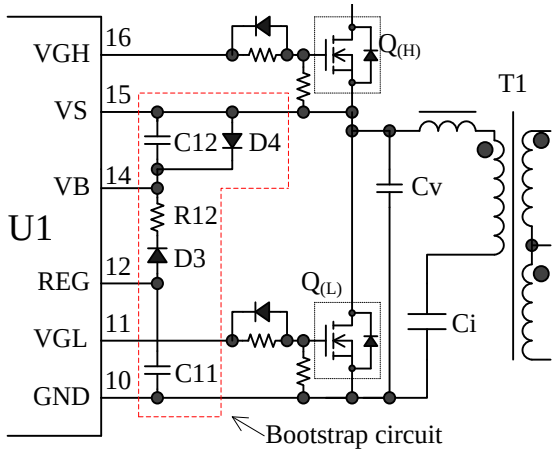


Figure 8-17. Bootstrap Circuit

8.8 Constant Voltage Control Operation

Figure 8-18 shows the FB pin peripheral circuit. The FB pin is sunk the feedback current by the photo-coupler, PC1, connected to FB pin. As a result, since the oscillation frequency is controlled by the FB pin, the output voltage is controlled to constant voltage (in inductance area).

The feedback current increases under slight load condition, and thus the FB pin voltage decreases. While the FB pin voltage decreases to the oscillation stop threshold voltage, $V_{FB(OFF)}$ = 0.20 V, or less, the IC stops switching operation. This operation reduces switching loss, and prevents the increasing of the secondary output voltage. In Figure 8-18, R8 and C9 are for phase compensation adjustment, and C5 is for high frequency noise rejection.

The secondary-side circuit should be designed so that the collector current of PC1 is more than 195 μA which is the absolute value of the maximum source current, $I_{FB(MAX)}$. Especially the current transfer ratio, CTR, of the photo coupler should be taken aging degradation into consideration.

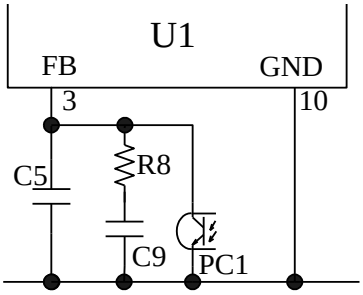


Figure 8-18. FB Pin Peripheral Circuit

8.9 Standby Function

The IC has the Standby Function in order to increase circuit efficiency in light load. When the Standby Function is activated, the IC operates in the burst oscillation mode as shown in Figure 8-19.

The burst oscillation has periodic non-switching intervals. Thus, the burst oscillation mode reduces switching losses. Generally, to improve efficiency under light load conditions, the frequency of the burst oscillation mode becomes just a few kilohertz. In addition, the IC has the Soft-on and the Soft-off Function in order to suppress rapid and sharp fluctuation of the drain current during the burst oscillation mode. thus, the audible noises can be reduced (see Section 8.9.2). The operation of the IC changes to the standby operation by the external signal (see Section 8.9.1).

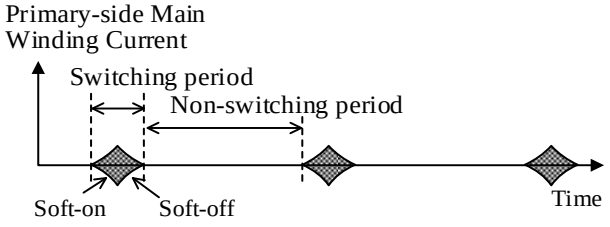


Figure 8-19. Standby Waveform

8.9.1 Standby Mode Changed by External Signal

Figure 8-20 shows the standby mode change circuit with external signal. Figure 8-21 shows the standby change operation waveforms. When the standby terminal of Figure 8-20 is provided with the L signal, Q1 turns off, C10 connected to the MODE pin is discharged by the sink current, $I_{MODE(SNK)}$ = 10 µA, and then the MODE pin voltage decreases. When the MODE pin voltage decrease to the MODE Pin Standby Threshold Voltage, $V_{MODE(STB)}$ = 1.5 V, the operation of the IC is changed to the standby mode. In the standby mode, the IC stops a switching operation while the following conditions are fulfilled: MODE pin voltage ≤ $V_{MODE(STB)}$ of 1.5 V, FB pin voltage ≤ $V_{FB(OFF)}$ of 0.20 V, and SB pin voltage ≤ $V_{SB(OFF)}$ of 0.5 V.

When the standby terminal is provided with the H signal and the SB pin voltage increases to Standby Release Threshold Voltage, $V_{MODE(NRM)}$ = 5.0 V, or more, the IC returns to normal operation.

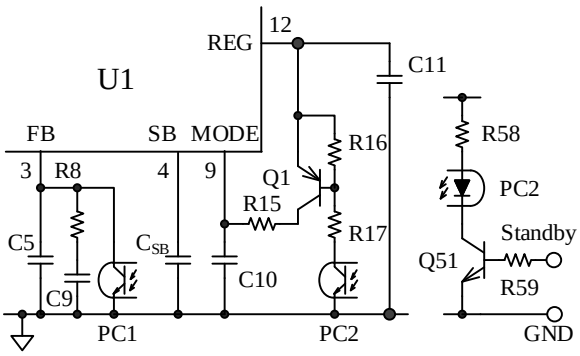


Figure 8-20. Standby Mode Change Circuit

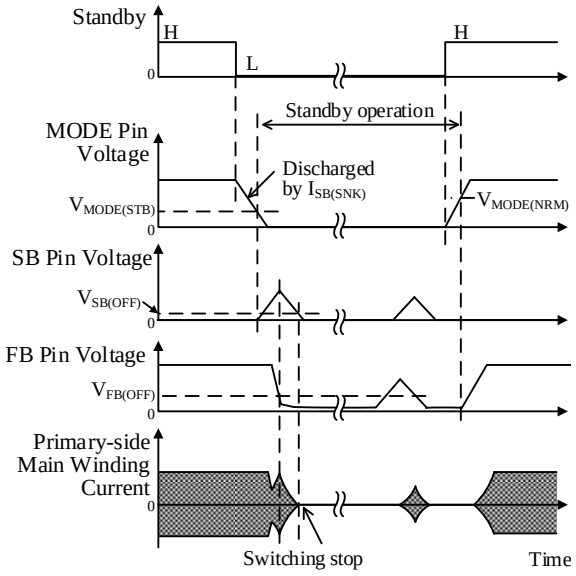


Figure 8-21. Standby Change Operation Waveforms

8.9.2 Burst Oscillation Operation

In standby operation, the IC operates burst oscillation where the peak drain current is suppressed by Soft-On /Soft-off Function in order to reduce audible noise from transformer. During burst oscillation operation, the switching oscillation is controlled by the SB pin voltage.

Figure 8-22 shows the burst oscillation operation waveforms.

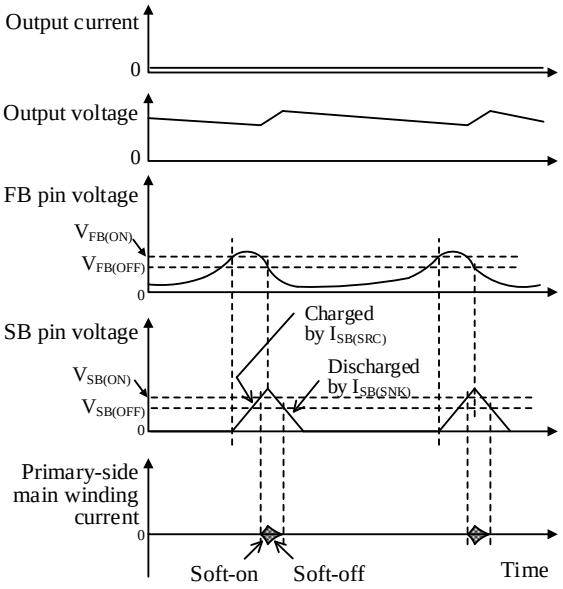


Figure 8-22. Burst Oscillation Operation Waveforms

When the SB pin voltage decreases to $V_{SB(OFF)}$ = 0.5 V or less and the FB pin voltage decreases to $V_{FB(OFF)}$ = 0.20 V or less, the IC stops switching operation, and then the output voltage decreases. Since the output voltage decreases, the FB pin voltage increases. When the FB pin voltage increases to the oscillation start threshold voltage, $V_{FB(ON)}$ = 0.30 V, C_{SB} connected to the SB pin is charged by $I_{SB(SRC)}$ = −10 µA, and the SB pin voltage gradually increases. When the SB pin voltage increases to the oscillation start threshold voltage, $V_{SB(ON)}$ = 0.6 V, the IC resumes switching operation, controlling the frequency control by the SB pin voltage. Thus, the output voltage increases (Soft-on). After that, when FB pin voltage decrease to oscillation stop threshold voltage, $V_{FB(OFF)}$ = 0.20 V, C_{SB} is discharged by $I_{SB(SNK)}$ = 10 µA and SB pin voltage decreases. When the SB pin voltage decreases to $V_{SB(OFF)}$ again, the IC stops switching operation. Thus, the output voltage decreases (Soft-off).

The SB pin discharge time in the Soft-on and Soft-off Function depends on the value of C_{SB}. When the value of C_{SB} increases, the Soft-On/Soft-off Function makes the peak drain current suppressed, and makes the burst period longer. Thus, the output ripple voltage may increase and/or the VCC pin voltage may decrease. If

the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.8 V, the Bias Assist Function is always activated, and it results in the increase of power loss (see Section 8.4).

Thus, it is necessary to adjust the value of C_{SB} during checking the input power, the output ripple voltage, and the VCC pin voltage. The reference value of C_{SB} is about 0.001 µF to 0.1 µF.

8.10 Automatic Dead Time Adjustment Function

The dead time is the period when both the high-side and the low-side power MOSFETs are off.

As shown in Figure 8-23, if the dead time is shorter than the voltage resonant period, the power MOSFET is turned on and off during the voltage resonant operation. In this case, the power MOSFET turned on/off in hard switching operation, and the switching loss increases.

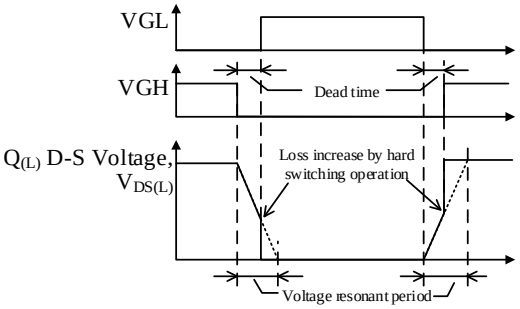


Figure 8-23. ZVS Failure Operation Waveform

The Automatic Dead Time Adjustment Function is the function that the ZVS (Zero Voltage Switching) operation of $Q_{(H)}$ and $Q_{(L)}$ is controlled automatically by the voltage resonant period detection of IC. The voltage resonant period is varied by the power supply specifications (input voltage and output power, etc.). However, the power supply with this function is unnecessary to adjust the dead time for each power supply specification.

As shown in Figure 8-24, the VS pin detects the dv/dt period of rising and falling of the voltage between drain and source of the low-side power MOSFET, $V_{DS(L)}$, and the IC sets its dead time to that period. This function controls so that the high-side and the low-side power MOSFETs are automatically switched to Zero Voltage Switching (ZVS) operation. This function operates in the period from $t_{d(MIN)}$ = 0.24 µs to $t_{d(MAX)}$ = 1.65 µs.

In minimum output power at maximum input voltage and maximum output power at minimum input voltage, the ZCS (Zero Current Switching) operation of IC (the drain current flows through the body diode is about 600 ns as shown in Figure 8-25), should be checked based on actual operation in the application.

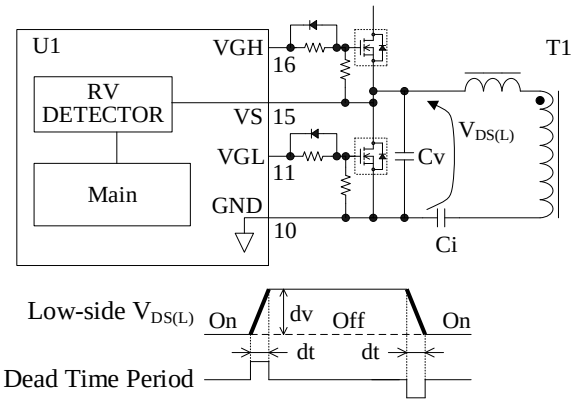


Figure 8-24. VS Pin and Dead Time Period

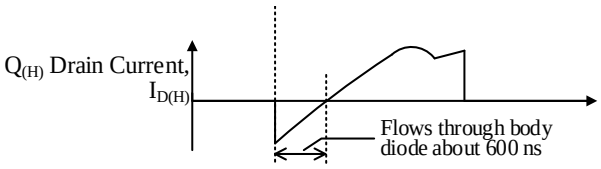


Figure 8-25. ZCS Check Point

8.11 Capacitive Mode Detection Function

The resonant power supply is operated in the inductance area shown in Figure 8-26. In the capacitance area, the power supply becomes the capacitive mode operation (see Section 8.1). In order to prevent the operation, the minimum oscillation frequency is needed to be set higher than f_0 on each power supply specification. However, the IC has the capacitive mode operation Detection Function kept the frequency higher than f_0. Thus, the minimum oscillation frequency setting is unnecessary and the power supply design is easier. In addition, the ability of transformer is improved because the operating frequency can operate close to the resonant frequency, f_0.

The resonant current is detected by the RC pin, and the IC prevents the capacitive mode operation. When the capacitive mode is detected, C7 connected to the CL pin is charged by $I_{CL(SRC)1}$ = −17 µA. When the CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated and the switching operation stops. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 8.18). The detection voltage is changed to V_{RC1} = ±0.10 V or V_{RC2} = ±0.30 V depending on the load as shown in Figure 8-28 and Figure 8-29. The Capacitive Mode Operation Detection Function operations as follows:

- **Period in Which the $Q_{(H)}$ is On**

  Figure 8-27 shows the RC pin waveform in the inductance area, and Figure 8-28 and Figure 8-29 shows the RC pin waveform in the capacitance area.

  In the inductance area, the RC pin voltage doesn't

cross the plus side detection voltage in the downward direction during the on period of $Q_{(H)}$ as shown in Figure 8-27. On the contrary, in the capacitance area, the RC pin voltage crosses the plus side detection voltage in the downward direction. At this point, the capacitive mode operation is detected. Thus, $Q_{(H)}$ is turned off, and $Q_{(L)}$ is turned on, as shown in Figure 8-28 and Figure 8-29.

- **Period in Which the $Q_{(L)}$ is On**
  Contrary to the above of $Q_{(H)}$, in the capacitance area, the RC pin voltage crosses the minus side detection voltage in the upward directiont during the on period of $Q_{(L)}$ At this point, the capacitive mode operation is detected. Thus, $Q_{(L)}$ is turned off and $Q_{(H)}$ is turned on.

As above, since the capacitive mode operation is detected by pulse-by-pulse and the operating frequency is synchronized with the frequency of the capacitive mode operation, and the capacitive mode operation is prevented. In addition to the adjusting method of R_{OCP}, C3, and R6 in Section 8.17, R_{OCP}, C3, and R6 should be adjusted so that the absolute value of the RC pin voltage increases to more than $|V_{RC2}|$ = 0.30 V under the condition caused the capacitive mode operation easily, such as startup, turning off the mains input voltage, or output shorted. The RC pin voltage must be within the absolute maximum ratings of −6 to 6 V.

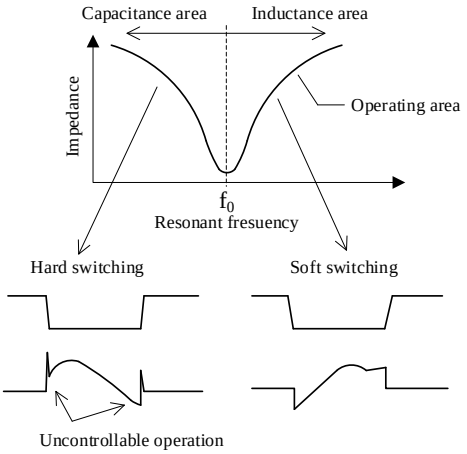


Figure 8-26. Operating Area of Resonant Power Supply

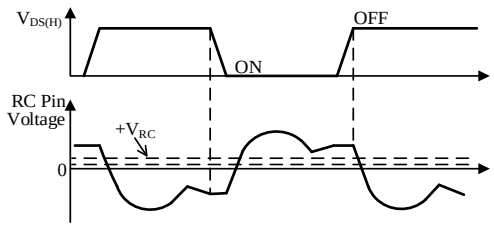


Figure 8-27. RC Pin Voltage in Inductance Area

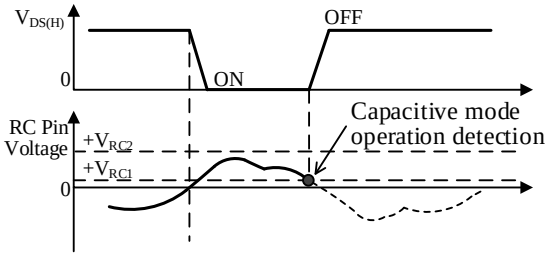


Figure 8-28. High-side Capacitive Mode Detection in Light Load

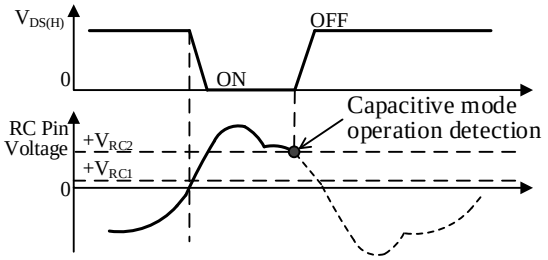


Figure 8-29. High-side Capacitive Mode Detection in Heavy Load

8.12 X-Capacitor Discharge Function

Generally, the line filter is set in the input circuit part of power supply as shown in Figure 8-30.

The voltage across the X-capacitor, C_X, must be decreased to 37 % of the peak voltage of AC input in one second to meet safety requirements such as IEC60950. Thus, the discharge resistor, R_{DIS}, is connected in parallel with C_X. While the AC input voltage is applied, R_{DIS} consumes power at all time. The dissipation power of R_{DIS}, P_{RDIS}, is calculated as follows:

$$P_{RDIS} = \frac{V_{AC(RMS)}{}^2}{R_{DIS}} \quad (7)$$

where, $V_{AC(RMS)}$ is the effective value of AC input voltage.

When the combined resistance of R_{DIS} is 1 MΩ and the AC input voltage is 265 V, P_{RDIS} becomes about 70 mW.

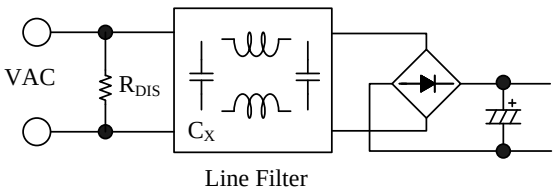


Figure 8-30. Typical Line Filter Circuit

In order to remove R_{ST} and improve the circuit efficiency, the IC has the X-capacitor Discharge Function. As shown in Figure 8-31, D_{ST1}, D_{ST2} and R_{ST} are connected to the ST pin from AC input line.

When the AC voltage is input and VSEN pin voltage reaches $V_{SEN(ON)}$ = 1.200 V at startup, the IC starts.

Then, following half-sinewaves are detected by two threshold voltages of the VSEN pin, $V_{SEN(OFF)1}$ = 1.000 V or $V_{SEN(AC)1}$ = 2.70 V (see Figure 8-32). Thus the IC's X-Capacitor Discharge Function achieves the wide range detection for universal specification.

When the AC input voltage is cut off, the VSEN pin voltage becomes practically constant and the VSEN pin cannot detect the both threshold, $V_{SEN(OFF)1}$ and $V_{SEN(AC)1}$. Then, the CD pin capacitor, C_{CD}, is discharged by $I_{CD(SRC)}$ = –10.2 µA, and the CD pin voltage increases. When the CD pin voltage reaches V_{CD1} = 3.0 V, the X-capacitor is discharged by the constant current, I_{ST} = 6.0 mA.

When the VSEN pin voltage becomes $V_{SEN(OFF)1}$ or $V_{SEN(AC)1}$, each internal threshold voltage becomes $V_{SEN(OFF)2}$ = 0.8 V or $V_{SEN(AC)2}$ = 2.4 V automatically. Thus, the input voltage can be detected stably.

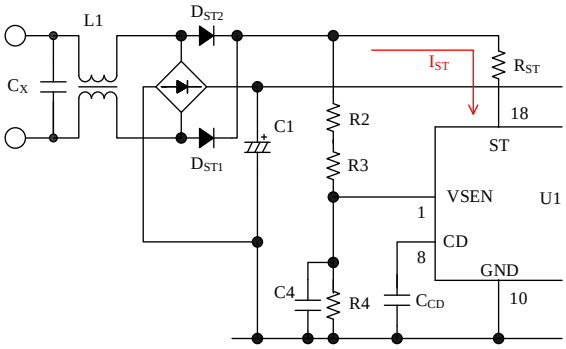


Figure 8-31. ST Pin Peripheral Circuit

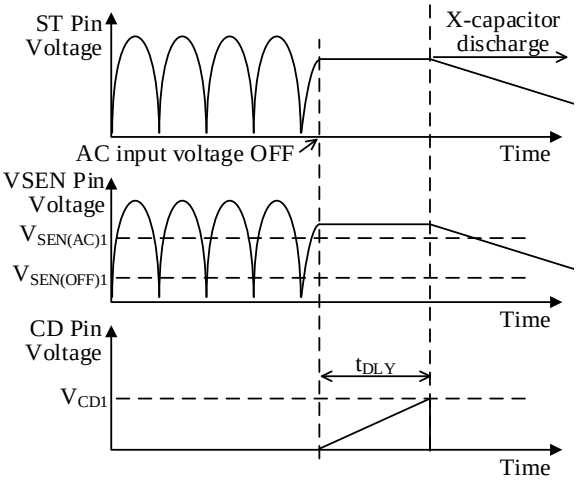


Figure 8-32. Operational Waveform of X-capacitor Discharge Function

The time until the CD pin voltage reaches V_{CD1} from the cutoff of AC input voltage is delay time, t_{DLY}.

The maximum value of t_{DLY}, t_{DLY_MAX}, can be set by the capacitor of the CD pin and is calculated by Equation (9) in Section 8.16.2.

The recommend value of R_{ST} is 5.6 kΩ to 10 kΩ. R_{ST} is applied high voltage and are high resistance, the following should be considered according to the requirement of the application:

- Select a resistor designed against electromigration, or
- Use a combination of resistors in series for that to reduce each applied voltage

8.13 Reset Detection Function

In the startup period, the feedback control for the output voltage is inactive. If a magnetizing current may not be reset in the on-period because of unbalanced operation, a negative current may flow just before a power MOSFET turns off. This causes a hard switching operation, increases the stresses of the power MOSFET. Where the magnetizing current means the circulating current applied for resonant operation, and flows only into the primary-side circuit. To prevent the hard switching, the IC has the reset detection function.

Figure 8-34 shows the high-side operation and the reference drain current waveforms in a normal resonant operation and a reset failure operation. To prevent the hard switching operation, the reset detection function operates such as an on period is extended until the absolute value of a RC pin voltage, $|V_{RC1}|$, increases to 0.10 V or more. When the on period reaches the maximum reset time, $t_{RST(MAX)}$ = 5 µs, the on-period expires at that moment, i.e., the power MOSFET turns off (see Figure 8-33).

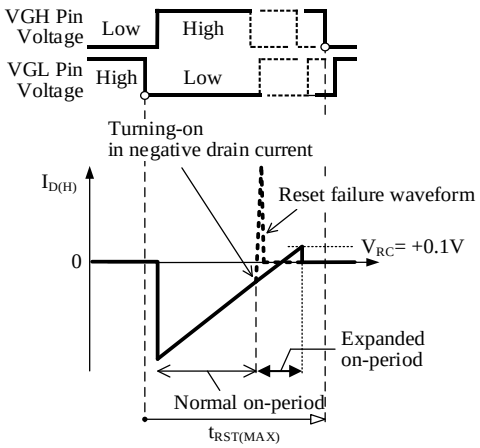


Figure 8-33. Reset Detection Operation Example at High-side On Period

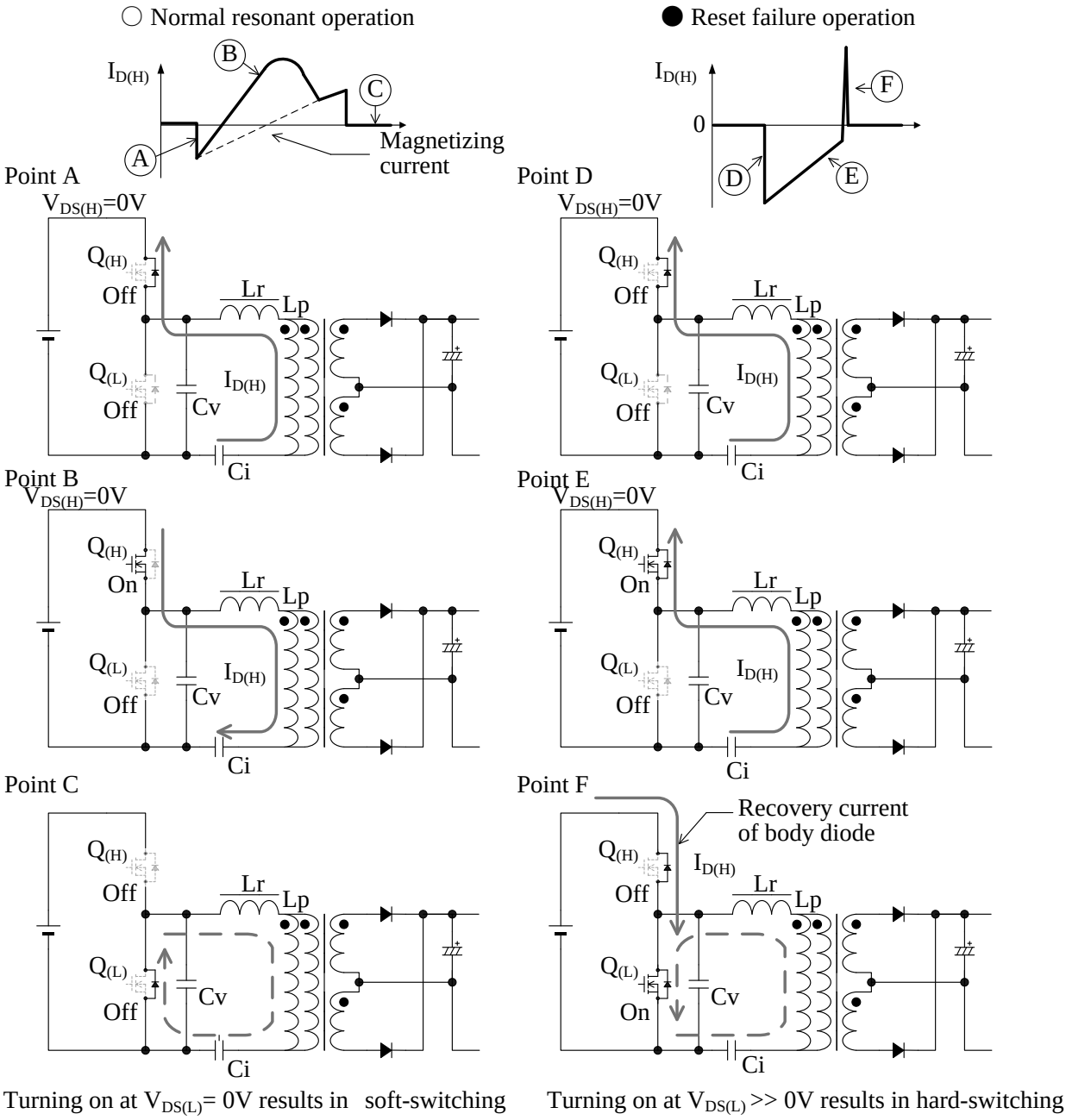


Figure 8-34. Reference High-side Operation and Drain Current Waveforms in Normal Resonant Operation and in Reset Failure Operation

8.14 Overvoltage Protection (OVP)

When the voltage between the VCC pin and the GND pin is applied to the OVP threshold voltage, $V_{CC(OVP)}$ = 32.0 V, or more, the Overvoltage Protection (OVP) is activated, and the IC stops switching operation in protection mode. When the OVP activates, the Bias Assist Function is disabled and the VCC pin voltage decreases. Then the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.9 V, the Undervoltage Lockout (UVLO) Function is activated, and the IC reverts to the state before startup again.

After that, the startup circuit activates, and the VCC pin voltage increases to $V_{CC(ON)}$ = 17.0 V, and the IC starts operation. During the protection mode, restart and stop are repeated. When the fault condition is removed, the IC returns to normal operation automatically. When the auxiliary winding supplies the VCC pin voltage, the OVP is able to detect an excessive output voltage, such as when the detection circuit for output control is open in the secondary-side circuit because the VCC pin voltage is proportional to the output voltage.

The output voltage of the secondary-side circuit at OVP operation, $V_{OUT(OVP)}$, is approximately given as below:

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 32(V) \quad (8)$$

where, $V_{OUT(NORMAL)}$ is output voltage in normal operation, and $V_{CC(NORMAL)}$ is VCC pin voltage in normal operation

8.15 REG Overvoltage Protection (REG_OVP)

The IC has REG Overvoltage Protection (REG_OVP) for the overvoltage of the REG pin.

When the REG pin voltage increases to REG Pin OVP Threshold Voltage, $V_{REG(OVP)}$ = 12.4 V, the REG_OVP is activated, and the IC stops switching operation and fixes the REG pin voltage to ground level.

When the REG_OVP activates, the Bias Assist Function is disabled and the VCC pin voltage decreases. Then the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.9 V, the Undervoltage Lockout (UVLO) Function is activated, and the IC reverts to the state before startup again.

After that, the startup circuit activates, and the VCC pin voltage increases. When the VCC pin voltage reaches $V_{CC(ON)}$ = 17.0 V, the IC starts operation and the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, FB pin voltage increases and switching operation starts.

When the switching operation starts at RC pin voltage within V_{RC1} = ±0.10 V, C7 connected to CL pin is rapidly charged by $I_{CL(SRC)2}$ = −135 μA. When the CL pin voltage reaches $V_{CL(OLP)}$ = 4.2 V, the IC stops switching operation and restarts after decreasing to $V_{CC(OFF)}$.

In this way, the intermittent operation by the CL pin protection and the UVLO is repeated.

When the fault condition is removed, the IC returns to normal operation automatically.

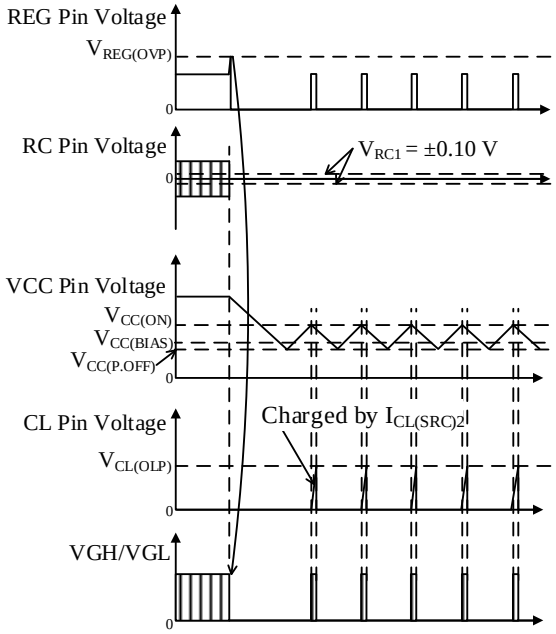


Figure 8-35. REG_OVP Waveform

8.16 Input Voltage Detection Function

This function has the following:

- Input Overvoltage Protection (HVP)
- Input Undervoltage Protection (UVP)

This function turns on and off switching operation according to the VSEN pin voltage detecting the AC input voltage, and thus prevents excessive input current and over heating. Section 8.16.1 shows HVP, Section 8.16.2 shows UVP. Figure 8-36 shows the pherepheral circuit of VSEN pin. Figure 8-37 shows Input Voltage Detection Function operational waveforms.

8.16.1 Input Overvoltage Protection (HVP)

When the AC input voltage increases from steady state and the VSEN pin voltage reaches $V_{SEN(HVP)}$ = 5.6 V or more, Input Overvoltage Protection (HVP) activates and the IC stops switching operation. During the HVP operation, the intermittent operation by UVLO is repeated (see Section 8.14). After that, when the AC input voltage decreases and the VSEN pin voltage falls to $V_{SEN(HVP)}$ or less, the IC starts switching operation.

8.16.2 Input Undervoltage Protection (UVP)

Even if the IC is in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, when the AC input voltage decreases from steady-state and the VSEN pin voltage falls to $V_{SEN(OFF)1}$ = 1.000 V or less for the delay time, t_{DLY}, the IC stops switching operation.

When the AC input voltage increases and the VSEN pin voltage reaches $V_{SEN(ON)}$ = 1.200 V or more in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, the IC starts switching operation.

The maximum delay time, t_{DLY_MAX}, can be calculated by Equation (9).

$$t_{DLY\_MAX} = \frac{V_{CD1} \times C_{CD}}{|I_{CD(SRC)}|} \quad (9)$$

Where,

V_{CD1} is CD Pin Threshold Voltage 1 (3.0 V),

C_{CD} is the capacitance value of CD pin connected capacitor (about 0.1µF to 0.47µF), and

$I_{CD(SRC)}$ is CD Pin Source Current (–10.2 µA)

For example, if C_{CD} is 0.1µF,

$$t_{DLY\_MAX} = \frac{3.0\ V \times 0.1\mu F}{|-10.2\ \mu A|} \approx 29.4\ ms$$

Neglecting the effect of both input resistance and forward voltage of rectifier diode, the effective value of AC input voltage when HVP and UVP are activated is calculated as follows:

$$V_{AC(OP)} = \frac{1}{\sqrt{2}} \times V_{SEN(TH)} \times \left(1 + \frac{R2 + R3}{R4}\right) \quad (10)$$

where,

$V_{DC(OP)}$ is the effective value of AC input voltage when HVP and UVP are activated, and

$V_{SEN(TH)}$ is any one of threshold voltage of VSEN pin (see Table 8-1).

Table 8-1. VSEN Pin Threshold Voltage

Parameter	Symbol	Value (Typ.)
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$	5.6 V
VSEN Pin Threshold Voltage (On)	$V_{SEN(OFF)1}$	1.000 V
VSEN Pin Threshold Voltage (Off)	$V_{SEN(ON)}$	1.200 V

Because R2 and R3 are applied high voltage and are high resistance, the following should be considered:

- Select a resistor designed against electromigration according to the requirement of the application, or
- Use a combination of resistors in series for that to reduce each applied voltage.

The reference value of R2 is about 10 MΩ.

C4 shown in Figure 8-36 is for reducing noises. The value is 1000 pF or more, and the reference value is about 0.01 µF.

The value of R2, R3 and R4 and C4 should be selected based on actual operation in the application.

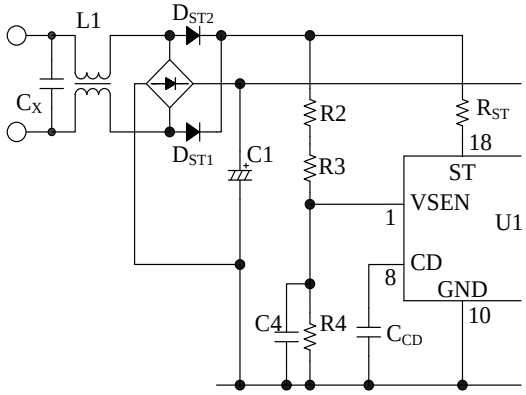


Figure 8-36. VSEN Pin Pherepheral Circuit

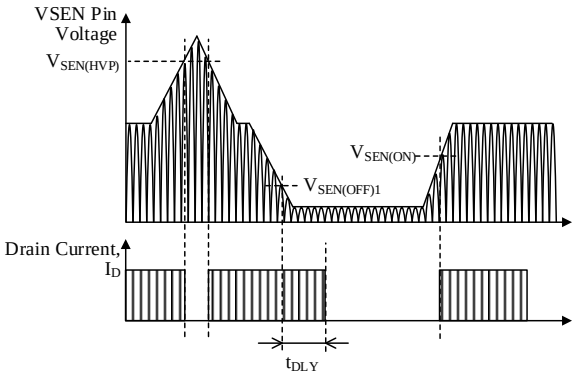


Figure 8-37. Input Voltage Detection Function Operational Waveforms

8.17 Overcurrent Protection (OCP)

The Overcurrent Protection (OCP) detects the drain current, I_D, on pulse-by-pulse basis, and limits output power. In Figure 8-38, this circuit enables the value of C3 for shunt capacitor to be smaller than the value of Ci for current resonant capacitor, and the detection current through C3 is small. Thus, the loss of the detection resistor, R_{OCP}, is reduced, and R_{OCP} is a small-sized one available.

There is no convenient method to calculate the accurate resonant current value according to the mains input and output conditions, and others. Thus, R_{OCP}, C3, and C6 should be adjusted based on actual operation in the application. The following is a reference adjusting method of R_{OCP}, C3, R6, and C8:

- C3 and R_{OCP}
  C3 is 100pF to 330pF (around 1 % of Ci value).
  R_{OCP} is around 100 Ω.
  Given the current of the high side power MOSFET at ON state as $I_{D(H)}$. R_{OCP} is calculated Equation (11).
  The detection voltage of R_{OCP} is used the detection of the capacitive mode operation (see Section 8.11). Therefore, setting of R_{OCP} and C3 should be taken account of both OCP and the capacitive mode operation.

$$R_{OCP} \approx \frac{|V_{RC(L)}|}{I_{D(H)}} \times \left(\frac{C3 + Ci}{C3}\right) \quad (11)$$

- R6 and C8 are for high frequency noise reduction.
  R6 is 100 Ω to 470 Ω. C6 is 100 pF to 1000 pF.

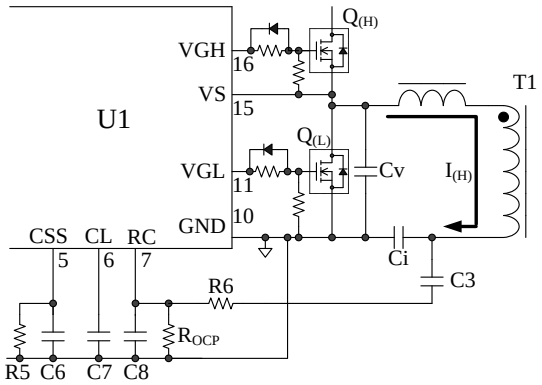


Figure 8-38. RC Pin Peripheral Circuit

The OCP operation has two-step threshold voltage as follows:

Step I, RC Pin Threshold Voltage (Low), $V_{RC(L)}$:
This step is active first. When the absolute value of the RC pin voltage increases to more than $|V_{OC(L)}|$ = 1.90 V, C6 connected to the CSS pin is discharged by $I_{CSS(L)}$ = 1.8 mA. Thus, the switching frequency increases, and the output power is limited. During discharging C6, when the absolute value of the RC pin voltage decreases to $|V_{RC(L)}|$ or less, the discharge stops.

Step II, RC Pin Threshold Voltage (High-speed), $V_{RC(S)}$:
This step is active second. When the absolute value of the RC pin voltage increases to more than $|V_{RC(S)}|$ = 2.80 V, the high-speed OCP is activated, and power MOSFETs reverse on and off. At the same time, C6 is discharged by $I_{CSS(S)}$ = 20.5 mA. Thus, the switching frequency quickly increases, and the output power is quickly limited. This step operates as protections for exceeding overcurrent, such as the output shorted.

When the absolute value of the RC pin voltage decreases to $|V_{RC(S)}|$ or less, the operation is changed to the above Step I.

8.18 Overload Protection (OLP)

Figure 8-39 shows the Overload Protection (OLP) waveforms.

When the absolute value of RC pin voltage increases to $|V_{RC(L)}|$ = 1.90 V by increasing of output power, the Overcurrent Protection (OCP) is activated. After that, the C7 connected to CL pin is charged by $I_{CL(SRC)1}$ = −17 μA. When the OCP state continues and CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated.

When CL pin voltage becomes the threshold voltage of OLP, $V_{CL(OLP)}$ = 4.2 V, the OLP is activated and the switching operation stops. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 8.14). When the fault condition is removed, the IC returns to normal operation automatically.

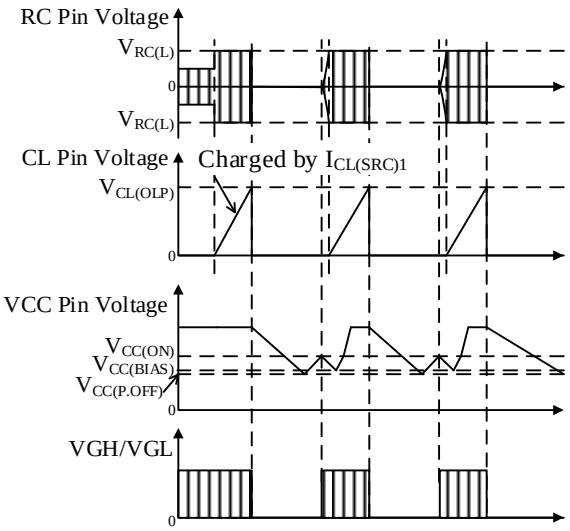


Figure 8-39. OLP Waveform

8.19 Thermal Shutdown (TSD)

When the junction temperature of the IC reach to the Thermal Shutdown Temperature $T_{J(TSD)}$ = 140 °C (min.), Thermal Shutdown (TSD) is activated and the IC stops switching operation. When the VCC pin voltage is decreased to $V_{CC(P.OFF)}$ = 8.9 V or less and the junction temperature of the IC is decreased to less than $T_{J(TSD)}$, the IC restarts.

During the protection mode, restart and stop are repeated. When the fault condition is removed, the IC returns to normal operation automatically.

9. Design Notes

9.1 External Components

Take care to use the proper rating and proper type of components.

9.1.1 Input and output electrolytic capacitors

Apply proper derating to a ripple current, a voltage, and a temperature rise. It is required to use the high ripple current and low impedance type electrolytic capacitor that is designed for switch mode power supplies.

9.1.2 Resonant transformer

The resonant power supply uses the leakage inductance of a transformer. Therefore, to reduce the effect of the eddy current and the skin effect, the wire of transformer should be used a bundle of fine litz wires.

9.1.3 Current detection resistor, R_{OCP}

To reduce the effect of the high frequency switching current flowing through R_{OCP}, choose the resister of a low internal inductance type. In addition, its allowable dissipation should be chosen suitable.

9.1.4 Current resonant capacitor, Ci

Since a large resonant current flows through Ci, Ci should be used a low loss and a high current capability capacitor such as a polypropylene film capacitor. In addition, Ci must be taken into account its frequency characteristic because a high frequency current flows.

9.1.5 Gate Pin Peripheral Circuit

The VGH and VGL pins are gate drive outputs for external power MOSFETs. These peak source and sink currents are –540 mA and 1.50 A, respectively.

To make a turn-off speed faster, connect the diode, D_S, as shown in Figure 9-1. When R_A and D_S is adjusted, the following contents should be taken into account: the power losses of power MOSFETs, gate waveforms (for a ringing reduction caused by a pattern layout, etc.), and EMI noises. To prevent the malfunctions caused by steep dv/dt at turn-off of power MOSFETs, connect R_{GS} of 10 kΩ to 100 kΩ between the Gate and Source pins of the power MOSFET with a minimal length of PCB traces. When these gate resistances are adjusted, the gate waveforms should be checked that the dead time is ensured as shown in Figure 9-2.

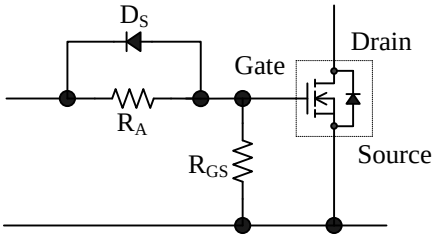


Figure 9-1. Power MOSFET Peripheral Circuit

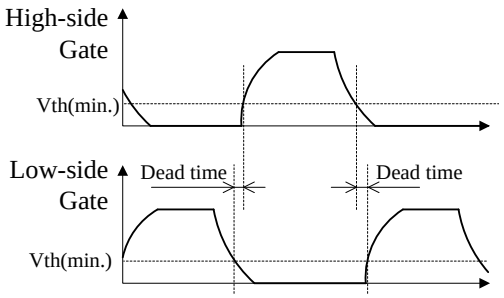


Figure 9-2. Dead Time Confirmation

9.2 PCB Trace Layout and Component Placement

The PCB circuit design and the component layout significantly affect a power supply operation, EMI noises, and power dissipation. Thus, to reduce the impedance of the high frequency traces on a PCB (see Figure 9-3), they should be designed as wide trace and small loop as possible. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

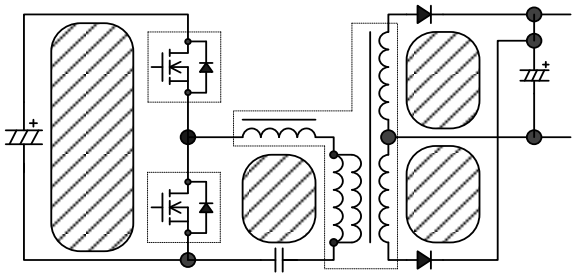


Figure 9-3 High Frequency Current Loops (Hatched Areas)

Figure 9-4 shows the circuit design example. The PCB trace design should be also taken into account as follows:

1) Main Circuit Trace
The main traces that switching current flows should be designed as wide trace and small loop as possible.

2) Control Ground Trace
If the large current flows through a control ground, it may cause varying electric potential of the control ground; and this may result in the malfunctions of the IC. Therefore, connect the control ground as close and short as possible to the GND pin at a single-point ground (or star ground) that is separated from the power ground.

3) VCC Trace
The trace for supplying power to the IC should be as small loop as possible. If C3 and the IC are distant from each other, a film capacitor C_f (about 0.1 µF to 1.0 µF) should be connected between the VCC and GND pins with a minimal length of PCB traces.

4) Trace of Peripheral Components for the IC Control
These components should be placed close to the IC, and be connected to the corresponding pin of the IC with as short trace as possible.

5) Trace of Bootstrap Circuit Components
These components should be connected to the IC pin with as short trace as possible. In addition, the loop for these should be as small as possible.

6) Secondary Side Rectifier Smoothing Circuit Trace
The traces of the rectifier smoothing loops carry the switching current. Thus it should be designed as wide trace and small loop as possible.

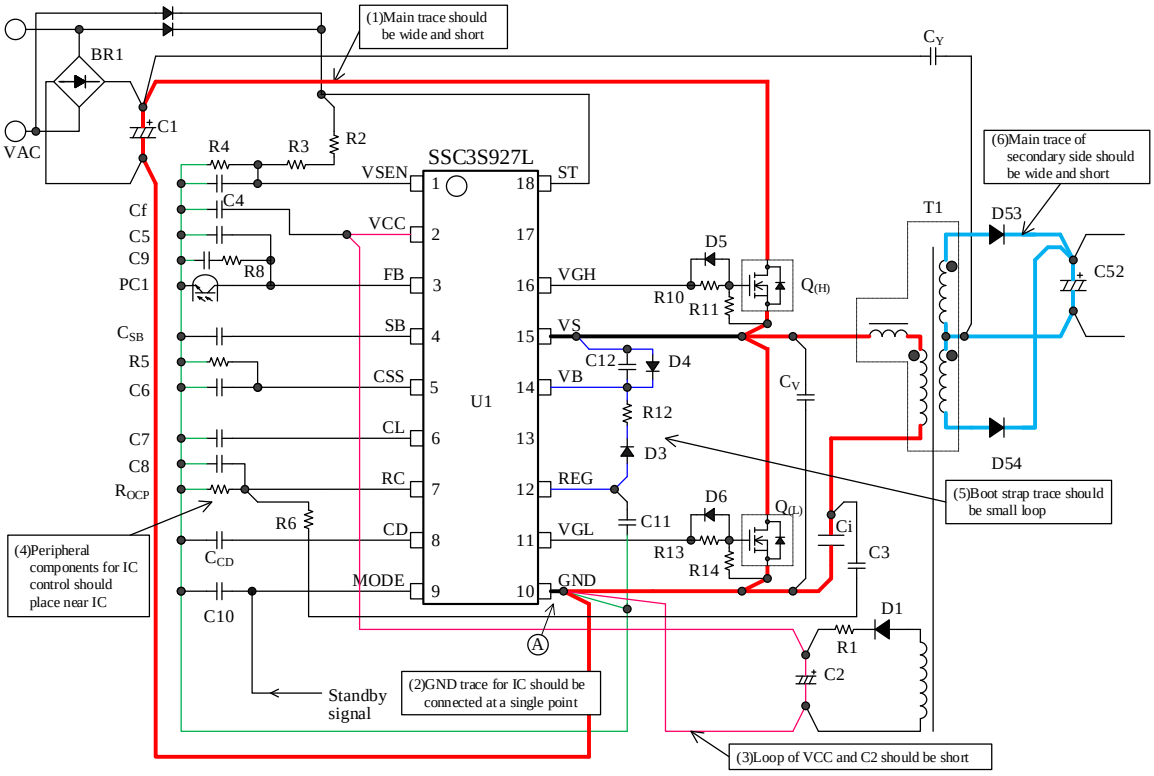


Figure 9-4 Peripheral Circuit Trace Example Around the IC

10. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of circuit using SSC3S927L.

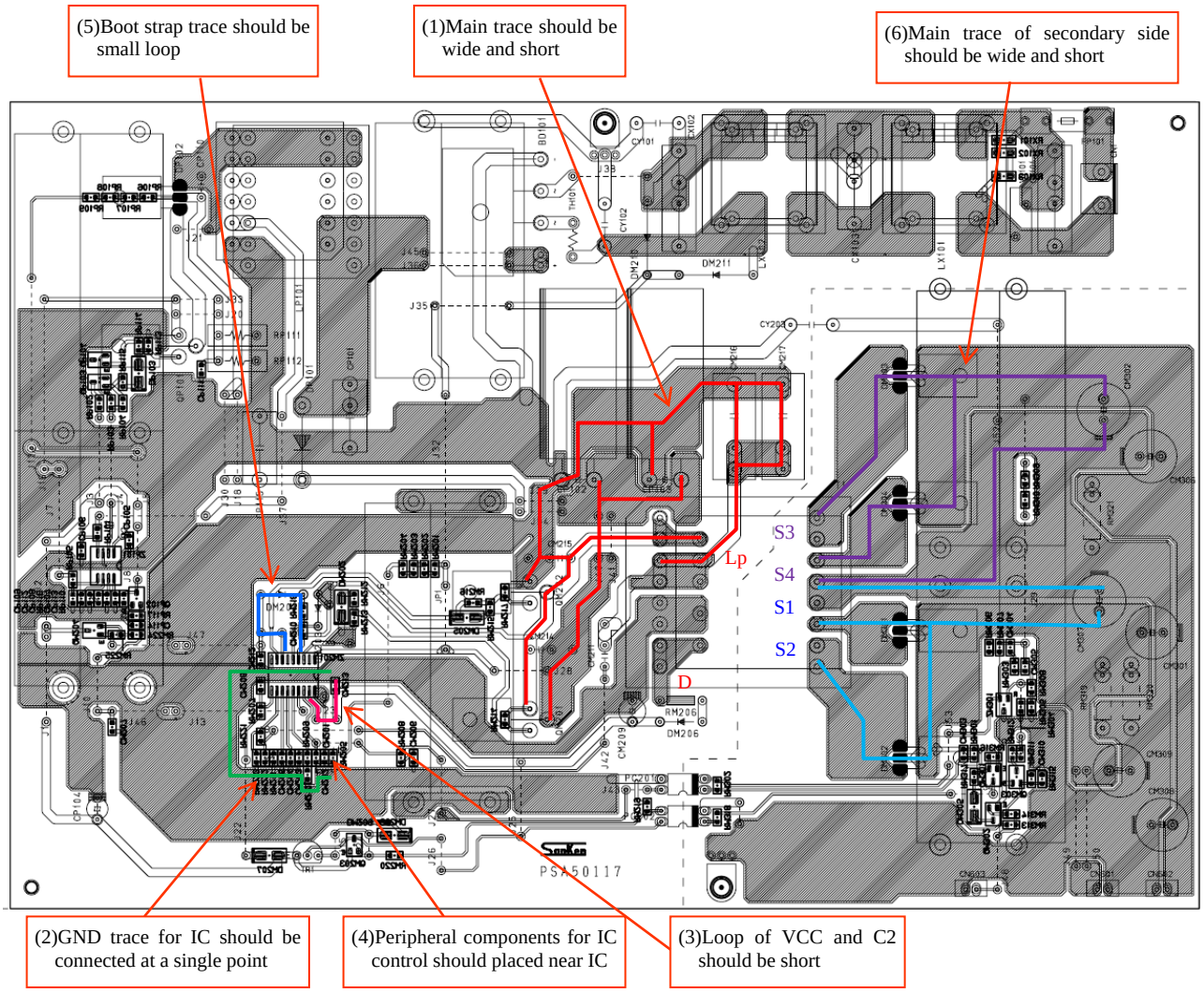


Figure 10-1. PCB Pattern Layout Example

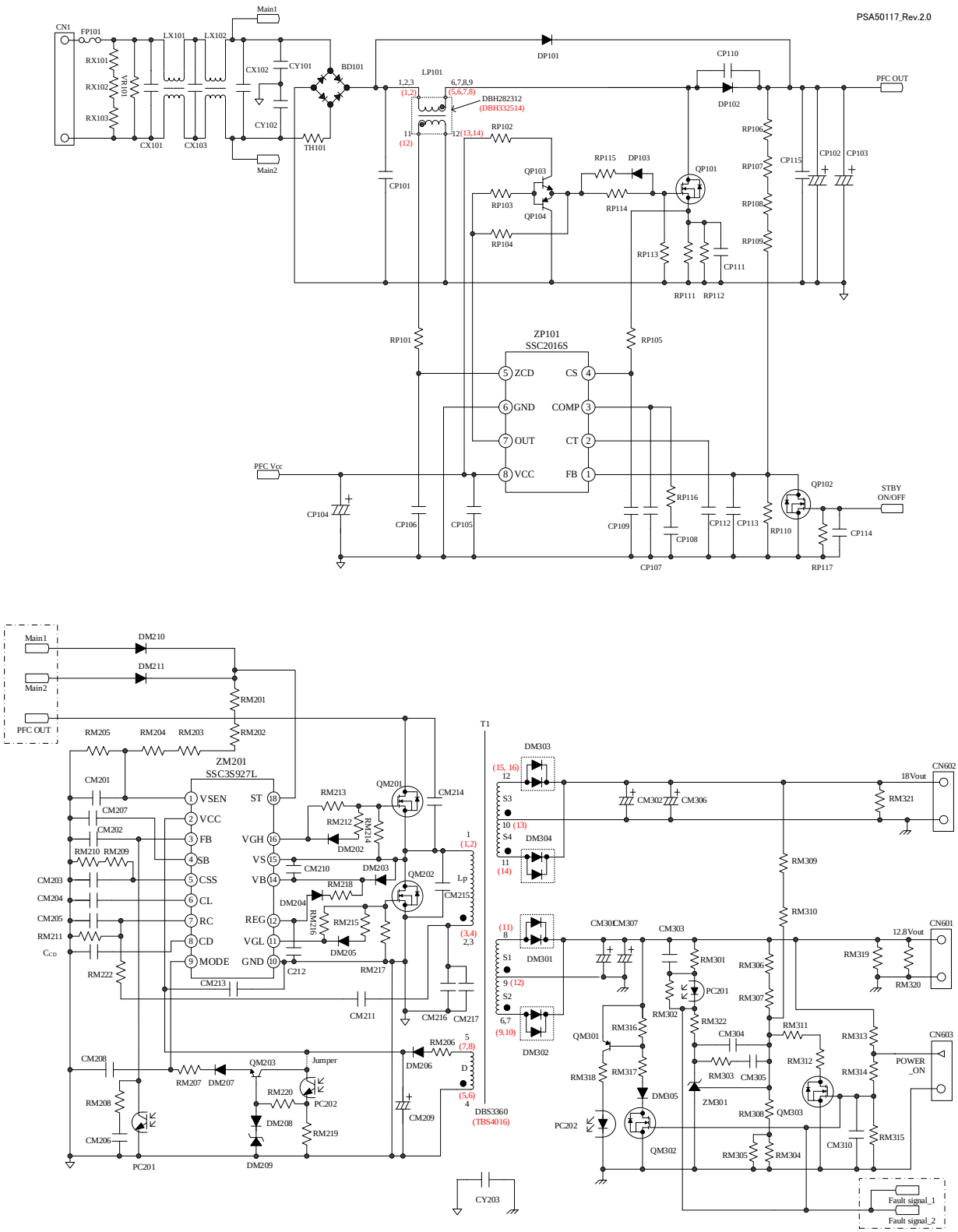


Figure 10-2. PCB Pattern Layout Example Circuit

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