Power Supply Control IC with Critical Conduction Mode PFC and LLC Current-resonant Circuits

SSC4S913

Data Sheet

Description

The SSC4S913 is a power supply IC, which incorporates a CRM-driven PFC control circuit and an LLC circuit. These internal circuits bring a small-sized, high-efficient, and low-noise power supply system into your application. The LLC stage has the high- and low-side drive circuits. The PFC and LLC stages are highly interlocked in startup and standby operations, thus requiring no individual circuit settings. Supplied in a small SSOP24 package, where multiple protections (e.g., the capacitive mode detection function) are highly integrated, the SSC4S913 offers design friendliness in your high-quality power supply systems with safety. The SSC4S913 has enough functions such as a startup circuit supporting DC input and efficiency improvement at light load.

Package

SSOP24

Not to scale

Features

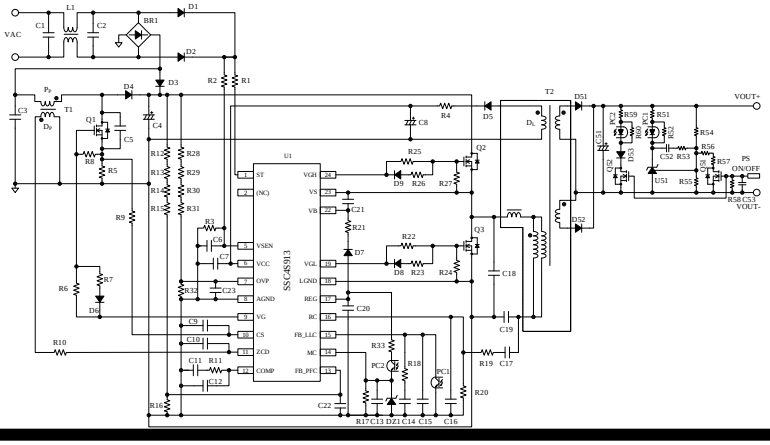
- Pb-free (RoHS Compliant)
- Highly Integrated PFC Control and LLC Current-resonant Control Circuits
- LLC Soft Start Function
- X-capacitor Discharge Function
  (No discharge resistor required, disabled at DC input)
- Critical Conduction Mode (CRM) PFC Control
- PFC Maximum Oscillation Frequency Limitation Function
- LLC Capacitive Mode Detection Function
- Standby Function (Interlocked between PFC and LLC Stages)
- Protections
- Input Voltage Protection (Under and Overvoltage)
- PFC FB_PFC Pin Undervoltage Protection
- PFC Output Overvoltage Protection (FB_PFC and OVP Pins)
- PFC Overcurrent Protection
- LLC High-side Driver Undervoltage Lockout
- LLC Overcurrent Protection
- LLC Overload Protection
- VCC Pin Overvoltage Protection
- Thermal Shutdown

Applications

For devices requiring high power supplies such as:

- Audiovisual Equipment (e.g., Monitor, LCD TV)
- Office Automation Equipment (e.g., Server, Multifunction Printer)
- Industrial Equipment
- Communication Equipment

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless specifically noted, T_A = 25 °C.
Surge withstand capability (HBM) of the SSC4S913 is guaranteed as follows: 1000 V for pin 1, 22, 23, 24, and 2000 V for other pins.

Parameter	Symbol	Conditions	Pin	Rating	Unit
ST Pin Voltage	V_{ST}		1 – 8	−0.3 to600	V
VSEN Pin Sink Current	I_{VSEN}		5 – 8	1	mA
VCC Pin Voltage	V_{CC}		6 – 8	−0.3 to 35	V
OVP Pin Voltage	V_{OVP}		7 – 8	−0.3 to 5.5	V
VG Pin Voltage	V_G		9 – 8	−0.3 to V_{REG} + 0.3	V
VG Pin Source Current	$I_{VG(SRC)}$		9 – 8	−500	mA
VG Pin Sink Current	$I_{VG(SNK)}$		9 – 8	1000	mA
CS Pin Voltage (DC)	$V_{CS(DC)}$		10 – 8	−0.3 to 5.5	V
CS Pin Voltage (Pulse)	$V_{CS(PULSE)}$	Pulse width ≤1 μs	10 – 8	−2.0 to 5.5	V
ZCD Pin Voltage	V_{ZCD}		11 – 8	−10 to 10	V
ZCD Pin Current	I_{ZCD}		11 – 8	−10 to 10	mA
COMP Pin Voltage	V_{COMP}		12 – 8	−0.3 to 5.5	V
COMP Pin Current	I_{COMP}		12 – 8	−100 to 100	μA
FB_PFC Pin Voltage	V_{FB_PFC}		13 – 8	−0.3 to 5.5	V
MC Pin Voltage	V_{MC}		14 – 8	−0.3 to 30	V
MC Pin Source Current	$I_{MC(SRC)}$		14 – 8	−500	μA
FB_LLC Pin Voltage	V_{FB_LLC}		15 – 8	−0.3 to 5.5	V
RC Pin Voltage	V_{RC}		16 – 8	−5.5 to 5.5	V
REG Pin Source Current	I_{REG}		17 – 8	−20	mA
LGND Pin Voltage	V_{LGND}		18 – 8	−0.3 to 0.3	V
VGL Pin Voltage	V_{GL}		19 – 18	−0.3 to V_{REG} + 0.3	V
VS Pin Voltage	V_S		23 – 18	−1.0 to 600	V
VGH Pin Voltage	V_{GH}		24 – 18	V_S − 0.3 to V_B + 0.3	V
VB–VS Pin Voltage	V_B–V_S		22 – 23	−0.3 to 30	V
Allowable Power Dissipation	P_D	T_A = 85 °C	—	0.542	W
Operating Ambient Temperature	T_{OP}		—	−40 to 85	°C
Storage Temperature	T_{STG}		—	−40 to 150	°C
Junction Temperature	T_J		—	150	°C

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 19 V.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit
Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		6 – 8	15.8	17.0	18.2	V
Operation Stop Voltage (1)	$V_{CC(OFF)}$		6 – 8	7.8	8.7	9.8	V
Startup Current Bias Threshold Voltage (1)	$V_{CC(BIAS)}$		6 – 8	9.0	9.8	10.6	V
Protection Release Threshold Voltage (1)	$V_{CC(P.OFF)}$		6 – 8	7.8	8.7	9.8	V
Startup Current	I_{CC}		6 – 8	−25.0	−11.0	−5.0	mA
Circuit Current in Operation	$I_{CC(ON)}$		6 – 8	—	—	6	mA
Circuit Current in Non-operation	$I_{CC(OFF)}$		6 – 8	—	1.0	3.0	mA
Circuit Current in Protection Operation	$I_{CC(P)}$		6 – 8	—	1.6	2.5	mA
LLC Operation Start Voltage	$V_{LLC(ON)}$		13 – 8	1.760	1.875	1.940	V
LLC Operation Stop Voltage	$V_{LLC(OFF)}$		13 – 8	1.250	1.350	1.410	V
AC Input Voltage Protection							
VSEN Pin UVP Threshold Voltage	$V_{SEN(ON)}$		5 – 8	0.873	0.900	0.927	V
VSEN Pin UVP Release Voltage 1	$V_{SEN(OFF)1}$		5 – 8	0.716	0.750	0.784	V
VSEN Pin UVP Release Voltage 2	$V_{SEN(OFF)2}$		5 – 8	—	0.600	—	V
VSEN Pin Delay Time	$t_{DLY(VSEN)}$		5 – 8	46	52	58	ms
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$		5 – 8	4.00	4.20	4.40	V
VSEN Pin Clamp Voltage	$V_{SEN(CLAMP)}$		5 – 8	10	—	—	V
VSEN Pin AC Detection Threshold Voltage 1	$V_{SEN(AC)1}$		5 – 8	—	2.025	—	V
VSEN Pin AC Detection Threshold Voltage 2	$V_{SEN(AC)2}$		5 – 8	—	1.800	—	V
PFC Frequency Control							
FB_PFC Pin Sink Current	I_{FB_PFC}		13 – 8	—	0.40	1.00	µA
FB_PFC Pin Feedback Reference Voltage	V_{REF_PFC}		13 – 8	2.475	2.500	2.525	V
V_{REF} Line Regulation	$V_{REF\_PFC(LR)}$		13 – 8	−8	1	12	mV
V_{REF} Voltage Variation Range (2)	V_{REF_RANGE}	T_J = −40 °C to 150 °C	13 – 8	—	±0.5	—	mV/°C
COMP Pin Source Current	$I_{COMP(SRC)}$		12 – 8	−22.0	−11.0	−1.0	µA
COMP Pin Sink Current	$I_{COMP(SNK)}$		12 – 8	1.0	11.0	22.0	µA
Error Amplifier Conductance	gm		12 – 8 13 – 8	60	100	140	µA/V
COMP Pin Voltage at Zero Duty Cycle	$V_{COMP(ZD)}$		12 – 8	0.50	0.65	0.90	V
Restart Time	t_{RS}		9 – 8	140	220	300	µs
On-time at Restart	$t_{ON(RS)}$		9 – 8	0.50	1.70	2.90	µs

(1) $V_{CC(OFF)} = V_{CC(P.OFF)} < V_{CC(BIAS)}$

(2) Design assurance item.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit
PFC Maximum On-time	t_{MAX_PFC}		9 – 8	16.5	18.3	20.1	µs
PFC Maximum Oscillation Frequency (3)	f_{MAX_PFC}		9 – 8	—	300	400	kHz
PFC Drive Output							
VG Pin Source Current	$I_{VG(SRC)}$	V_G = 8 V	9 – 8	—	−100	—	mA
VG Pin Sink Current	$I_{VG(SNK)}$	V_G = 0.75 V	9 – 8	—	200	—	mA
PFC Zero Current Detection (ZCD)							
ZCD Pin Threshold Voltage (high)	$V_{ZCD(H)}$		11 – 8	1.25	1.40	1.55	V
ZCD Pin Threshold Voltage (low)	$V_{ZCD(L)}$		11 – 8	0.60	0.70	0.80	V
ZCD Delay Time	$t_{DLY(ZCD)}$		11 – 8	—	70	160	ns
ZCD Pin Clamp Voltage	$V_{ZCD(CL)}$		11 – 8	6.5	7.7	9.0	V
PFC Protection							
PFC_OCP Threshold Voltage 1	$V_{CS(OCP1)}$		10 – 8	0.49	0.50	0.51	V
PFC_OCP Threshold Voltage 2	$V_{CS(OCP2)}$		10 – 8	1.35	1.50	1.65	V
PFC_OCP Delay Time	$t_{DLY(OCP)}$		10 – 8	90	300	340	ns
CS Pin Source Current	I_{CS}		10 – 8	−40	−20	−10	µA
FB_PFC Pin PFC_OVP Threshold Voltage	V_{OVP_PFC1}		13 – 8	1.030 × V_{REF_PFC}	1.060 × V_{REF_PFC}	1.090 × V_{REF_PFC}	V
FB_PFC Pin PFC_OVP Hysteresis(3)	$V_{OVP\_PFC1(HYS)}$		13 – 8	20	45	80	mV
OVP Pin PFC_OVP Threshold Voltage	V_{OVP_PFC2}		7 – 8	2.63	2.70	2.77	V
FB_PFC_UVP Threshold Voltage	V_{UVP_PFC}		13 – 8	200	300	400	mV
FB_PFC_UVP Hysteresis	$V_{UVP\_PFC(HYS)}$		13 – 8	70	110	150	mV
LLC Soft Start							
Maximum Oscillation Frequency at Soft Start	$f_{SS(MAX)}$		24 – 23 19 – 18	500	600	700	kHz
Soft Start Period	t_{ss}		24 – 23 19 – 18	—	28	—	ms
Standby Operation							
MC Pin Standby Transition Voltage	$V_{MC(ON)}$	External input signal	14 – 8	0.20	0.55	0.90	V
MC Pin Standby Release Voltage	$V_{MC(OFF)}$	External input signal	14 – 8	0.30	0.80	1.20	V
MC Pin Current	I_{MC}	V_{RC} = 1 V	14 – 8	−150	−105	−55	µA
LLC Oscillator							
LLC Minimum Oscillation Frequency	f_{MIN_LLC}		24 – 23 19 – 18	40.5	45.0	49.5	kHz
LLC Maximum Oscillation Frequency	f_{MAX_LLC}		24 – 23 19 – 18	230	300	380	kHz
Minimum Dead Time	$t_{d(MIN)}$		24 – 23 19 – 18	0.04	0.24	0.40	µs
Maximum Dead Time	$t_{d(MAX)}$		24 – 23 19 – 18	1.20	1.65	2.20	µs

(3) Design assurance item.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit
LLC Feedback Control							
FB_LLC Pin Oscillation Start Threshold Voltage	$V_{FB\_LLC(ON)}$		15 – 8	0.15	0.30	0.45	V
FB_LLC Pin Oscillation Stop Threshold Voltage	$V_{FB\_LLC(OFF)}$		15 – 8	0.05	0.20	0.35	V
FB_LLC Pin Maximum Source Current	$I_{FB\_LLC(MAX)}$	V_{FB_LLC} = 0 V	15 – 8	−300	−195	−100	µA
FB_LLC Pin Reset Current	$I_{FB\_LLC(R)}$	V_{FB_LLC} = 3 V	15 – 8	4	10	14	mA
LLC Reset Detection							
Maximum Reset Time	$t_{RST(MAX)}$		24 – 23 19 – 18	—	5	—	µs
LLC Driver Power Supply							
LLC Driver Power Supply Voltage	V_{REG}		17 – 8	9.2	10.0	10.8	V
LLC High-side Driver							
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		22 – 23	5.7	6.8	7.9	V
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		22 – 23	5.5	6.4	7.3	V
LLC Drive Circuit							
Output Source Current 1	$I_{GL(SRC)1}$ $I_{GH(SRC)1}$	V_B = 15 V V_{GL} = 0 V V_{GH} = 0 V	24 – 23 19 – 18	—	−540	—	mA
Output Sink Current 1	$I_{GL(SNK)1}$ $I_{GH(SNK)1}$	V_B = 15 V V_{GL} = 15 V V_{GH} = 15 V	24 – 23 19 – 18	—	800	—	mA
Output Source Current 2	$I_{GL(SRC)2}$ $I_{GH(SRC)2}$	V_B = 10 V V_{GL} = 7.5 V V_{GH} = 8.5 V	24 – 23 19 – 18	−200	—	−20	mA
Output Sink Current 2	$I_{GL(SNK)2}$ $I_{GH(SNK)2}$	V_B = 10 V V_{GL} = 1.5 V V_{GH} = 1.5 V	24 – 23 19 – 18	46	—	300	mA
LLC Capacitive Mode Detection, LLC Overcurrent Protection (LLC_OCP)							
Capacitive Mode Detection Voltage 1	V_{RC1}		16 – 8	0.02	0.10	0.18	V
				−0.18	−0.10	−0.02	V
Capacitive Mode Detection Voltage 2	V_{RC2}		16 – 8	0.20	0.30	0.40	V
				−0.40	−0.30	−0.20	V
RC Pin OCP1 Threshold Voltage	V_{RC_OCP1}		16 – 8	1.75	1.87	1.97	V
				−1.97	−1.87	−1.75	V
RC Pin OCP2 Threshold Voltage	V_{RC_OCP2}		16 – 8	2.58	2.76	2.94	V
				−2.94	−2.76	−2.58	V
LLC Overload Protection (LLC_OLP)							
LLC_OLP Delay Time	$t_{DLY(OLP)}$		16 – 8	80	100	120	ms
VCC Pin Overvoltage Protection (VCC_OVP)							
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		6 – 8	30.0	32.0	34.0	V
REG Pin Overvoltage Protection (REG_OVP)							
REG Pin OVP Threshold Voltage	$V_{REG(OVP)}$		17 – 8	11.5	12.4	13.5	V

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit
Thermal Shutdown (TSD)							
TSD Operating Temperature	$T_{J(TSD)}$		—	140	—	—	°C
Thermal Characteristic							
Junction-to-Air Thermal Resistance	θ_{J-A}		—	—	—	120	°C/W

3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.15	—	g

4. Typical Application

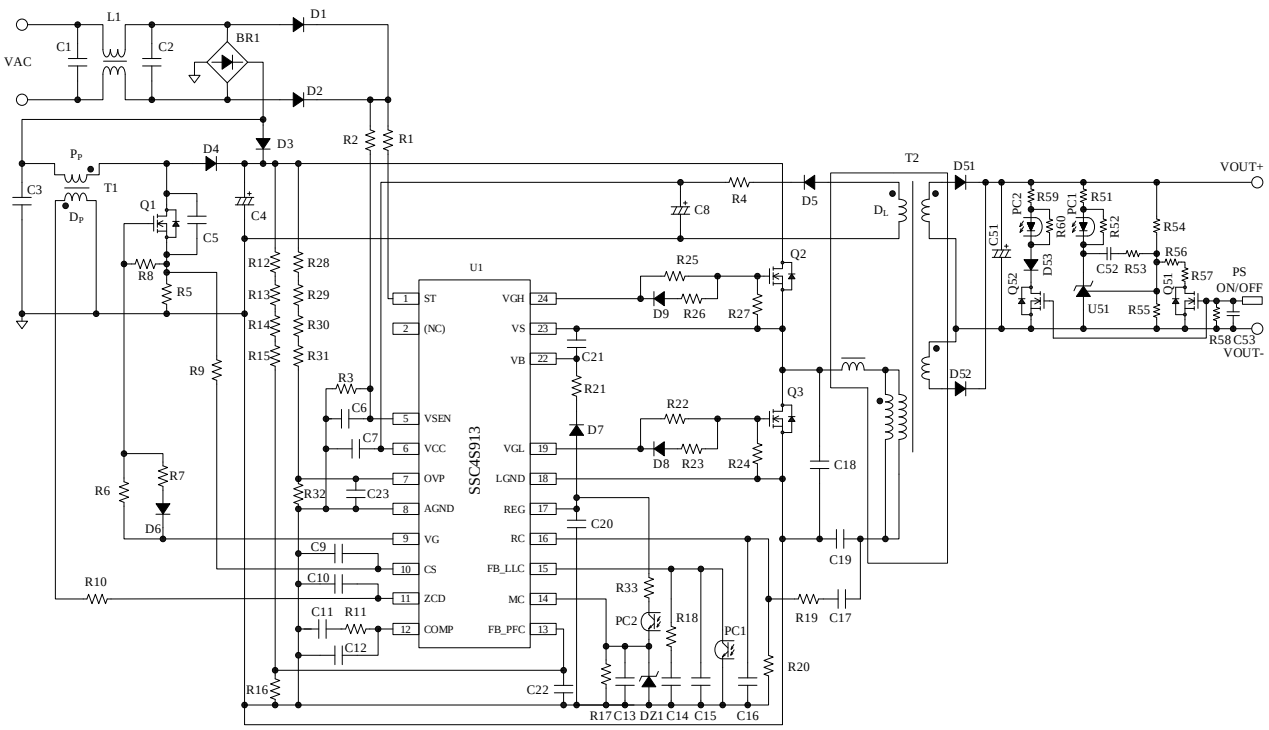
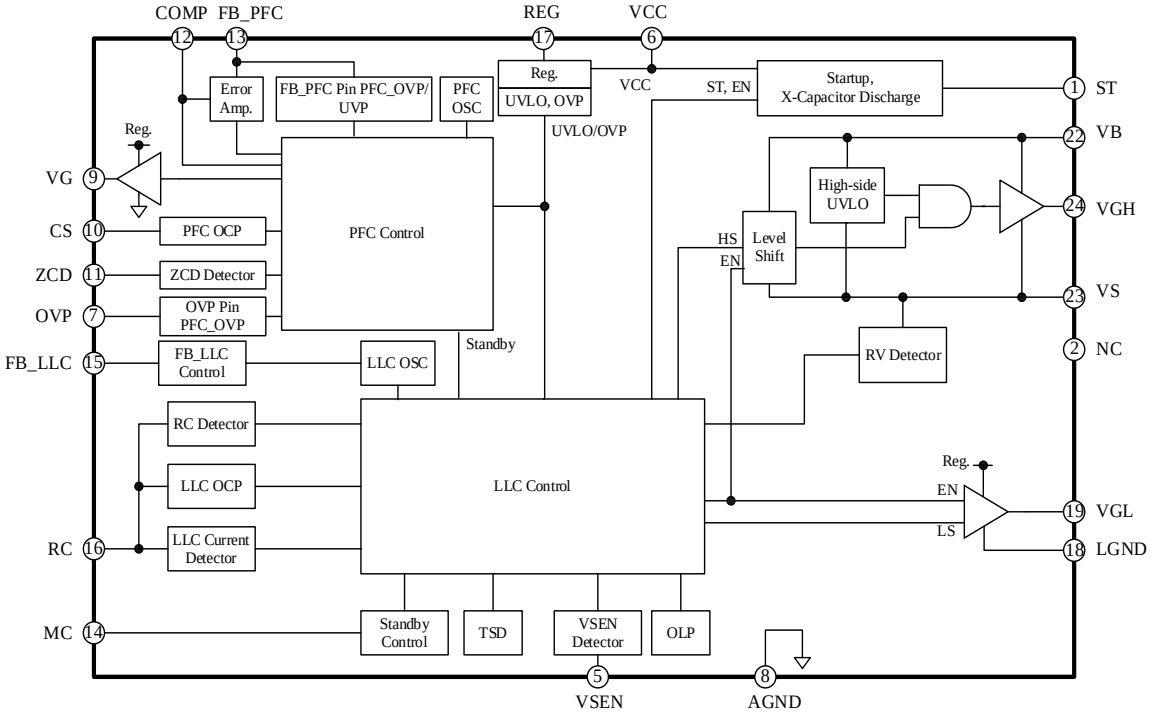


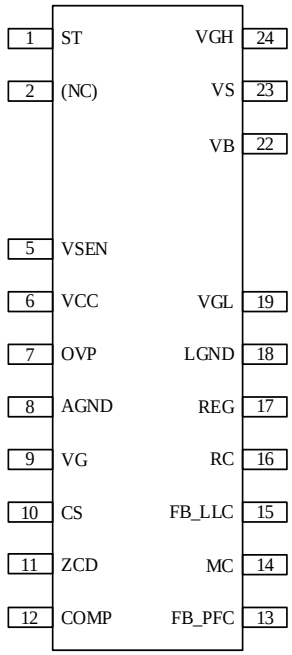
Figure 4-1. Typical Application

5. Block Diagram



6. Pin Configuration Definitions

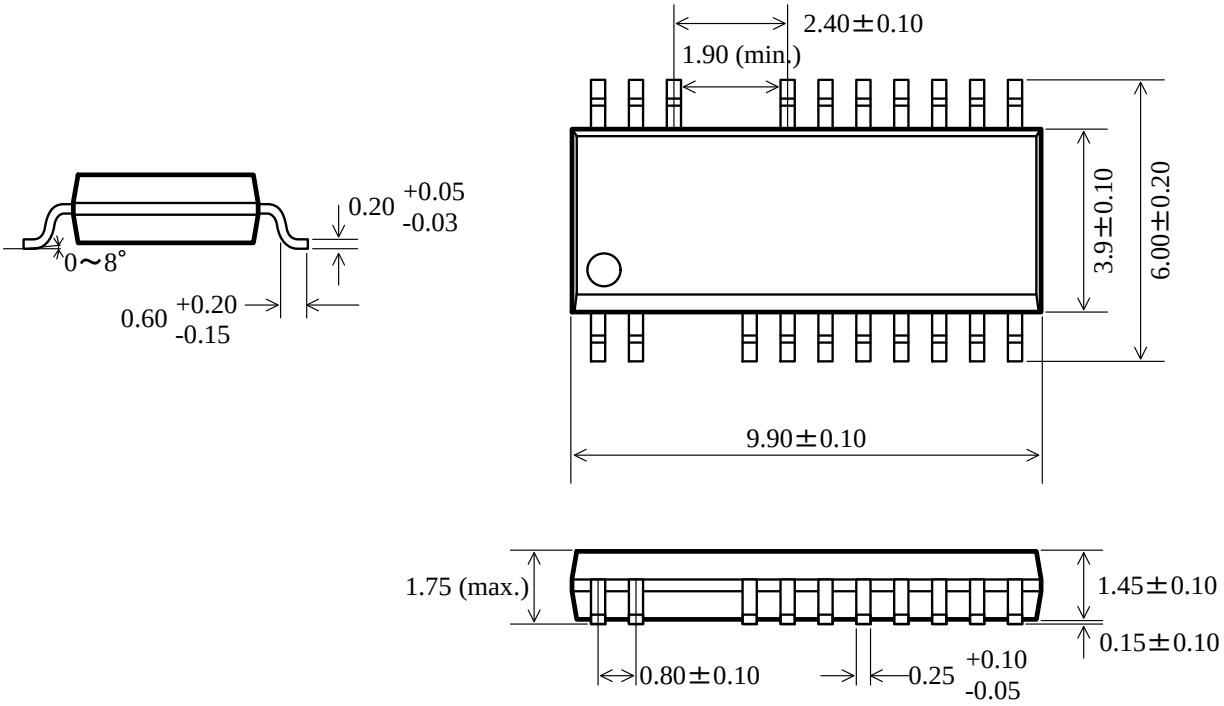
Top View



Pin Number	Pin Name	Description
1	ST	Startup current input, X-capacitor discharge current input
2	(NC)	No connection
3	—	(Pin removed)
4	—	(Pin removed)
5	VSEN	Input voltage protection signal input
6	VCC	Logic power supply input; VCC_OVP signal input
7	OVP	OVP pin PFC_OVP signal input
8	AGND	Ground (Externally connected to PGND)
9	VG	PFC gate drive output
10	CS	PFC_OCP signal input
11	ZCD	PFC zero current detection (ZCD) signal input
12	COMP	PFC phase compensation adjustment
13	FB_PFC	PFC feedback signal input; FB_PFC pin PFC_OVP signal input; FB_PFC_UVP signal input
14	MC	Standby signal input
15	FB_LLC	LLC constant voltage control signal input
16	RC	Resonant current detection signal input; LLC_OCP detection signal input
17	REG	REG output for driver
18	LGND	LLC power ground
19	VGL	LLC low-side gate drive output
20	—	(Pin removed)
21	—	(Pin removed)
22	VB	Power supply input for LLC high-side gate drive; VB_UVLO signal input
23	VS	Floating ground of LLC high-side driver
24	VGH	LLC high-side gate drive output

7. Physical Dimensions

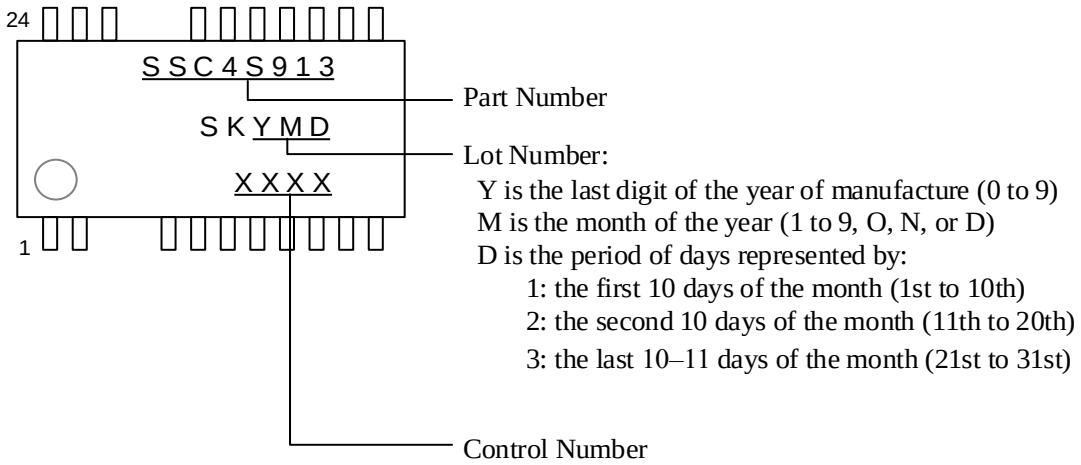
● SSOP24



NOTES:

● Dimensions in millimeters
● Dimensions do not include mold burrs.
● Pb-free (RoHS compliant)

8. Marking Diagram



9. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 2 and the electronic symbol names of the typical application in Section 4.

"GND" represents a potential across the AGND and LGND pins, which must be externally connected by PCB layout.

9.1. General Description

The SSC4S913 integrates two controls: the PFC control driven with critical conduction mode and the LLC current resonant control.

The PFC control of the IC is a critical conduction mode. By monitoring the output voltage of the PFC circuit with the FB_PFC pin, the IC controls the VG pin on-time and provides regulated outputs. Zero current in critical mode is detected by inputting the voltage of the auxiliary winding, D_P, to the ZCD pin.

The IC has a built-in high-side driver and low-side driver that drive the LLC half-bridge circuit. By monitoring the secondary-side output voltage through an optocoupler, which is connected to the FB pin, the IC controls the oscillation frequencies of the VGH and VGL pins to provide regulated outputs (Section 9.15). The capacitive mode detection function (Section 9.18) requires no user-setting of minimum oscillation frequencies in your design phase. The IC also automatically controls its dead time between the VGH and VGL pins according to power supply specifications; therefore, individual dead time settings are unnecessary (Section 9.17). The IC has the X-capacitor discharge function (Section 9.5). The X-capacitor discharge function needs no discharge resistor for the input filter of a switching power supply.

Both the PFC and LLC stages highly incorporate protections such as the overcurrent and overvoltage protections.

9.2. Pin Descriptions

9.2.1. VSEN

As shown in Figure 9-1, the input voltage, $V_{IN(AC)}$, divided by the detection resistors is applied to the VSEN pin. Signals input to the VSEN pin are used for the input voltage protection. Section 9.5.2 describes the input voltage protection and how to set the peripheral constants of the VSEN pin.

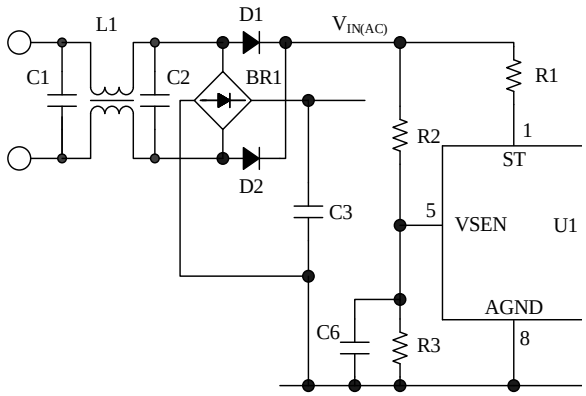


Figure 9-1. VSEN Pin and Its Peripheral Circuit

9.2.2. VCC

This is the power supply pin for the built-in control MICs. When the VCC pin voltage increases to $V_{CC(ON)}$ = 17.0 V or more, the IC starts operating. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.7 V or less, the IC stops operating. This sequence of operations is the VCC pin undervoltage lockout (VCC_UVLO). In addition to this function, the VCC pin also has the VCC pin overvoltage protection (VCC_OVP). When the VCC pin power is supplied through the auxiliary winding of the LLC transformer, the VCC pin voltage is proportional to the secondary-side output voltage. Thus, the VCC pin can detect overvoltage conditions in the secondary side.

Section 9.3 describes the startup operation of the IC and the setting of the auxiliary winding; Section 9.5.2 provides more details on the VCC_OVP. To prevent malfunction induced by supply ripples or other factors, connect a 0.1 µF to 1.0 µF capacitor, C7, between the VCC and AGND pins with a minimal length of traces.

9.2.3. AGND and LGND

The AGND pin is the logic ground pin of the IC; and the LGND pin is the power ground pin of the LLC stage where driving currents for an external power MOSFET flow through. The AGND and LGND pins must be externally connected by PCB layout with a minimal length of traces.

Varying electric potential of the logic ground can be a cause of improper operations. Therefore, extreme care should be taken in designing a PCB so that currents from the power ground do not affect these pins. For the notes on PCB pattern layouts, see Section 10.3.

9.2.4. VG

This is the drive output pin for driving the power MOSFET (Q1) in the PFC stage. To increase a falling speed of the gate at power MOSFET turn-off, connect the

diode, D6, as shown in Figure 9-2. D6, R6, and R7 should be adjusted based on the operation performance checked with an actual board, including a loss in the power MOSFET, gate waveform (e.g., ringing due to pattern layout), and EMI noise. R8 for preventing malfunction of power MOSFET is 10 kΩ to 100 kΩ and be placed as close as possible to the gate and source.

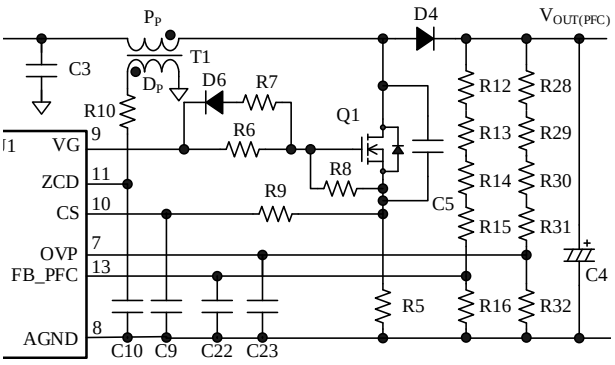


Figure 9-2. PFC Circuit

9.2.5. CS

This is the current detection pin of the PFC stage. As shown in Figure 9-2, the switching current of the PFC stage is detected by R5 to be input to the CS pin. The CR filter consisting of R9 and C9 is connected to the CS pin.

- **PFC_OCP Detection: R5**

The detection resistor R5 monitors the currents through the power MOSFET (Q1) for the PFC_OCP function. High-frequency switching currents flow through the current detection resistor, R5; therefore, be sure to use a resistor with low internal inductance and allowable power dissipation. For more details on the PFC_OCP function, see Section 9.11.

- **CR Filter: R9, C9**

Using a CR filter prevents unstable IC operations caused by a drain current surge at power MOSFET turn-on. The detection accuracy of the PFC_OCP function depends on the resistance of R9; accordingly, R9 should be set about 47 Ω. C9 should be set so that cut-off frequency of CR filter (C9 and R9) is approximately 0.5 MHz to 3.0 MHz.

When R9 is 47 Ω, C9 is 1 nF to 6.8 nF. Be sure to confirm the actual operation in the application, and adjust the values.

9.2.6. ZCD

This is the PFC zero current detection pin. As shown in Figure 9-2, the zero current detection signal is input to the ZCD pin from the auxiliary winding, D_P, of the transformer in the PFC through the current-limiting resistor, R10. C10 is the bottom-on timing adjustment capacitor.

The constants of the peripheral components must be set within the maximum ratings defined for the ZCD pin. For details on the setting of R10 and C10, see Section 9.8.2.

9.2.7. COMP

The COMP pin voltage determines the VG pin on-time, thus allowing the PFC stage output voltage to be constant. Figure 9-3 shows the peripheral components connected to the COMP pin: the capacitor C11 and resistor R11 for the phase compensation function; the capacitor C12 for averaging output ripples. Section 9.8.1 thoroughly explains the PFC constant voltage control and how to set the constants of the COMP pin.

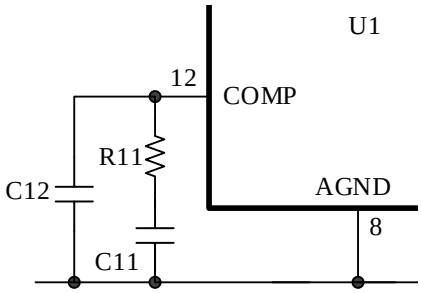


Figure 9-3. COMP Pin Peripheral Circuit

9.2.8. FB_PFC

The feedback signal of the constant output voltage control for the PFC stage is input to the FB_PFC pin. In addition, the FB_PFC pin has the PFC_OVP (see Section 9.12) and UVP (see Section 9.13).

As shown in Figure 9-2, the output voltage of the PFC stage, $V_{OUT(PFC)}$, divided by the detection resistors is applied to the FB_PFC pin. $V_{OUT(PFC)}$ is determined by the detection resistors, R12 to R16, and can be calculated by the equation below:

$$V_{OUT(PFC)} = \left(\frac{R_{REF1}}{R_{REF2}} + 1\right) \times V_{REF\_PFC} \qquad (1)$$

Where:

V_{REF_PFC} is the FB_PFC pin feedback reference voltage (2.500 V),

R_{REF1} is the combined resistance of the resistors R12 to R15, and

R_{REF2} is the resistance of R16 (≈ 33 kΩ).

The resistors of R_{REF1} are set at high resistance such that high DC voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; configure R_{REF1} with some serial

resistors to reduce each applied voltage.

When your application needs less switching noise, connect a capacitor, C22, of about 1 nF between the FB_PFC pin and AGND with a minimum length of traces.

9.2.9. OVP

In case an abnormal status occurs on the output voltage detection line of the FB_PFC pin, the OVP pin is used for the overvoltage protection detection of the PFC output (PFC_OVP).

As shown in Figure 9-2, the output voltage of the PFC stage, $V_{OUT(PFC)}$, divided by the detection resistors is applied to the OVP pin. The OVP pin PFC_OVP threshold voltage, V_{OVP_PFC2}, is 2.70 V. Care should be taken in setting the values of R28 to R32 so that the PFC_OVP by the OVP pin is not activated during IC startup. The resistors of R28 to R31 are set at high resistance such that high DC voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; configure with some serial resistors to reduce each applied voltage.

When your application needs less switching noise, connect the capacitor, C23, of about 1 nF between the OVP pin and AGND with a minimum length of traces.

9.2.10. MC

This pin serves as the on/off controller of the standby operation. Connect an on/off circuit to the MC pin.

Section 9.16 fully explains the settings of the standby function and the MC pin.

9.2.11. FB_LLC

This pin is used for controlling the LLC stage output voltage to be constant. As Figure 9-4 shows, the optocoupler, PC1, and the capacitor C14, C15, and R18 should be connected to the FB_LLC pin. The FB_LLC pin controls the on-times of high- and low-side power MOSFETs (Q2, Q3) with 50% duty cycle. Section 9.15 describes the LLC constant voltage control and the settings of the FB_LLC pin peripheral circuit.

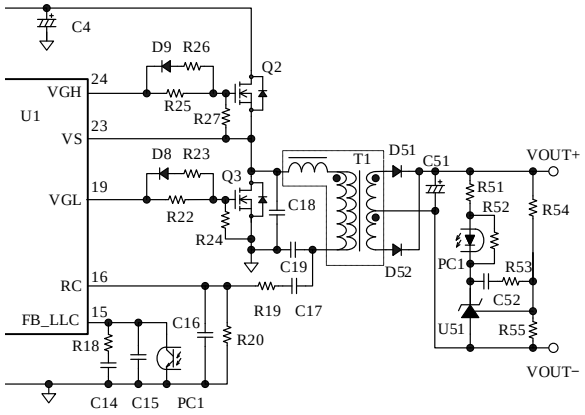


Figure 9-4. LLC Circuit

9.2.12. RC

The RC pin detects the capacitive operation and an overcurrent condition in the LLC stage, with C17 and R20 connected as shown in Figure 9-4. In addition, R19 and C16 are connected as a high-frequency noise filter.

Section 9.18 explains the capacitive mode detection function; Section 9.21 provides details on the LLC overcurrent protection and the settings of the RC pin peripheral circuit.

9.2.13. REG

This pin is the output of the regulator for supplying power to the VB pin. Connect C20 between REG and AGND pins. C20 value is about 1.0 µF.

9.2.14. VGL and VGH

These pins are the drive output pins for driving the power MOSFETs in the LLC stage. The VGL pin acts as a low-side driver, whereas the VGH pin acts as a high-side driver.

The description hereafter holds up the peripheral circuit of Q2 as an example (but is also applicable to Q3). To increase a rising speed of the gate at power MOSFET turn-off, connect the diode, D9, as shown in Figure 9-4. R25, R26, and D9 should be adjusted based on operation performance in an actual application, including a loss in the power MOSFET, gate waveform (e.g., ringing due to pattern layout), and EMI noise. R27 for preventing malfunction of the power MOSFET is 10 kΩ to 100 kΩ and be placed as close as possible to the gate and source of the power MOSFET. When adjusting gate resistances, note that gate waveforms of the power MOSFETs must be checked whether a proper amount of dead time is ensured based on the reference waveforms depicted in Figure 9-5.

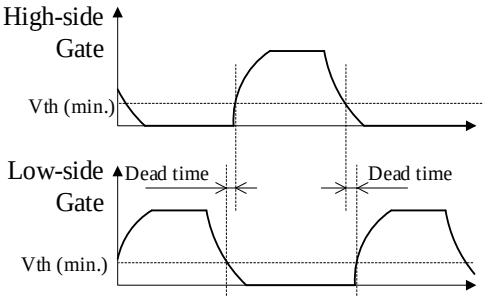


Figure 9-5. Dead Time Confirmation

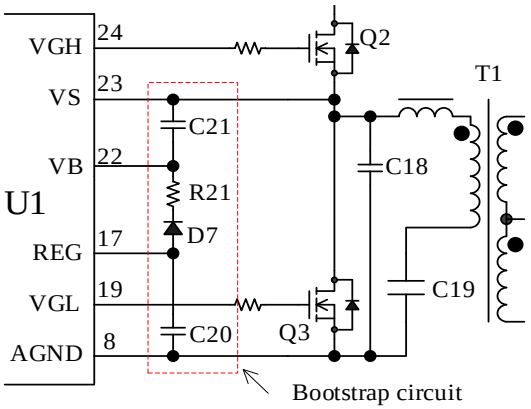


Figure 9-6. Bootstrap Circuit

9.2.15. VB and VS

The VB pin is the input of the high-side floating power supply, whereas the VS pin is the ground of the high-side floating power supply. The SSC4S913 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins (see Section 9.20). Figure 9-6 is a schematic diagram of the bootstrap circuit that drives the high-side power MOSFET (Q2). In the condition where the high-side power MOSFET is turned off and the low-side power MOSFET (Q3) is turned on, the VS pin voltage has almost the same potential as the ground. Then, C21 is charged with the REG pin. When the voltage between the VB and VS pins (hereafter "VB–VS voltage") increases to $V_{BUV(ON)}$ = 6.8 V or more, the internal high-side driver starts operating. When the VB–VS voltage decreases to $V_{BUV(OFF)}$ = 6.4 V or less, the internal high-side driver stops operating. This sequence of operations is the VB pin undervoltage lockout (VB_UVLO). In case both the ends of C21 are shorted, the IC is protected by VB_UVLO. The bootstrap circuit components must meet the following:

- **D7**

D7 should be a fast recovery diode with a short recovery time and a low reverse current. When the maximum supply input voltage is specified at 265 VAC, it is recommended to use a fast recovery diode with V_{RM} = 600 V.

- **C20, C21, and R21**

The values of C20, C21, and R21 are determined by the following parameters: the total amount of Q2 gate charge, Qg; the amount of a voltage dip between the VB and VS pins during operation at the lowest oscillation frequency. C20, C21, and R21 should be adjusted according to voltages measured by a high-voltage differential probe so that VB–VS voltage exceeds $V_{BUV(ON)}$ = 6.8 V. C20 and C21 should be film or ceramic capacitors with a low ESR and a low leakage current. The reference value of C20 is 1.0 µF. The time constants of C21 and R21 should be set within 500 ns. C21 is 0.047 µF to 0.1 µF; R21 is 2.2 Ω to 10 Ω.

9.2.16. ST

This is the input pin for startup currents and for X-capacitor discharge currents at power supply cutoff. For startup operation, see Section 9.3; for the X-capacitor discharge function, see Section 9.5.

The resistor R1 (about 10 kΩ) is connected to the ST pin. Since a high voltage is applied on R1, the following must be taken into account in actual designing: select a resistor designed to stand against electromigration; configure R1 with come serial resistors to reduce each applied voltage.

9.3. Startup and Shutdown Operations

Figure 9-7 shows the ST and VCC pins and their peripheral circuit. Figure 9-8 shows the operation waveforms during the startup.

The SSC4S913 incorporates its own startup circuit, which is connected to the ST pin. When the ST pin voltage rises after power-on, the constant startup current regulated inside the IC (I_{CC} = −11.0 mA) starts charging the electrolytic capacitor C8, which is connected to the VCC pin. When the VCC pin voltage increases to $V_{CC(ON)}$ = 17.0 V, the VG pin starts oscillating, and the IC starts the PFC stage controls. The VG pin on-time persists longer as the COMP pin voltage increases.

When the PFC output voltage, $V_{PFC(OUT)}$, increases and the FB_PFC pin voltage increases to $V_{LLC(ON)}$ = 1.875 V or more, the startup circuit is stopped. At the same time, the VGH and VGL pins in the LLC stage start oscillating in the soft start mode. During the soft start operation, the secondary-side output power increases as the oscillation frequencies of the VGH and VGL pins gradually decrease (see Figure 9-9). After the secondary-side output power increases, the LLC stage shifts to the operation with the oscillation frequency control using feedback signals. The related characteristics are defined as follows: the Maximum Oscillation Frequency at Soft Start, $f_{SS(MAX)}$ = 600 kHz; the Soft Start Period, t_{ss} =28 ms. The LLC soft start function suppresses electrical stress on the peripheral components and prevents any capacitive operation in the LLC stage from occurring.

After the LLC stage starts switching operation, a voltage to be applied on the VCC pin is the rectified auxiliary winding voltage, V_{DL}, as shown in Figure 9-7. After the power startup sequence ends, the startup circuit turns off automatically to eliminate the power dissipation by itself.

t_{START} is a period of time until the PFC stage starts operating (see Figure 9-8), and is determined by the capacitance of C8. The approximate startup time, t_{START}, can be calculated by Equation (2) below: The capacitance of C8 must be set to ≥ 47 μF.

$$t_{START} = C8 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{I_{CC} - I_{CC(OFF)}} \quad (2)$$

Where:

t_{START} is the startup time of the IC (s),

$V_{CC(INT)}$ is the initial VCC pin voltage (V),

I_{CC} is the startup current (−11.0 mA), and

$I_{CC(OFF)}$ is the circuit current in non-operation (1.0 mA).

The winding turns of the auxiliary winding, D, should be adjusted so that the VCC pin voltage falls within the range defined by Equation (3), in accordance with the power supply specifications giving the variation range of input and output voltages. The reference voltage across an auxiliary winding is about 17 V.

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.})$$

$$\Rightarrow 10.6\ \text{V} < V_{CC} < 30.0\ \text{V} \quad (3)$$

Once the power supply stops, the PFC output voltage, $V_{PFC(OUT)}$, decreases. Along with the decrease in $V_{PFC(OUT)}$, the FB_PFC pin voltage also decreases. When the FB_PFC pin voltage falls below $V_{LLC(OFF)}$ = 1.350 V, the VGH and VGL pins stop oscillating. Note that the bias assist function (Section 9.4) is disabled at this point. Accordingly, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.7 V or less, the IC stops its operations, including the VG pin oscillation.

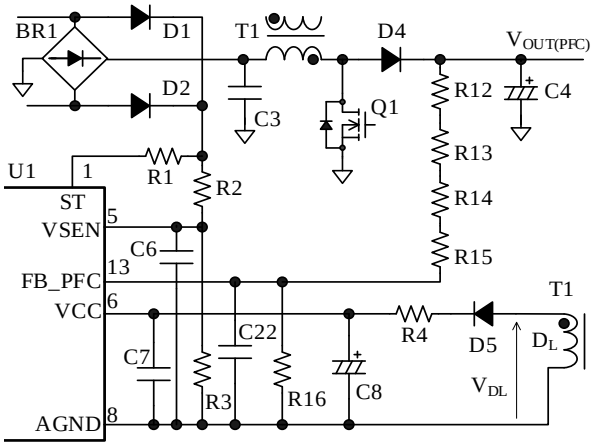


Figure 9-7. ST and VCC Pins and Their Peripheral Circuit

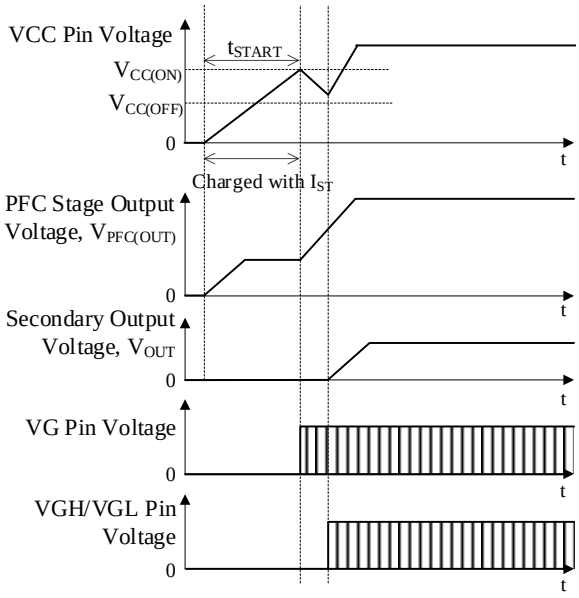


Figure 9-8. Operational Waveforms at Startup

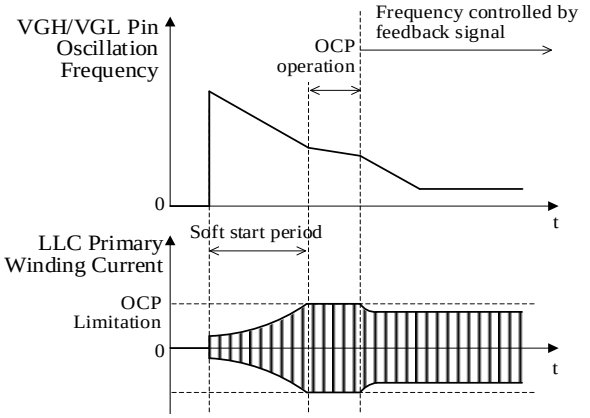


Figure 9-9. LLC Soft Start Operation

9.4. Bias Assist Function

The IC has the bias assist function to suppress a voltage drop in the VCC pin voltage. When the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.8 V, even during normal operation, the bias assist function is activated. When the bias assist function is activated, the startup current, I_{CC} = −11.0 mA, is supplied to the VCC pin through the startup circuit. As a result, the VCC pin voltage drop can be suppressed.

9.5. X-capacitor Discharge Function

In general, a line filter is inserted in the input side of a switching power supply, as illustrated in Figure 9-10.

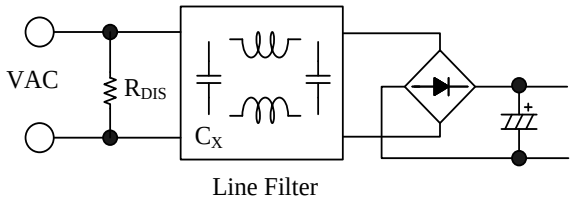


Figure 9-10. Typical Line Filter Circuit

As per IEC 62368-1 safety requirements, the voltage across the capacitor of line filter (i.e., X-capacitor, C_X) of ≥0.3 µF must be decreased to 60 V or less within 2 seconds after AC input voltage cutoff. Therefore, the discharge resistor, R_{DIS}, is connected in parallel with C_X, as a common approach to meet the requirements. While the AC input voltage is applied, R_{DIS} constantly consumes power. However, the IC implements the X-capacitor discharge function to remove such commonly used R_{DIS}, thus enhancing its circuit efficiency. Power dissipation in R_{DIS}, P_{RDIS}, can be obtained by Equation (4), below:

$$P_{RDIS} = \frac{V_{AC(RMS)}{}^2}{R_{DIS}} \quad (4)$$

Let $V_{AC(RMS)}$ be the effective value of the AC input voltage.

Hence, if the combined resistance of R_{DIS} = 1 MΩ and the AC input voltage = 265 V, P_{RDIS} becomes about 70 mW.

By determining whether the input voltage is AC or DC, the IC enables the X capacitor discharge function (AC input mode) when the input voltage is AC and disables it (DC input mode) when the input voltage is DC.

The IC determines whether the input voltage is AC or DC by counting how many times the rising edge of the signal input to the VSEN pin exceeds the reference voltage of 0.65 V inside the IC (internal AC determination signal) during the determination period. The determination period is the period during which the VCC pin voltage rises from $V_{CC(BIAS)}$ to $V_{CC(ON)}$ during IC startup. The determination period depends on the capacitance of the capacitor, C8, connected to the VCC pin. C8 must be set so that the full-wave rectified signal is input three times or more during the determination period (i.e. the determination period is 30 ms or more when the AC input is 50 Hz).

9.5.1. AC Input Mode

As shown in Figure 9-11, if the internal AC determination signal during the determination period is 2 counts or more, the input voltage is determined to be AC. When the VCC pin voltage exceeds $V_{CC(ON)}$, the X-capacitor discharge function is enabled (AC input mode).

Figure 9-12 illustrates the ST pin and its peripheral circuit, whereas Figure 9-13 depicts operational waveforms at X-capacitor discharge.

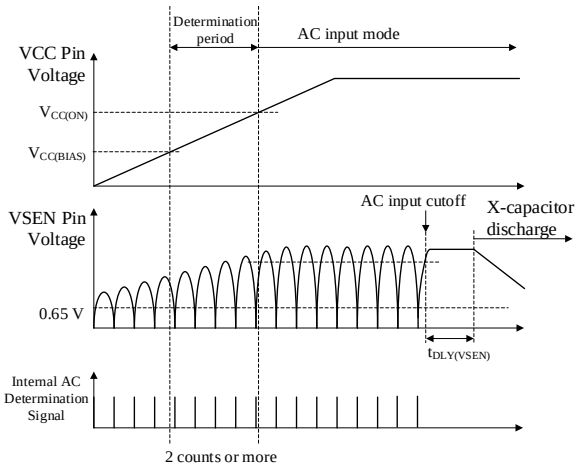


Figure 9-11. AC Input Voltage

When a supply input voltage is applied at startup, the VSEN pin voltage increases to the on threshold voltage, $V_{SEN(ON)}$ = 0.900 V or more, and the IC starts operating. From the half-wave rectified voltage yielded immediately after the operation start (as in Figure 9-13), the IC detects the AC input voltage whichever threshold the VSEN pin voltage reaches, $V_{SEN(OFF)1}$ = 0.750 V or $V_{SEN(AC)1}$ = 2.025 V. By this means, the X-capacitor discharge function supports a wide range of input specifications such as universal input standards.

After an AC input voltage cutoff, the VSEN pin voltage becomes almost constant and the two thresholds, $V_{SEN(OFF)1}$ and $V_{SEN(AC)1}$, are no longer detectable. When the VSEN Pin Delay Time, $t_{DLY(VSEN)}$ = 52 ms or longer, elapses after the IC stops detecting these thresholds, X-capacitor is discharged with a constant current, I_{ST} = 15.0 mA. The internal threshold voltages are automatically shifted according to which of the VSEN pin threshold voltages has been detected: $V_{SEN(OFF)2}$ = 0.600 V when $V_{SEN(OFF)1}$, and $V_{SEN(AC)2}$ = 1.800 V when $V_{SEN(AC)1}$. This is how the IC ensures its stable detection of AC input voltages.

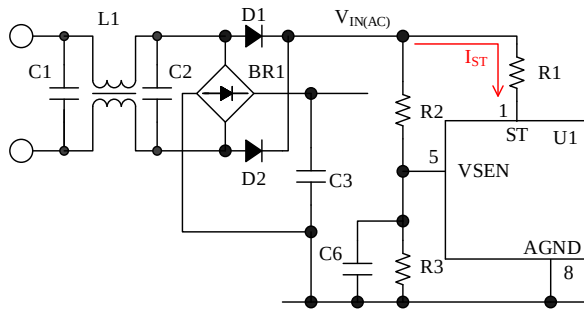


Figure 9-12. ST and VSEN Pins and Their Peripheral Circuit

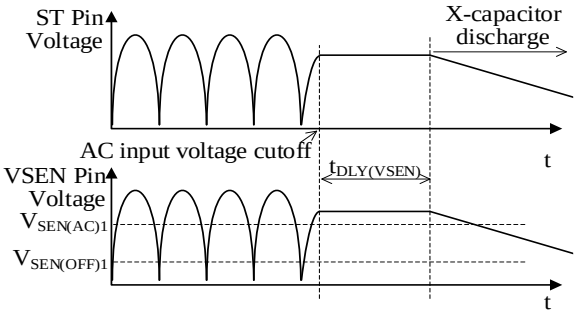


Figure 9-13. Operational Waveform at X-capacitor Discharge

9.5.2. DC Input Mode

As shown in Figure 9-14, if the internal AC determination signal during the determination period is less than 2 counts, the input voltage is determined to be DC. When the VCC pin voltage exceeds $V_{CC(ON)}$, the X-capacitor discharge function is disabled (DC input mode). In DC input mode, when the input voltage drops after a power supply cutoff, both the PFC circuit and LLC circuit stop switching operation by the undervoltage protection (see Section 9.6.2).

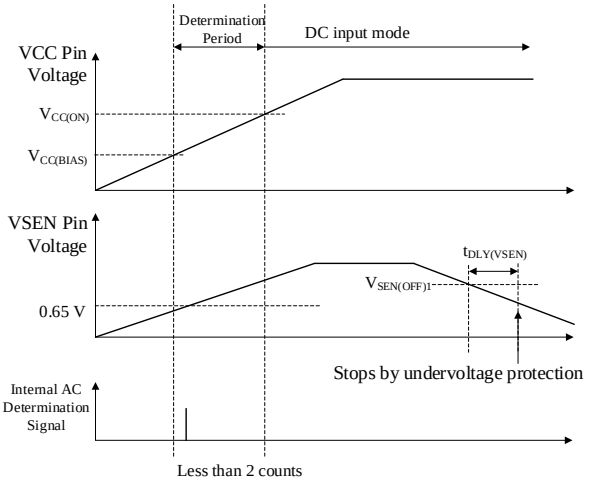


Figure 9-14. DC Input Voltage

9.6. Input Voltage Protection

The input voltage protection includes two protections: the high-voltage protection (HVP) for higher supply input voltages, and the undervoltage protection (UVP) for lower supply input voltages. These protections suppress the component overheating and thermal damage caused by overcurrent or overvoltage. The VSEN pin is used for detecting AC input voltages. According to the levels that the VSEN pin voltage reaches, the IC turns on and off the PFC stage (the VG pin) and the LLC stage (the VGH and VGL pins) switching operation. Sections 9.6.1 and 9.6.2 describe the two functions, HVP and UVP, respectively. Figure 9-15 illustrates the VSEN pin and its peripheral circuit, whereas Figure 9-16 depicts operational waveforms during the AC input voltage protection.

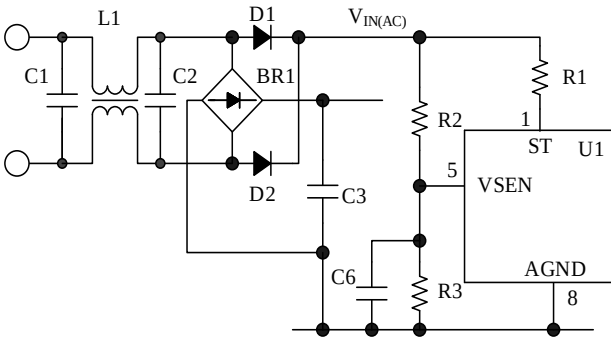


Figure 9-15. VSEN Pin and Its Peripheral Circuit

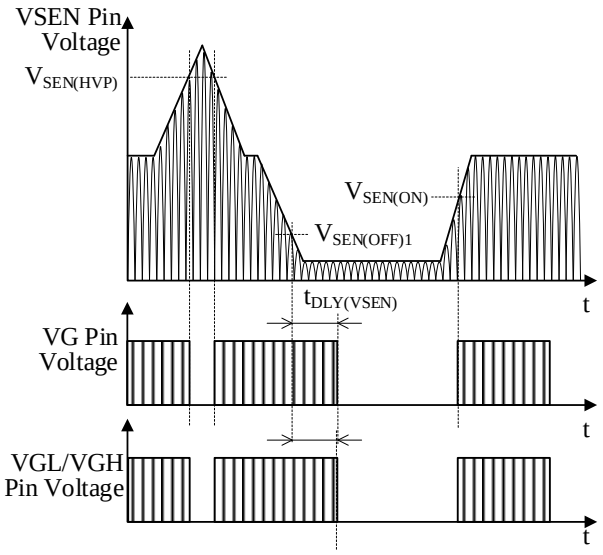


Figure 9-16. Waveforms during Input Voltage Protection

If an input resistance or a forward voltage of a rectifier diode is not factored into, the equation below determines a reference effective value of the AC input voltage at which the HVP or UVP is activated:

$$V_{AC(OP)} = \frac{1}{\sqrt{2}} \times V_{SEN(TH)} \times \left(1 + \frac{R2}{R3}\right) \quad (5)$$

Where:
$V_{AC(OP)}$ is the effective value of AC input voltage at which the HVP or UVP operates, and
$V_{SEN(TH)}$ is the VSEN pin threshold voltage (see Table 9-1).

Table 9-1. VSEN Pin Threshold Voltages

Parameter	Symbol	Value (Typ.)
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$	4.20 V
VSEN Pin UVP Release Voltage 1	$V_{SEN(OFF)1}$	0.750 V
VSEN Pin UVP Threshold Voltage	$V_{SEN(ON)}$	0.900 V

R2 is set at high resistance such that high voltage is applied on it. Therefore, the following must be taken into account in actual designing: select a resistor designed to stand against electromigration; configure R2 with some serial resistors to reduce each applied voltage.

The reference resistance of R2 is about 10 MΩ. The reference capacitance of C6, the noise filter capacitor shown in Figure 9-15 is 1 nF to 10 nF. R2, R3, and C6 should be selected based on operation performance in an actual application.

9.6.1. Input High-voltage Protection

As Figure 9-15 shows, the input voltage, $V_{IN(AC)}$, divided by the detection resistors is applied to the VSEN pin for the input voltage protection. When the VSEN pin voltage, V_{VSEN}, increases along with an input voltage rise from its steady-state level and reaches the VSEN pin HVP threshold voltage, $V_{SEN(HVP)}$ = 4.20 V or more, the high-voltage protection (HVP) is activated. Then, the LLC stage switching operation stops. The VCC pin voltage then decreases with a stop of switching operation. When VCC ≤ $V_{CC(P.OFF)}$, the IC releases the HVP operation and restarts. When the VCC pin voltage is increased by startup current and reaches $V_{CC(ON)}$ after the HVP release, the control circuit resumes operating. In this way, the intermittent operation by the VCC_UVLO is repeated during the HVP operation.

When $V_{VSEN} \leq V_{SEN(HVP)}$ after the input voltage lowers, the IC returns to its normal operation.

9.6.2. Input Undervoltage Protection

When an input voltage falls below its steady-state level, the VSEN pin voltage, V_{VSEN}, decreases to the off threshold, $V_{SEN(OFF)1}$ = 0.750 V or less. And when this condition persists for the VSEN Pin Delay Time, $t_{DLY(VSEN)}$ = 52 ms or longer, even with the IC being in an operation state (i.e., $V_{CC(OFF)} \leq$ VCC), the LLC stage switching operation stops. The VCC pin voltage then decreases with a stop of switching operation. When VCC ≤ $V_{CC(OFF)}$, the IC stops operating. When VCC ≥ $V_{CC(ON)}$ and $V_{VSEN} \geq V_{SEN(ON)}$ of 0.900 V after the input voltage rises, the IC returns to its normal operation.

9.7. VCC Pin Overvoltage Protection

When the voltage between the VCC and GND pins increases to $V_{CC(OVP)}$ = 32.0 V or more, the VCC pin overvoltage protection (VCC_OVP) is activated. Then, the LLC stage (the VGH and VGL pins) stops its switching operation. During the VCC_OVP operation, the circuit current decreases to $I_{CC(P)}$ = 1.6 mA, and the bias assist function is disabled. The VCC pin voltage then decreases. When VCC ≤ $V_{CC(P.OFF)}$, the IC releases the VCC_OVP operation. When the VCC pin voltage is increased by startup current and reaches $V_{CC(ON)}$ after the VCC_OVP release, the control circuit resumes operating. In this way, the intermittent operation by the VCC_UVLO is repeated during the VCC_OVP operation.

When the VCC pin voltage is supplied through the auxiliary winding of the transformer, the VCC pin voltage is proportional to the output voltage. As a result, the VCC pin can detect a secondary-side overvoltage condition caused by abnormality (e.g., when an output voltage detection circuit is open). The approximate value of the secondary-side output voltage, $V_{OUT(OVP)}$, at the VCC_OVP activation can be calculated by Equation (6)

below.

$$V_{OUT(OVP)} = \frac{V_{OUT(NRM)}}{V_{CC(NRM)}} \times 32.0\ (V) \qquad (6)$$

Where:

$V_{OUT(NRM)}$ is the secondary-side output voltage in normal operation, and

$V_{CC(NRM)}$ is the VCC pin voltage in normal operation.

9.8. PFC Constant Voltage Control and Critical Conduction Mode Control

The SSC4S913 employs the critical conduction mode (CRM) control for the PFC stage. When detecting a state that the current through the boost winding, P_P, of T1 becomes zero during Q1 turn-off, the IC turns on the power MOSFET (Q1). The auxiliary winding, D_P, of T1 and ZCD pin detect zero-current signals. The FB_PFC pin is used for controlling the PFC output voltage, $V_{OUT(PFC)}$, to be constant. In this control, a value of Q1 on-time is suitably determined according to the load range applied.

9.8.1. PFC Constant Voltage and On-time Controls

Figure 9-17 is an internal block diagram describing the FB_PFC and COMP pins and their peripheral circuit.

The VG pin on-time is controlled as follows. The internal error amplifier ("Error Amp." In Figure 9-17) connected to the FB_PFC pin compares the FB_PFC pin input voltage to the FB_PFC Pin Feedback Reference Voltage, V_{REF_PFC} = 2.500. The output voltage of the error amplifier is averaged and phase-compensated by C11 and R11 connected to the COMP pin. The waveforms of the COMP pin voltage, V_{COMP}, and the ramp voltage, V_{OSC}, are then compared to determine an on-time of the VG pin. Through C11 set to respond to a low frequency of ≤ 20 Hz, the on-times are regulated to be almost constant within the cycles of commercial AC input voltages (Figure 9-18).

The on-times vary depending on load ranges. C11 and R11 can also be used for adjusting a response speed at load variation. C11 is about 1 µF; R11 is about 68 kΩ. When C11 has a very large capacitance, unstable operations such as an output voltage drop may occur due to a slower response at dynamic variation. Therefore, be sure to adjust setting values based on the operational performance checked with an actual board. C12 for averaging output ripples is about 1 µF. When C12 has a very small capacitance, the IC may become more prone to unstable operations due to output ripples.

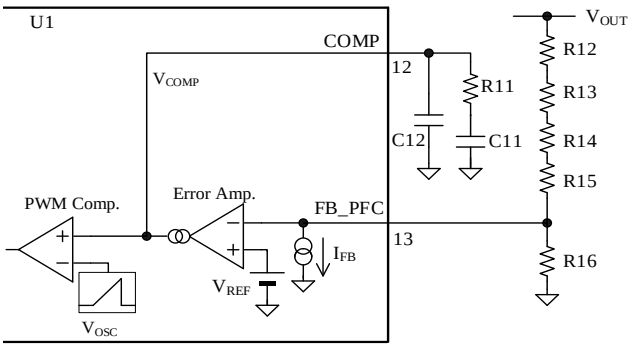


Figure 9-17. Internal Block Diagram of FB_PFC and COMP Pins and Their Peripheral Circuit

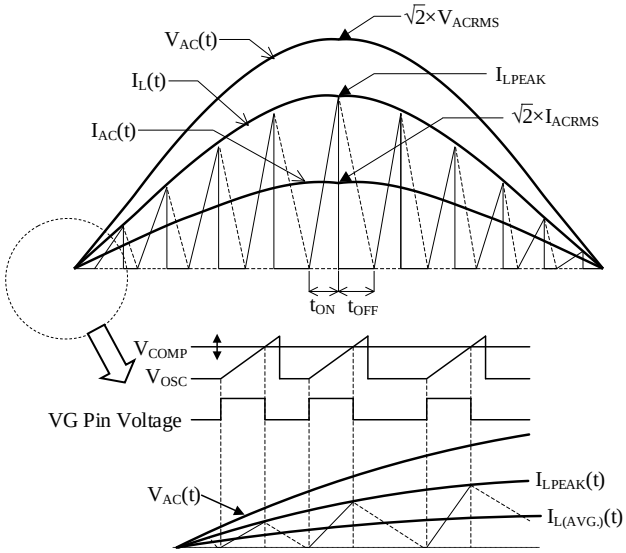


Figure 9-18. Operational Waveforms

9.8.2. Critical Conduction Mode (CRM) and Off-time Control

An off-time ends at the timing when the IC detects that the current through the boost winding, P_P, of T1 becomes zero. The zero current detection proceeds as follows. A zero-current signal detected by R10 and C10, which are connected to the auxiliary winding, D_P, is input to the ZCD pin. The winding, P_P, and winding, D_P, of transformer, T1, have the polarities shown in Figure 9-19.

When the VG pin voltage becomes low and Q1 turns off, the positive voltage of auxiliary winding, D_P, is applied on the ZCD pin as shown in Figure 9-20. After Q1 turns off, VG pin voltage maintains low while the ZCD pin voltage is above $V_{ZCD(H)}$ = 1.40 V. The ZCD pin voltage then decreases to $V_{ZCD(L)}$ = 0.70 V or less. And this condition indicates that the current through L1 has become zero, thus the IC turns on Q1 by turning the VG pin voltage high after a lapse of $t_{DLY(ZCD)}$ = 70 ns or longer.

When the current through the boost winding, P_P, becomes zero after the Q1 turn-off, the waveform of the drain-to-source voltage, V_{DS}, of Q1 starts free oscillation at the frequency based on the inductance, L_P, of P_P, the output capacitance, C_{OSS}, of Q1, and the parasitic capacitance. The bottom point of V_{DS} is the half cycle of the free oscillation and can be calculated by the Equation (7) below.

$$t_{HFP} \approx \pi\sqrt{L_P \times C_V}\ (s) \qquad (7)$$

Where:
t_{HFP} is the half cycle of free oscillation (s),
L_P is the inductance of boost winding, P_P (H), and
C_V is the combined capacitance (F) of output capacitance of power MOSFET, C_{OSS}, and parasitic capacitance.

Equation (8) defines DOFF, the off duty of a CRM-driven boost converter, where $V_{AC}(t)$ is the AC input voltage at a point in time. As expressed by the equation below, D_{OFF} has a proportional relationship to input voltages.

$$D_{OFF}(t) = \frac{V_{AC}(t)}{V_{OUT(PFC)}} \qquad (8)$$

As explained above, the IC detects zero current with the ZCD pin voltage and controls the turn-on timing of Q1. This determines the Q1 off-time and I_{LPEAK}, the peak current of the inductance current (I_L), is formed into a sinusoidal waveform as seen in Figure 9-18. Smoothing ripple currents by a low pass filter in the input side can yield the input currents whose waveforms are similar to the sinusoidal AC input voltage waveform. This results in a circuit with a high power factor. To calculate the inductance, set the minimum operating frequency higher than the audible frequency of 20 kHz.

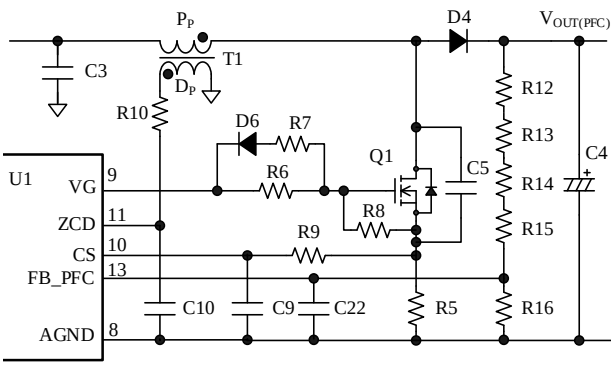


Figure 9-19. PFC Circuit

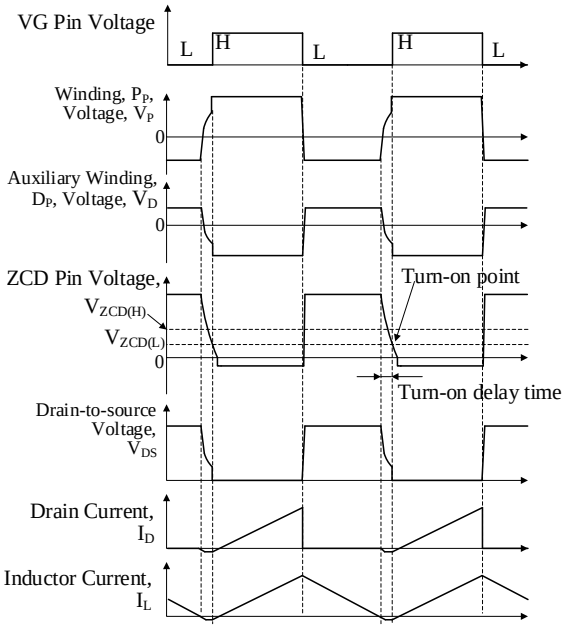


Figure 9-20. CRM Operation vs. Bottom-on Operation

Set the value of the current-limiting resistor R10 so that the input/output current of the ZCD pin does not exceed the absolute maximum ratings. The recommended value of ZCD pin current is 3 mA or less. For the resistance of R10, choose the values that satisfy both Equations (9) and (10).

1) Limitation by ZCD pin source current (at power MOSFET turn-on)

$$R10 > \frac{\sqrt{2} \times V_{ACRMS(MAX)} \times \frac{N_D}{N_P}}{3 \times 10^{-3}(A)}\ (\Omega) \qquad (9)$$

Where:
$V_{ACRMS(MAX)}$ is the maximum effective value of the AC input voltage (V),
N_P is the number of turns of boost winding, P_P, (turns), and
N_D is the number of turns of auxiliary winding, D_P, (turns).

2) Limitation by ZCD pin sink current (at power MOSFET turn-off)

$$R1 > \frac{V_{OUT} \times \frac{N_D}{N_P}}{3 \times 10^{-3}(A)}\ (\Omega) \qquad (10)$$

Where:
V_{OUT} is the output voltage (V),
N_P is the number of turns of boost winding, P_P, (turns), and
N_D is the number of turns of auxiliary winding, D_P, (turns).

Adjust the bottom-on timing with C10 and R1 as shown in Figure 9-21.

Be sure to adjust the peripheral constants of the ZCD pin based on the operational performance, including EMI noise levels, checked with an actual board.

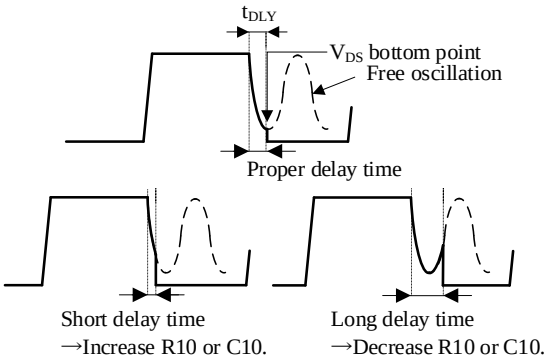


Figure 9-21. V_{DS} Turn-on Timing

9.9. PFC Maximum Oscillation Frequency Limitation Function

In the CRM-driven PFC stage, an oscillation frequency of the power MOSFET (Q1) varies in a single cycle of the sine wave of AC input voltage signals. The oscillation frequency becomes the lowest at the peak of a sine wave but becomes higher as it gets close to the bottom of the sine wave. Besides, when a load decreases, the overall oscillation frequency increases.

To suppress an increase in switching loss, the IC has the maximum oscillation frequency limitation function that limits the maximum frequency to f_{MAX} = 300 kHz.

9.10. PFC Maximum On-time

For a reduction in audible noises induced by a transient-state transformer, the maximum on-time of the power MOSFET (Q1) in the PFC stage is limited to t_{MAX_PFC} = 18.3 µs.

9.11. PFC Overcurrent Protection

Figure 9-22 shows the CS pin and its peripheral circuit. The IC has the PFC overcurrent protection (PFC_OCP). For overcurrent detection, the inductor current at power MOSFET (Q1) turn-on, $I_{L(ON)}$, is detected by the current detection resistor, R5. The voltage across R5, V_{RCS}, is then input to the CS pin. The CR filter consisting of R9 and C9 is connected to the CS pin.

The PFC_OCP includes two types that are activated at different current levels.

9.11.1. PFC Overcurrent Protection 1

When the voltage across R5, V_{RCS}, increases to $V_{CS(OC1)}$ = 0.50 V or more, the output of the VG pin is turned off on a pulse-by-pulse basis, resulting in the reduction of the drain current of Q1. As a result, the increase in the drain current of Q1 is suppressed.

9.11.2. PFC Overcurrent Protection 2

The PFC overcurrent protection 2 (PFC_OCP2) is the overcurrent protection that works when instantaneous large currents flow such as a short circuit of the boost diode, D4. When the CS pin voltage increases to $V_{CS(OC2)}$ = 1.50 V or more due to an instantaneous large current, the PFC_OCP2 gets activated and puts the VG pin output into a latched low state. When the FB_PFC pin voltage decreases to $V_{LLC(OFF)}$ or less with a drop of the PFC output voltage, the LLC stage operation stops. To release the latched state, decrease the VCC pin voltage to $V_{CC(OFF)}$ or less.

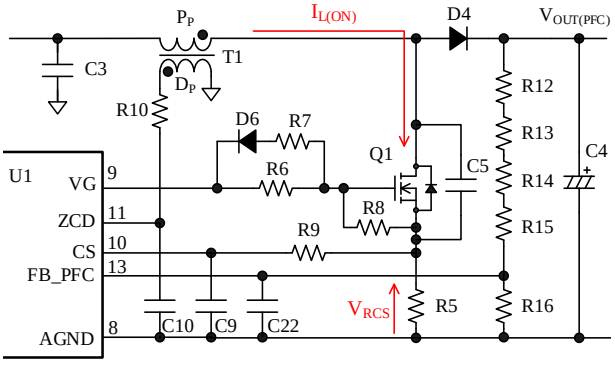


Figure 9-22. CS Pin and Its Peripheral Circuit

9.12. PFC Output Overvoltage Protection

The output overvoltage of the PFC stage is protected by the FB_PFC or OVP pins. Two types of overvoltage protection functions are available: automatic reset type of the FB_PFC pin, and latch type of the OVP pin. Therefore, activate the overvoltage protection of the FB_PFC pin normally. If the FB_PFC pin cannot be used for the overvoltage protection when some abnormality occurs, use the overvoltage protection of the OVP pin.

- **PFC Output Overvoltage Protection of FB_PFC Pin**

When the FB_PFC pin voltage reaches V_{OVP_PFC} (i.e., 1.060 times higher than V_{REF_PFC} = 2.500 V), the PFC output overvoltage protection (PFC_OVP) of the FB_PFC pin is activated. Then, the VG pin output immediately becomes logic low and the switching operation stops. This prevents any increase in the output voltage. When the FB_PFC pin voltage decreases to

$V_{OVP\_PFC} - V_{OVP\_PFC(HYS)}$ after the PFC_OVP activation, the VG pin resumes switching operation.

- **PFC Output Overvoltage Protection of OVP Pin**

When the OVP pin voltage reaches V_{OVP_PFC2} = 2.70 V or more, the PFC output overvoltage protection (PFC_OVP) of the OVP pin is activated. Then, the VG pin output immediately becomes logic low and the switching operation stops with the latched state. To release the output overvoltage protection, cut off the AC input voltage, and then decrease the VCC pin voltage to $V_{CC(P.OFF)}$ or less.

9.13. FB_PFC Pin Undervoltage Protection

The FB_PFC pin undervoltage protection (FB_PFC_UVP) is activated when the FB_PFC pin voltage drops by abnormal feedback loops. Abnormal feedback loops include the following states: R12 to R15 opened, R16 shorted, the FB_PFC pin opened. When the FB_PFC pin voltage decreases to V_{UVP_PFC} = 300 mV or less due to one or more of the abnormal feedback loops above, the VG pin output immediately becomes logic low and the PFC stage switching operation stops. This prevents any increase in $V_{OUT(PFC)}$. When the FB_PFC pin voltage increases to V_{UVP_PFC} + $V_{UVP(HYS)\_PFC}$ after the causes of the abnormal feedback loop are eliminated, the VG pin resumes switching operation.

9.14. Restart Circuit

This IC operates by self-oscillation. The VG pin off-time is determined by detecting the zero-current signal at the ZCD pin. When the VG pin off-time is maintained for t_{RS} = 220 µs or more, the restart circuit gets activated and turns on the VG pin. The VG pin on-time is $t_{ON(RS)}$ = 1.70 µs in the restart operation. At startup or light load, the IC operates in the intermittent oscillation that repeats oscillation and stop. In intermittent oscillation, the restart circuit operates for stable switching operation.

9.15. LLC Constant Voltage Control

Figure 9-23 shows a peripheral circuit of the FB_LLC and RC pins.

The capacitor, C15, and the optocoupler, PC1, should be connected to the FB_LLC pin. The feedback current depending on load ranges is sunk from the FB_LLC pin by the optocoupler. The FB_LLC pin voltage, V_{FB_LLC}, is regulated through this control technique.

In light load operation, V_{FB_LLC} decreases due to an increase in the current sunk by the optocoupler from the FB_LLC pin, resulting in a shorter on-time and a higher operating frequency. In heavy load operation, conversely, V_{FB_LLC} increases. And this results in a longer on-time and a lower operating frequency. By regulating oscillation frequencies in this manner, the IC can stabilize an output voltage (controlled in an inductance area).

When the peak value of V_{RC} increases to V_{RC_OCP1} = 1.87 V or more along with a rise in V_{FB_LLC} during heavy load operation, the LLC overcurrent protection (LLC_OCP) is activated to limit the currents through the LLC stage on a pulse-by-pulse basis. For more details on the LLC_OCP function, see Section 9.21.

C15 value is about 1 µF to 10 µF. Care must be taken in setting the value of C15 because it affects the maximum output power.

The secondary-side error amplifier should be designed so that collector current passing through the optocoupler PC1 is higher than 195 µA, i.e., higher than the absolute maximum source current of the FB_LLC pin. In particular, the current transfer ratio, CTR, of the optocoupler must take its performance decline over time into account in actual designing. The resistor R18 and capacitor C14 are used for phase compensation. R18 is about 2.2 kΩ; C14 is 0.1 µF. Be sure to confirm the actual operation in the application, and adjust the values.

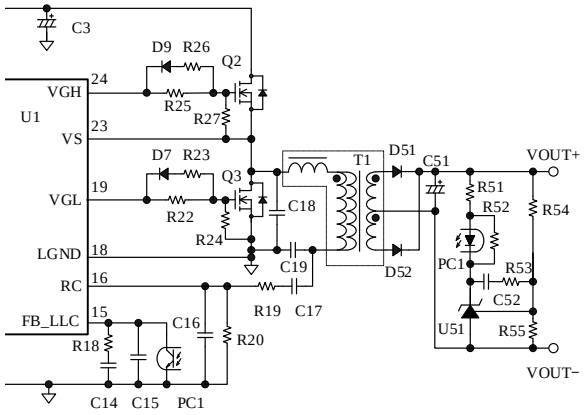


Figure 9-23. FB_LLC and RC Pins and Their Peripheral Circuit

9.16. Standby Function

The IC has the standby function that improves efficiency in light load operation. The IC can be shifted to standby operation with an external signal. The standby operation is interlocked between the LLC and PFC stages. For more details, see Section 9.16.2.

9.16.1. Shifting with External Signal

To switch standby and normal operations on an external signal basis, connect an on/off circuit to the MC pin as shown in Figure 9-24.

When the standby signal input pin in the secondary side becomes logic high, the optocoupler PC2 is turned on. This setting allows the IC to shift into the standby operation when the MC pin voltage decreases to $V_{MC(ON)}$ = 0.20 V (min.) or less. With the standby signal input pin being held at logic low, the IC returns from the standby operation to its normal operation when $V_{MC(OFF)}$ = 1.20 V (max.) or more, or V_{FB_LLC} > 1.50 V (typ.) (internal reference voltage).

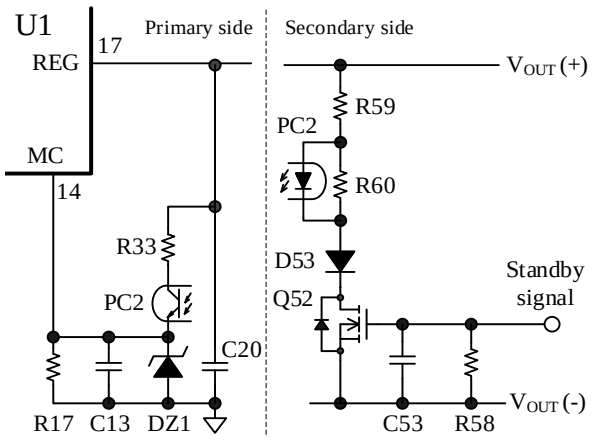


Figure 9-24. Standby Signal Input Circuit

9.16.2. Standby Operation

Figure 9-25 shows operational waveforms during the standby operation. Decrease in the MC pin voltage allows the IC to shift into the standby operation when $V_{MC} \leq V_{MC(ON)}$ of 0.55 V. During standby operation, both the PFC and LLC stages operate with burst oscillation for switching loss reduction.

In addition, the LLC stage prevents drain currents from varying steeply in burst oscillation by monitoring the FB_LLC pin voltage. This is the soft turn-on/off function which controls the switching frequencies of the VGH and VGL pins and thus suppresses audible noises produced by transformers used. The period of the LLC burst oscillation is internally controlled. When the LLC stage shifts to the burst oscillation, the IC controls the output voltage of the PFC stage based on the value of the FB_PFC pin voltage. When the FB_PFC pin voltage decreases to about 90% of the reference voltage, V_{REF_PFC}, the PFC stage (i.e., the VG pin) stops oscillating. When the FB_PFC pin voltage decreases further and reaches about 89% of V_{REF_PFC}, the VG pin resumes oscillating. In this way, the PFC stage performs the burst oscillation by detecting a variation in the FB_PFC pin voltage.

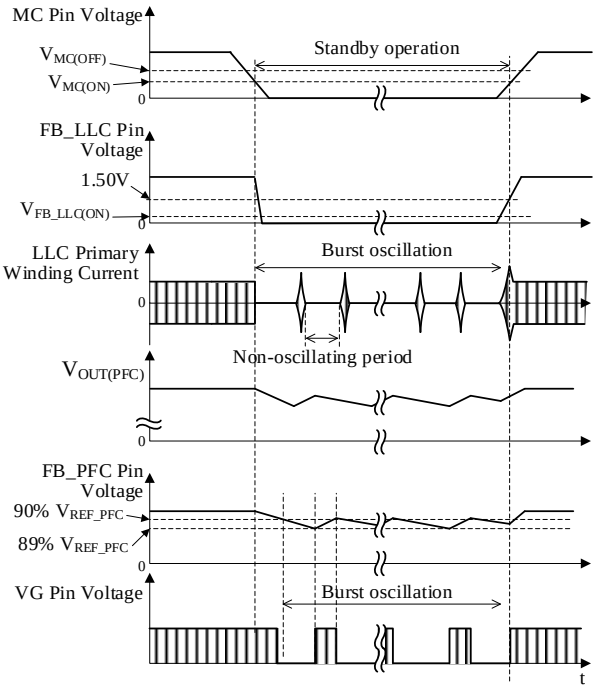


Figure 9-25. Operational Waveforms in Standby Operation

The LLC protection of the IC is also activated during the non-oscillating period during burst oscillation.

When burst oscillation stops in the condition of capacitive operation or overcurrent and non-oscillating period exceeds ≥ 80 ms (min.), the restart circuit (see Section 9.14) is activated. When the restart circuit operates during standby operation, check if there is capacitive mode operation occurring or if the overcurrent protection is activated due to switching noise.

9.17. LLC Automatic Dead Time Adjustment Function

A dead time is a period of time when both of the high- and low-side power MOSFETs (i.e., Q2 and Q3) in the LLC stage turn off. When the dead time is shorter than a voltage resonant period as in Figure 9-26, the power MOSFETs turn on or off during the voltage resonant period. In such case, switching loss increases due to hard switching by the power MOSFETs. To prevent such hard switching, the IC has the automatic dead time adjustment

function that the IC detects voltage resonant periods and automatically controls the zero voltage switching (ZVS) operations of Q2 and Q3. Even though voltage resonant periods differ according to the power supply specifications (input voltage, output power, etc.), the IC requires no dead time adjustment based on individual power supply specifications because of this function.

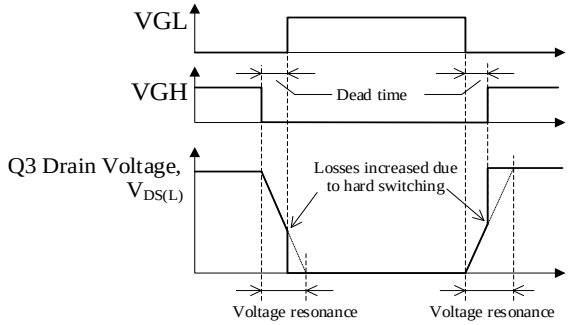


Figure 9-26. Waveforms When ZVS Failure Occurs

As shown in Figure 9-27, a dead time period is determined by the dv/dt period that is defined by the rising and falling voltage waveforms of $V_{DS(L)}$, the drain-to-source voltage of the low-side power MOSFET. The dv/dt period is detected by the VS pin. The ZVS operations of the high- and low-side power MOSFETs are automatically controlled based on this detection system. Note that the automatic dead time adjustment function operates within the period ranging from $t_{d(MIN)}$ = 0.24 µs to $t_{d(MAX)}$ = 1.65 µs.

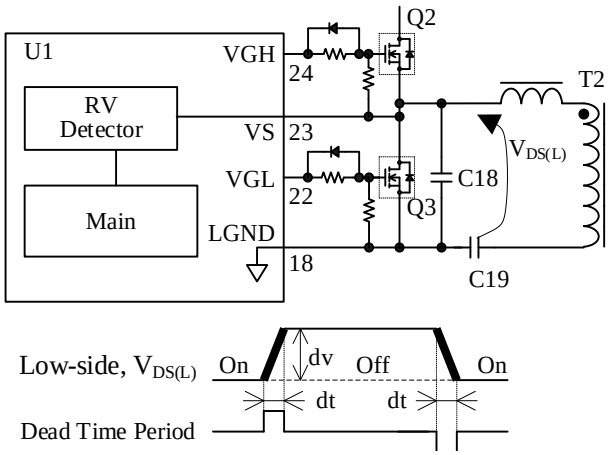


Figure 9-27. VS Pin and Dead Time Period

Also, actual operations must be checked to ensure that power MOSFETs operate with the zero current switching (ZCS) under the following conditions (i.e., check if a period in which drain current flows through a body diode exists for about 600 ns, as in Figure 9-28):

– When an output power is minimum in a maximum input voltage specification

– When an output power is maximum in a minimum input voltage specification

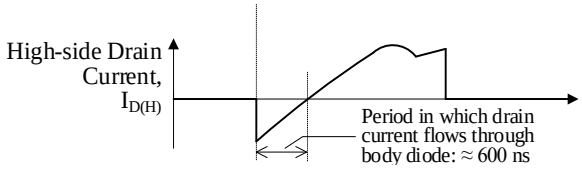


Figure 9-28. Point to Be Checked in ZCS

9.18. LLC Capacitive Mode Detection Function

The current resonant power supply must operate in the inductive area shown in Figure 9-29. In the capacitive area, the power supply enters capacitive mode. To prevent such operation, it is generally required to set a minimum oscillation frequency higher than f_0 defined for each power supply specification. The IC has the capacitive mode detection function that constantly maintains its frequency higher than f_0, thereby requiring no setting of minimum oscillation frequencies. Accordingly, enhanced design-friendliness will be added to your application. In addition, using resonant frequency of near f_0 increases the transformer use efficiency.

The RC pin detects a resonant current to determine if a capacitive operation has occurred. When the capacitive mode is maintained for 100 ms or longer, the LLC switching operation stops. During the LLC_OLP operation, the intermittent operation by the VCC_UVLO is repeated (see Section 9.21). As shown in Figure 9-31 and Figure 9-32, the threshold voltage for the capacitive mode detection changes according to the load ranges: V_{RC1} = ±0.10 V or V_{RC2} = ±0.30 V. The capacitive mode detection function is described further below. In the following descriptions, $Q_{(H)}$ represents the high-side power MOSFET, whereas $Q_{(L)}$ represents the low-side power MOSFET.

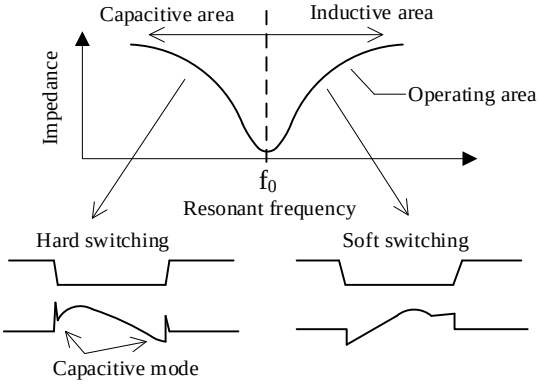


Figure 9-29. Operating Area of Resonant Power Supply

- **Q(H) Turn-on Period**

Figure 9-30 illustrates the RC pin waveform in the inductive area; Figure 9-31 and Figure 9-32 illustrate the RC pin waveforms in the capacitive area. In the inductive area, the RC pin voltage does not cross over the positive threshold voltage from high to low during the $Q_{(H)}$ turn-on period (see Figure 9-30). Conversely, in the capacitive area, the RC pin voltage crosses over the positive threshold voltage from high to low. At this point, a capacitive mode operation is detected. Then, $Q_{(H)}$ is turned off, whereas $Q_{(L)}$ is turned on (see Figure 9-31, Figure 9-32).

- **Q(L) Turn-on Period**

Contrary to the $Q_{(H)}$ case, in the capacitive area, the RC pin voltage crosses over the threshold, $-V_{RC1}$ or $-V_{RC2}$, from low to high during the $Q_{(L)}$ turn-on period. At this point, a capacitive mode operation is detected. Then, $Q_{(L)}$ is turned off, whereas $Q_{(H)}$ is turned on. Based on the capacitive mode detection on a pulse-by-pulse basis, the IC prevents any capacitive operation by synchronizing the LLC operating frequency with the capacitive mode frequency.

C17 and R20 must be set so that the absolute value of the RC pin voltage is higher than $|V_{RC2}| = 0.30$ V and is maintained within its absolute maximum rating of ±5.5 V. In addition to the peripheral component settings required for the LLC_OCP function (Section 9.21), the following operations prone to be capacitive mode must be taken into account when you set these components: startup, supply input voltage turn-off, output shorted, and dynamic load effect on a power system.

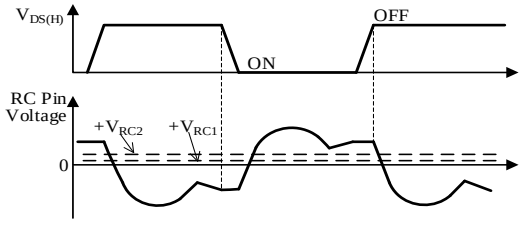


Figure 9-30. RC Pin Voltage Waveform in Inductive Area

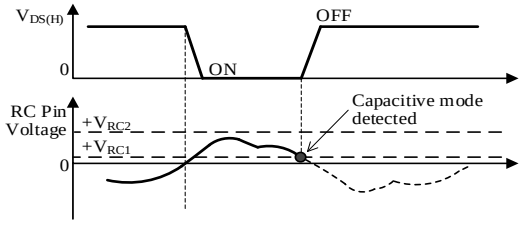


Figure 9-31. High-side Capacitive Mode Detection (in Light Load)

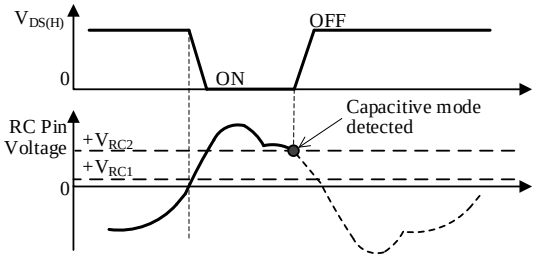


Figure 9-32. High-side Capacitive Mode Detection (in Heavy Load)

9.19. LLC Reset Detection Function

In a condition where the LLC feedback control remains inactive (e.g., during power startup), unbalanced circulating currents for resonant operation control will be incurred. This unbalanced circulating current can cause a hard switching operation that increases the stress of the power MOSFET. The unbalanced circulating current occurs when the LLC power MOSFET turns on at a negative current with the circulating current being not reset during an on-time. The circulating current is a current that flows through the primary side for carrying out a resonant operation. To prevent the hard switching operation, the IC has the reset detection function.

Figure 9-34 represents a high-side operation and the drain current waveforms at each case; normal resonant operation and reset failure. The reset detection function prevents hard-switching operations by extending an on-time until the absolute value of the RC pin voltage increases to $|V_{RC1}| = 0.10$ V or more. If the on-time is extended longer than the maximum Rest Time, $t_{RST(MAX)} = 5$ µs, the on-time immediately ends and the power MOSFET turns off (see Figure 9-33).

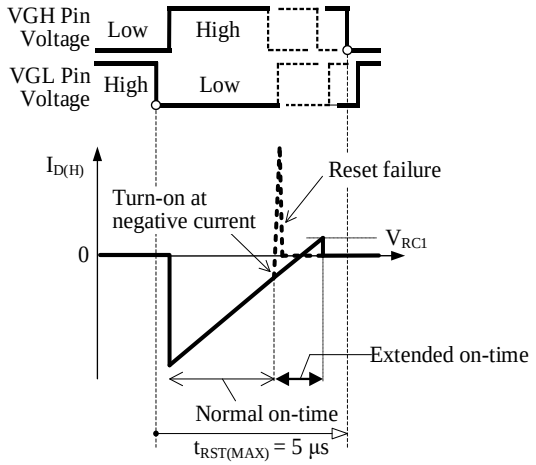


Figure 9-33. Typical Reset Detection during High-side Turn-on Period

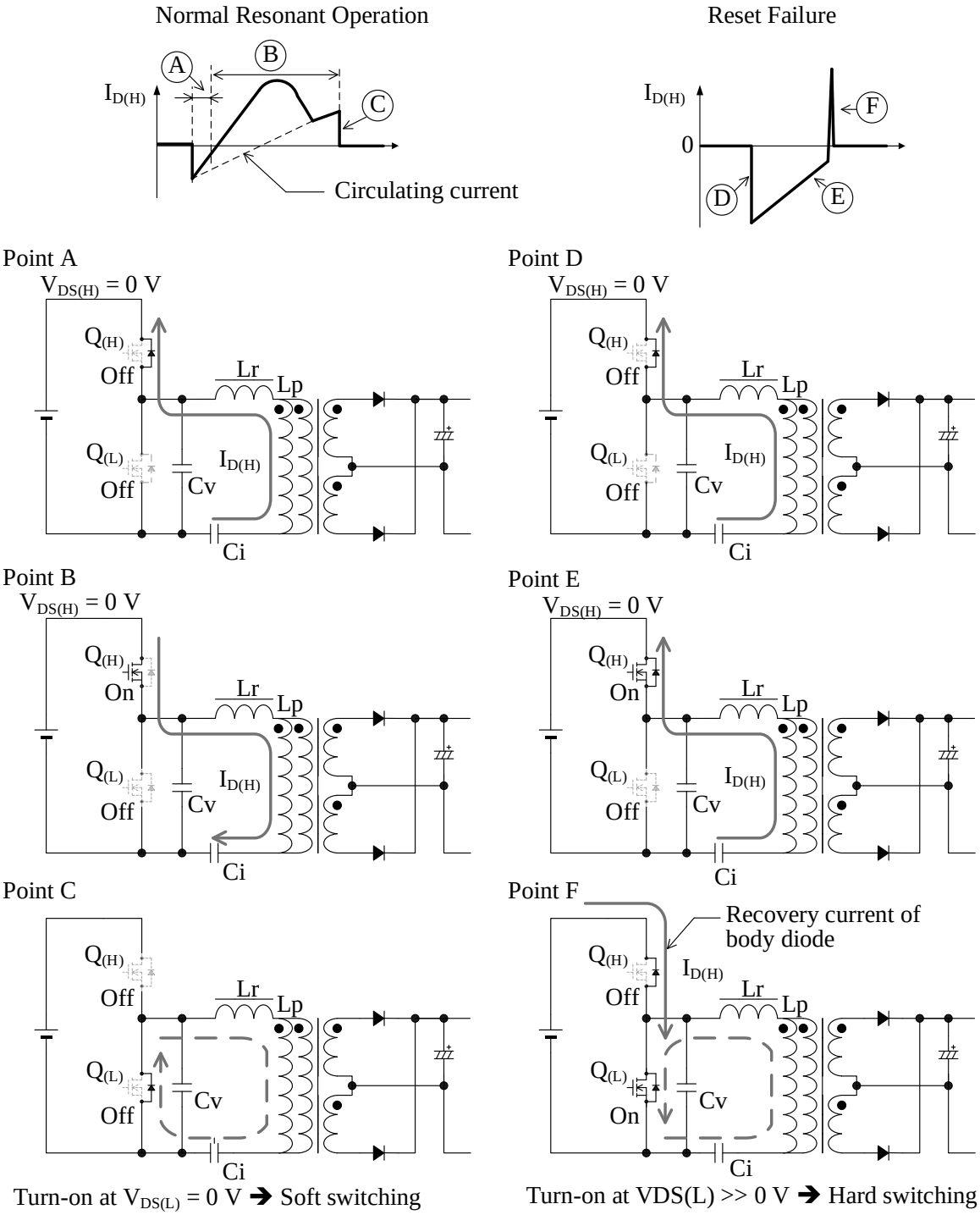


Figure 9-34. High-side Operation and Drain Current Waveforms at Normal Resonant Operation and Reset Failure

9.20. LLC High-side Driver Undervoltage Lockout

The SSC4S913 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins. When the voltage between the VB and VS pins (i.e., "VB–VS voltage") increases to $V_{BUV(ON)}$ = 6.8 V or more, the internal high-side driver starts operating. When the VB–VS voltage decreases to $V_{BUV(OFF)}$ = 6.4 V or less, the internal high-side driver stops operating. The VB_UVLO circuit protects the IC when the bootstrap circuit capacitor, C21, is shorted.

9.21. LLC Overcurrent Protection, LLC Overload Protection

The LLC overcurrent protection (LLC_OCP) detects the peak drain current of the power MOSFET on a pulse-by-pulse basis, and limits the output power. The value of the shunt capacitor, C17, shown in Figure 9-35, is set to be considerably smaller than that of the current resonant capacitor, C19. Thus, the loss of detection resistor R20 is minimized because the detection current which is shunted from the primary-side winding is low. And this allows R20 to be smaller in size. There is no simplified method to obtain an accurate value of resonant current with parameters such as input and output conditions of the power supply. Therefore, R20 and C17 must be adjusted based on the operational performance checked with an actual board.

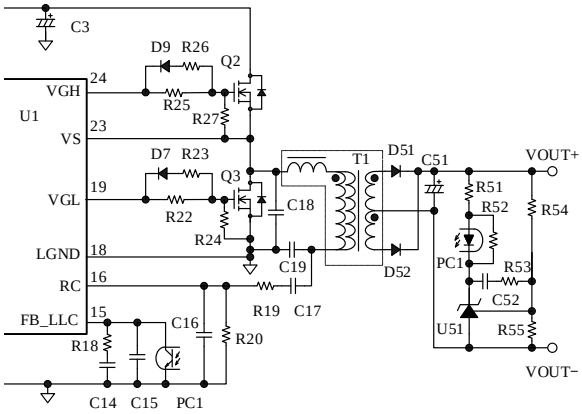


Figure 9-35. RC Pin and Its Peripheral Circuit

Here are reference constants for R20, C17, R19, and C16 and their adjustment methods:

- **R20, C17**

R20 is about 100 Ω; C17 is 0.1 nF to 0.33 nF (i.e., about 1% of a C19). The detection voltage across R20 is also used for the capacitive mode detection described in Section 9.18. Therefore, R20 and C17 require adjustments for using in both the overcurrent detection and capacitive mode detection.

- **R19, C16**

These are used for reducing high-frequency noises. R19 is 100 Ω to 470 Ω; C16 is 0.1 nF to 1 nF.

The LLC_OCP includes two types that are activated at different current levels.

9.21.1. LLC Overcurrent Protection 1

When the current through the LLC power MOSFET increases and the absolute value of the RC pin voltage rises above $|V_{RC\_OCP1}|$ = 1.87 V, the LLC overcurrent protection 1 (LLC_OCP1) is activated. Then, the IC increases the LLC switching frequency to suppress the output power.

9.21.2. LLC Overcurrent Protection 2

The LLC overcurrent protection 2 (LLC_OCP2) protects the LLC power MOSFET from having large currents. When the absolute value of the RC pin voltage rises above $|V_{RC\_OCP2}|$ = 2.76 V, the LLC_OCP2 is activated to immediately invert the on/off states of the power MOSFETs. At the same time, the switching frequency is promptly increased for suppressing the output power. When the output power decreases and the RC pin voltage decreases to $|V_{RC\_OCP2}|$ or less, the IC shifts into the LLC_OCP1 operation.

9.21.3. LLC Overload Protection

When the LLC_OCP1 condition persists for the LLC_OLP Delay Time, $t_{DLY(OLP)}$ = 100 ms or longer, the LLC overload protection (LLC_OLP) is activated. During the LLC_OLP operation, the LLC stage (the VGL and VGL pins) stops its switching operation. After the switching operation stops, the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(P.OFF)}$ or less, the IC releases the PFC_OLP operation and restarts. When the VCC pin voltage is increased by startup current and reaches $V_{CC(ON)}$ after the VCC_OVP release, the control circuit resumes operating. In this way, the intermittent operation by the VCC_UVLO is repeated during the LLC_OLP operation. When the causes of the overload condition are eliminated, the IC automatically returns to normal operation.

9.22. Thermal Shutdown

When the control circuit temperature reaches $T_{J(TSD)}$ = 140 °C (min.), the thermal shutdown (TSD) is activated. Then, the PFC stage (the VGP pin) and the LLC stage (the VGH and VGL pins) stop their switching

operations. To release the TSD, cut off the AC input voltage, and then decrease the VCC pin voltage to $V_{CC(P.OFF)}$ or less.

10. Design Notes

10.1. PFC Inductor Design

Inductor T1 consists of a boost winding P_P and auxiliary winding D_P. The winding P_P is used for boosting the voltage and winding D_P is used for off-timing detection.

The calculation methods of winding P_P and winding D_P are as shown below. Since the following calculating formulas are approximated, the peak current and the frequency of operational waveforms may be different from the setting value at calculating. Eventually, the inductance value should be adjusted in actual operation.

Apply proper design margin to temperature rise by core loss and copper loss.

10.1.1. Boost winding, P_P

Inductance L_P of PFC in CRM mode is calculated as follows:

1) Output Voltage, $V_{OUT(PFC)}$

The output voltage $V_{OUT(PFC)}$ of boost-converter should be set higher than peak value of input voltage as following equation:

$$V_{OUT(PFC)} \geq \sqrt{2} \times V_{ACRMS(MAX)} \times V_{DIF} \ (V) \qquad (11)$$

where

$V_{ACRMS(MAX)}$: Maximum AC input voltage rms value (V)

V_{DIF}: Boost voltage (about 10V) (V)

2) Operational Frequency, $f_{SW(SET)}$

Determine $f_{SW(SET)}$ that is minimum operational frequency at the peak of the AC line waveform. The frequency becomes higher with lowering the input voltage. The frequency at the peak of the AC line waveform, $f_{SW(SET)}$ should be set more than the audible frequency (20 kHz).

3) Inductance, L_P

Substituting both minimum and maximum of AC input voltage to V_{ACRMS}, choose a smaller one as L_P value. L_P is calculated as follows:

$$L_P = \frac{\eta \times {V_{ACRMS}}^2 \times \left(V_{OUT} - \sqrt{2} \times V_{ACRMS}\right)}{2 \times P_{OUT(PFC)} \times f_{SW(SET)} \times V_{OUT(PFC)}} \ (H) \quad (12)$$

where

V_{ACRMS}: Maximum or minimum AC input voltage rms value (V)

$P_{OUT(PFC)}$: Output Power (W)

$f_{SW(SET)}$: Minimum operational frequency at the peak of the AC line waveform (kHz)

(The operational frequency becomes lowest at the peak of the AC line waveform. $f_{SW(SET)}$ should be set above frequency of 20 kHz.)

η: Efficiency of PFC

(In general, the range of η is 0.90 to 0.97, depending on on-resistance of power MOSFET $R_{DS(ON)}$ and forward voltage drop of rectifier diode V_F.)

4) Inductor peak current, I_{LP}

I_{LP} is peak current at the minimum of AC input voltage waveform. I_{LP} calculated as follows:

$$I_{LP} = \frac{2\sqrt{2} \times P_{OUT(PFC)}}{\eta \times V_{ACRMS(MIN)}} \ (A) \qquad (13)$$

where,

$P_{OUT(PFC)}$: Output power (W)

$V_{ACRMS(MIN)}$: Minimum AC input voltage rms value (V)

η : Efficiency of PFC (About 0.90 to 0.97)

5) Maximum On-time, t_{MAX_PFC}

$t_{ON(MAX)\_OP}$ is calculated by Equation (14) with results of Equation (12) and Equation (13). $t_{ON(MAX)\_OP}$ is the maximum on time of the peak voltage of the minimum AC input voltage.

$$t_{ON(MAX)\_OP} = \frac{L_P \times I_P}{\sqrt{2} \times V_{ACRMS(MIN)}} \ (s) \qquad (14)$$

where,

L_P : Inductance value of the result of Equation (12)

$V_{ACRMS(MIN)}$: Minimum AC input voltage rms value (V)

The maximum on-time, t_{MAX_PFC}, is fixed at 18.3 µs inside the IC. Be sure to set the inductance value to be $t_{ON(MAX)\_OP} < t_{MAX\_PFC}$.

10.1.2. Auxiliary Winding, D_P

Figure 10-1 shows the polarity of boost winding P_P and auxiliary winding D_P. Given the number of windings of each winding as N_P and N_D, the turn ratio N_D/N_P is set satisfying following conditions.

The condition of N_D/N_P making ZCD pin voltage above $V_{ZCD(H)}$ = 1.40 V after power MOSFET turns off is expressed as follows:

$$\frac{N_D}{N_P} > \frac{V_{ZCD(H)}}{V_{OUT(PFC)} - \sqrt{2} \times V_{ACRMS(MAX)}} \quad (15)$$

where
N_P: The number of turns of boost winding P_P (turns)
N_D: The number of turns of auxiliary winding D_P (turns)
V_{OUT}: Output voltage (V)
$V_{ACRMS(MAX)}$: Maximum AC input voltage rms value (turns)

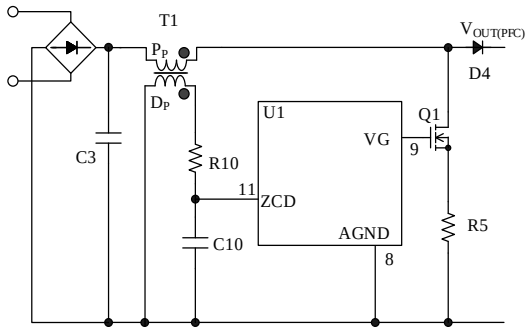


Figure 10-1. ZCD Peripheral Circuit

10.2. External Components

10.2.1. Resonant Transformer

The resonant power supply uses the leakage inductance of a transformer. Therefore, to reduce influences from eddy current and skin effect, use a bundle of fine litz wires as the wire of the transformer.

10.2.2. Inductor in PFC Stage

Apply proper design margin to temperature rise or magnetic saturation due to copper loss and iron loss.

10.2.3. Power MOSFET

Use a power MOSFET with a breakdown voltage, V_{DSS}, providing enough margin to the PFC output voltage, $V_{OUT(PFC)}$. Choose a proper size of heatsink that takes switching and on-resistance losses due to power MOSFETs into account.

10.2.4. PFC Boost Diode (D4)

Choose a boost diode with a peak reverse voltage, V_{RSM}, allowing enough margin to the PFC output voltage, $V_{OUT(PFC)}$. A fast recovery diode with a short reverse recovery time, t_{rr}, is recommended to reduce noise and loss due to switching. Choose a proper size of heatsink that takes losses caused by forward voltage, V_F, and recovery current into considerations.

10.2.5. Output Capacitor (C4, C51)

Apply proper design margin to ripple current, ripple voltage, and temperature rise. A low-ESR capacitor is recommended to reduce ripple voltage, in terms of designing switch-mode power supplies.

10.2.6. Current-resonant Capacitor (C19)

Because large resonant current flows through C19, it should be a capacitor that supports high-current applications with small losses such as a polypropylene film capacitor. High-frequency current flows through C19; therefore, capacitor-specific frequency characteristics must also be taken into account.

10.3. PCB Pattern Layout

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. High-frequency and high-voltage current loops (see Figure 10-2) should be as small and wide as possible in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

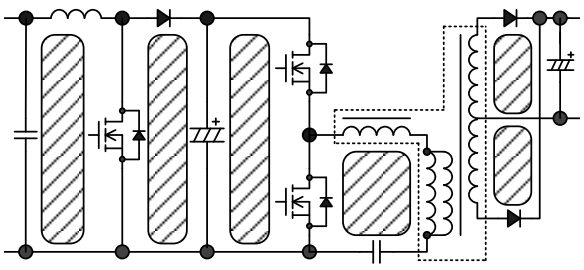


Figure 10-2. High-frequency Current Loop

Figure 10-3 is a peripheral circuit example of the IC. The following considerations should be taken into

account in designing pattern layouts for your application.

1) Main Circuit Trace Layout

The AGND and LGND pins must be connected on a PCB with a minimal length of traces.

Traces of the PFC and LLC circuits, where switching currents pass through, should be as wide and looped small as possible.

The LGND pin is the main circuit ground of the LLC circuit. The LGND pin should be separated from control ground traces, and connected to the root of the output capacitor, C4, at a single point. In addition, for the power MOSFET drive circuit of the LLC circuit, the root of the LGND pin and the ground side of the VCC pin capacitor should be separately connected.

2) Logic Ground Trace Layout

If a large current flows through a logic ground, electric potential across the logic ground may vary and thus cause the IC to malfunction. Ground traces should be as wide and short as possible.

Logic ground traces should be designed as close as possible to the AGND pin, at a single-point ground (or star ground) that is separated from the main circuit. Do not connect the LGND pin to these traces. Traces of the ground (i.e., the capacitors of the AGND pin and the ground of VCC pin capacitor) should be separately connected at a single-point ground whose connection is configured to the root of the output capacitor C4 in the PFC stage.

3) Peripheral Connections to VCC Pin

Traces connected to the VCC pin should be looped small as possible because the pin supplies power to the IC. If the IC and the electrolytic capacitor C7 are distant from each other, connect the film capacitor C7 (about 0.1 µF to 1.0 µF) between the VCC and AGND pins with a minimal length of traces.

4) Peripheral Connections to VB Pin

The components of the bootstrap circuit connected between the VCC and VB pins (D7, R21) should be placed as close as possible to the IC. The capacitor, C21, connected between the VB and VS pins should also be placed with a minimal length of traces.

5) Components for Logic Control System

These components should be placed close to the IC, and be connected to the corresponding pin of the IC with a minimal length of traces.

6) Secondary-side Rectifier Smoothing Circuit

This is the secondary-side main circuit in which switching current flows, should be wide and looped small as possible.

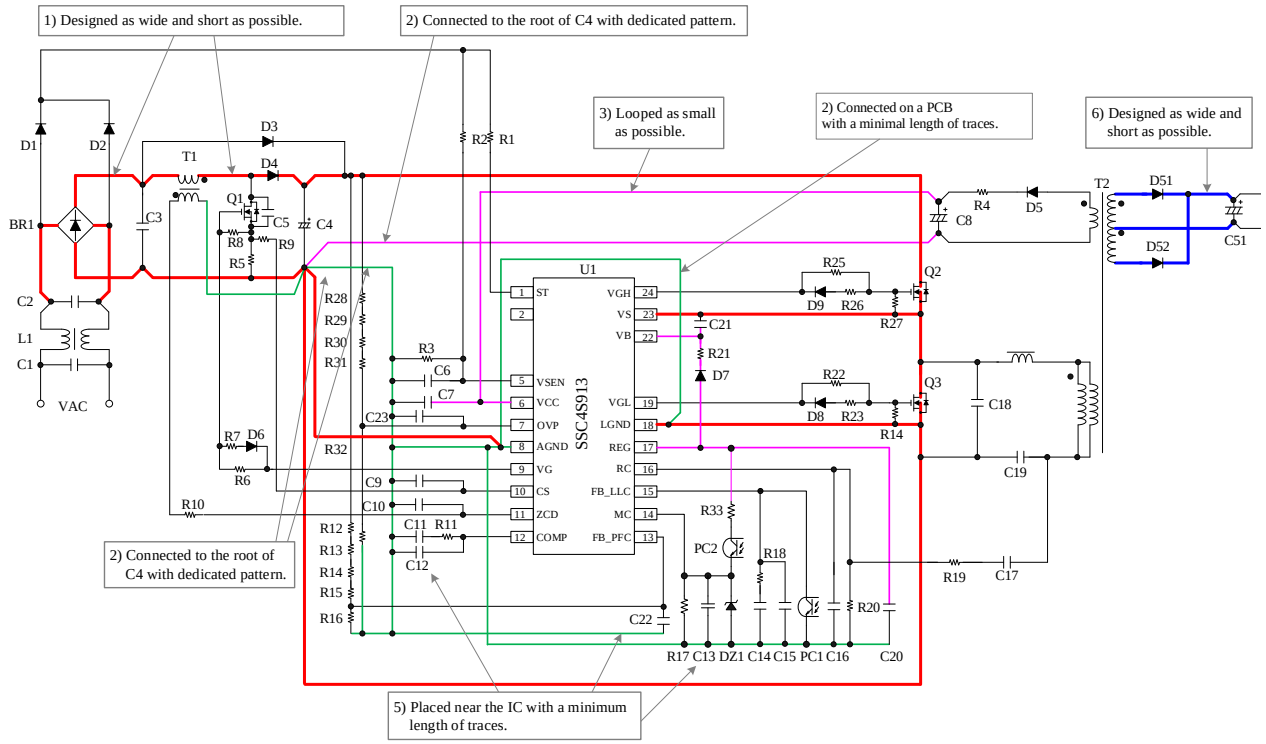


Figure 10-3. Example Connections to IC and Its Peripheral Circuits

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