SX1A5201E1S

Data Sheet

Description

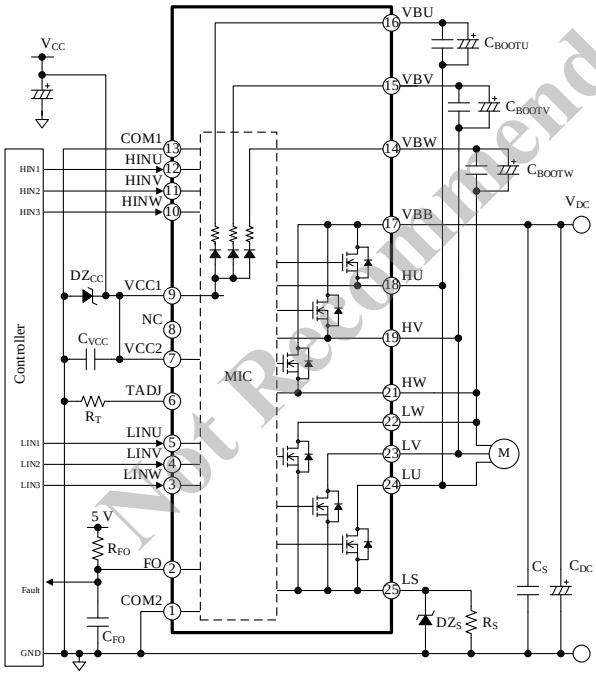
The SX1A5201E1S is a high voltage 3-phase motor driver IC in which transistors, a pre-driver IC (MIC), and bootstrap circuits (diodes and resistors) are highly integrated.

The product can optimally control the inverter systems of small- to medium-capacity motors that require universal input standards.

Features

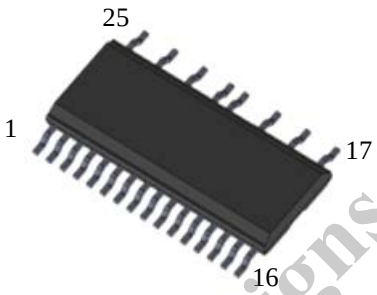
- Built-in Bootstrap Diodes
- CMOS-compatible Input (3.3 V or 5 V)
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Isolation Voltage: 1500 V (for 1 min)
- Fault Signal Output at Protection Activation (FO Pin)
- Protections Include:
  Overcurrent Protection (OCP): Auto-restart
  Undervoltage Lockout for Power Supply
  High-side (UVLO_VB): Auto-restart
  Low-side (UVLO_VCC): Auto-restart
  Thermal Shutdown (TSD): Auto-restart

Typical Application



Package

SOP25



Not to scale

Specifications

- Breakdown Voltage: 500 V
- Output Current: 1.5 A
- Power MOSFET On-resistance: 2 Ω

Applications

For motor drives such as:

- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBB–LS	400	V	
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBB–LS	450	V	
Power MOSFET Breakdown Voltage	V_{DSS}	V_{CC} = 15 V, I_D = 1 µA, V_{IN} = 0 V	500	V	
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	20	V	
	V_{BS}	VBU–HU, VBV–HV, VBW–HW	20		
Output Current(1)	I_O	T_C = 25 °C, T_J < 150 °C	1.5	A	
Output Current (Pulse)	I_{OP}	T_C = 25 °C, V_{CC} = 15 V, $P_W \leq$ 1 ms, single pulse	2.25	A	
Input Voltage	V_{IN}	HINU–COM, HINV–COM, HINW–COM; LINU–COM, LINV–COM, LINW–COM	− 0.5 to 7	V	
FO Pin Voltage	V_{FO}	FO–COM	−0.5 to 7	V	
LS Pin Voltage	V_{LS}	LS–COM	−10 to 7	V	
Operating Case Temperature(2)	$T_{C(OP)}$		−30 to 100	°C	
Junction Temperature(3)	T_J		150	°C	
Storage Temperature	T_{stg}		−40 to 150	°C	
Isolation Voltage(4)	$V_{ISO(RMS)}$	Between surface of the case and each pin; AC, 60 Hz, 1 min	1500	V	

(1) Should be derated depending on an actual case temperature. See Section 13.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the controller IC (MIC), transistors, and fast recovery diodes.
(4) Refers to voltage conditions to be applied between the case and all pins. All pins have to be shorted.

2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBB–COM	—	300	400	V	
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	13.5	15.0	16.5	V	
	V_{BS}	VBU–HU, VBV–HV, VBW–HW	13.5	—	16.5	V	
Input Voltage (HINx, LINx, FO)	V_{IN}		0	—	5.5	V	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	—	—	µs	
	$t_{IN(MIN)OFF}$		0.5	—	—	µs	
Dead Time of Input Signal	t_{DEAD}		1.5	—	—	µs	
FO Pin Pull-up Resistor	R_{FO}		3.3	—	10	kΩ	
FO Pin Pull-up Voltage	V_{FO}		3.0	—	5.5	V	
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	µF	
Bootstrap Capacitor	C_{BOOT}		10	—	220	µF	
Shunt Resistor	R_S	$I_P \leq 2.25$ A	220	—	—	mΩ	
PWM Carrier Frequency	f_c		—	—	20	kHz	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCC1–COM, VCC2–COM	9.5	10.5	11.5	V	
	$V_{BS(ON)}$	VBU–HU, VBV–HV, VBW–HW	9.5	10.5	11.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC1–COM, VCC2–COM	9.0	10.0	11.0	V	
	$V_{BS(OFF)}$	VBU–HU, VBV–HV, VBW–HW	9.0	10.0	11.0	V	
Logic Supply Current	I_{CC}	VCC1 = VCC2, VCC pin current in 3-phase operation	—	3.3	—	mA	
	I_{BS}	VBU–HU or VBV–HV or VBW–HW; HINx = 5 V; VBx pin current in 1-phase operation	—	140	—	µA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx, FO)	V_{IH}		—	2.0	2.5	V	
Low Level Input Threshold Voltage (HINx, LINx, FO)	V_{IL}		1.0	1.5	—	V	
High Level Input Current (HINx, LINx)	I_{IH}	V_{IN} = 5 V	—	230	500	µA	
Low Level Input Current (HINx, LINx)	I_{IL}	V_{IN} = 0 V	—	—	2	µA	
Fault Signal Output							
FO Pin Voltage at Fault Signal Output	V_{FOL}	V_{FO} = 5 V, R_{FO} = 10 kΩ	0	—	0.5	V	
FO Pin Voltage in Normal Operation	V_{FOH}	V_{FO} = 5 V, R_{FO} = 10 kΩ	4.8	—	—	V	
Protection							
OCP Threshold Voltage	V_{TRIP}		0.475	0.500	0.525	V	
OCP Hold Time	t_P		20	31	—	µs	
OCP Blanking Time	$t_{BK(OCP)}$		—	2	—	µs	
TSD Operating Temperature	T_{DH}	Leave the TADJ pin open.	105	120	135	°C	
TSD Releasing Temperature	T_{DL}	Leave the TADJ pin open.	—	90	—	°C	

3.2 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 500 V	—	—	10	μA	
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 10 mA	—	3.0	—	V	

3.3 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance*	R_{J-C}	All power MOSFETs operating	—	—	4.0	°C/W	
Junction-to-Ambient Thermal Resistance	R_{J-A}	All power MOSFETs operating	—	—	31.25	°C/W	

* Refers to a case temperature at the measurement point described in Figure3-1, below.

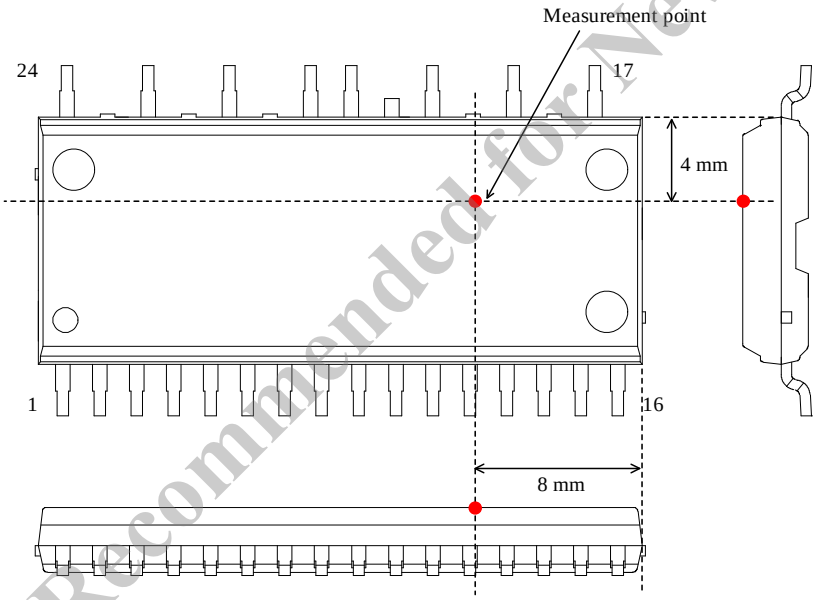


Figure3-1. Case Temperature Measurement Point

3.4 Transistor Characteristics

Figure3-2 provides the definitions of switching characteristics described in this and the following sections.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	µA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 0.75 A, V_{IN} = 5 V	—	1.7	2.0	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 0.75A, V_{IN} = 0 V	—	0.85	1.35	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 1.5 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	670	—	ns
Rise Time	t_r		—	40	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	690	—	ns
Fall Time	t_f		—	30	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 1.5 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	740	—	ns
Rise Time	t_r		—	40	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	760	—	ns
Fall Time	t_f		—	45	—	ns

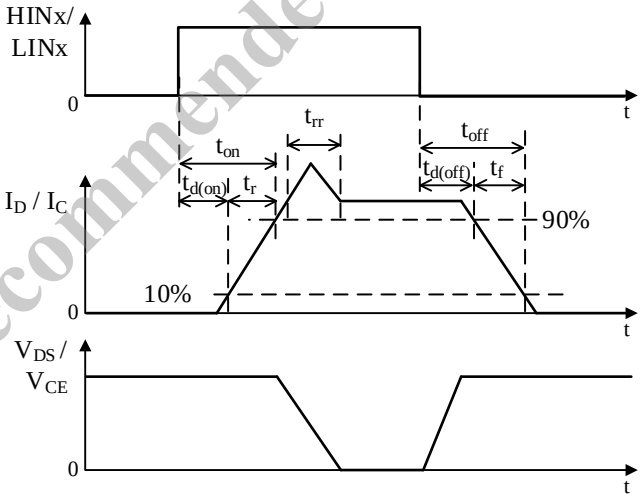


Figure3-2. Switching Characteristics Definitions

4. Truth Table

Table 4-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx signals in each phase are high at the same time, both the high- and low-side transistors become on (simultaneous on-state). Therefore, HINx and LINx signals, the input signals for the HINx and LINx pins, require dead time setting so that such a simultaneous on-state event can be avoided.

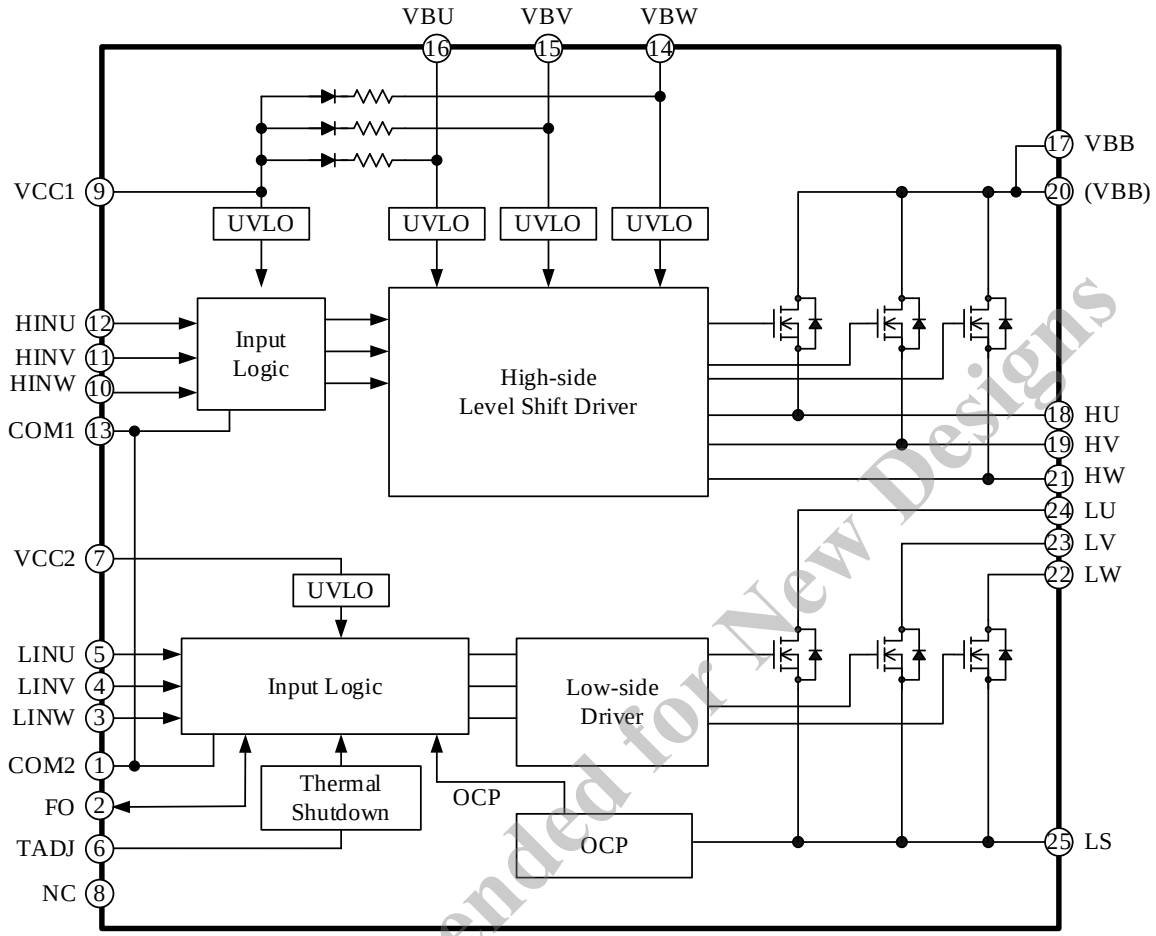
After the IC recovers from a UVLO_VCC condition, the high- and low-side transistors resume switching, according to the input logic levels of the HINx and LINx signals (level-triggered).

After the IC recovers from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

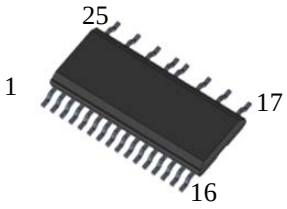
Table 4-1. Truth Table for Operation Modes

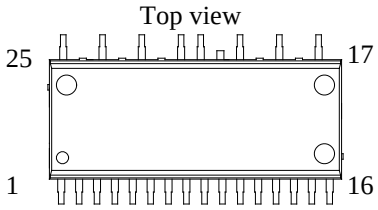
Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON
External Shutdown Signal Input, FO = Low Level	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Undervoltage Lockout for High-side Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Thermal Shutdown (TSD)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF

5. Block Diagram



6. Pin Configuration Definitions

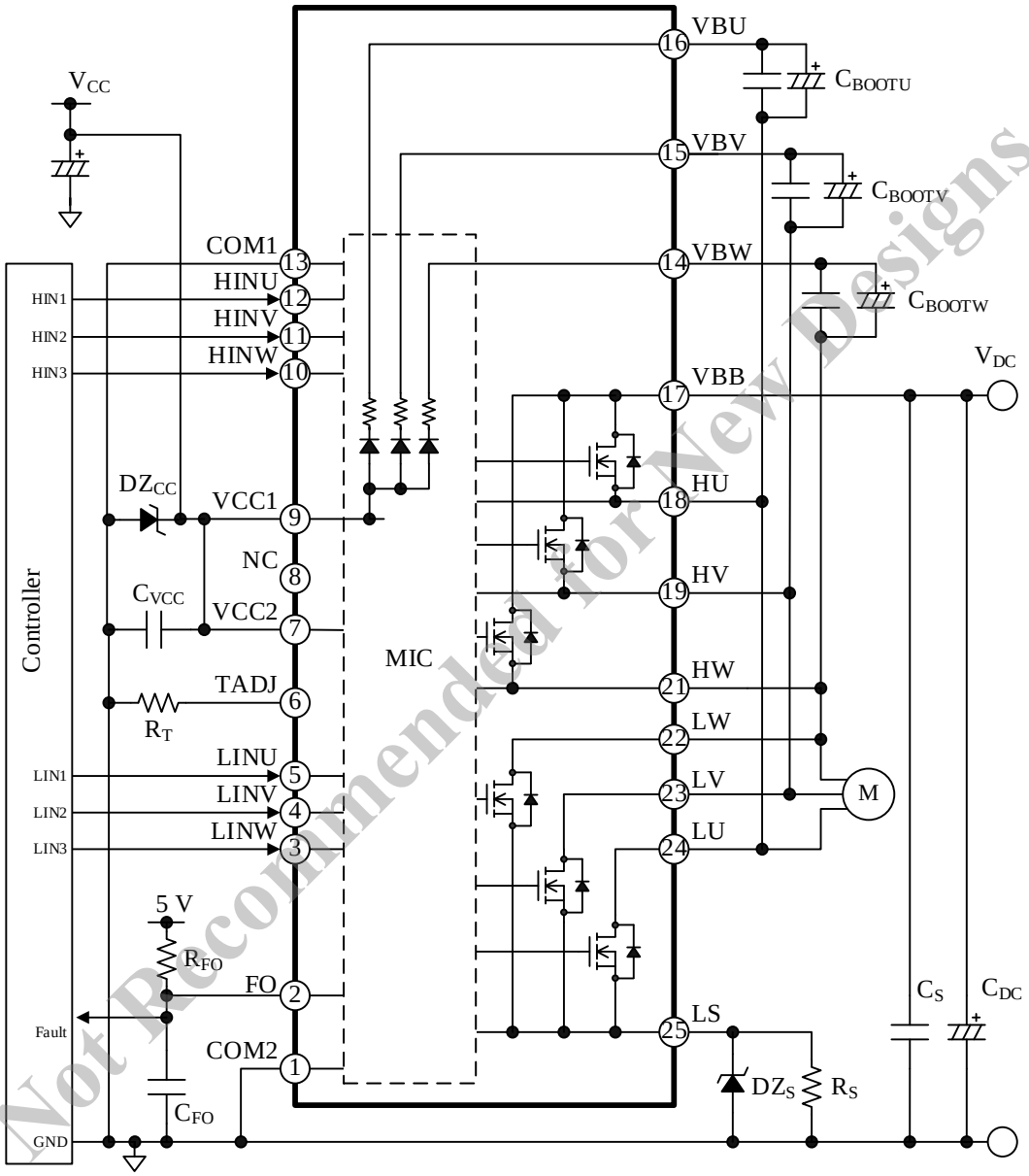




Pin Number	Pin Name	Description
1	COM2	Low-side logic ground
2	FO	Fault signal output and shutdown signal input
3	LINW	Logic input for W-phase low-side gate driver
4	LINV	Logic input for V-phase low-side gate driver
5	LINU	Logic input for U-phase low-side gate driver
6	TADJ	Resister connection for TSD threshold temperature control
7	VCC2	Low-side logic supply voltage input
8	NC	(No connection)
9	VCC1	High-side logic supply voltage input
10	HINW	Logic input for W-phase high-side gate driver
11	HINV	Logic input for V-phase high-side gate driver
12	HINU	Logic input for U-phase high-side gate driver
13	COM1	High-side logic ground
14	VBW	W-phase high-side floating supply voltage input
15	VBV	V-phase high-side floating supply voltage input
16	VBU	U-phase high-side floating supply voltage input
17	VBB	Positive DC bus supply voltage
18	HU	U-phase output
19	HV	V-phase output
20	VBB	(Pin trimmed) positive DC bus supply voltage
21	HW	W-phase output
22	LW	W-phase output
23	LV	V-phase output
24	LU	U-phase output
25	LS	Power MOSFET sources of the U-, V-, and W-phases; input for overcurrent protection

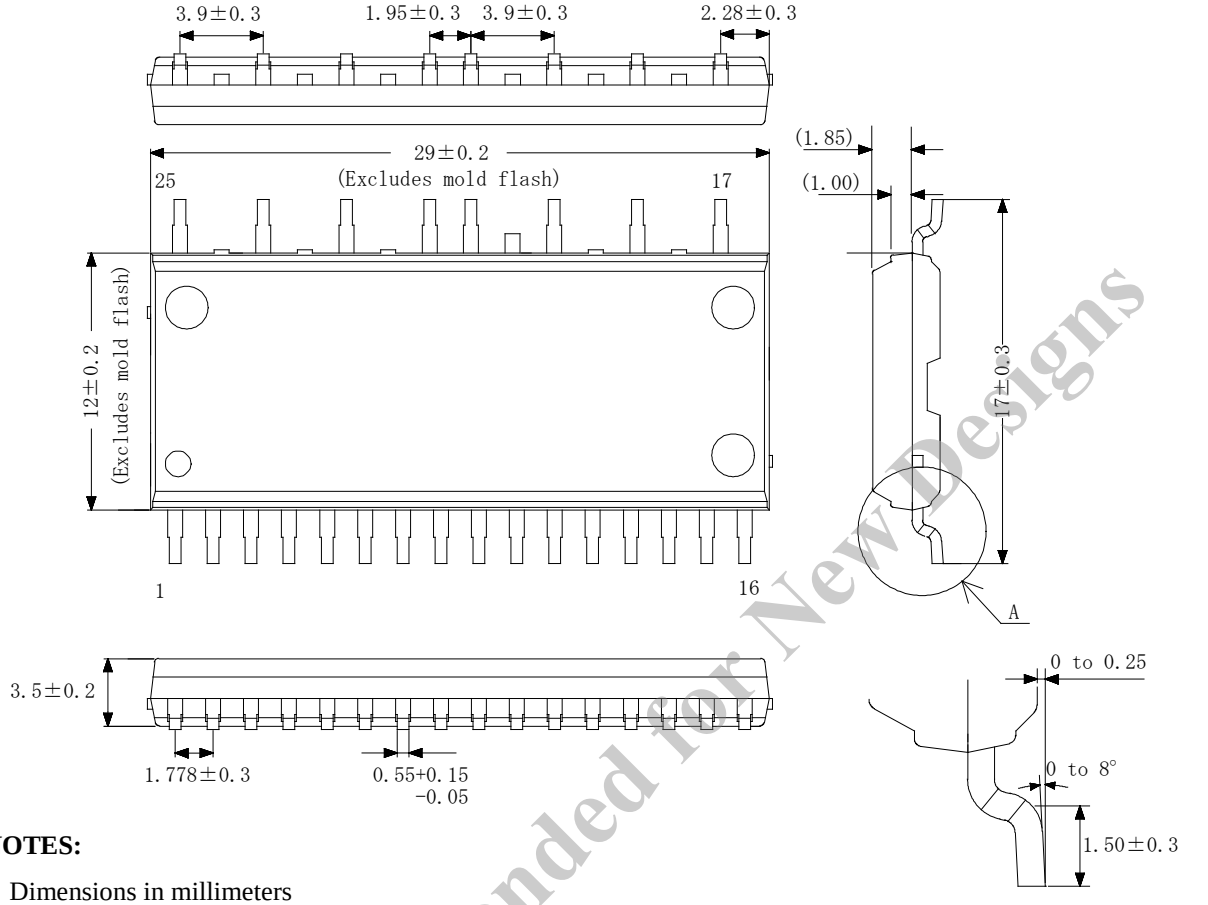
7. Typical Application

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.



8. Physical Dimensions

● **SOP25 Package**

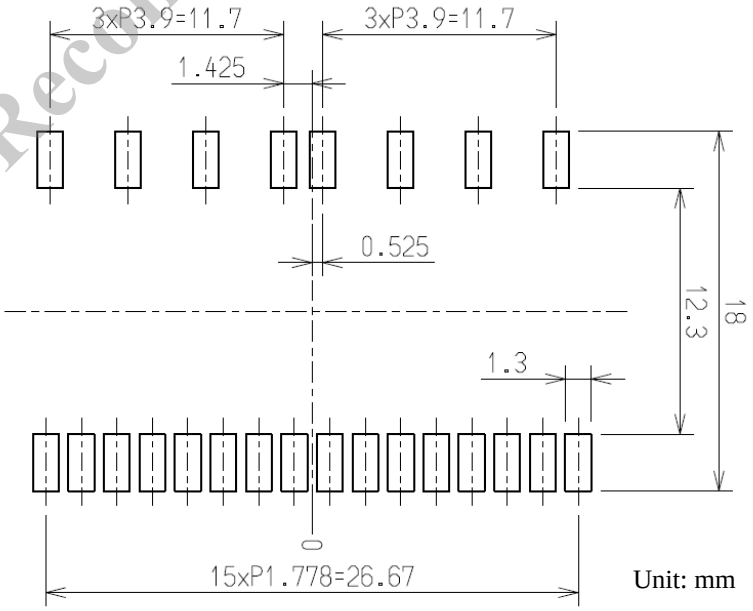


Enlarged view of A (S=10/1)

NOTES:

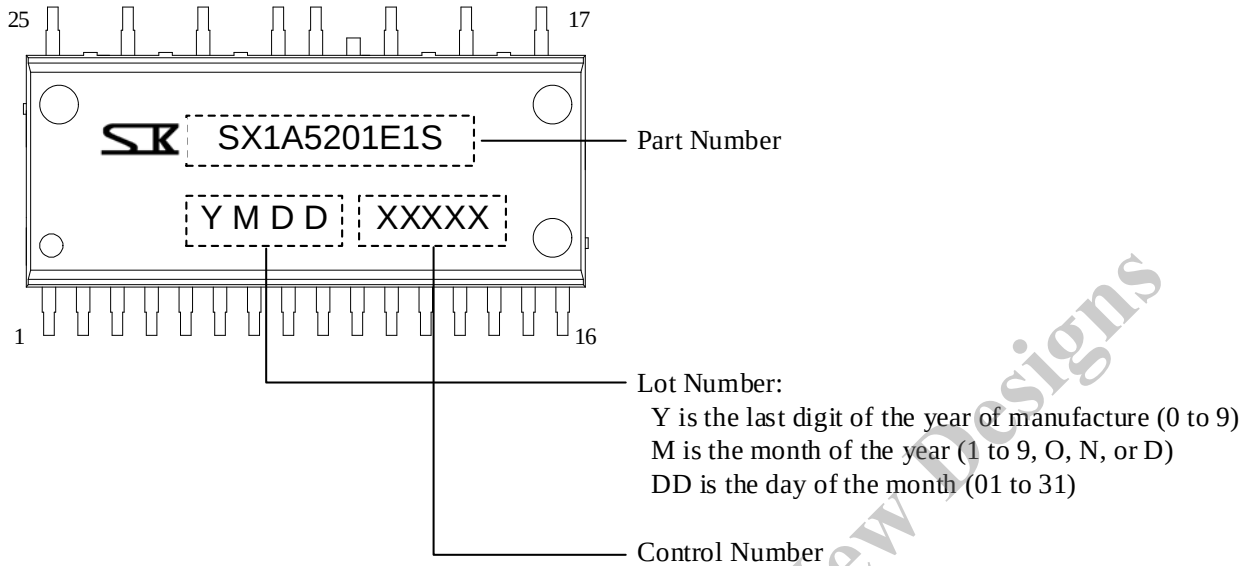
- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)

● **Land Pattern Example**



Unit: mm

9. Marking Diagram



10. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name or an electronic symbol name with the arbitrary letter "x" as a suffix representing the certain letters (U, V, W, 1, and 2). Thus, "the VCCx pin" is used when referring to either or both of the VCC1 and VCC pins; similarly, "the HINx pin" is used when referring to any or all of the HINU, HINV, and HINW pins. Also, when different pin names are mentioned as a pair (e.g., "the Hx and Lx pins"), they are meant to be the pins in the same phase.
- Unless specifically noted, COM1 = COM2 = COM.

10.1 Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 11.5$ V).

It is required to fully charge bootstrap capacitors, C_{BOOTx}, at startup (see Section 10.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

10.2 Pin Descriptions

10.2.1 HU, HV, and HW; LU, LV, and LW

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. In each phase, the Hx and Lx pins must be connected on a PCB.

The Hx pin is the ground for the VBx pin. The Hx pin is connected to the negative node of the corresponding bootstrap capacitor, C_{BOOTx}.

Since high voltages are applied to the Hx and Lx pins, it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

10.2.2 VBU, VBV, and VBW

These are the inputs of the high-side floating power supplies for the individual phases. A bootstrap capacitor, C_{BOOTx}, should be connected in each trace between the VBx and the corresponding output (Hx and Lx) pins .

Voltages across the VBx and Hx pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

As Figure 10-1 shows, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are internally placed in series between the VBx and VCC1 pins.

For proper startup, turn on the low-side transistor first, then fully charge the bootstrap capacitor, C_{BOOTx}. Table 10-1 shows a relation between the charging time and capacitance of C_{BOOTx} at startup.

For the capacitance of the bootstrap capacitors, C_{BOOTx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{BOOTx}.

Even while the high-side transistor is off, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 10.3.3.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

$$C_{BOOTx}(\mu F) > 800 \times t_{L(OFF)}\ (s) \quad (1)$$

$$10\ \mu F \leq C_{BOOTx} \leq 220\ \mu F \quad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{BOOTx}), measured in seconds.

Table 10-1. C_{BOOTx} Capacitance vs. Charging Time at Startup

C_{BOOTx} Capacitance (μF)	Reference Charging Time (s)
10	0.5
22	0.5
47	0.5
100	1.0
220	1.0

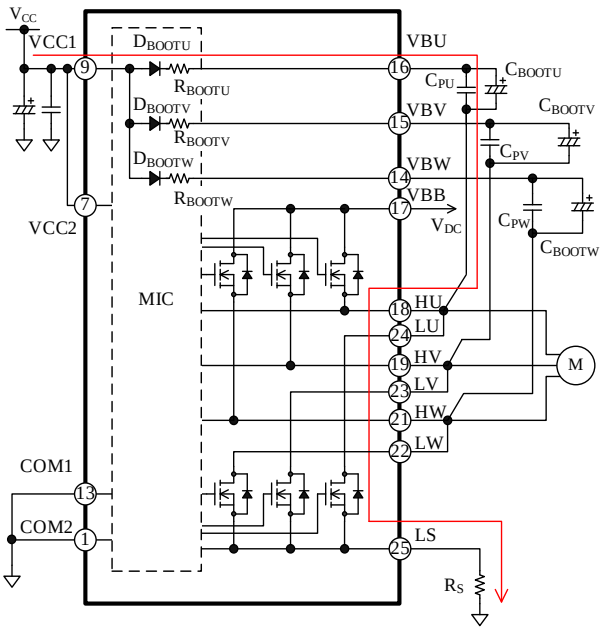


Figure 10-1. Bootstrap Circuit

Figure 10-2 shows an internal level-shifting circuit. A high-side output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a "Set" signal is generated. When the HINx input signal transits from high to low (falling edge), a "Reset" signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

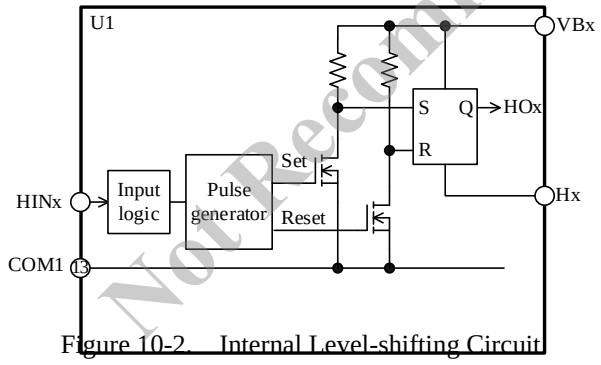


Figure 10-2. Internal Level-shifting Circuit

Figure 10-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and Hx pins (hereafter "VBx–Hx") occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of an HOx signal stays logic high (or "H") because the SR flip-flop does not respond. With the HOx state being held high (i.e., the high-side transistor is in an on-state), the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition, which may result in critical damage to the IC. To protect the VBx pin against such a noise effect, add a bootstrap capacitor, C_{BOOTx}, in each phase. C_{BOOTx} must be placed near the IC, and be connected between the VBx and Hx pins with a minimal length of traces. To use an electrolytic capacitor, add a 0.01 µF to 0.1 µF bypass capacitor, C_{Px}, in parallel near these pins used for the same phase.

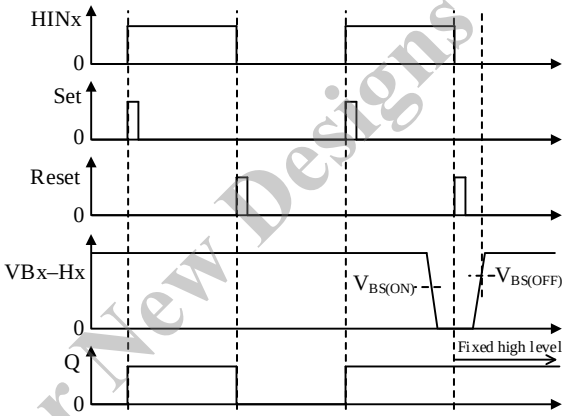


Figure 10-3. Waveforms at VBx-HSx Voltage Drop

10.2.3 VCC1 and VCC2

These are the power supply pins for the built-in control IC. The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{VCC}, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ_{CC}, between the VCCx and COMx pins.

Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

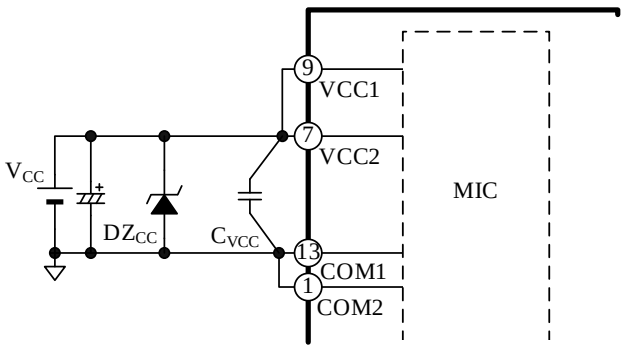


Figure 10-4. VCCx Pin Peripheral Circuit

10.2.4 COM1 and COM2

These are the logic ground pins for the built-in control IC. The COM1 and COM2 pins should be connected externally on a PCB. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 10-5).

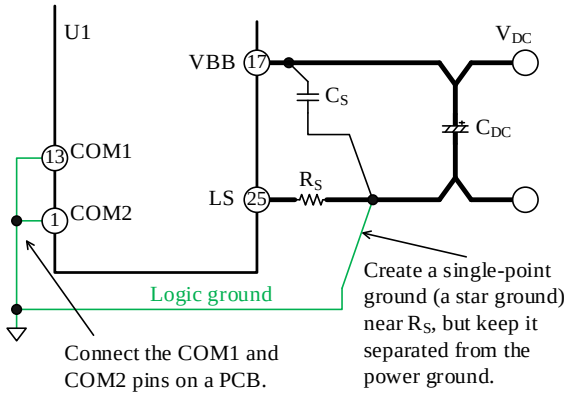


Figure 10-5. Connections to Logic Ground

10.2.5 HINU, HINV, and HINW; LINU, LINV, and LINW

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller.

Figure 10-6 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 20 kΩ pull-down resistor, and its input logic is active high.

Input signals applied across the HINx–COMx and the LINx–COMx pins in each phase should be set within the ranges provided in Table 10-2, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, the outputs from the microcontroller output line should not be high impedance. Also, if the traces from the microcontroller to the HINx or LINx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 10-7).

Here are filter circuit constants for reference:
– R_{IN1x}: 33 Ω to 100 Ω
– R_{IN2x}: 1 kΩ to 10 kΩ
– C_{INx}: 100 pF to 1000 pF

Care should be taken when adding R_{IN1x} and R_{IN2x} to the traces. When they are connected to each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

Table 10-2. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 µs	≥0.5 µs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥1.5 µs	

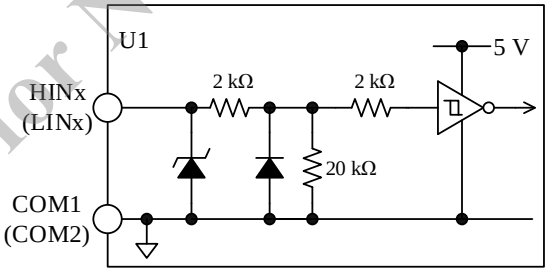


Figure 10-6. Internal Circuit Diagram of HINx or LINx Pin

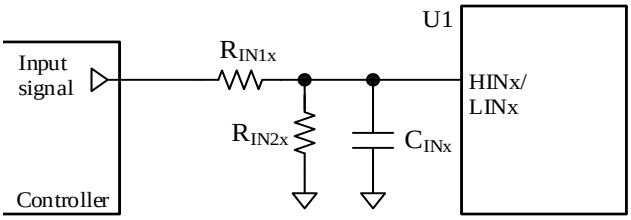


Figure 10-7. Filter Circuit for HINx or LINx Pin

10.2.6 VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the power MOSFET drains of the high-side are connected to this pin. Voltages between the VBB and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

10.2.7 LS

This pin is internally connected to the power MOSFET source in each phase and the overcurrent protection (OCP) circuit. For current detection, the LS pin should be connected externally on a PCB via a shunt resistor, R_S, to the COMx pin.

For more details on the OCP, see Section 10.3.4.

When connecting a shunt resistor, place it as near as possible to the IC with a minimum length of traces to the LS and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LS and COMx pins in order to prevent the IC from malfunctioning.

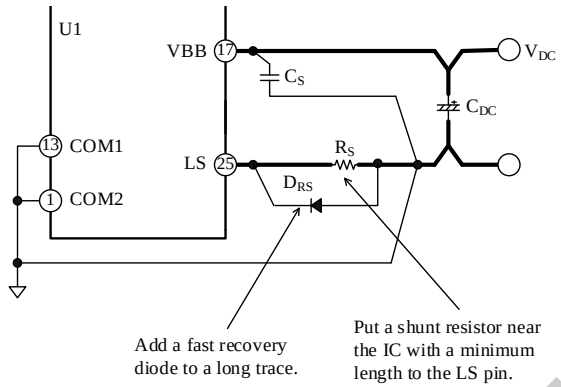


Figure 10-8. Connections to LS Pin

10.2.8 FO

This pin operates as the fault signal output and the low-side shutdown signal input. Immediately after a fault signal is output from this pin, the microcontroller stops sending input signals to the IC. To resume IC operations thereafter, set the IC to be resumed after a lapse of ≥2 seconds. Sections 10.3.1 and 10.3.2 explain the two functions in detail, respectively. Figure 10-9 illustrates an internal circuit diagram of the FO pin and its peripheral circuit.

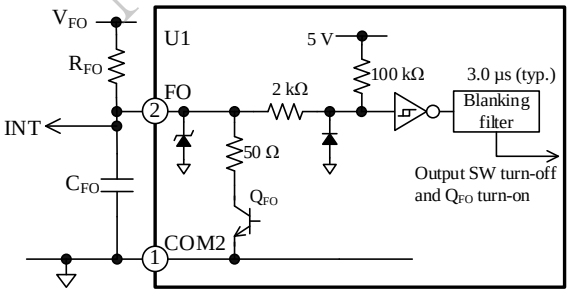


Figure 10-9. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

Because of its open-collector nature, the FO pin should be tied by a pull-up resistor, R_{FO}, to the external power supply. The external power supply voltage (i.e., the FO Pin Pull-up Voltage, V_{FO}) should range from 3.0 V to 5.5 V. When R_{FO} has a too small resistance, the FO pin voltage at fault signal output becomes high due to the saturation voltage drop of a built-in transistor, Q_{FO}. Therefore, it is recommended to use a 3.3 kΩ to 10 kΩ pull-up resistor. To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FO and COMx pins.

To avoid the repetition of OCP activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P, which occurs after the internal MOSFET (Q_{FO}) turn-on. t_P is 20 µs where minimum values of thermal characteristics are taken into account. (For more details, see Section 10.3.4.) Our recommendation is to use a 0.001 µF to 0.01 µF filter capacitor.

10.3 Protection Functions

This section describes the various protection circuits provided in the SX1A5201E1S. The protection circuits include the undervoltage lockout for power supplies (UVLO), the overcurrent protection (OCP), and the thermal shutdown (TSD). In case one or more of these protection circuits are activated, the FO pin outputs a fault signal; as a result, the external microcontroller can stop the operations of the three phases by receiving the fault signal. The external microcontroller can also shut down IC operations by inputting a fault signal to the FO pin.

In the following functional descriptions, "HOx" denotes a gate input signal on the high-side transistor, whereas "LOx" denotes a gate input signal on the low-side transistor.

10.3.1 Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor, Q_{FO}, turns on, then the FO pin becomes logic low (≤0.5 V).

1) Low-side undervoltage lockout (UVLO_VCC)
2) Overcurrent protection (OCP)
3) Thermal shutdown (TSD)

While the FO pin is in the low state, all the low-side transistors turn off. In normal operation, the FO pin outputs a high signal of 5 V. The fault signal output time of the FO pin at OCP activation is the OCP hold time (t_P) of 31 µs (typ.), fixed by a built-in feature of the IC itself (see Section 10.3.4). The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HINx and LINx pins to logic low within the predetermined OCP hold time, t_P.

10.3.2 Shutdown Signal Input

The FO pin also acts as the input pin of shutdown signals. When the FO pin becomes logic low, all the low-side transistors turn off. The voltages and pulse widths of shutdown signals should be set as listed in Table 10-3.

Table 10-3. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	—	≥10 µs

10.3.3 Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SX1A5201E1S has the undervoltage lockout (UVLO) circuits for both of the high- and low-side power supplies in the monolithic IC (MIC).

10.3.3.1. Undervoltage Lockout for High-side Power Supply (UVLO_VB)

Figure 10-10 shows operational waveforms of the undervoltage lockout for high-side power supply (i.e., UVLO_VB).

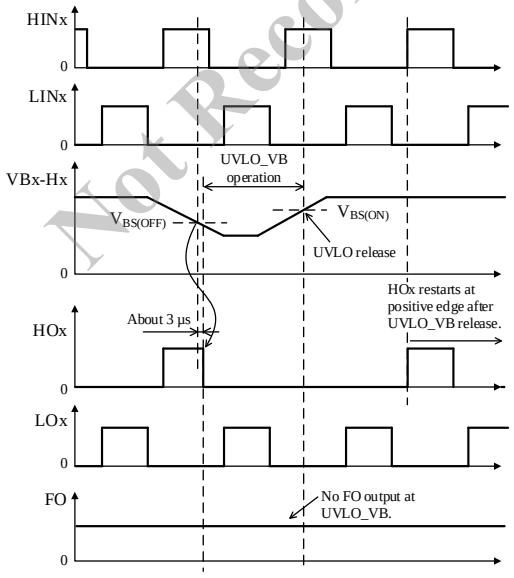


Figure 10-10. UVLO_VB Operational Waveforms

When the voltage between the VBx and output pins ("VBx–Hx" in Figure 10-10) decreases to the Logic Operation Stop Voltage ($V_{BS(OFF)}$, 10.0 V) or less, the UVLO_VB circuit in the corresponding phase gets activated and sets an HOx signal to logic low. When the voltage between the VBx and Hx pins increases to the Logic Operation Start Voltage ($V_{BS(ON)}$, 10.5 V) or more, the IC releases the UVLO_VB operation. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VB release.

Any fault signals are not output from the FO pin during the UVLO_VB operation. In addition, the VBx pin has an internal UVLO_VB filter of about 3 µs, in order to prevent noise-induced malfunctions.

10.3.3.2. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 10-11 shows operational waveforms of the undervoltage lockout for low-side power supply (i.e., UVLO_VCC).

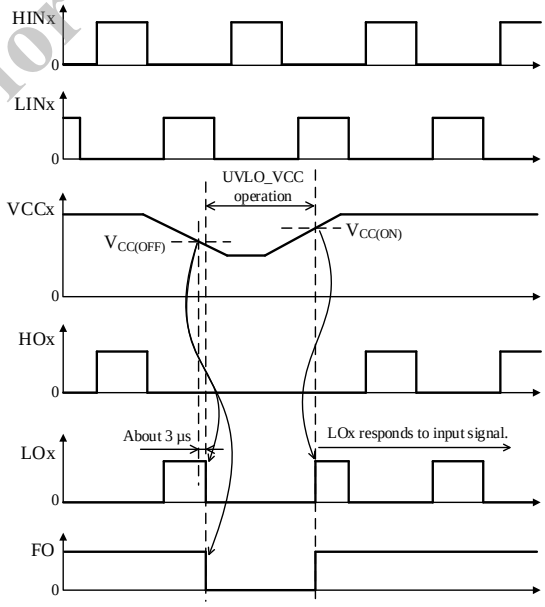


Figure 10-11. UVLO_VCC Operational Waveforms

When the VCCx pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$, 10.0 V) or less, the UVLO_VCC circuit in the corresponding phase gets activated and sets both of HOx and LOx signals to logic low. When the VCCx pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$, 10.5 V) or more, the IC releases the UVLO_VCC operation. The IC then resumes transmitting HOx and LOx signals according to input commands on the HINx and LINx pins, respectively. During the UVLO_VCC operation, the FO

pin becomes logic low and sends fault signals.

In addition, the VCC2 pin has an internal UVLO_VCC filter of about 3 µs, in order to prevent noise-induced malfunctions.

10.3.4 Overcurrent Protection (OCP)

The overcurrent protection (OCP) is a protection against large inrush currents (i.e., high di/dt). Figure 10-12 is an internal circuit diagram describing the LS pin and its peripheral circuit.

The OCP circuit, which is connected to the LS pin, detects overcurrents with voltage across an external shunt resistor, R_S. Because the LS pin is internally pulled down, the LS pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S.

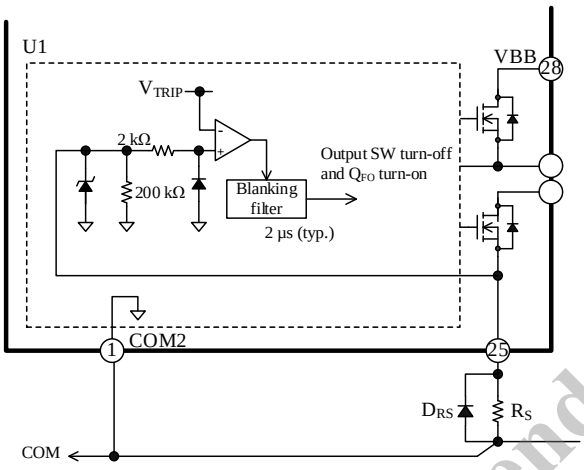


Figure 10-12. Internal Circuit Diagram of LS Pin and Its Peripheral Circuit

Figure 10-13 is a timing chart that represents operation waveforms during OCP operation. When the LS pin voltage increases to the OCP Threshold Voltage (V_{TRIP}, 0.500 V) or more, and remains in this condition for a period of the OCP Blanking Time (t_{BK}, 2 µs) or longer, the OCP circuit is activated. The enabled OCP circuit shuts off the low-side transistors and puts the FO pin into a low state.

Then, output current decreases as a result of the output transistors turn-off. Even if the OCP pin voltage falls below V_{TRIP}, the IC holds the FO pin in the low state for a fixed OCP hold time (t_P) of 31 µs (typ.). Then, the output transistors operate according to input signals.

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. To resume IC operations thereafter, set the IC to be resumed after a lapse of ≥2 seconds.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Set the LS pin input voltage to vary within the rated LS pin voltages, V_{LS} (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

Note that overcurrents are undetectable when one or more of the HU, HV, and HW pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

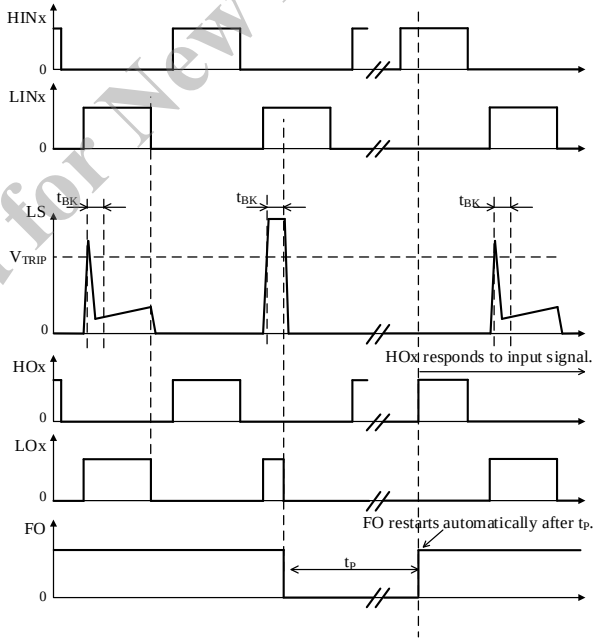


Figure 10-13. OCP Operational Waveforms

10.3.5 Thermal Shutdown (TSD)

The SX1A5201E1S incorporates a thermal shutdown (TSD) circuit. Figure 10-14 shows TSD operational waveforms. In case of overheating (e.g., increased power dissipation due to overload, a rise in ambient temperature at the device, etc.), the IC shuts down the low-side output transistors.

The TSD circuit in the monolithic IC (MIC) monitors temperatures (see Section 5). When the temperature of the monolithic IC (MIC) exceeds the TSD Operating Temperature (T_{DH}), the TSD circuit is activated. When the temperature of the monolithic IC (MIC) decreases to the TSD Releasing Temperature (T_{DL}) or less, the shutdown condition is released. The transistors then

resume operating according to input signals. During the TSD operation, the FO pin becomes logic low and transmits fault signals.

A pull-down resistor, R_T, is externally connected to the TADJ pin (see Figure 10-15) so that its resistance can control the setting values of the TSD Operating Temperature, T_{DH}, and the TSD Releasing Temperature, T_{DL}. Table 10-4 lists the resistance-dependent TSD threshold temperatures of the SX1A5201E1S (i.e., R_T vs. T_{DH}, T_{DL}). Note that junction temperatures of the output transistors themselves are not monitored as TSD-detecting temperature; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

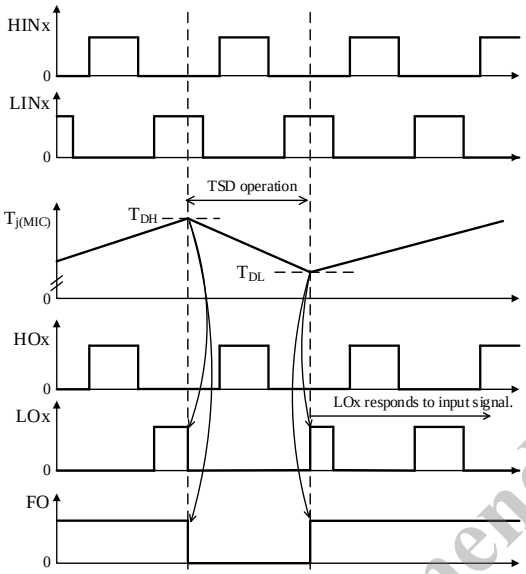


Figure 10-14. TSD Operational Waveforms

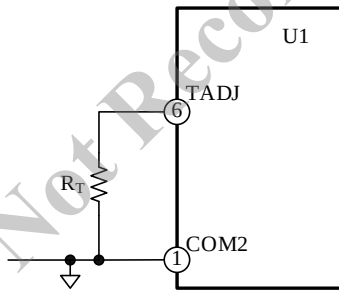


Figure 10-15. TADJ Pin and Its Peripheral Circuit

Table 10-4. R_T vs. T_{DH}, T_{DL}

Pull-down Resistor, R_T	T_{DH} (typ.)	T_{DL} (typ.)
Open	120 °C	90 °C
82 kΩ	135 °C	110 °C
33 kΩ	150 °C	130 °C

11. Design Notes

This section also employs the notation system described in the beginning of the previous section.

11.1 PCB Pattern Layout

Figure 11-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

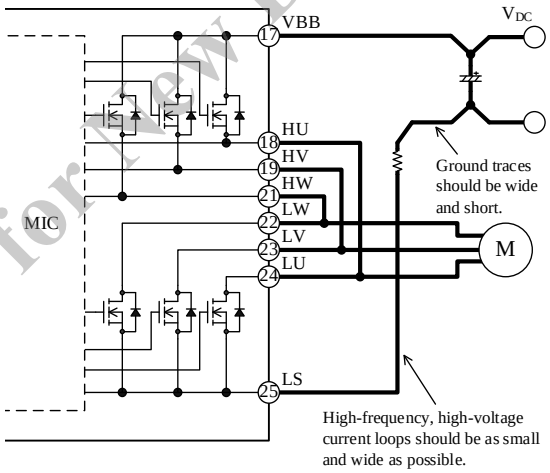


Figure 11-1. High-frequency, High-voltage Current Paths

11.2 Considerations in IC Characteristics Measurement

All of the drains of the high-side transistors are internally connected to the VBB pin. The gates of the high-side transistors are pulled down to the corresponding Hx pin; similarly, the gates of low-side transistors are pulled down to the COM2 pin.

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, make sure that all the pins are appropriately connected and that the gate and source of each transistor have the same potential. Otherwise the switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 11-2 shows the high-side transistor (Q_{UH}) in the U-phase; Figure 11-3 shows the low-side transistor (Q_{UL}) in the U-phase. And all the pins that are not

represented in these figures are open.

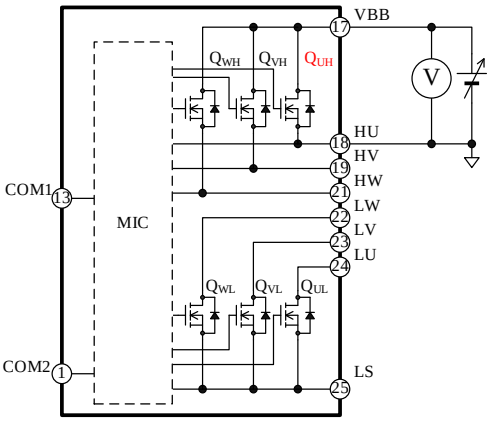


Figure 11-2. Typical Measurement Circuit for High-side Transistor (Q_{UH}) in U-phase

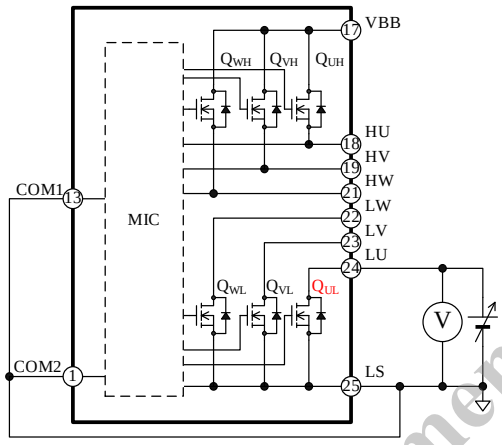


Figure 11-3. Typical Measurement Circuit for Low-side Transistor (Q_{UL}) in U-phase

12. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in switching transistors, and to estimate a junction temperature. Note that the descriptions listed here are applicable to the SX1A5201E1S, which is controlled by a 3-phase sine-wave PWM driving strategy.

Total power loss in a power MOSFET can be obtained by taking the sum of the following losses: steady-state loss, P_{RON}; switching loss, P_{SW}; the steady-state loss of a body diode, P_{SD}. In the calculation procedure we offer, the recovery loss of a body diode, P_{RR}, is considered negligibly small compared with the ratios of other losses. The following subsections contain the mathematical procedures to calculate these losses (P_{RON}, P_{SW}, and P_{SD}) and the junction temperature of all power MOSFETs operating.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0032: SX1A Calculation Tool
  http://www.semicon.sanken-ele.co.jp/calc-tool/sx1a_caltool_jp.html

12.1.1 Power MOSFET Steady-state Loss, P_{RON}

Steady-state loss in a power MOSFET can be computed by using the $R_{DS(ON)}$ vs. I_D curves, listed in Section 13.3.1. As expressed by the curves in Figure 12-1, linear approximations at a range the ID is actually used are obtained by: $R_{DS(ON)} = \alpha \times I_D + \beta$. The values gained by the above calculation are then applied as parameters in Equation (3), below. Hence, the equation to obtain the power MOSFET steady-state loss, P_{RON}, is:

$$P_{RON} = \frac{1}{2\pi}\int_0^{\pi} I_D(\varphi)^2 \times R_{DS(ON)}(\varphi) \times DT \times d\varphi$$

$$= 2\sqrt{2}\alpha\left(\frac{1}{3\pi} + \frac{3}{32}M \times \cos\theta\right) {I_M}^3 + 2\beta\left(\frac{1}{8} + \frac{1}{3\pi}M \times \cos\theta\right) {I_M}^2 . \quad (3)$$

Where:

I_D is the drain current of the power MOSFET (A),
$R_{DS(ON)}$ is the drain-to-source on-resistance of the power MOSFET (Ω),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve, and
β is the intercept of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve.

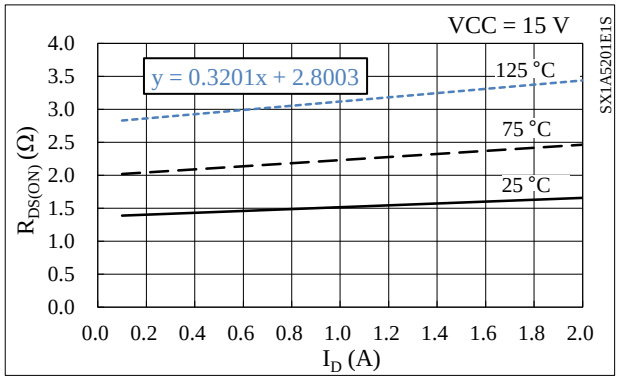


Figure 12-1. Linear Approximate Equation of $R_{DS(ON)}$ vs. I_D Curve

12.1.2 Power MOSFET Switching Loss, P_{SW}

Switching loss in a power MOSFET can be calculated by Equation (4), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (4)$$

Where:
f_C is the PWM carrier frequency (Hz),
V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and
α_E is the slope on the switching loss curve (see Section 13.3.2).

12.1.3 Body Diode Steady-state Loss, P_{SD}

Steady-state loss in the body diode of a power MOSFET can be computed by using the V_{SD} vs. I_{SD} curves, listed in Section 13.3.1. As expressed by the curves in Figure 12-2, linear approximations at a range the ISD is actually used are obtained by: $V_{SD} = \alpha \times I_{SD} + \beta$.

The values gained by the above calculation are then applied as parameters in Equation (5), below. Hence, the equation to obtain the body diode steady-state loss, P_{SD}, is:

$$P_{SD} = \frac{1}{2\pi}\int_0^{\pi} V_{SD}(\varphi) \times I_{SD}(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right) I_M . \quad (5)$$

Where:
V_{SD} is the source-to-drain diode forward voltage of the power MOSFET (V),
I_{SD} is the source-to-drain diode forward current of the power MOSFET (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the V_{SD} vs. I_{SD} curve, and
β is the intercept of the linear approximation in the V_{SD} vs. I_{SD} curve.

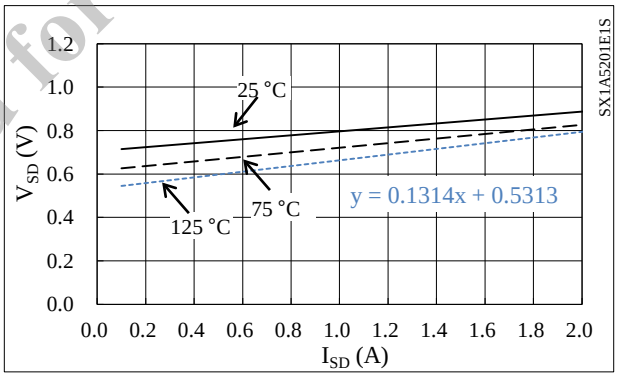


Figure 12-2. Linear Approximate Equation of V_{SD} vs. I_{SD} Curve

12.1.4 Estimating Junction Temperature of Power MOSFET

The junction temperature of all power MOSFETs operating, T_J, can be estimated with Equation (6):

$$T_J = R_{J-C} \times \{(P_{ON} + P_{SW} + P_{SD}) \times 6\} + T_C . \quad (6)$$

Where:
R_{J-C} is the junction-to-case thermal resistance (°C/W) of all the power MOSFETs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure3-1.

13. Performance Curves

13.1 Performance Curves of Control Parts

Figure 13-1 to Figure 13-20 provide performance curves of the control parts integrated in the SCM1200MF series, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 13-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 13-1	Logic Supply Current, I_{CC} vs. T_C (INx = 0 V)
Figure 13-2	Logic Supply Current, I_{CC} vs. VCCx Pin Voltage, V_{CC}
Figure 13-3	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C
Figure 13-4	Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C
Figure 13-5	VBx Pin Voltage, V_B vs. Logic Supply Current, I_{BS} (HINx = 0 V)
Figure 13-6	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 13-7	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 13-8	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 13-9	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 13-10	UVLO_VB Filtering Time vs. T_C
Figure 13-11	UVLO_VCC Filtering Time vs. T_C
Figure 13-12	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 13-13	Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C
Figure 13-14	Input Current at High Level (HINx or LINx), I_{IN} vs. T_C
Figure 13-15	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 13-16	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 13-17	FO Pin Filtering Time vs. T_C
Figure 13-18	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 13-19	OCP Hold Time, t_P vs. T_C
Figure 13-20	OCP Blanking Time, $t_{BK(OCP)}$ vs. T_C

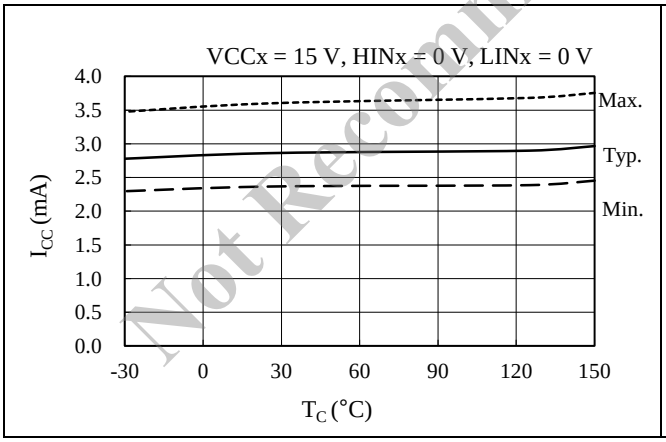


Figure 13-1. Logic Supply Current, I_{CC} vs. T_C (INx = 0 V)

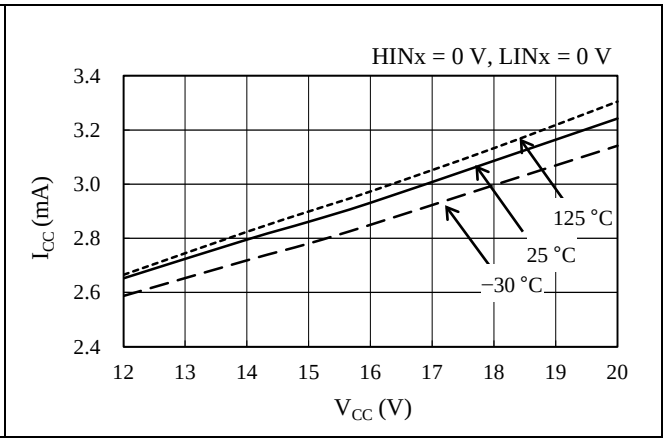


Figure 13-2. Logic Supply Current, I_{CC} vs. VCCx Pin Voltage, V_{CC}

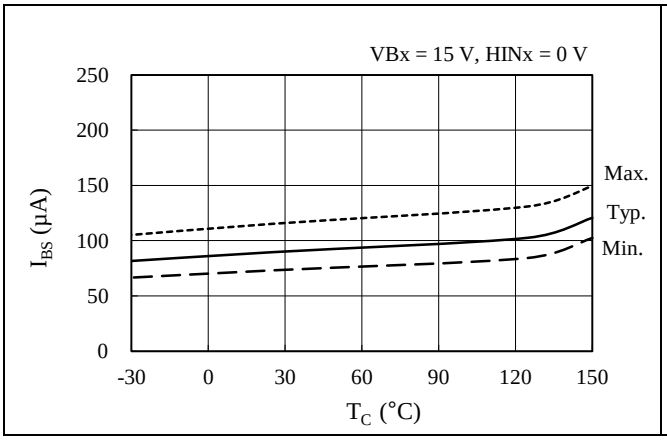


Figure 13-3. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C

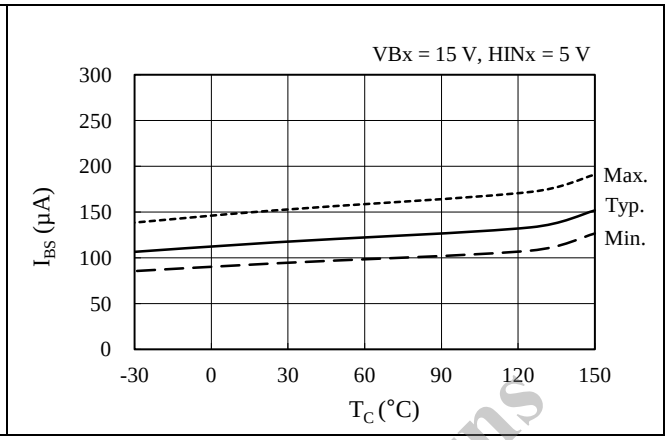


Figure 13-4. Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C

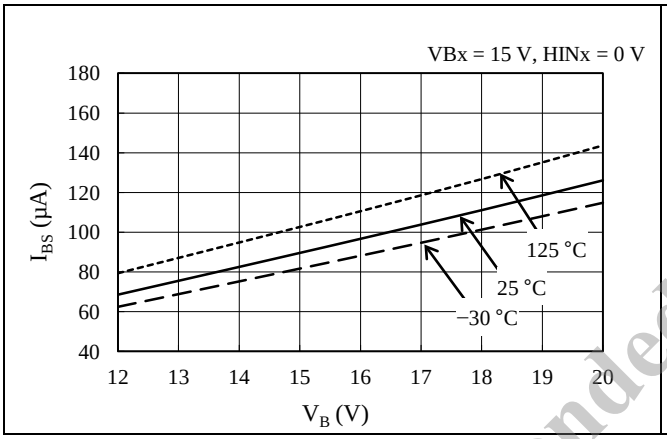


Figure 13-5. VBx Pin Voltage, V_B vs. Logic Supply Current, I_{BS} (HINx = 0 V)

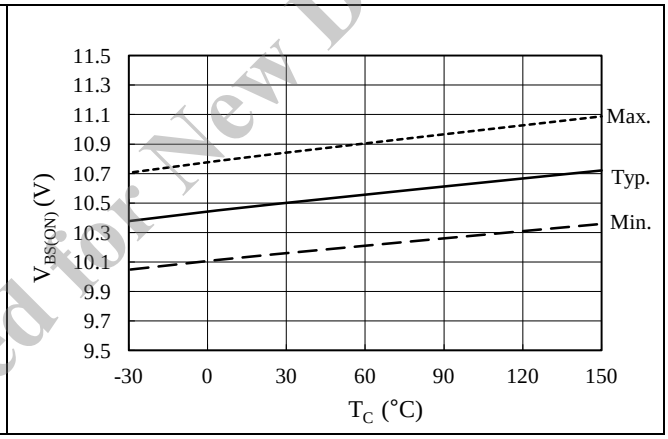


Figure 13-6. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

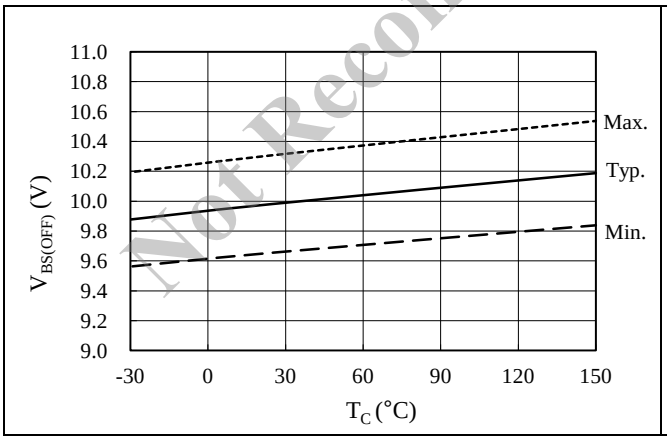


Figure 13-7. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

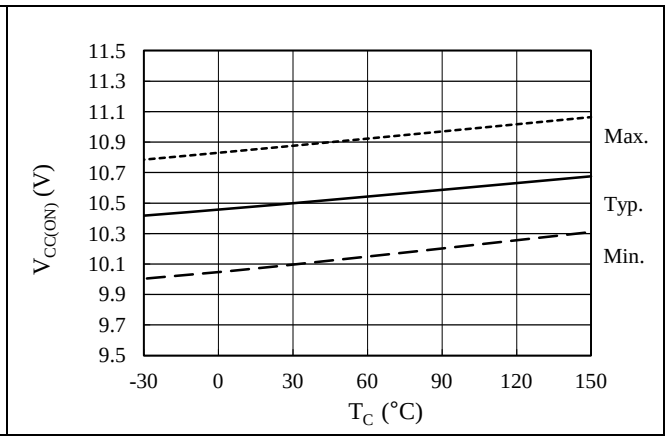


Figure 13-8. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

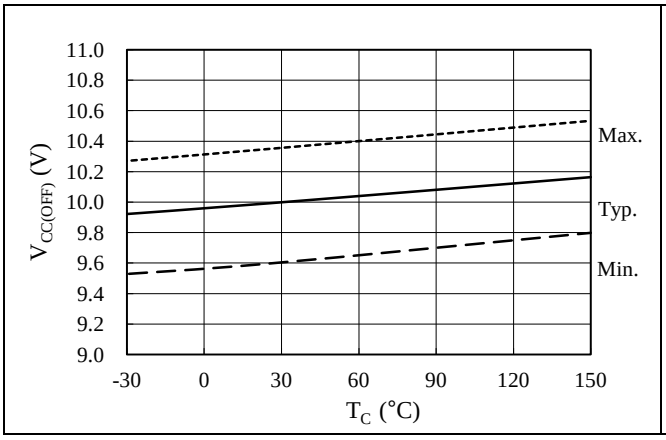


Figure 13-9. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

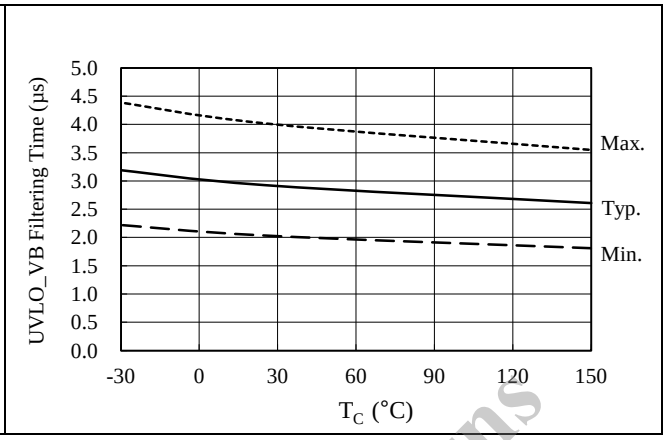


Figure 13-10. UVLO_VB Filtering Time vs. T_C

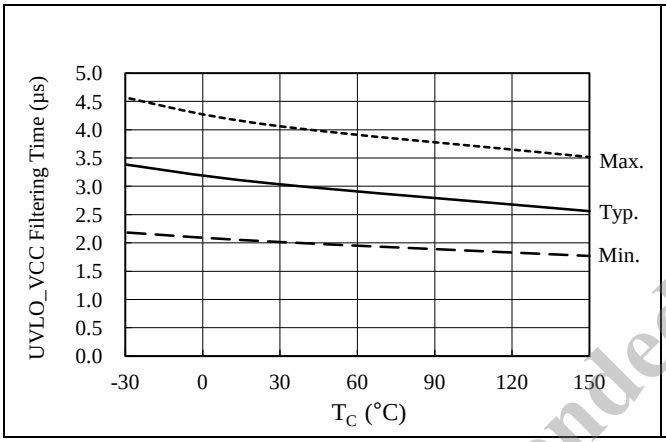


Figure 13-11. UVLO_VCC Filtering Time vs. T_C

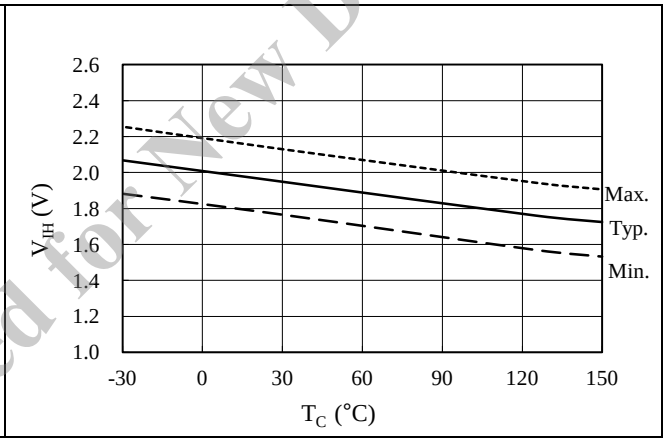


Figure 13-12. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

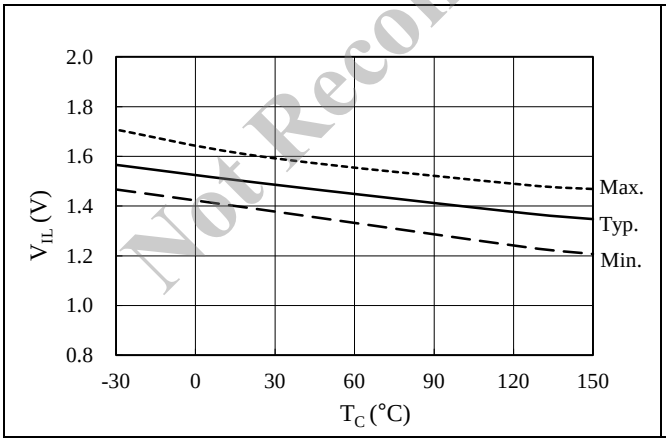


Figure 13-13. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

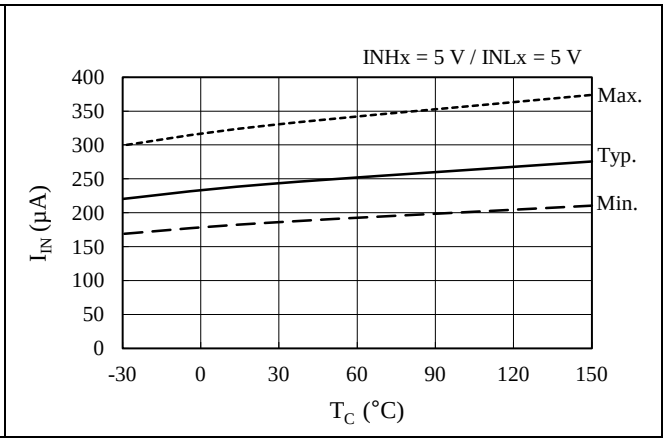


Figure 13-14. Input Current at High Level (HINx or LINx), I_{IN} vs. T_C

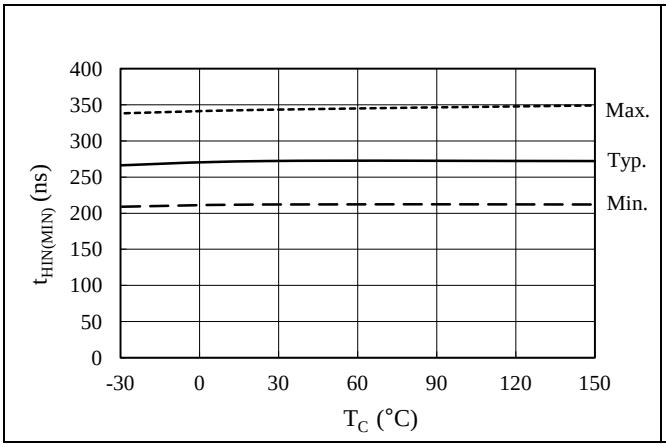


Figure 13-15. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

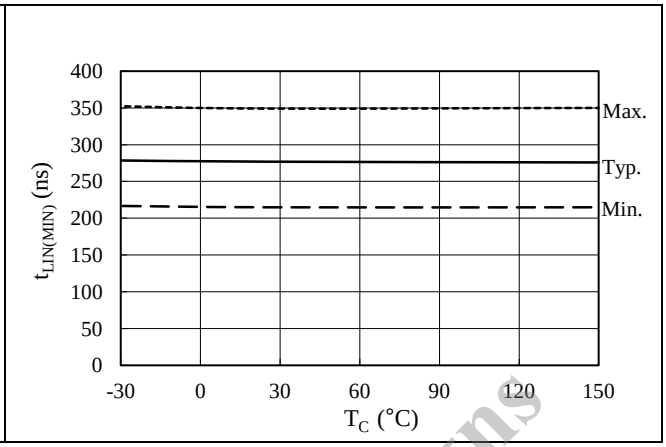


Figure 13-16. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

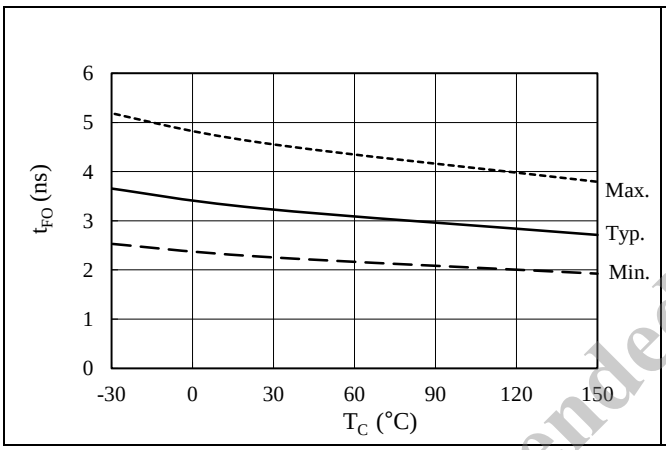


Figure 13-17. FO Pin Filtering Time vs. T_C

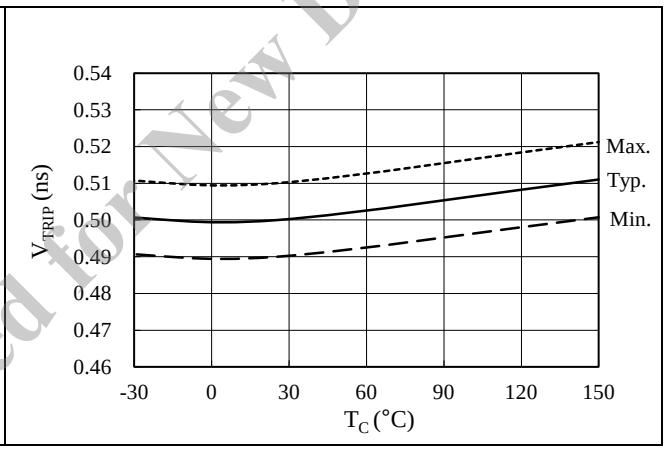


Figure 13-18. OCP Threshold Voltage, V_{TRIP} vs. T_C

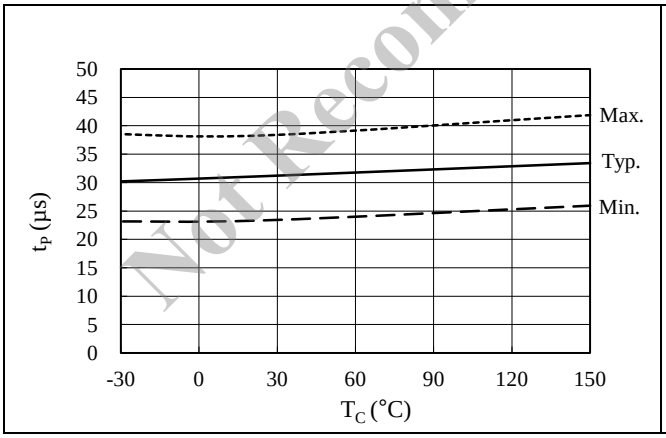


Figure 13-19. OCP Hold Time, t_P vs. T_C

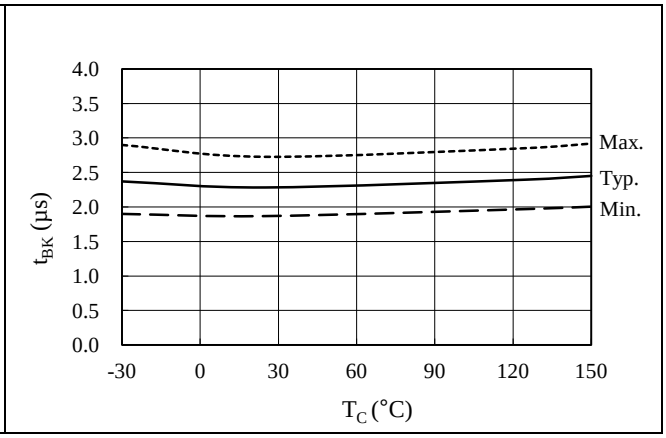
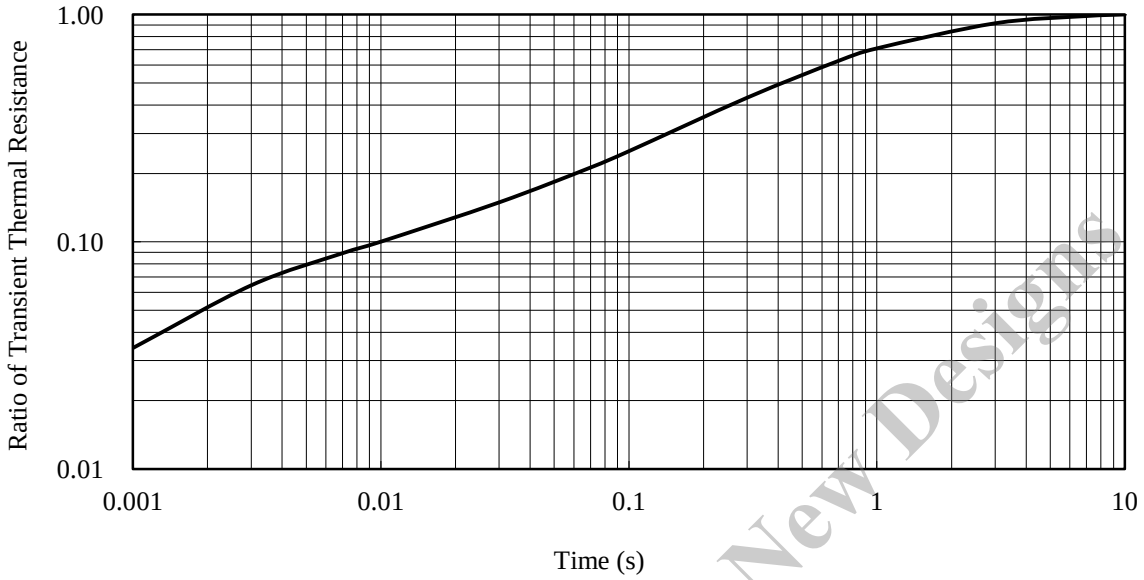


Figure 13-20. OCP Blanking Time, $t_{BK(OCP)}$ vs. T_C

13.2 Transient Thermal Resistance Curves

The following graph represents transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.



13.3 Performance Curves of Output Parts

13.3.1 Output Transistor Performance Curves

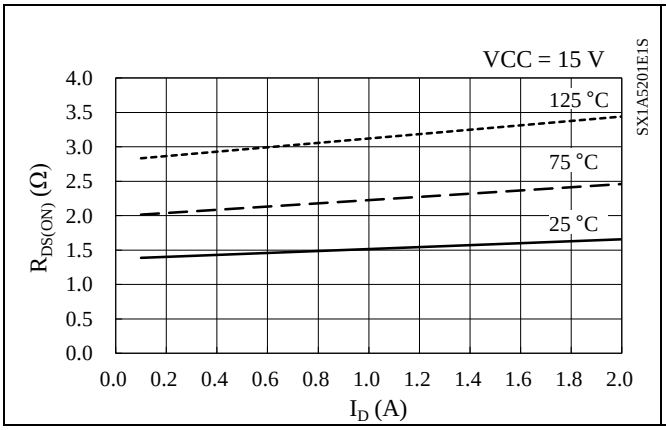


Figure 13-21. Power MOSFET $R_{DS(ON)}$ vs. I_D

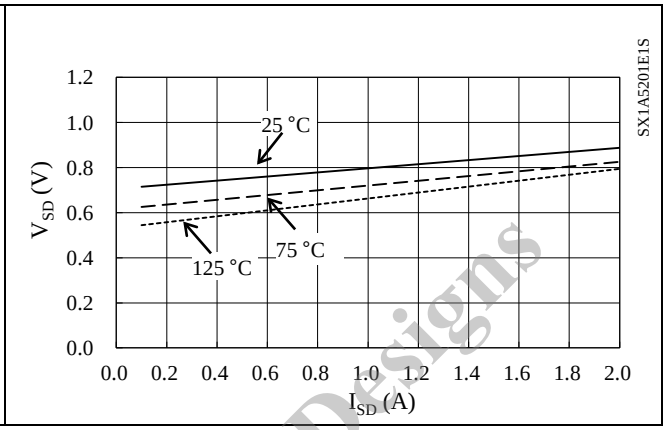


Figure 13-22. Power MOSFET V_{SD} vs. I_{SD}

13.3.2 Switching Losses

Conditions: VBB = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

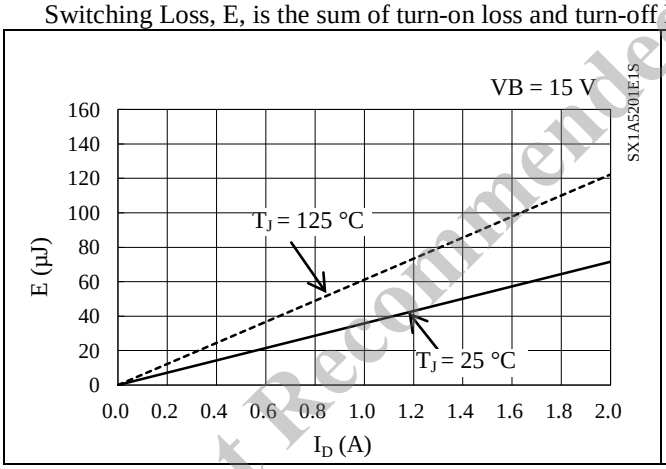


Figure 13-23. High-side Switching Loss

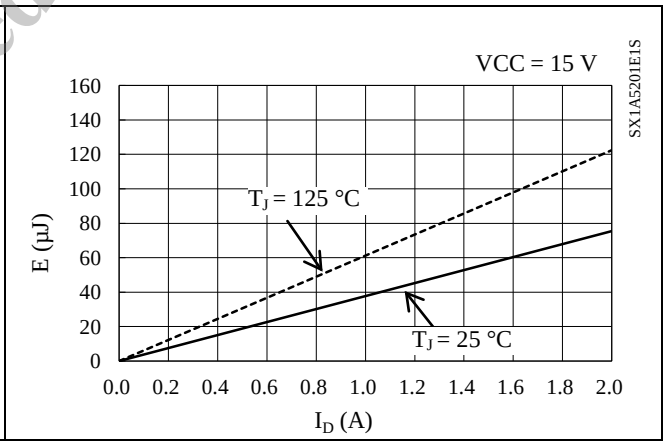


Figure 13-24. Low-side Switching Loss

13.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $R_{DS(ON)}$ and typical switching losses.

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCC pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

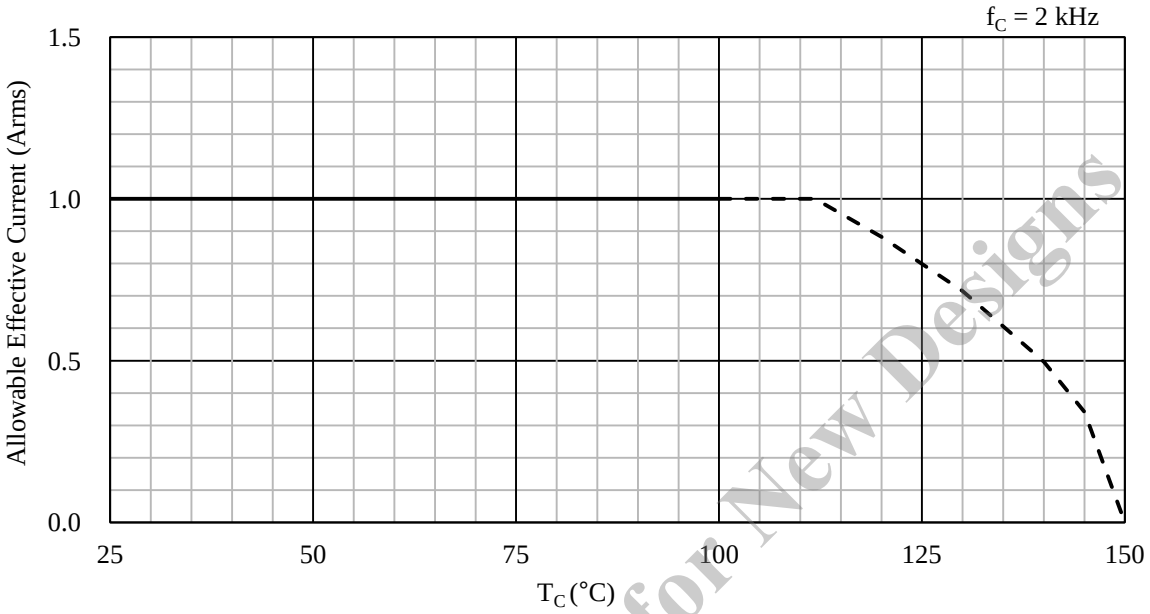


Figure 13-25. Allowable Effective Current (f_C = 2 kHz)

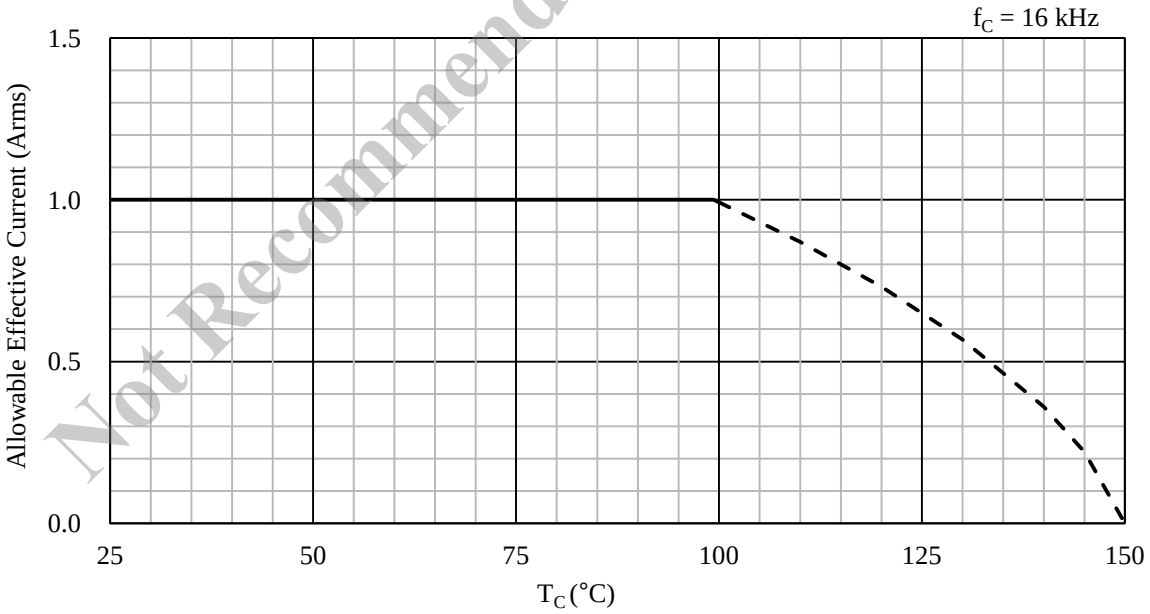


Figure 13-26. Allowable Effective Current (f_C = 16 kHz)

14. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using the SX1A5201E1S. For details on the land pattern example of the IC, see Section 8.

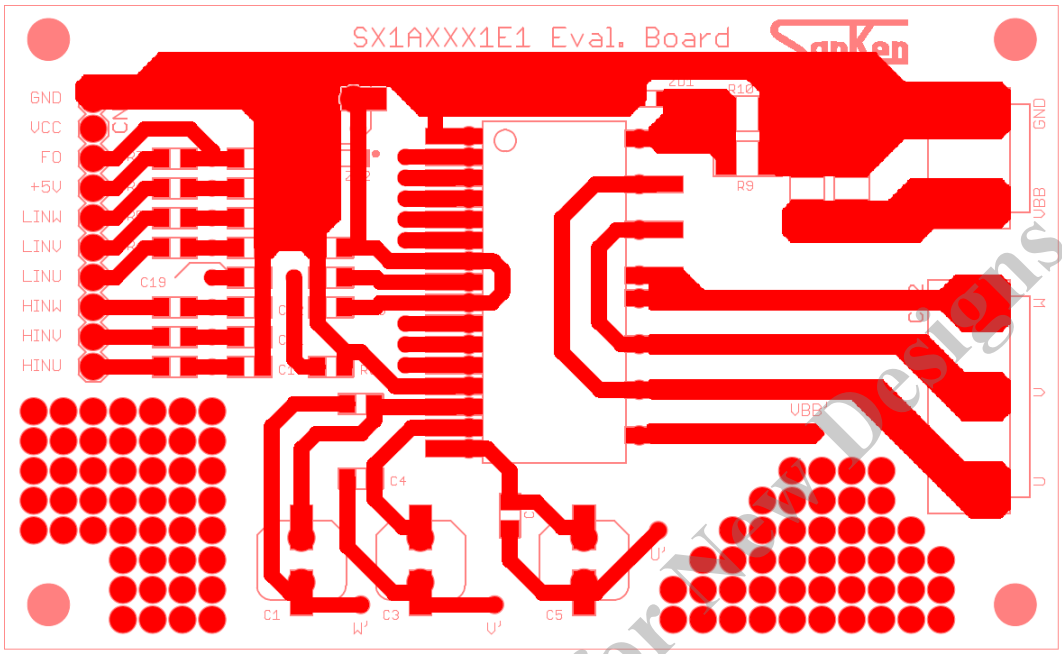


Figure 14-1. Top View

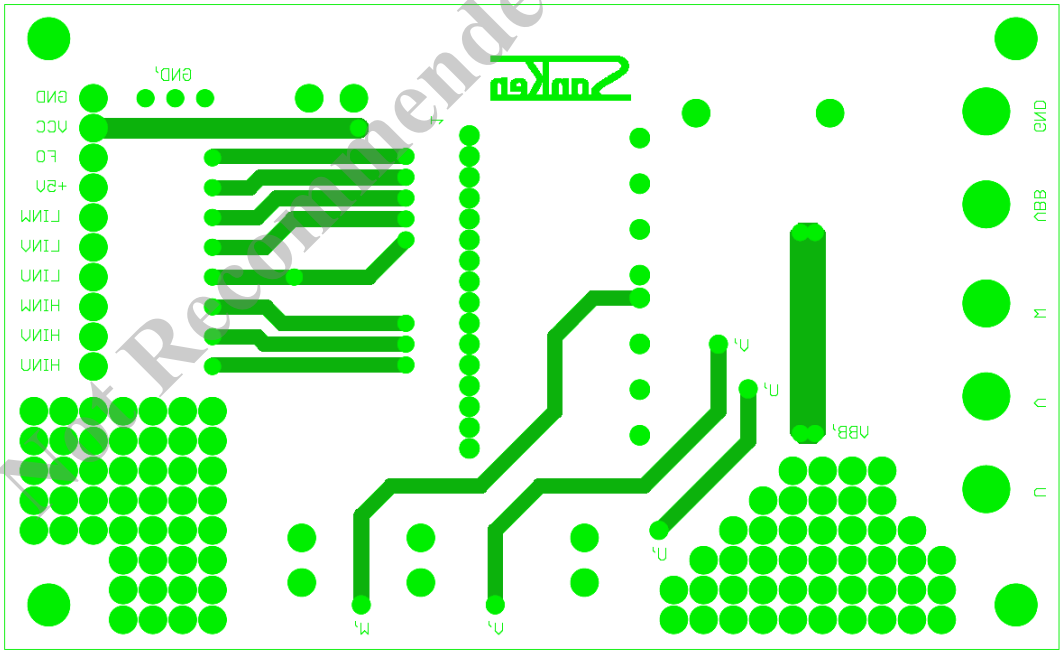


Figure 14-2. Bottom View

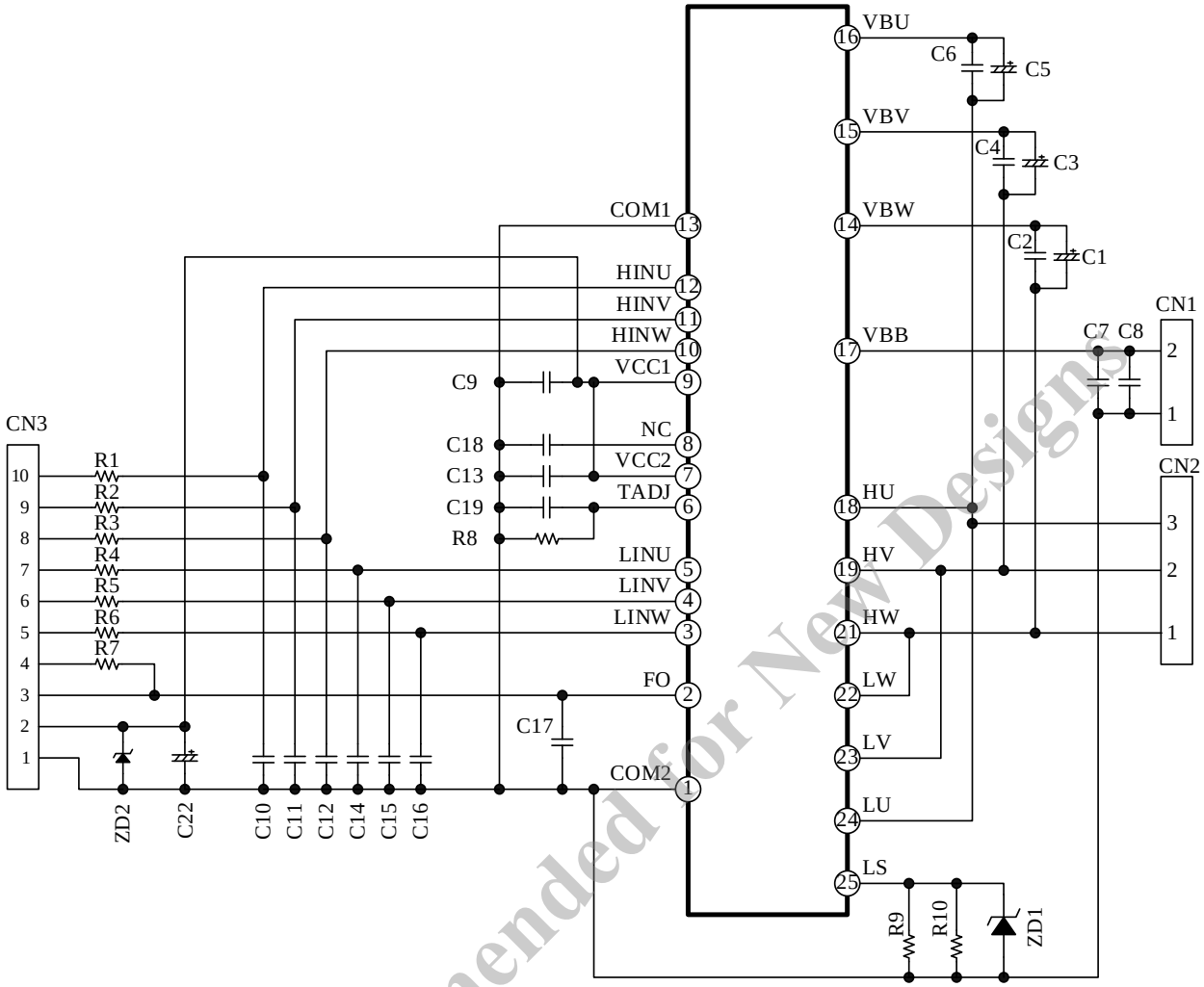


Figure14-3. Circuit Diagram of PCB Pattern Layout Example

15. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

● **Motor Driver Specifications**

IC	SX1A5201E1S
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	150 W

● **Circuit Diagram**

See Figure14-3.

● **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Electrolytic	47 µF, 35 V	C19	Ceramic	0.01 µF, 50 V
C2	Ceramic	0.1 µF, 50 V	C22	Electrolytic	47 µF, 35 V
C3	Electrolytic	47 µF, 35 V	R1	General	100 Ω, 1/8 W
C4	Ceramic	0.1 µF, 50 V	R2	General	100 Ω, 1/8 W
C5	Electrolytic	47 µF, 35 V	R3	General	100 Ω, 1/8 W
C6	Ceramic	0.1 µF, 50 V	R4	General	100 Ω, 1/8 W
C7	Film	0.033 µF, 500 V	R5	General	100 Ω, 1/8 W
C8	Film	0.033 µF, 500 V	R6	General	100 Ω, 1/8 W
C9	Ceramic	0.1 µF, 50 V	R7*	General	3.3 kΩ, 1/8 W
C10	Ceramic	100 pF, 50 V	R8*	General	3.3 kΩ, 1/8 W
C11	Ceramic	100 pF, 50 V	R9*	Metal plate	0.47 Ω, 1/4 W
C12	Ceramic	100 pF, 50 V	R10	Metal plate	0.47 Ω, 1/4 W
C13	Ceramic	100 pF, 50 V	ZD1	Zener diode	V_Z = 1 V (max.)
C14	Ceramic	0.1 µF, 50 V	ZD2	Zener diode	V_Z = 21 V (max.)
C15	Ceramic	100 pF, 50 V	IPM1	IC	SX1A5201E1S
C16	Ceramic	100 pF, 50 V	CN1	Pin header	Equiv. to B2P3-VH
C17	Ceramic	0.01 µF, 50 V	CN2	Pin header	Equiv. to B2P5-VH
C18	Ceramic	Open	CN3	Connector	Equiv. to MA10-1

* Refers to a part that requires adjustment based on operation performance in an actual application.

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