Sine-wave Driving, High Voltage 3-phase Motor Drivers with Built-in Hall Amplifiers

SX6814xM Series

Data Sheet

Description

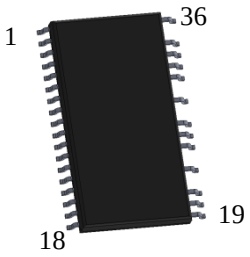
The SX6814xM series are high voltage 3-phase motor drivers, which are driven by a sinusoidal control and suitable for 8- and 10-pole motor systems. Whereas a typical 10-pole DC motor outputs a rotation signal of 15 pulses, the IC can output a 12-pulse rotation signal which is equivalent to an 8-pole motor. This enables your application to use an existing 8-pole DC motor system for 10-pole DC motor driving with no change. The IC supports Hall elements and Hall IC inputs. In addition, with its sensorless-controlled sine-wave driving system at startup, the IC offers suppressed audible noise, such as in a spoke motor startup operation. Supplied in a thin SOP36 package, where a controller, a gate driver, the output transistors of three phases, and bootstrap diodes are highly integrated, the SX6814xM series requires only a few external components for building a motor driver. This also allows a motor driver to be highly reliable in performance and design-friendly with its compactness.

Features

- Pb-free (RoHS Compliant)
- Low Noise, High Efficiency
  (Sinusoidal Current Waveform)
- Suppressed Audible Noise at Startup and Stop
- Reduced Number of Parts Achieved by Built-in Bootstrap Diodes with Current-limiting Resistors
- Hall Element and Hall IC Inputs
- Selectable Rotation Pulse Signal FG Output
  (0.8 ppr, 1.0 ppr, 2.4 ppr, 3.0 ppr)
- Application-specific Optimal Settings with External Signals: Rotation Speed, Phase Advance Angle, Rotation Direction, Enabling/Disabling of Motor Lock Detection
- Various Phase Advance Settings
  (External Phase Advance; Internal Phase Advance with Linear to Cubic Function Operations)
- 3.3 V Reference Voltage Output
  (Used for Driving Hall Elements etc.)
- Standby Function
- Adjustable Oscillation Frequency (OSCR Pin)
- Protections Include:
  - VREG Pin Undervoltage Lockout (UVLO_VREG)
  - Undervoltage Lockout for Power Supplies
    VBx Pin (UVLO_VB)
    VCC1 Pin (UVLO_VCC)
  - Overcurrent Limit (OCL)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Motor Lock Protection (MLP)
  - Reverse Rotation Detection
  - Hall Signal Abnormality Detection

Package

SOP36 (Leadform: 1891)



Not to scale

Selection Guide

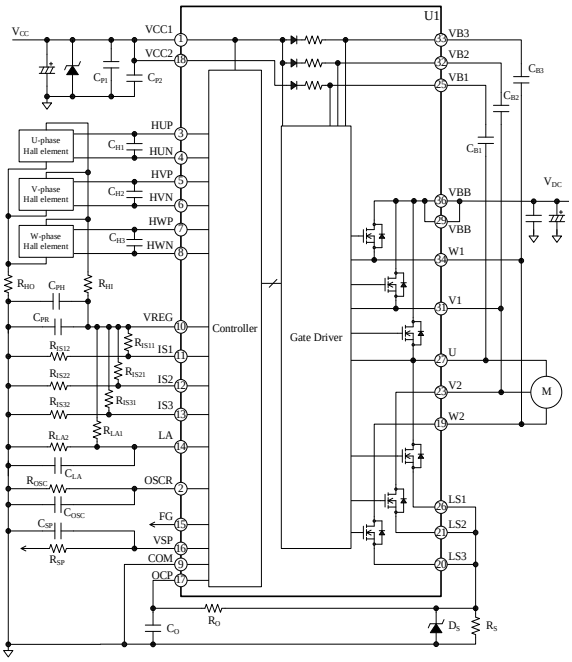
Part Number	V_{DSS}	I_O	$R_{DS(ON)}$ (max.)
SX68141M*	250 V	2.0 A	1.5 Ω
SX68140M*	600 V	1.0 A	6.0 Ω
SX68144M		1.5 A	3.6 Ω
SX68145M		2.0 A	2.5 Ω

* Under development

Applications

- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Power MOSFET Breakdown Voltage	V_{DSS}	I_D = 100 µA	250	V	SX68141M
			600		SX68140M SX68144M SX68145M
Logic Supply Voltage	V_{CC}	VCCx–COM	20	V	
	V_{BS}	VB1–U, VB2–V1, VB3–W1	20		
Output Current (DC)(1)	I_O	T_C = 25 °C, T_J < 150 °C	1.0	A	SX68140M
			1.5		SX68144M
			2.0		SX68141M
			2.0		SX68145M
Output Current (Pulse)	I_{OP}	T_C = 25 °C, pulse width ≤ 100 µs	1.5	A	SX68140M
			2.25		SX68144M
			3.0		SX68141M
			3.0		SX68145M
VREG Pin Output Voltage	V_{REG}		3.59	V	
VREG Pin Output Current	I_{REG}		30	mA	
Input Voltage 1 (HUP, HUN, HVP, HVN, HWP, HWN, OSCR, LA, OCP, IS1, IS2, IS3)	$V_{IN(1)}$		−0.5 to V_{REG}	V	
Input Voltage 2 (VSP)	$V_{IN(2)}$		−0.5 to 10	V	
Output Voltage (FG)	V_O		−0.5 to V_{REG}	V	
LSx Pin Voltage (DC)	$V_{LS(DC)}$	LSx–COM	−0.7 to 7	V	
LSx Pin Voltage (Surge)	$V_{LS(SURGE)}$	LSx–COM	−4 to 7	V	
Allowable Power Dissipation	P_D	T_C = 25 °C	3.5	W	
Operating Case Temperature(2)	$T_{C(OP)}$		−30 to 100	°C	
Junction Temperature(3)	T_J		150	°C	
Storage Temperature	T_{STG}		−40 to 150	°C	

(1) Should be derated depending on an actual case temperature. See Section 16.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the control stage, gate drive stage, power MOSFETs, and bootstrap diodes.

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBB–LSx	—	140	200	V	SX68141M
			—	300	400		SX68140M SX68144M SX68145M
Logic Supply Voltage	V_{CC}	VCCx–COM	13.5	—	16.5	V	
	V_{BS}	VB1–U, VB2–V1, VB3–W1	13.5	—	16.5	V	
Input Voltage 1 (HUP, HUN, HVP, HVN, HWP, HWN, OSCR, LA, OCP, IS1, IS2, IS3)	$V_{IN(1)}$		0	—	3.3	V	
Input Voltage 2 (VSP)	$V_{IN(2)}$		0	—	5.4	V	
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	μF	
Bootstrap Capacitor	C_B		1	—	—	μF	
Shunt Resistor [(1)]	R_S	$I_{OP} \leq 2.0$ A	0.45	—	—	Ω	SX68140M
		$I_{OP} \leq 3.0$ A	0.3	—	—		SX68141M
		$I_{OP} \leq 2.25$ A	0.4	—	—		SX68144M
		$I_{OP} \leq 3.75$ A	0.24	—	—		SX68145M
RC Filter Resistor	R_O		—	—	100	Ω	
RC Filter Capacitor	C_O		100	—	2200	pF	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	
IS Pin Setting Resistor [(2)]	R_{IS}		1	—	10	kΩ	

[(1)] Should be a low-inductance resistor.
[(2)] In case the ISx and GND pins or the ISx and VREG pins are shorted, noise may be superimposed depending on the pattern layout. In case a resistor with the value out of the recommended operating conditions is used, the IC may start operating before the ISx pin reaches the setting voltage (see Section 11). In those cases, be sure to check the actual operations.

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Operation						
Low-side Logic Operation Start Voltage	$V_{CC(ON)}$	VCCx–COM	10.5	11.5	12.5	V
Low-side Logic Operation Stop Voltage	$V_{CC(OFF)}$		10.0	11.0	12.0	V
High-side Logic Operation Start Voltage	$V_{BS(ON)}$	VB1–U, VB2–V1, VB3–W1	9.5	10.5	11.5	V
High-side Logic Operation Stop Voltage	$V_{BS(OFF)}$		9.0	10.0	11.0	V
Logic Supply Current	I_{CC}	V_{SP} = 5.4 V, I_{REG} = 0 A	2	6	10	mA
	$I_{CC(STBY)}$	V_{SP} = 0 V	30	80	180	µA
	I_{BS}	V_{Bx} = 15 V, V_{SP} = 5.4 V; VBx pin current in 1-phase operation	30	90	300	µA
Input Signal						
High Level Input Current 1 (LA, VSP, IS1, IS2, IS3)	I_{IH1}	V_{IN} = V_{REG}	—	20	60	µA
Low Level Input Current 1 (LA, VSP, IS1, IS2, IS3)	I_{IL1}	V_{INL} = 0 V	—	—	2	µA
High Level Input Current 2 (OCP)	I_{IH2}	V_{IN} = V_{REG}	−5	—	5	µA
Low Level Input Current 2 (OCP)	I_{IL2}	V_{INL} = 0 V	—	15	50	µA
FG Pin High Level Output Voltage	V_{OH}		2.97	—	3.63	V
FG Pin Low Level Output Voltage	V_{OL}		—	—	0.5	V
PWM Control						
PWM Carrier Frequency[(1)]	f_C	OSCR = COM	19	20	21	kHz
Internal Oscillator Frequency[(1)]	f_{OSC}	OSCR = COM	9.55	10.2	10.8	MHz
Dead Time[(1)]	t_D	OSCR = COM	—	1.2	—	µs
Control IC Output Pulse Duty Cycle[(1)]	D	V_{SP} = 2.0 V	—	0	3	%
		V_{SP} = 3.75 V	47	50	53	%
		V_{SP} = 5.4 V (driven by sinusoidal control)	93.7	—	100	%
Protection						
OCL Threshold Voltage	V_{LIM}		0.46	0.50	0.54	V
OCL Blanking Time	$t_{BK(OCL)}$	OSCR = COM	—	2.1	3.7	µs
OCP Threshold Voltage	V_{TRIP}		0.7	0.8	0.9	V
OCP Blanking Time	$t_{BK(OCP)}$	OSCR = COM	—	1.5	2.7	µs
OCP Hold Time	t_P	OSCR = COM	12.2	12.8	13.4	ms
MLP Detection Time	t_{LD}	OSCR = COM	4.7	5.0	5.3	s
MLP Hold Time	t_{LH}	OSCR = COM	28.5	30	31.5	s

[(1)] Refers to an internal signal; guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
TSD Operating Temperature(2)	T_{DH}	I_{REG} = 0 mA; without heatsink	—	130	—	°C
TSD Releasing Temperature(2)	T_{DL}		—	90	—	°C
TSD Hysteresis Temperature(2)	$T_{D(HYS)}$		—	40	—	°C
VREG Pin Output Voltage	V_{REG}	I_{REG} = 0 mA to 30 mA	2.97	3.3	3.58	V
VREG Pin Undervoltage Lockout Operating Voltage (2)	V_{UVRL}		2.45	2.48	2.52	V
VREG Pin Undervoltage Lockout Releasing Voltage (2)	V_{UVRH}		2.74	2.75	2.77	V

(2) Refers to the junction temperature of the gate drive stage.

3.2 Transistor Characteristics

Figure 3-1 provides the definitions of switching characteristics described in this and the following sections. V_{GS} represents the voltage between the gate and source of an internal power MOSFET.

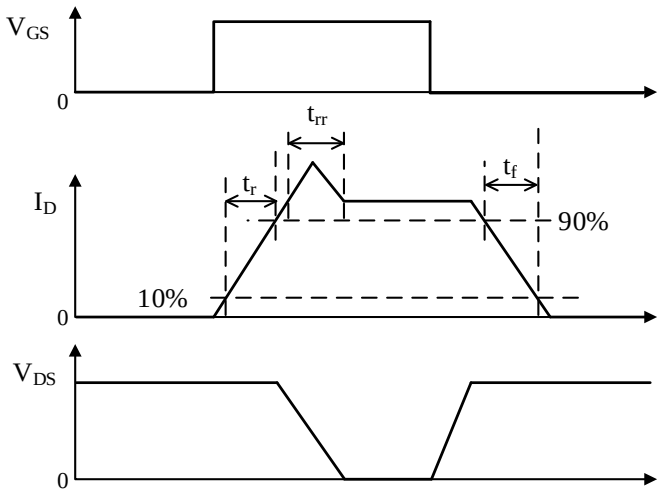


Figure 3-1. Switching Characteristics Definitions

3.2.1 SX68140M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 0.5 A	—	5.8	6.0	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} =0.5 A	—	1.0	1.6	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.5 A, V_{GS} = 0⟶15 V or 15⟶0 V, T_J = 25 °C, inductive load	—	120	—	ns
Rise Time	t_r		—	50	—	ns
Fall Time	t_f		—	40	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.5 A, V_{GS} = 0⟶15 V or 15⟶0 V, T_J = 25 °C inductive load	—	120	—	ns
Rise Time	t_r		—	50	—	ns
Fall Time	t_f		—	40	—	ns

3.2.2 SX68141M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	—	—	100	µA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1.0 A	—	1.25	1.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} =1.0 A	—	1.0	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 150 V, V_{CC} = 15 V, I_D = 1.0 A, V_{GS} = 0→15 V or 15→0 V, T_J = 25 °C, inductive load	—	75	—	ns
Rise Time	t_r		—	60	—	ns
Fall Time	t_f		—	55	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 150 V, V_{CC} = 15 V, I_D = 1.0 A, V_{GS} = 0→15 V or 15→0 V, T_J = 25 °C, inductive load	—	95	—	ns
Rise Time	t_r		—	50	—	ns
Fall Time	t_f		—	20	—	ns

3.2.3 SX68144M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	—	—	100	µA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 0.75 A	—	2.9	3.6	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} =0.75 A	—	0.95	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.75 A, V_{GS} = 0→15 V or 15→0 V, T_J = 25 °C, inductive load	—	125	—	ns
Rise Time	t_r		—	60	—	ns
Fall Time	t_f		—	25	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.75 A, V_{GS} = 0→15 V or 15→0 V, T_J = 25 °C, inductive load	—	130	—	ns
Rise Time	t_r		—	65	—	ns
Fall Time	t_f		—	30	—	ns

3.2.4 SX68145M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1.0 A	—	2.0	2.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} =1.0 A	—	1.0	1.6	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 1.0 A, V_{GS} = 0→15 V or 15→0 V, T_J = 25 °C, inductive load	—	125	—	ns
Rise Time	t_r		—	60	—	ns
Fall Time	t_f		—	25	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 1.0 A, V_{GS} = 0→15 V or 15→0 V, T_J = 25 °C, inductive load	—	130	—	ns
Rise Time	t_r		—	65	—	ns
Fall Time	t_f		—	30	—	ns

3.3 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	—	—	10	μA
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A; R_{BOOT} excluded	—	1.0	1.3	V
Bootstrap Diode Series Resistor	R_{BOOT}		45	60	75	Ω

3.4 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case Thermal Resistance(1)	R_{J-C}	All power MOSFETs operating(2)	—	—	10	°C/W
Junction-to-Ambient Thermal Resistance	R_{J-A}	All power MOSFETs operating(2)	—	—	35	°C/W

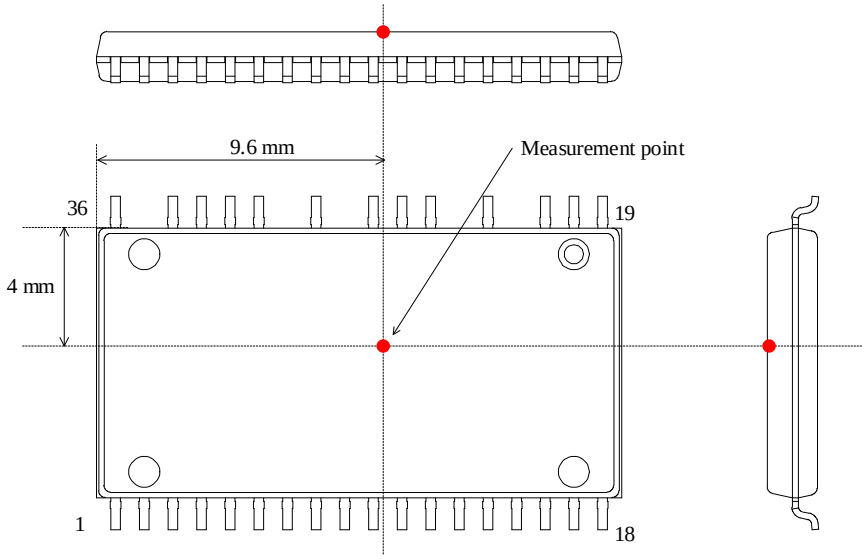


Figure 3-2. Case Temperature Measurement Point

(1) Refers to a case temperature at the measurement point described in Figure 3-2.
(2) Mounted on a CEM-3 glass (1.6 mm in thickness, 35 μm in copper foil thickness), and measured under natural air cooling without silicone potting.

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	1.4	—	g

5. Block Diagram

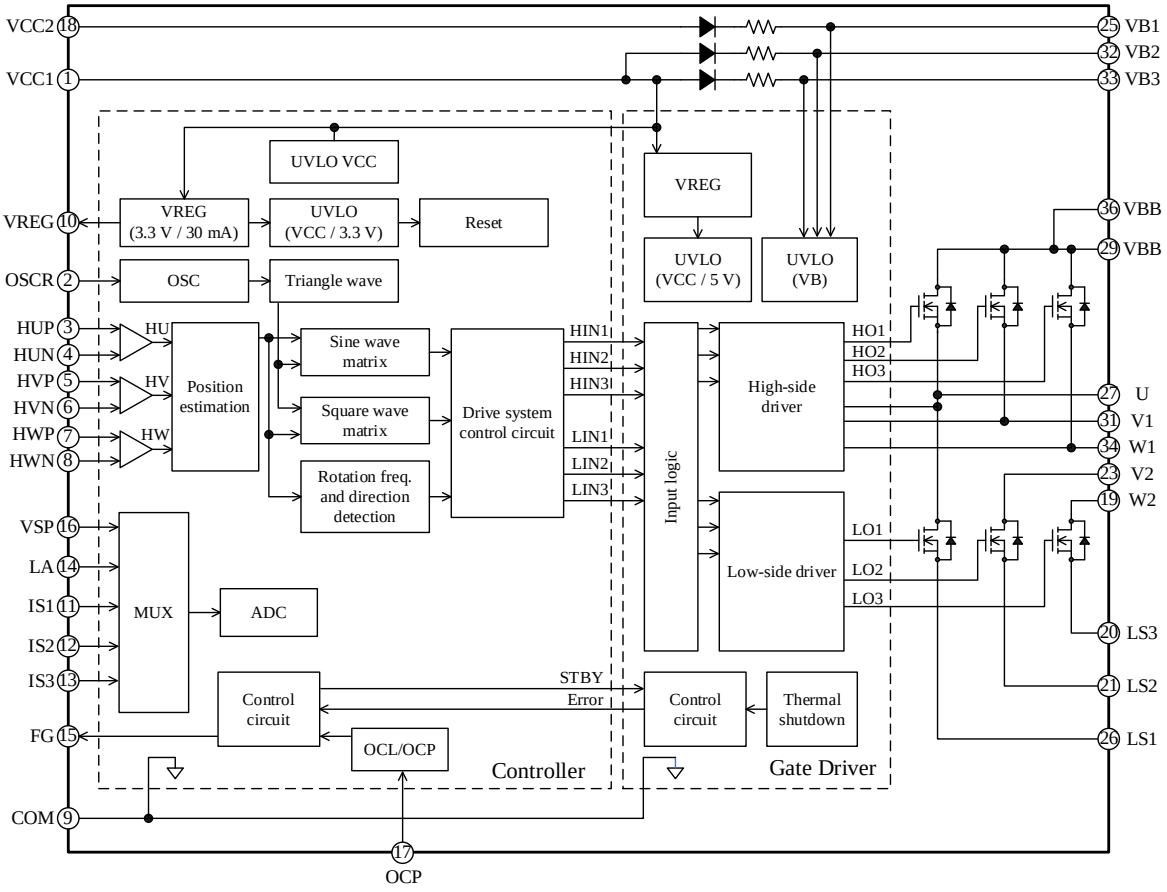
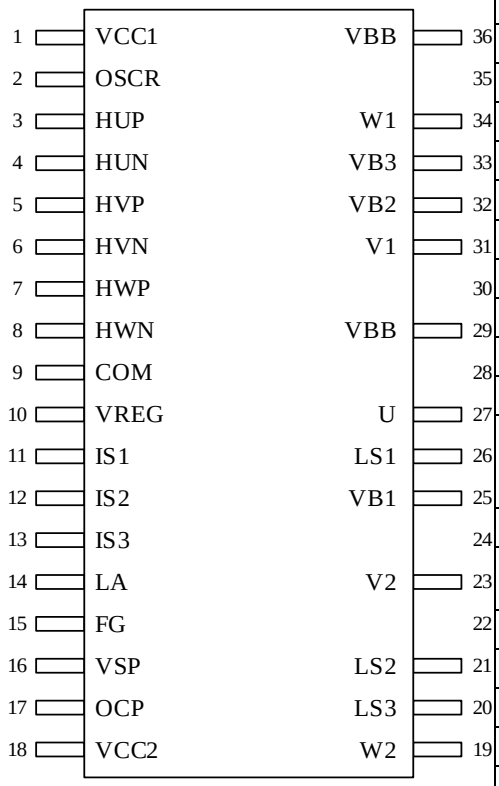


Figure 5-1. Block Diagram

6. Pin Configuration Definitions

Top View



Pin Number	Pin Name	Description
1	VCC1	Logic supply voltage input 1
2	OSCR	Input for oscillator frequency setting signal
3	HUP	U-phase Hall element positive signal input (+)
4	HUN	U-phase Hall element negative signal input (−)
5	HVP	V-phase Hall element positive signal input (+)
6	HVN	V-phase Hall element negative signal input (−)
7	HWP	W-phase Hall element positive signal input (+)
8	HWN	W-phase Hall element negative signal input (−)
9	COM	Logic ground
10	VREG	Internal regulator output
11	IS1	Function setting pin 1 (the number of rotation pulses, the number of motor poles, standby function setting)
12	IS2	Function setting pin 2 (phase advance setting)
13	IS3	Function setting pin 3 (rotation direction, motor lock protection, load setting)
14	LA	Input for phase advance angle setting signal
15	FG	Rotation pulse signal output (2.4 ppr)
16	VSP	Input for motor speed control signal
17	OCP	Input for overcurrent detection signal
18	VCC2	Logic supply voltage input 2
19	W2	W-phase output (connected to W1 externally)
20	LS3	W-phase low-side power MOSFET source
21	LS2	V-phase low-side power MOSFET source
22	—	Pin removed
23	V2	V-phase output (connected to V1 externally)
24	—	Pin removed
25	VB1	U-phase high-side floating supply voltage input
26	LS1	U-phase low-side power MOSFET source
27	U	U-phase output
28	—	Pin removed
29	VBB	Positive DC bus supply voltage (+)
30	—	Pin removed
31	V1	V-phase output (connected to V2 externally)
32	VB2	V-phase high-side floating supply voltage input
33	VB3	W-phase high-side floating supply voltage input
34	W1	W-phase output (connected to W2 externally)
35	—	Pin removed
36	VBB	Positive DC bus supply voltage (+)

7. Typical Application

Figure 7-1 is a typical application which uses signals input from the Hall elements.

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

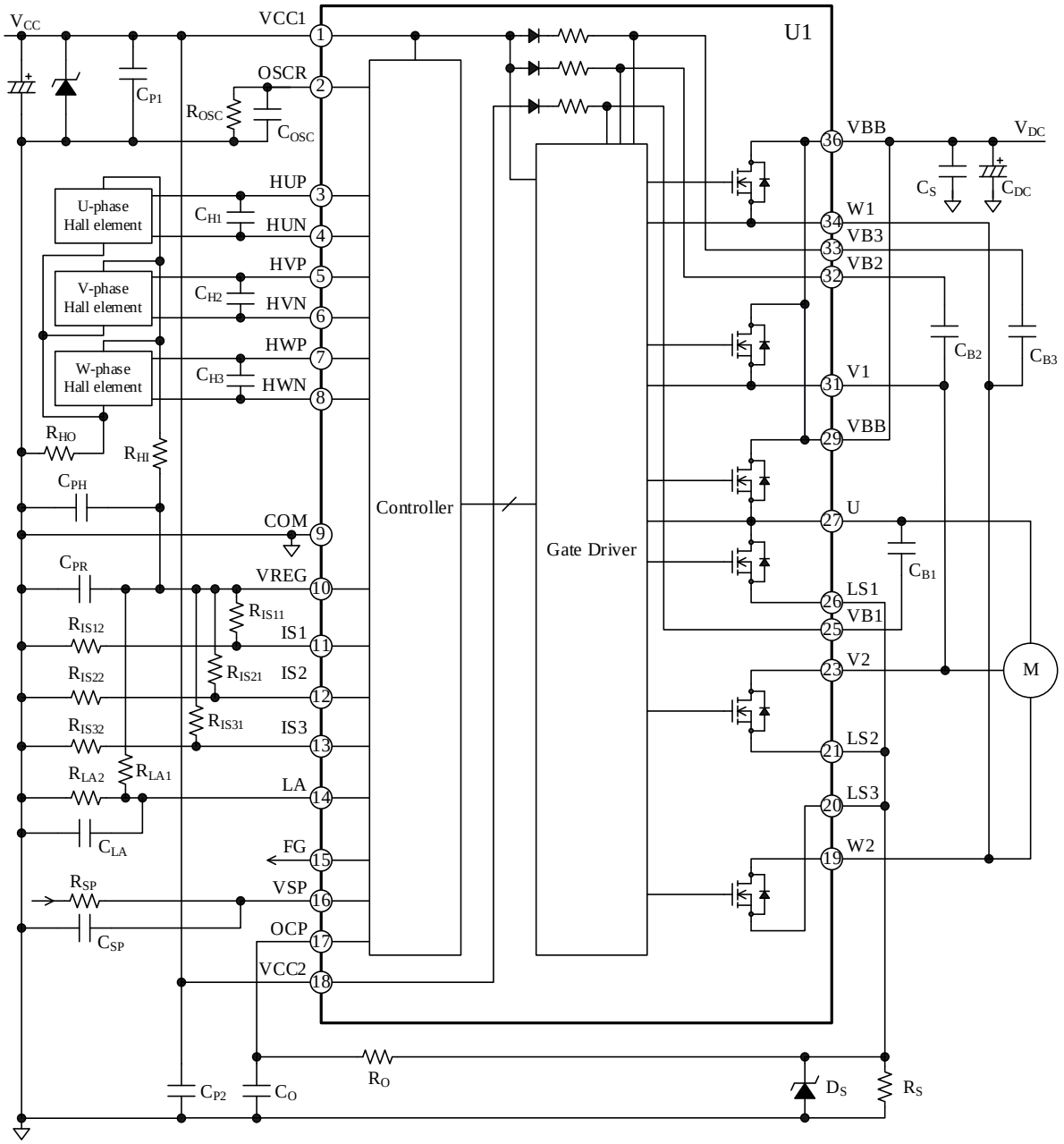
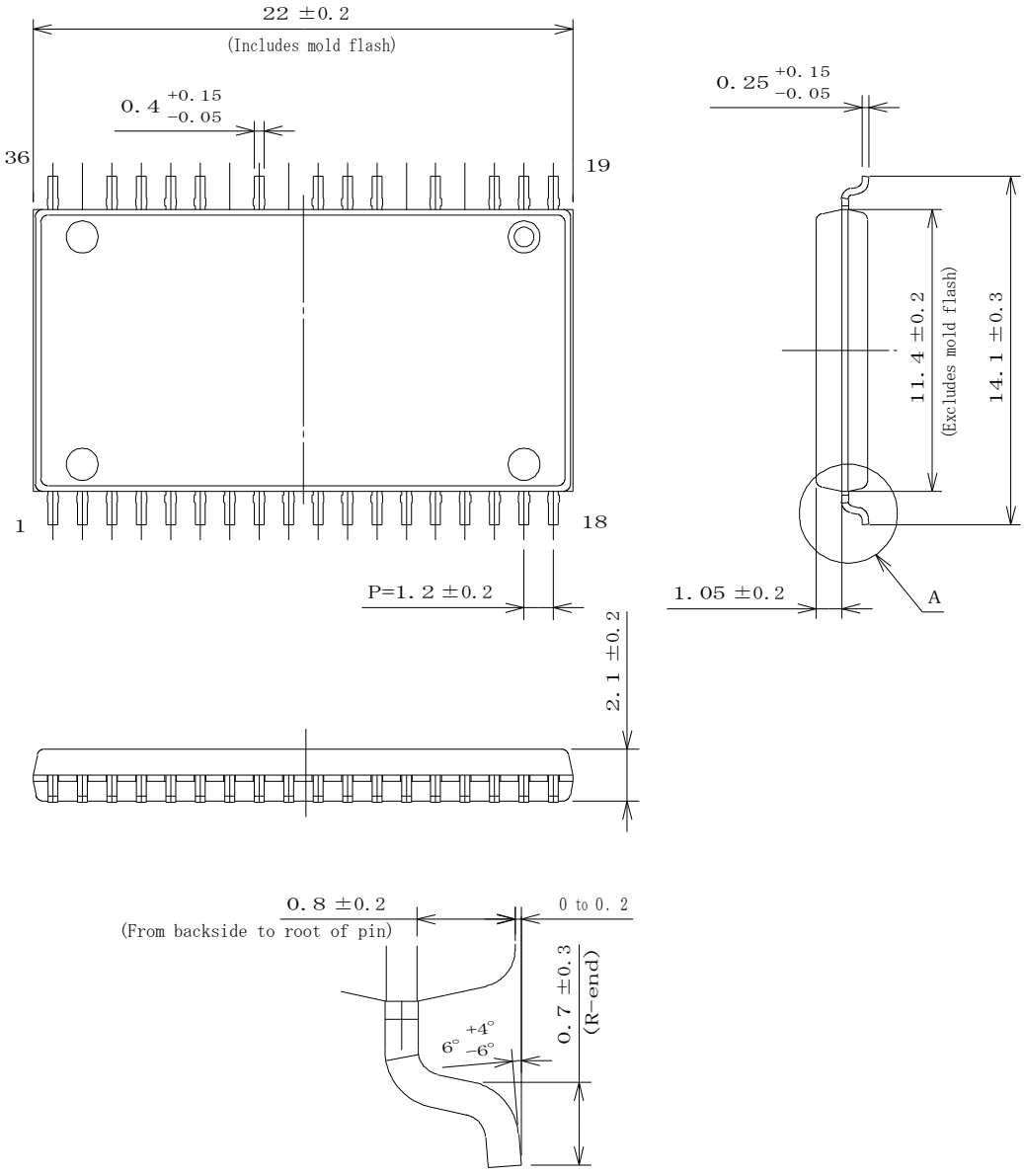


Figure 7-1. Application Using Signals Input from Hall Elements

8. Physical Dimensions

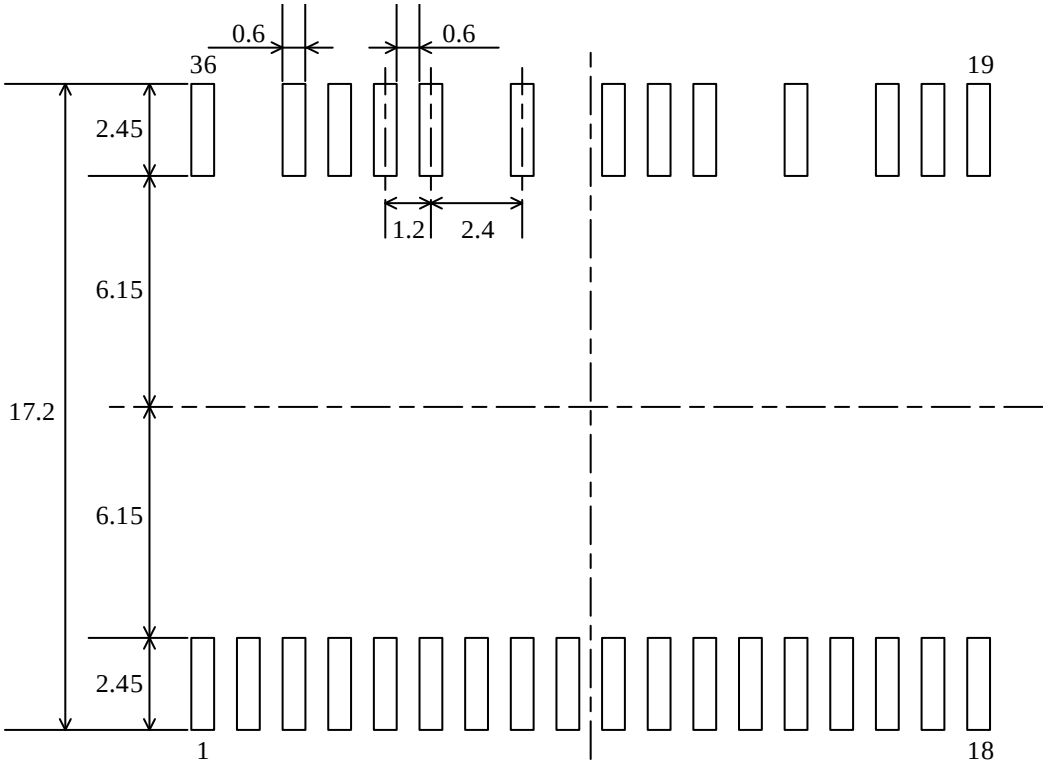
● **SOP36 Package (Leadform: 1891)**



NOTES:

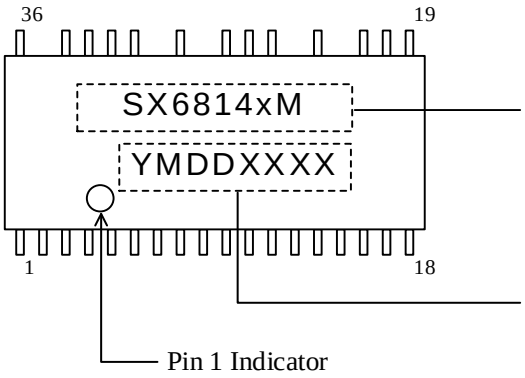
- Dimensions in millimeters
- Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Reflow (MSL3):
  Preheating: 180 °C / 90 ± 30 s
  Solder heating: 250 °C / 10 ± 1 s (260 °C peak, 2 times)
  Soldering iron: 380 ± 10 °C / 3.5 ± 0.5 s, 1 time

● **Land Pattern Example**



Unit: mm

9. Marking Diagram



10. Truth Tables

Table 10-1 and Table 10-2 are truth tables for motor driving by the trapezoidal control in a forward or reverse rotation, respectively. The IC drives the motor with the sinusoidal control, based on the trapezoidal control defined in the truth tables. In the reverse rotation detection, the IC drives the motor with the trapezoidal control.

Table 10-1. Truth Table for Trapezoidal Control (Forward)

Position Sensing Signal			U-phase		V-phase		W-phase	
HU	HV	HW	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor
H	L	H	OFF	ON	ON	OFF	OFF	OFF
H	L	L	OFF	ON	OFF	OFF	ON	OFF
H	H	L	OFF	OFF	OFF	ON	ON	OFF
L	H	L	ON	OFF	OFF	ON	OFF	OFF
L	H	H	ON	OFF	OFF	OFF	OFF	ON
L	L	H	OFF	OFF	ON	OFF	OFF	ON
L	L	L	OFF	OFF	OFF	OFF	OFF	OFF
H	H	H	OFF	OFF	OFF	OFF	OFF	OFF

Table 10-2. Truth Table for Trapezoidal Control (Reverse)

Position Sensing Signal			U-phase		V-phase		W-phase	
HU	HV	HW	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor
L	H	L	OFF	ON	ON	OFF	OFF	OFF
L	H	H	OFF	ON	OFF	OFF	ON	OFF
L	L	H	OFF	OFF	OFF	ON	ON	OFF
H	L	H	ON	OFF	OFF	ON	OFF	OFF
H	L	L	ON	OFF	OFF	OFF	OFF	ON
H	H	L	OFF	OFF	ON	OFF	OFF	ON
H	H	H	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	OFF	OFF	OFF	OFF	OFF	OFF

11. Pin Settings: IS1, IS2, and IS3

Table 11-1 to Table 11-3 list the settings for the ISx pin. Setting the ISx pin voltages at startup enables the individual pin settings (e.g., the number of rotation pulse signals, phase advance angles, rotation directions).

Table 11-1. IS1 Pin Settings

IS1 Pin Voltage (Typ.)	Number of FG Output Pulses			Standby Function
	Number of Motor Poles	Rotation Pulse Periods per Electrical Angle of 360°	Number of FG Output Pulses per Motor Rotation	
0 to 1/8 V_{REG}	8 poles	3 ppr	12 pulses	Enabled
1/8 V_{REG} to 2/8 V_{REG}	8 poles	3 ppr	12 pulses	Disabled
2/8 V_{REG} to 3/8 V_{REG}	10 poles	2.4 ppr	12 pulses	Enabled
3/8 V_{REG} to 4/8 V_{REG}	10 poles	2.4 ppr	12 pulses	Disabled
4/8 V_{REG} to 5/8 V_{REG}	10 poles	0.8 ppr	4 pulses	Disabled
5/8 V_{REG} to 6/8 V_{REG}	10 poles	0.8 ppr	4 pulses	Enabled
6/8 V_{REG} to 7/8 V_{REG}	8 poles	1 ppr	4 pulses	Disabled
7/8 V_{REG} to 8/8 V_{REG}	8 poles	1 ppr	4 pulses	Enabled

Table 11-2. IS2 Pin Settings

IS2 Pin Voltage (Typ.)	Phase Advance Function	Setting Range of Phase Advance Angle
0 to 1/8 V_{REG}	External phase advance	0° to 59.53125°
1/8 V_{REG} to 2/8 V_{REG}	Cubic function operation	0° to 58°
2/8 V_{REG} to 3/8 V_{REG}	Quadratic function operation	0° to 29°
3/8 V_{REG} to 4/8 V_{REG}	Quadratic function operation	0° to 41°
4/8 V_{REG} to 5/8 V_{REG}	Quadratic function operation	0° to 58°
5/8 V_{REG} to 6/8 V_{REG}	Linear function operation	0° to 29°
6/8 V_{REG} to 7/8 V_{REG}	Linear function operation	0° to 41°
7/8 V_{REG} to 8/8 V_{REG}	Linear function operation	0° to 58°

Table 11-3. IS3 Pin Settings

IS3 Pin Voltage (Typ.)	Rotation Direction	Motor Lock Protection	Torque at Startup
0 to 1/8 V_{REG}	Reverse (CCW)	Enabled	Small
1/8 V_{REG} to 2/8 V_{REG}	Reverse (CCW)	Enabled	Large
2/8 V_{REG} to 3/8 V_{REG}	Reverse (CCW)	Disabled	Small
3/8 V_{REG} to 4/8 V_{REG}	Reverse (CCW)	Disabled	Large
4/8 V_{REG} to 5/8 V_{REG}	Forward (CW)	Disabled	Large
5/8 V_{REG} to 6/8 V_{REG}	Forward (CW)	Disabled	Small
6/8 V_{REG} to 7/8 V_{REG}	Forward (CW)	Enabled	Large
7/8 V_{REG} to 8/8 V_{REG}	Forward (CW)	Enabled	Small

12. Timing Charts

The timing charts below represent the operational waveforms of each pin under different conditions, e.g., forward rotation (no phase advance), forward rotation (phase advance by 15°), and reverse rotation: Figure 12-1 to Figure 12-3 show 10-pole DC motor operations, and Figure 12-4 to Figure 12-6 show 8-pole DC motor operations. The following symbols used in these figures represent the signals generated inside the IC: S_U, S_V, S_W, S_X, S_Y, S_Z.

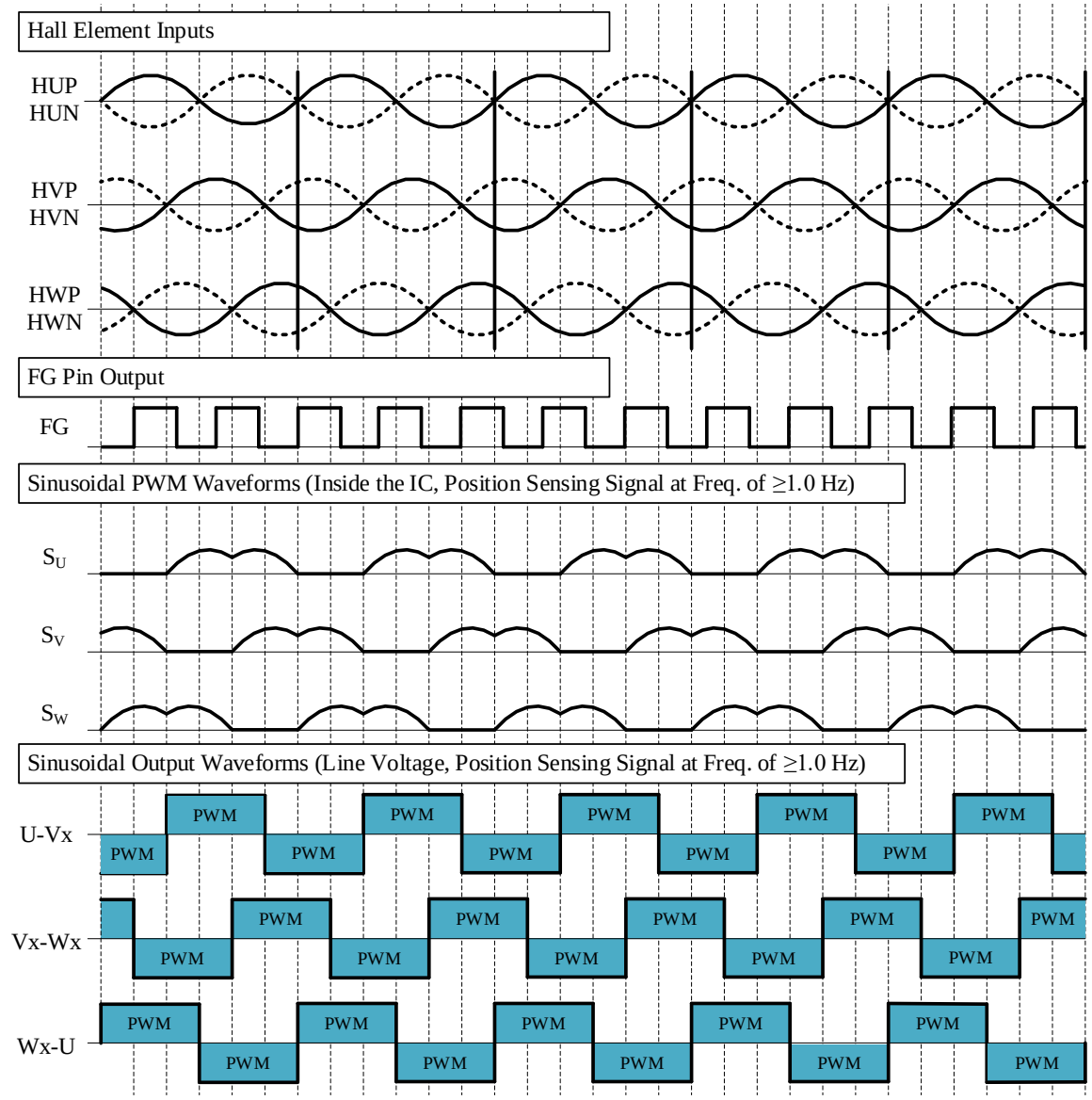


Figure 12-1. 10-pole DC Motor Operational Waveforms (Forward, No Phase Advance)

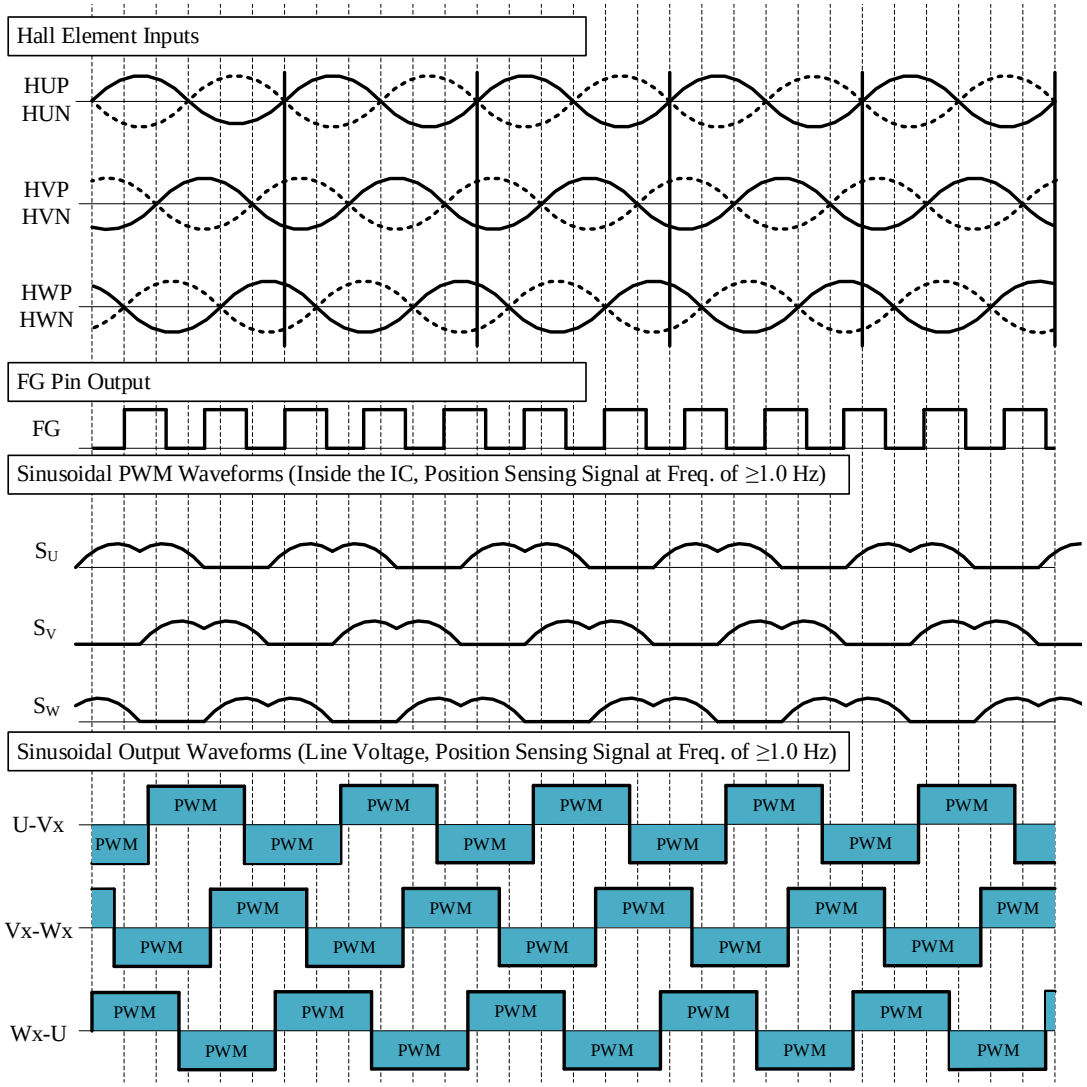


Figure 12-2. 10-pole DC Motor Operational Waveforms (Forward, Phase Advance by 15°)

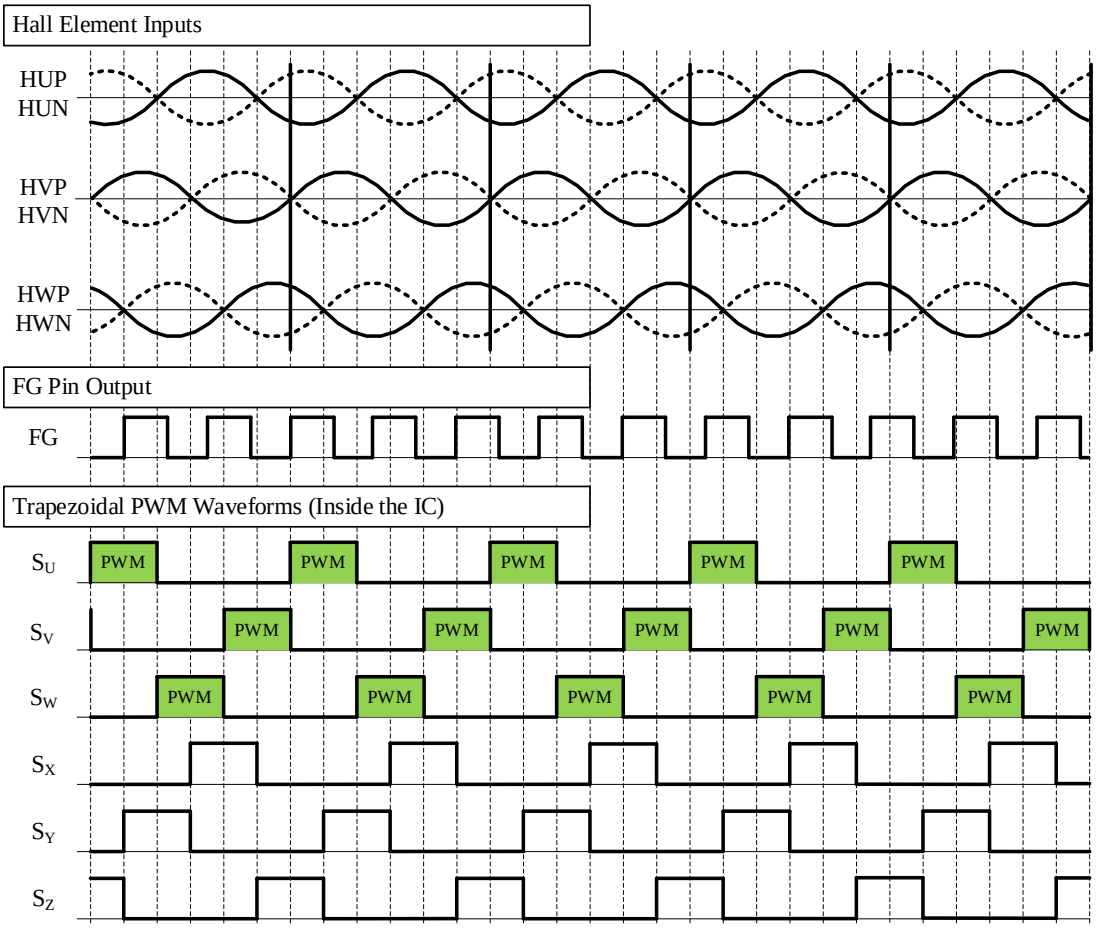


Figure 12-3. 10-pole DC Motor Operational Waveforms (in Reverse Rotation Detection)

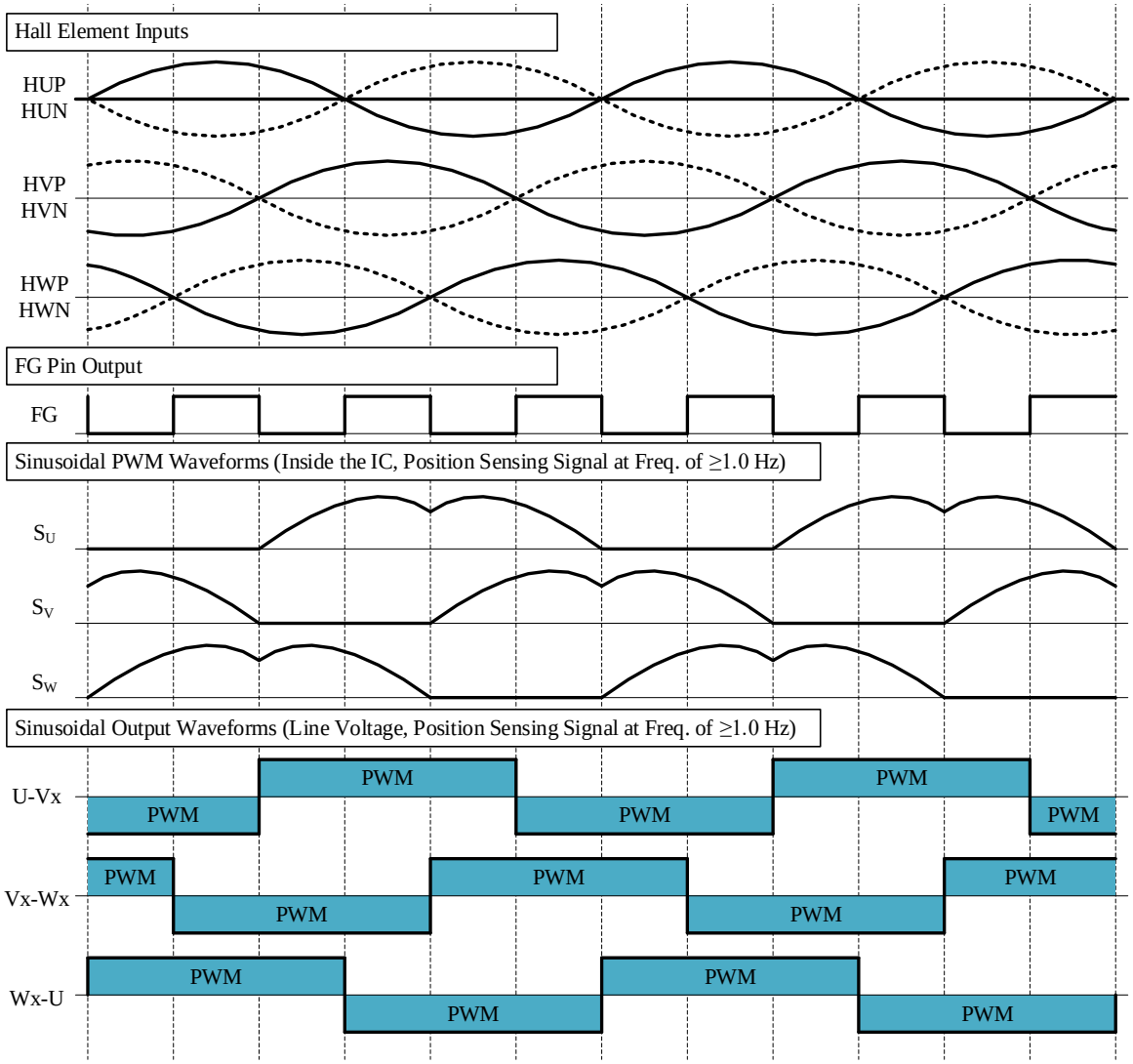


Figure 12-4. 8-pole DC Motor Operational Waveforms (Forward, No Phase Advance)

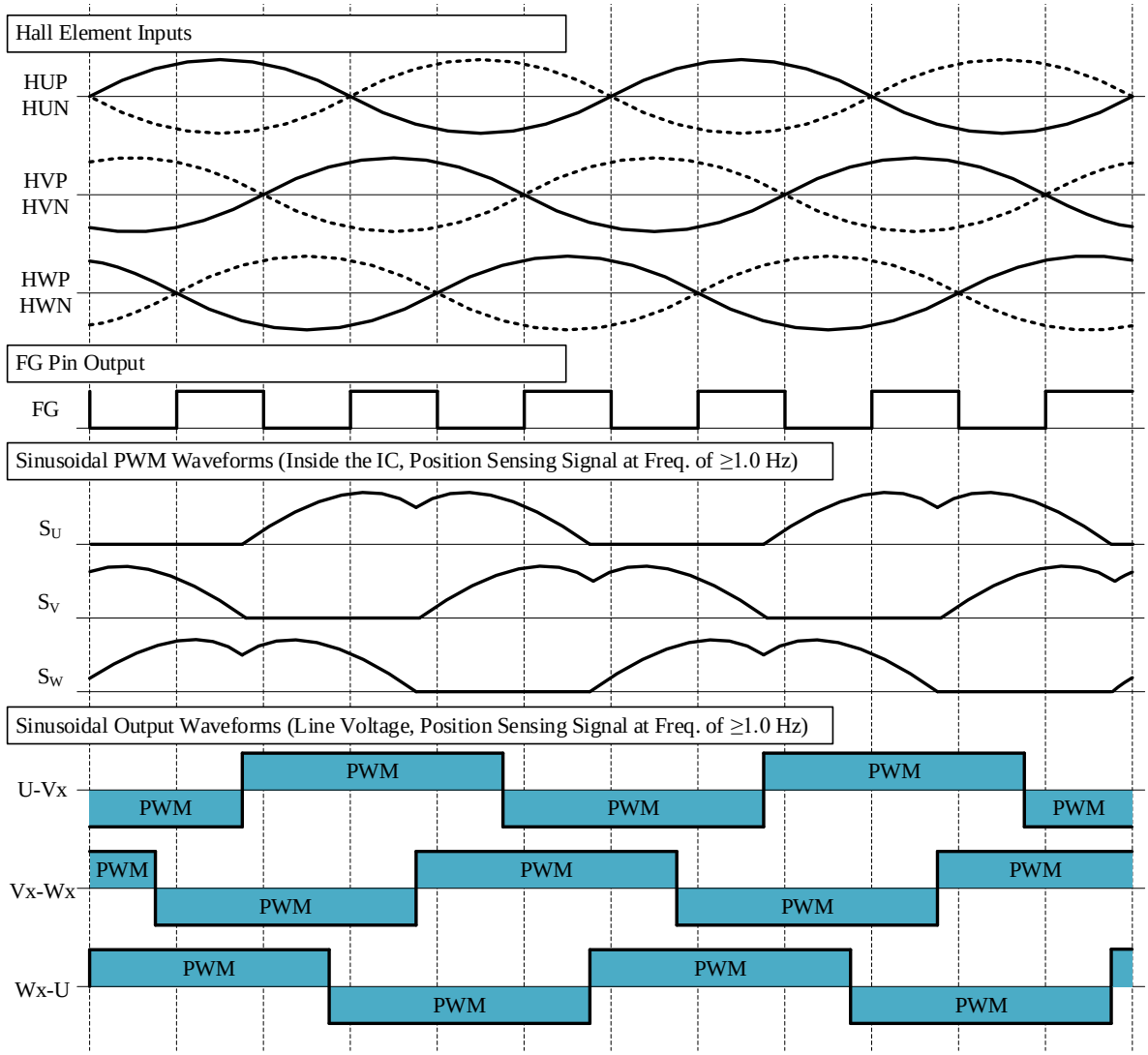


Figure 12-5. 8-pole DC Motor Operational Waveforms (Forward, Phase Advance by 15°)

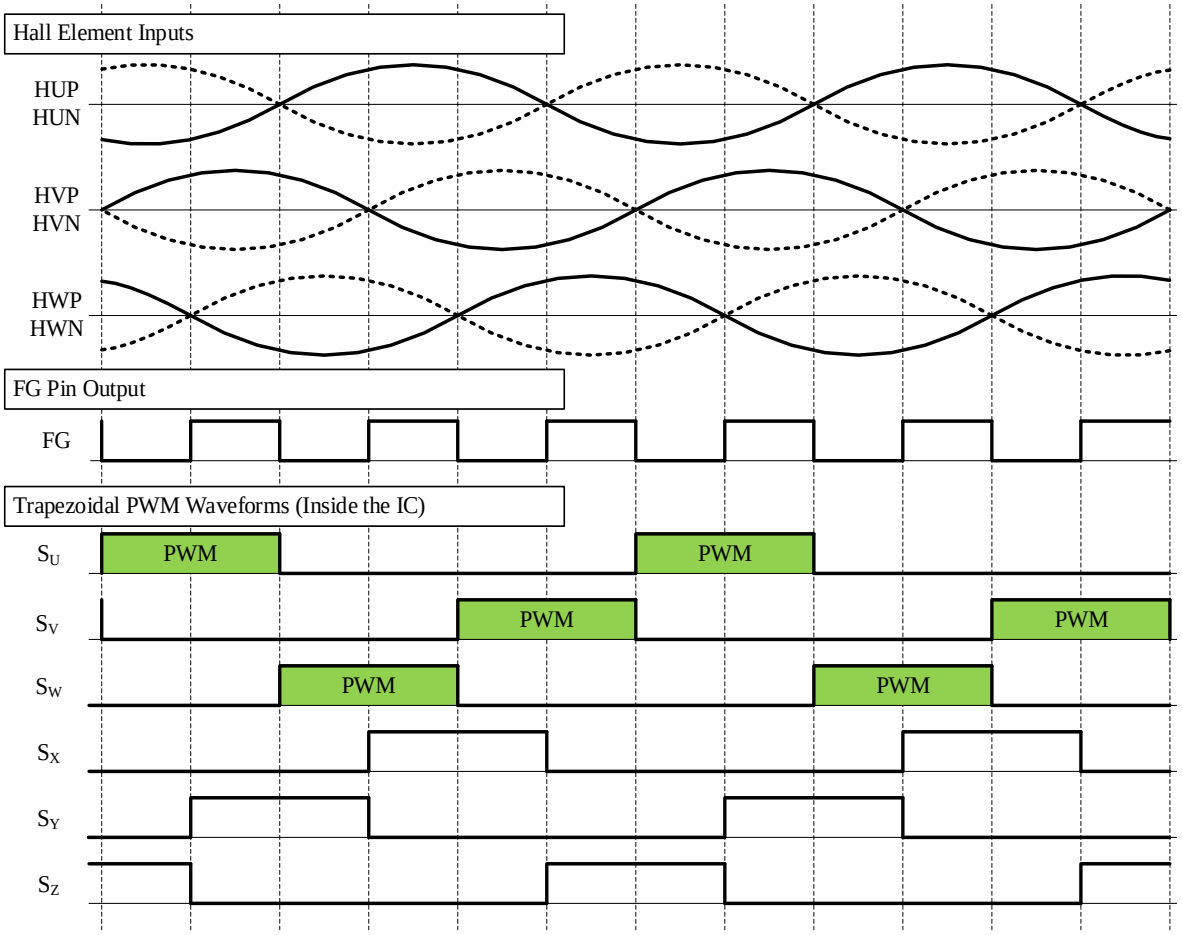


Figure 12-6. 8-pole DC Motor Operational Waveforms (in Reverse Rotation Detection)

13. Functional Descriptions

For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 3 and the electronic symbol names of the typical applications in Section 7. All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name or an electronic symbol name with the arbitrary letter "x", representing the certain numbers and letters (1 to 3 and U to W). Thus, "the VCCx pin" is used when referring to either or both of the VCC1 and VCC2 pins.

13.1 Pin Descriptions

13.1.1 VCC1 and VCC2

These are the logic supply pins for the built-in control ICs. The VCC1 pin has the undervoltage lockout for power supply (see Section 13.7.2.2). The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{Px}, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCCx and COM pins. Voltages to be applied between the VCCx and COM pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

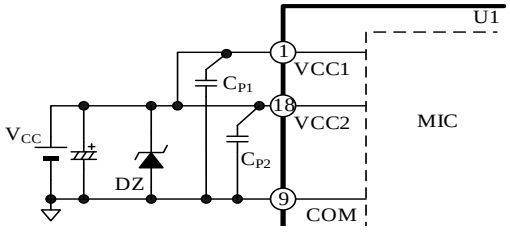


Figure 13-1. VCCx Pin Peripheral Circuit

13.1.2 OSCR

Figure 13-2 shows the OSCR pin and its peripheral circuit. To adjust a frequency of the internal oscillator, connect a resistor, R_{OSC}, to the OSCR pin. To reduce noises on the pin, connect a noise filter capacitor, C_{OSC}, with a capacitance of about 0.1 µF. Figure 13-3 shows how the carrier frequency, f_{PWM}, and the resistance, R_{OSC}, are related. When the OSCR and COMP pins are shorted, the carrier frequency is set to f_C = 20 kHz. The following characteristics depend on a frequency of the internal oscillator:

- OCP Hold Time, t_P
- OCL Blanking Time, $t_{BK(OCL)}$
- OCP Blanking Time, $t_{BK(OCP)}$
- MLP Detection Time, t_{LD}
- MLP Hold Time, t_{LH}

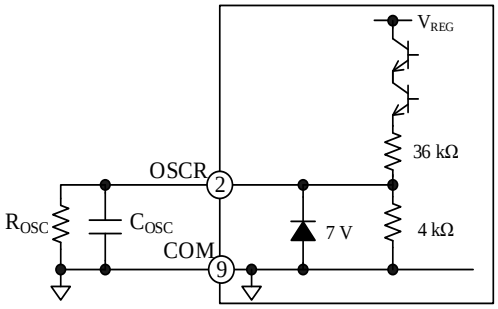


Figure 13-2. Internal Circuit Diagram of OSCR Pin and Its Peripheral Circuit

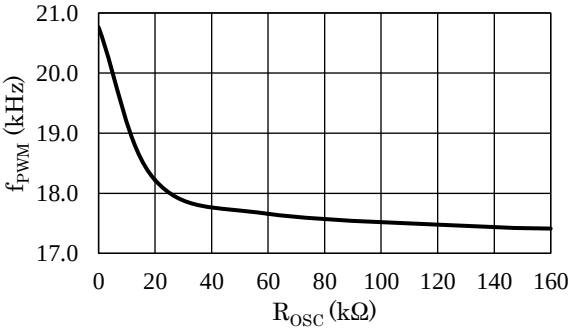


Figure 13-3. Typical Performance Curve of OSCR Pin

13.1.3 HUP, HVP, and HWP; HUN, HVN and HWN

These are the input pins for Hall element signals. The HxP pin is connected to the positive node of a Hall element, whereas the HxN pin is connected to the negative node of a Hall element. As Figure 13-4 illustrates, connect a noise filter capacitor, C_{Hx}, with a capacitance of about 0.1 µF, between the HxP and HxN pins. C_{Hx} must be placed near the IC with a minimal length of traces. The IC incorporates the protection circuit that detects abnormal signals from the external Hall elements (see Section 13.7.7).

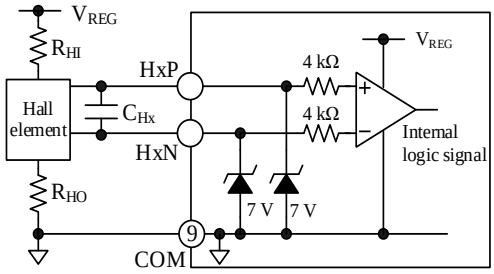


Figure 13-4. Internal Circuit Diagram of HxP and HxN Pins and Their Peripheral Circuit

13.1.4 COM

This is the logic ground pin for the built-in control ICs. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 13-5).

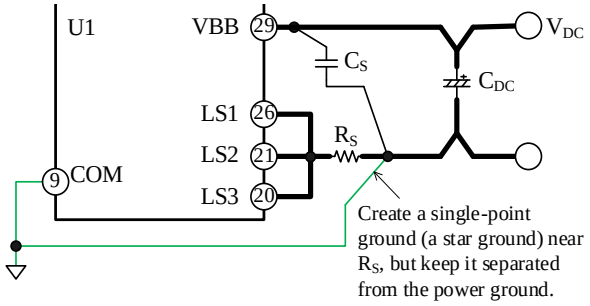


Figure 13-5. Connections to Logic Ground

13.1.5 VREG

This is the 3.3 V regulator output pin, which can be used for the power supply of the external Hall elements. A maximum output current of the VREG pin is 30 mA. To stabilize the VREG pin output, connect a capacitor, C_{PR}, of about 0.1 µF to the pin. The VREG pin also has the undervoltage lockout. For more details on this function, see Section 13.7.1.

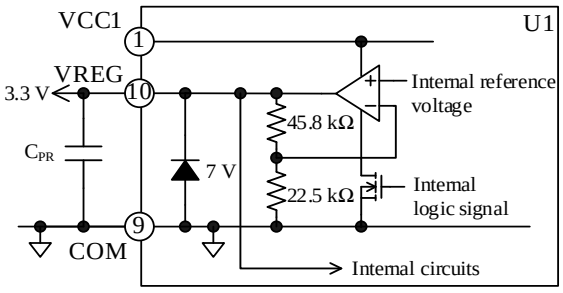


Figure 13-6. Internal Circuit Diagram of VREG Pin

13.1.6 IS1, IS2, and IS3

These are the function setting pins. The ISx pin is for changing pin voltages to be applied and for setting the corresponding functions.

The IS1 pin sets the number of FG output pulses based on the number of motor poles to be connected, and enables and disables the standby function. The IS2 pin determines the phase advance control. The IS3 pin selects the motor's rotation direction, enables and disables the motor lock protection, and sets the torque level at startup. For more details on the pin settings, see Table 11-1 to Table 11-3, respectively.

Section 13.4 describes the standby function; Section 13.7.5 explains the motor lock protection.

13.1.7 LA

The IC features the phase advance function. When the external phase advance is selected by the IS2 pin, an analog voltage applied to the LA pin determines the phase advance angle. When the internal phase advance is selected by the IS2 pin, a voltage input to the LA pin determines the coefficient of the internal function operation. Section 13.6 gives detailed explanations on the LA pin settings and the phase advance function.

13.1.8 FG

The FG pin outputs a rotation pulse signal that is generated based on a position sensing signal. A rotation pulse signal is inverted at each edge of the Hall element signal assigned to the U-, V-, and W-phases. As shown in Figure 13-7, the FG pin is internally pulled down to the COM pin.

Use the IS1 pin to set the number of rotation pulses to be output from the FG pin (see Table 11-1). The IC outputs a rotation signal equivalent to an 8-pole DC motor operation even in the operation where a 10-pole DC motor is connected. This enables your application to use an existing 8-pole DC motor system for 10-pole DC motor driving with no change. Equation (1) defines the number of signals per motor rotation.

$$N = \frac{1}{2} \times Pole \times ppr \,. \qquad (1)$$

Where:

N is the number of signals per motor rotation (pulse),
Pole is the number of poles (pole), and
T is the rotation pulse periods per electrical angle of 360° (ppr).

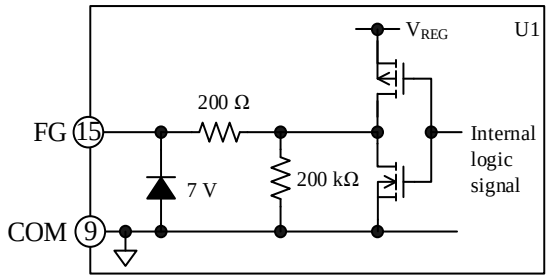


Figure 13-7. Internal Circuit Diagram of FG Pin

13.1.9 VSP

The IC controls the speed of motor rotation with an

analog voltage applied to the VSP pin. For more details on the motor speed control, see Section 13.5.

13.1.10 OCP

This pin serves as the input of the overcurrent protection (OCP) which monitors the currents flowing through the output transistors. The IC determines which of the overcurrent limit (OCL) and overcurrent protection (OCP) functions to activate according to the level of a voltage applied to the OCP pin. Section 13.7.3 provides further information about the OCP circuit configuration and its mechanism.

13.1.11 VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the power MOSFET drains of the high-side are connected to this pin. Voltages between the VBB and COM pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

13.1.12 VB1, VB2, and VB3

The VB1, VB2, and VB3 pins are connected to bootstrap capacitors, C_{Bx}, for the high-side floating supply. For proper startup, turn on the low-side transistors first, then fully charge the bootstrap capacitors, C_{Bx}.

For the capacitance of the bootstrap capacitors, C_{Bx}, choose the values that satisfy Equations (2) and (3). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{Bx}.

$$C_{Bx}(\mu F) > 800 \times t_{L(OFF)} \quad (2)$$

$$1\ \mu F \leq C_{Bx} \leq 220\ \mu F \quad (3)$$

In Equation (2), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{Bx}), measured in seconds.

Even while the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 13.7.2.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 13-8 shows, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are internally placed in series between the VCCx and VBx pins. Time constant for the charging time of C_{Bx}, τ, can be computed by Equation (4):

$$\tau = C_{Bx} \times R_{BOOTx}, \quad (4)$$

where C_{Bx} is the optimized capacitance of the bootstrap capacitor, and R_{BOOTx} is the resistance of the current-limiting resistor (60 Ω ± 20%).

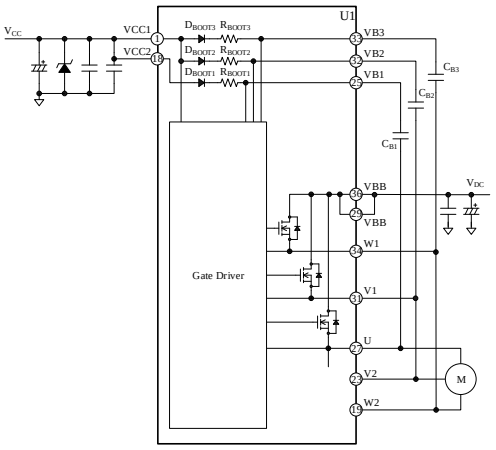


Figure 13-8. Bootstrap Circuit

Section 13.2 describes the startup sequences of the IC in detail; Section 13.3 explains the procedures to charge the bootstrap capacitors.

C_{Bx} of about 1 µF must be placed near the IC, and connected between the VBx and output (U, V1, W1) pins with a minimal length of trances.

Care must be taken not to apply negative potentials between the VBx and COM pins because it may cause permanent damage to the IC.

13.1.13 U, V1, V2, W1, and W2

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The V1 and W1 pins must be connected to the V2 and W2 pins on a PCB, respectively. The U, V, and W1 pins are the grounds for the VB1, VB2, and VB3 pins. The U, V1, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{Bx}. Since high voltages are applied to these output pins (U, V1, V2, W1, W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

13.1.14 LS1, LS2, and LS3

The LS1, LS2, and LS3 pins are internally connected to the low-side power MOSFET sources of the U-, V-, and W-phases, respectively. The LSx pin should be connected to an external shunt resistor, R_S, on a PCB. When connecting the shunt resistor, use the resistor with low inductance (required), and place it as near as possible to the IC with a minimum length of traces to the LSx and COM pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_S, between the LSx and COM pins in order to prevent the IC from malfunctioning.

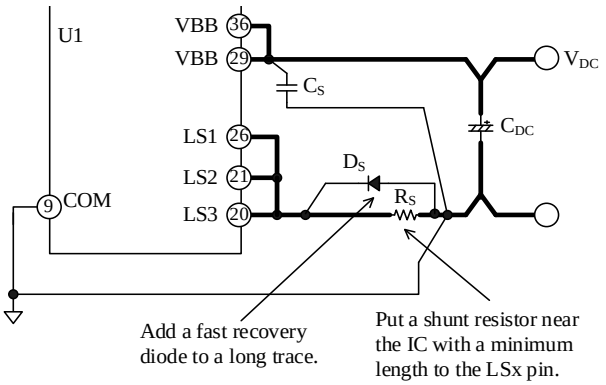


Figure 13-9. Connections to LSx Pin

13.2 Startup and Stop Operations

For audible noise suppression, the IC employs two different motor driving strategies: the sinusoidal control for startup operation and the ramp-down control for stop operation to gradually decrease a current value.

When the VCCx pin voltage reaches $V_{CC(ON)}$ = 11.5 V, the IC starts operating. At this time, the IC detects all information about the IS1 to IS3 pin settings and reflects the information to the motor driving control. The IC identifies a motor rotation state from position sensing signals detected by the HxP and HxN pins. Then, according to the IS1 to IS3 pin settings, the IC generates a sine-wave signal to rotate the motor (forced commutation, open-loop). In addition, the IC can change a current value at forced commutation (i.e., torque level) which is optimal for your application (with the IS3 pin settings).

The IC then waits for the VSP pin voltage to reach a certain level at which output duty cycles are controllable. At startup, the IC operates according to the VSP pin voltage levels as follows:

- **V_{SP} < 1.0 V**
  All the output signals are off.
- **1.0 V ≤ V_{SP} < 2.1 V**
  The IC starts charging bootstrap capacitors. For more details, see Section 13.3.
- **2.1 V ≤ V_{SP} ≤ 5.4 V**
  The IC controls its output duty cycles according to the VSP pin voltage levels. Regardless of the IS1 pin settings, the standby function is disabled at startup.

Table 10-1 and Table 10-2 are truth tables for motor driving by the trapezoidal control in a forward or reverse rotation, respectively. Figure 12-1 to Figure 12-6 are timing charts showing 10- and 8-pole DC motor operations.

When the IC detects a state in which the motor rotates inversely to the preset direction, the motor driving system is immediately switched to the trapezoidal control before a rotation of 60° electrical angle completes. For detailed descriptions on the reverse rotation detection, see Section 13.7.6.

The following are the important considerations for appropriate power startup and shutdown sequences.

- To turn on the IC, be sure to increase the VSP pin voltage last. To turn off the IC, be sure to decrease the VSP pin voltage first.
- The IC has a hysteresis for the output duty cycle control start voltage (2.1 V ≤ V_{SP}). To restart the IC, decrease the VSP pin voltage to ≤ 1.9 V.
- When you have enabled the motor lock protection by the IS3 pin, be sure to apply a voltage to the VBB pin at the timing described below. At startup, apply a voltage to the VCCx pin and the VREG pin voltage, VREG, increases. Then, apply a main supply voltage to the VBB pin within the period from VREG increase to an MLP detection time, t_{LD}. When a position sensing signal stays unchanged even after a lapse of t_{LD}, the IC determines this condition as a motor lockup state and activates the motor lock protection (see Section 13.7.5).

13.3 Charging of Bootstrap Capacitors

It is required to fully charge bootstrap capacitors, C_{Bx}, at startup. The charging sequence depends on the VSP pin voltage, V_{SP}. When 1.0 V ≤ V_{SP} ≤ 2.1 V at startup, the IC turns on the low-side power MOSFETs at every PWM cycle in order to charge C_{Bx}. When V_{SP} ≥ 2.1 V, the IC controls the motor speed according to the VSP pin voltage levels (see Section 13.5). However, note that the IC does not charge C_{Bx} even when 1.0 V ≤ V_{SP} ≤ 2.1 V along with the motor rotating inversely to the preset direction, or the motor coasting at a frequency of ≥0.25 Hz. If a sudden rise in the VSP pin voltage up to 2.1 V or more occurs at startup, the IC starts the motor speed control after charging C_{Bx} for a period of 1 ms ± 5%.

13.4 Standby Function

The IC has the standby function. When the VSP pin voltage decreases to 0.7 V or less and the Hall element input cycle becomes 0.25 Hz, the IC shifts to the standby mode. During the standby operation, the IC stops oscillating to minimize power consumed by the IC. When the VSP pin voltage increases to 1.0 V or more, the IC releases the standby mode and shifts back to its normal operation.

Set the IS1 pin to enable or disable the standby function (see Table 11-1). For stable startup operation, the standby function is disabled during the IC startup regardless of the setting value of the VSP pin voltage.

13.5 Motor Speed Control

The IC controls the speed of motor rotation with an analog voltage applied to the VSP pin. When 2.1 V ≤ V_{SP} ≤ 5.4 V, the IC controls its output duty cycles depending on the VSP pin voltage levels. For the IC operation when V_{SP} < 2.1 V (i.e., the startup sequence), see Section 13.2.

A duty cycle of an output signal is determined according to a digital signal that is generated by the built-in AD converter from the VSP pin input voltage. The higher the VSP pin voltage increases, the higher the duty cycle becomes, thus causing the motor to rotate faster. When decelerating the motor, do not decrease V_{SP} rapidly to prevent an increase in phase current due to phase shift. Figure 13-10 depicts how a duty cycle varies according to the VSP pin voltage, V_{SP}. While V_{SP} maintains at 5.4 V or more, the IC controls its output signals at duty cycle = 100%.

Figure 13-11 is an internal circuit diagram describing the VSP pin and its peripheral circuit. A voltage to be applied on the VSP pin, V_{SPP}, must be set to <10 V, i.e., below the rated VSP pin input voltage. R_{SP} should have a resistance of about 100 Ω; C_{SP} should have a capacitance of about 0.1 μF.

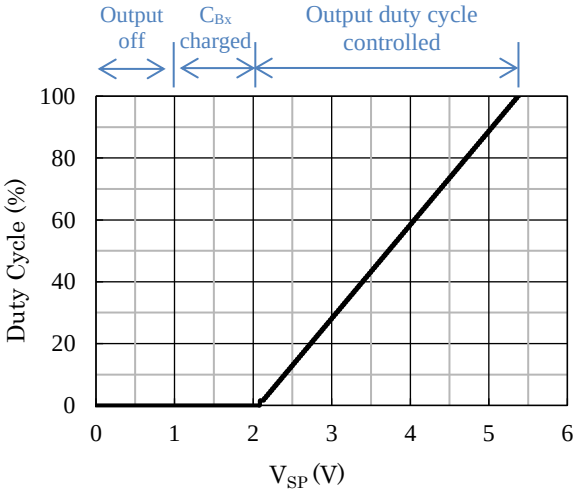


Figure 13-10. VSP Pin Voltage vs. Duty Cycle

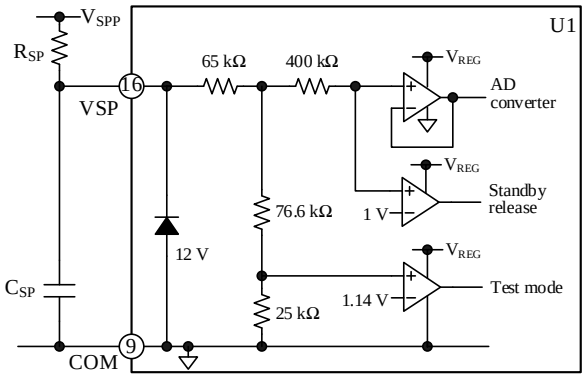


Figure 13-11. Internal Circuit Diagram of VSP Pin and Its Peripheral Circuit

13.6 Phase Advance Function

The IC features the phase advance function. The phase advance function has options allowing motor-appropriate settings: the external phase advance and the internal phase advance (with linear to cubic function operations). Use the IS2 pin to set the phase advance function (see Table 11-2).

13.6.1 External Phase Advance

When the external phase advance is selected, an analog voltage applied to the LA pin determines the phase advance angle. As shown in Figure 13-12, the VREG pin voltage divided by two resistors, R_{LA1} and R_{LA2}, is applied to the LA pin. Figure 13-13 plots how a phase advance angle changes over the LA pin voltage. Once the phase advance angle is set, each phase shifts ±0.46875° every 4 cycles of a Hall signal to the preset angle. The phase advance angle should range from 0° to 59.53125°

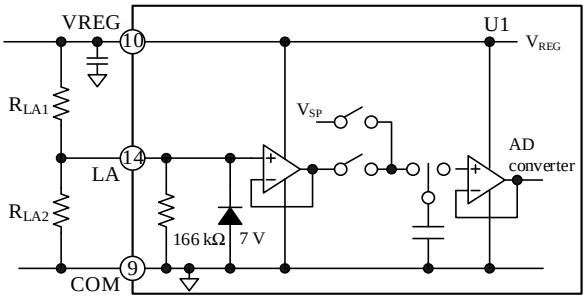


Figure 13-12. Internal Circuit Diagram of LA Pin and Its Peripheral Circuit

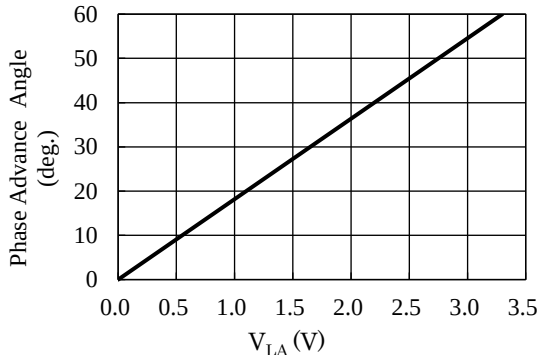


Figure 13-13. LA Pin Voltage vs. Phase Advance Angle

13.6.2 Internal Phase Advance

When the internal phase advance is selected, a phase advance angle is calculated based on the motor rotation speed (i.e., the VSP pin voltage, V_{SP}). The built-in AD converter reads the value of V_{SP} every 50 µs and calculates a value of the phase advance angle in each case. The calculated phase advance angle is stored in the internal register as a target value at the timing of the V_{SP} value reading. The IC then compares an actual phase advance angle with the stored target value every mechanical angle of 360°. And PWM signals shift through 0.4687° until the actual value reaches the target value.

There are three functions available to calculate values for the internal phase advance: linear function, quadratic function, and cubic function. For the linear and quadratic functions, you can select the upper limit of the phase advance angle. Additionally, coefficients applied to these calculations are adjustable by the angle, LA_{IN} corresponding to the LA pin voltage.

Below are the equations applied to individual function operations.

- **Cubic Function Operation**

Note that which equation to apply depends on the value of V_{SP}. The following equations determine the phase advance angle, LA. The phase advance angle should range from 0° to 58°.

When 2.1 V ≤ V_{SP} ≤ 3.75 V:

$$LA = a \times (V_{SP} - 2.1)^2 \quad . \tag{5}$$

When 3.75 V < V_{SP} ≤ 5.4 V:

$$LA = LA_{IN} - a \times \left(3.3 - (V_{SP} - 2.1)\right)^2 \quad . \tag{6}$$

Where:
LA is the phase advance angle (°),
V_{SP} is the VSP pin voltage (V),
LA_{IN} is the angle corresponding to the LA pin voltage (°), and
a is the coefficient (see the equation below).

$$a = \frac{LA_{IN}}{2 \times 1.65^2} . \tag{7}$$

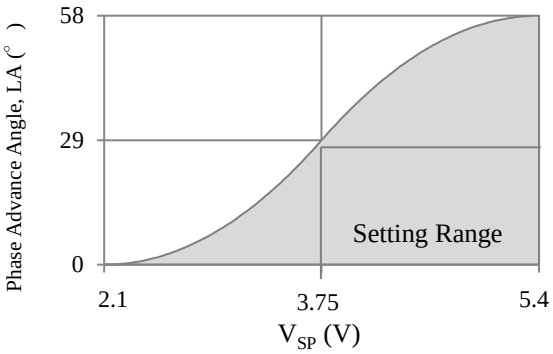


Figure 13-14. Cubic Function Characteristics

- **Quadratic Function Operation**

When 2.1 V ≤ V_{SP} ≤ 5.4 V, the phase advance angle, LA, is calculated by Equation (8):

$$LA = a \times (V_{SP} - 2.1)^2 \quad . \tag{8}$$

Where:
LA is the phase advance angle (°),
V_{SP} is the VSP pin voltage (V),
a is the coefficient (see the equation below).

$$a = \frac{LA_{IN}}{1.65^2}, \tag{9}$$

letting LA_{IN} be the angle corresponding to the LA pin voltage (°).

When the quadratic function is applied to the internal phase advance, you can select the upper limit of the phase advance angle (29°, 41°, 58°) by setting the IS2 pin. The quadratic function operation uses the soft-clip function that allows the phase advance angle to reach the upper limit selected. Table 13-1 shows the upper limit of the phase advance angle and the phase advance angle at which the soft-clip function operates.

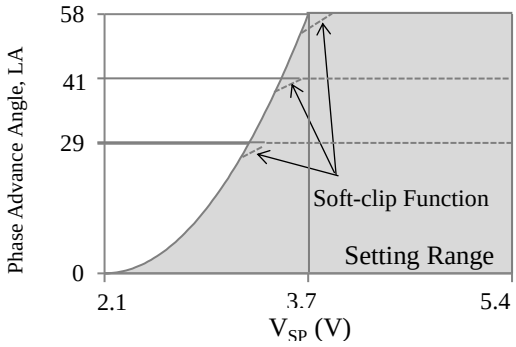


Figure 13-15. Quadratic Function Characteristics

Table 13-1. Soft-clip Function

Upper Limit of Phase Advance Angle	Phase Advance Angle at Which Soft-clip Function Operates
29°	24°
41°	35°
58°	49°

- **Linear Function Operation**

When 2.1 V ≤ V_{SP} ≤ 5.4 V, the phase advance angle, LA, is calculated by Equation (10):

$$LA = a \times (V_{SP} - 2.1) . \quad (10)$$

Where:
LA is the phase advance angle (°),
V_{SP} is the VSP pin voltage (V),
a is the coefficient (see the equation below).

$$a = \frac{LA_{IN}}{1.65}, \quad (11)$$

letting LA_{IN} be the angle corresponding to the LA pin voltage (°).

When the linear function is applied to the internal phase advance, you can select the upper limit of the phase advance angle (29°, 41°, 58°) by setting the IS2 pin.

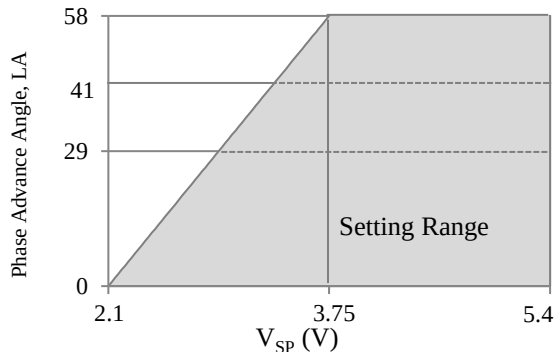


Figure 13-16. Linear Function Characteristics

13.7 Protection Functions

This section describes the various protection circuits provided in the SX6814xM series, such as those designed to detect a voltage drop across power supplies, an overcurrent condition, an abnormal motor state, and so on.

13.7.1 VREG Pin Undervoltage Lockout (UVLO_VREG)

When the VREG pin voltage decreases to V_{UVRL} = 2.48 V or less, the VREG pin undervoltage lockout (UVLO_VREG) circuit gets activated and turns off the high- and low-side power MOSFETs. When the VREG pin voltage increases to V_{UVRH} = 2.75 V or more, the IC releases the UVLO_VREG operation. Then, the high- and low-side power MOSFETs resume operating according to position sensing signals.

13.7.2 Undervoltage Lockout for Power Supplies (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SX6814xM series has the undervoltage lockout (UVLO) circuits for each of the high-side (the VBx pin) and the low-side (the VCC1 pin) power supplies.

13.7.2.1. VBx Pin (UVLO_VB)

When the voltage between the VBx and output (U, V1/V2, or W1/W2) pins (VBx–HSx) decreases to $V_{BS(OFF)}$ = 10.0 V or less, the UVLO_VB circuit gets activated and turns off the high-side power MOSFETs. When the voltage between the VBx and output pins increases to $V_{BS(ON)}$ = 10.5 V or more, the IC releases the UVLO_VB operation. Then, the high-side power MOSFETs resume operating according to position sensing signals.

13.7.2.2. VCC1 Pin (UVLO_VCC)

When the VCC1 pin voltage decreases to $V_{CC(OFF)}$ = 11.0 V or less, the UVLO_VCC circuit gets activated and turns off the high- and low-side power MOSFETs. When the VCC1 pin voltage increases to $V_{CC(ON)}$ = 11.5 V or more, the IC releases the UVLO_VCC operation. Then, the high- and low-side power MOSFETs resume operating according to position sensing signals.

13.7.3 Overcurrent Limit (OCL) and Overcurrent Protection (OCP)

The IC has two different protections against overcurrent conditions: the overcurrent limit (OCL) and the overcurrent protection (OCP).

Figure 13-17 is an internal circuit diagram describing the OCP pin and its peripheral circuit. The OCP pin detects overcurrents with voltage across an external shunt resistor, R_S. Because the OCP pin is internally pulled up, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S.

Note that overcurrents are undetectable when one or more of the U, V1/V2, and W1/W2 pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

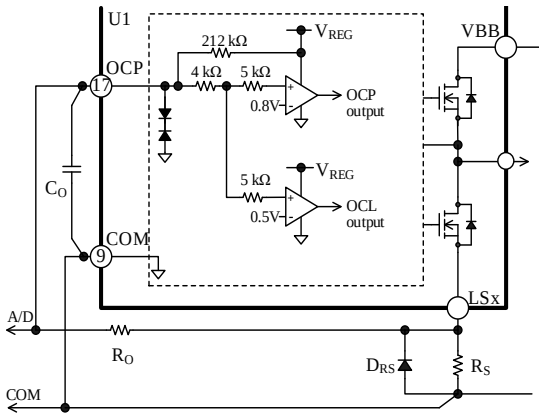


Figure 13-17. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

The overcurrent limit (OCL) is a protection against relatively low overcurrent conditions. When the OCP pin voltage increases to V_{LIM} = 0.50 V or more, and remains in this condition for a period of a blanking time ($t_{BK(OCL)}$ = 2.1 µs when OSCR = open) or longer, the IC turns off the high- and low-side power MOSFETs. The OCL operation is automatically released at each PWM cycle.

The overcurrent protection (OCP) is a protection against large inrush currents. When the OCP pin voltage increases to V_{TRIP} = 0.8 V or more, and remains in this condition for the blanking time or longer, the OCP circuit is activated. The blanking time depends on the OSCR pin setting. When OSCR = COM, $t_{BK(OCP)}$ = 1.5 µs. Then, the high- and low-side power MOSFETs are turned off for a certain period of time (t_P = 12.8 ms when OSCR = open). After that, the high- and low-side power MOSFETs resume operating according to position sensing signals.

In case the OCP circuit is activated 10 times in a row, the IC stops operating in a latched state. To release the latched state, turn off the power supply and decrease the VREG pin voltage to V_{UVRL} = 2.48 V or less.

The OCL and OCP are used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. For this reason, motor operations must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. If you need to resume the IC operation thereafter, set the IC to be resumed after a lapse of ≥2 seconds.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Set the OCP pin input voltage to vary within the rated input voltage 1, $V_{IN(1)}$ (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

13.7.4 Thermal Shutdown (TSD)

The SX6814xM series incorporates the thermal shutdown (TSD) circuit. In case of overheating (e.g., increased power dissipation due to overload, or elevated ambient temperature at the device), the IC shuts down the high- and low-side power MOSFETs.

The TSD circuit in the MIC for gate driver monitors temperatures (see Figure 5-1). When the junction temperature of the MIC for gate driver, $T_{J(DRV)}$, exceeds T_{DH} = 130 °C, the TSD circuit is activated. When $T_{J(DRV)}$ decreases to T_{DL} = 90 °C or less, the shutdown condition is released. The output transistors then resume operating according to input signals. Note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

13.7.5 Motor Lock Protection (MLP)

When the state in which a position sensing signal stays unchanged within a rotation of 60° electrical angle persists for a motor lock hold time (t_{LD} = 5.0 s when OSCR = COM) or longer, the motor lock protection (MLP) circuit gets activated. Then, the high- and low-side power MOSFETs are turned off for a certain period of time (t_{LH} = 30 s when OSCR = COM).

After that, the high- and low-side power MOSFETs resume operating according to position sensing signals.

In case the MLP circuit is activated 10 times in a row, the IC stops operating in a latched state.

Also, in case the OCL circuit is activated with the motor remaining locked even when the operations started

after a lapse of t_{LH}, the IC stops operating in a latched state.

To release the latched state, turn off the power supply and decrease the VREG pin voltage to V_{UVRL} = 2.48 V or less.

During the MLP operation, direct currents through one or more of the power MOSFETs raise their junction temperatures. Therefore, care must be taken not to allow the junction temperatures to exceed the absolute maximum rating.

13.7.6 Reverse Rotation Detection

This function switches the motor driving system to the trapezoidal control when the motor rotates in a direction opposite to the preset direction (see Table 13-2). When the IC detects a reverse rotation state during motor rotations, the motor driving system is immediately switched to the trapezoidal control before a rotation of 60° electrical angle completes.

Table 13-2. Motor Driving Controls during Reverse Rotation

IS3 Pin Settings	Motor Direction	Driving System
Reverse (CCW)	Forward	Trapezoidal
	Reverse	Sinusoidal
Forward (CW)	Forward	Sinusoidal
	Reverse	Trapezoidal

13.7.7 Hall Signal Abnormality Detection

As Figure 3-1 shows, signals from the external Hall elements are input into the corresponding comparators. The IC then receives the comparator outputs as the motor positional information, i.e., position sensing signals.

When all the position sensing signals (HU, HV, HW) are either in a high or low state, the Hall signal abnormality detection function gets activated and turns off the high- and low-side power MOSFETs. When the IC detects input states other than those above, each of the high- and low-side power MOSFETs responds in accordance with the input logic levels of the position sensing signals. For the truth tables for the position sensing signals and the output transistors, see Table 10-1 and Table 10-2.

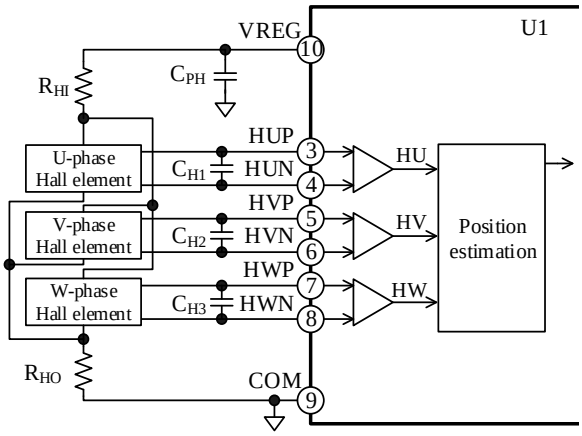


Figure 13-18. Internal Circuit Diagram of HxP and HxN Pins and Their Peripheral Circuit

14. Design Notes

14.1 PCB Pattern Layout

Figure 14-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

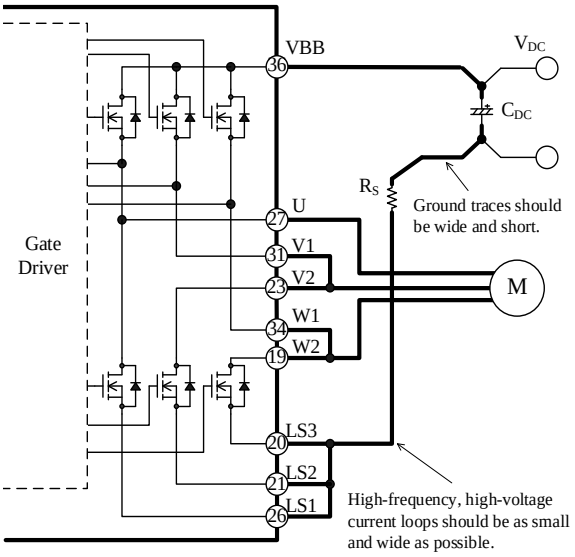


Figure 14-1. High-frequency, High-voltage Current Paths

14.2 Considerations in IC Characteristics Measurement

When measuring the leakage current of the output transistors (power MOSFETs) incorporated in the IC, note that all of the output (U, V1, V2, W1, W2), LSx, and COM pins must be appropriately connected. Otherwise, the output transistors may result in permanent damage. Also note that the gate and source of each output transistor should have the same potential during the leakage current measurement. Moreover, care should be taken during the measurement because each output transistor is connected as follows:

- All the high-side drains are internally connected to the VBB pin.
- In the U-phase, the high-side source and the low-side drain are internally connected to the U pin. (In the V- and W-phases, the high- and low-side transistors are unconnected inside the IC.)
- The high-side gates are internally pulled down to the output pins.
- The low-side gates are internally pulled down to the COM pin.

The following are circuit diagrams representing typical measurement circuits for leakage current: Figure 14-2 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 14-3 shows the low-side transistor (Q1L) in the U-phase. And all the pins that are not represented in these figures are open. When measuring the high-side transistors, leave all the non-measuring pins open. When measuring the low-side transistors, connect only the measuring LSx pin to the COM pin and leave the other pins open.

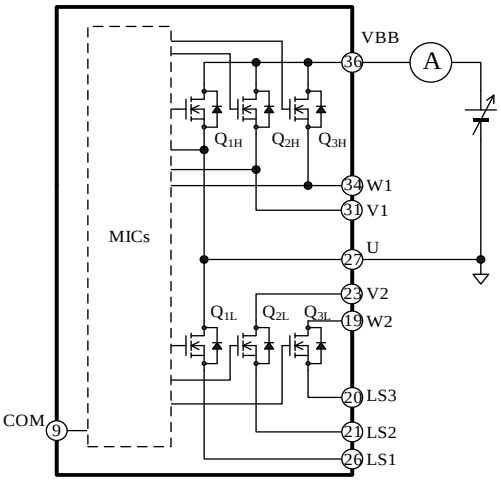


Figure 14-2. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

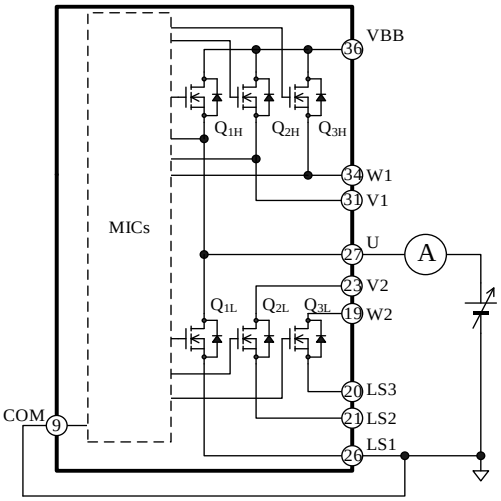


Figure 14-3. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

15. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in output transistors (power MOSFETs), and to estimate a junction temperature. Note that the descriptions listed here are applicable to the IC, which is controlled by a 3-phase sine-wave PWM driving strategy. For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0050: SX6814xM Series Calculation Tool
  https://www.semicon.sanken-ele.co.jp/en/calc-tool/mosfet_caltool_en.html

Total power loss in a power MOSFET can be obtained by taking the sum of the following losses: steady-state loss, P_{RON}; switching loss, P_{SW}; the steady-state loss of a body diode, P_{SD}. In the calculation procedure we offer, the recovery loss of a body diode, P_{RR}, is considered negligibly small compared with the ratios of other losses.

The following subsections contain the mathematical procedures to calculate these losses (P_{RON}, P_{SW}, and P_{SD}) and the junction temperature of all power MOSFETs operating.

15.1 Power MOSFET Steady-state Loss, P_{RON}

Steady-state loss in a power MOSFET can be computed by using the $R_{DS(ON)}$ vs. I_D curves, listed in Section 16.3.1. As expressed by the curves in Figure 15-1, a linear approximation at a range the I_D is actually used is obtained by: $R_{DS(ON)} = \alpha \times I_D + \beta$.

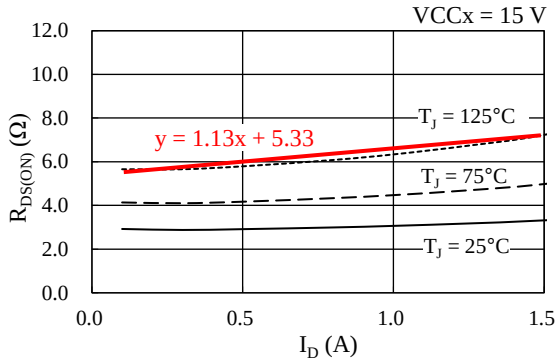


Figure 15-1. Linear Approximate Equation of $R_{DS(ON)}$ vs. I_D

The values gained by the above calculation are then applied as parameters in Equation (12), below. Hence, the equation to obtain the power MOSFET steady-state loss, P_{RON}, is:

$$P_{RON} = \frac{1}{2\pi}\int_0^{\pi} I_D(\varphi)^2 \times R_{DS(ON)}(\varphi) \times DT \times d\varphi$$

$$= 2\sqrt{2}\alpha\left(\frac{1}{3\pi} + \frac{3}{32}M \times \cos\theta\right){I_M}^3 + 2\beta\left(\frac{1}{8} + \frac{1}{3\pi}M \times \cos\theta\right){I_M}^2. \quad (12)$$

Where:

I_D is the drain current of the power MOSFET (A),

$R_{DS(ON)}$ is the drain-to-source on-resistance of the power MOSFET (Ω),

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current (A),

α is the slope of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve, and

β is the intercept of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve.

15.2 Power MOSFET Switching Loss, P_{SW}

Switching loss in a power MOSFET can be calculated by Equation (13) or (14), letting I_M be the effective current value of the motor:

- **SX68141M**

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{150}. \quad (13)$$

- **SX68140M / SX68144M / SX68145M**

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (14)$$

Where:

f_C is the PWM carrier frequency (Hz),

V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and

α_E is the slope on the switching loss curve (see Section 16.3.1.2).

15.3 Body Diode Steady-state Loss, P_{SD}

Steady-state loss in the body diode of a power MOSFET can be computed by using the V_{SD} vs. I_{SD} curves, listed in Section 16.3.1. As expressed by the curves in Figure 15-2, a linear approximation at a range the I_{SD} is actually used is obtained by: $V_{SD} = \alpha \times I_{SD} + \beta$.

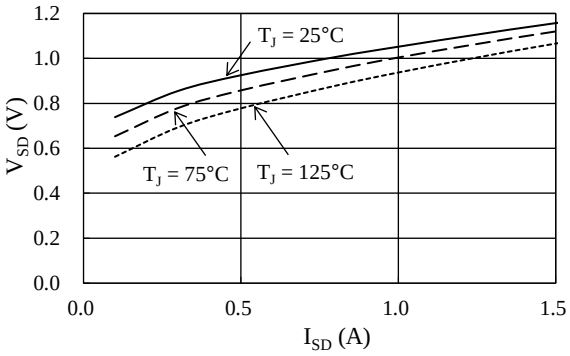


Figure 15-2. Linear Approximate Equation of V_{SD} vs. I_{SD}

The values gained by the above calculation are then applied as parameters in Equation (15), below. Hence, the equation to obtain the body diode steady-state loss, P_{SD}, is:

$$P_{SD} = \frac{1}{2\pi}\int_0^{\pi} V_{SD}(\varphi) \times I_{SD}(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right){I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right)I_M . \quad (15)$$

Where:

V_{SD} is the source-to-drain diode forward voltage of the power MOSFET (V),
I_{SD} is the source-to-drain diode forward current of the power MOSFET (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the V_{SD} vs. I_{SD} curve, and
β is the intercept of the linear approximation in the V_{SD} vs. I_{SD} curve.

15.4 Estimating Junction Temperature of Power MOSFET

The junction temperature of all power MOSFETs operating, T_J, can be estimated with Equation (16):

$$T_J = R_{J-C} \times \{(P_{RON} + P_{SW} + P_{SD}) \times 6\} + T_C . \quad (16)$$

R_{J-C} is the junction-to-case thermal resistance (°C/W) of all the power MOSFETs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

16. Performance Curves

16.1 Transient Thermal Resistance Curves

The following graph represents transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

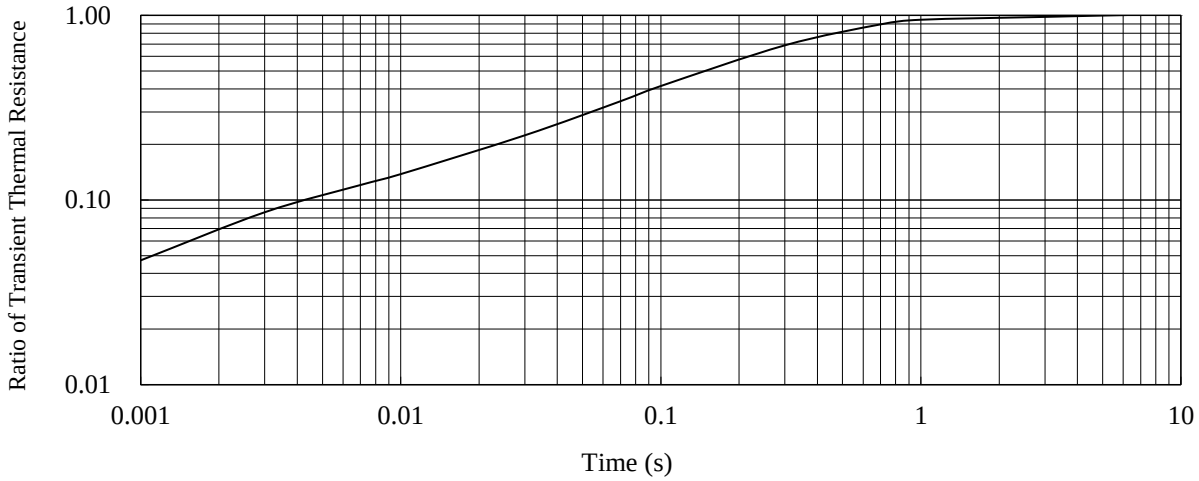


Figure 16-1. Transient Thermal Resistance

16.2 Performance Curves of Control Parts

Figure 16-2 to Figure 16-24 provide performance curves of the control parts integrated in the SX6814xM series, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 16-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 16-2	Logic Supply Current, I_{CC} vs. T_C (V_{SP} = 0 V)
Figure 16-3	Logic Supply Current, I_{CC} vs. T_C (V_{SP} = 5.4 V)
Figure 16-4	Logic Supply Current, $I_{CC(STBY)}$ vs. T_C (V_{SP} = 0 V)
Figure 16-5	Logic Supply Current, I_{CC} vs. Logic Supply Voltage, V_{CC}
Figure 16-6	Logic Supply Current, $I_{CC(STBY)}$ vs. Logic Supply Voltage, V_{CC}
Figure 16-7	Logic Supply Current in 1-phase Operation (V_{SP} = 0 V), I_{BS} vs. T_C
Figure 16-8	Logic Supply Current in 1-phase Operation (V_{SP} = 5.4 V), I_{BS} vs. T_C
Figure 16-9	IS1/IS2/IS3/LA Pin High Level Input Current, I_{IH1} vs. T_C
Figure 16-10	VSP Pin High Level Input Current, I_{IH1} vs. T_C
Figure 16-11	OCP Pin High Level Input Current, I_{IH2} vs. T_C
Figure 16-12	FG Pin High Level Output Voltage, V_{OH} vs. T_C
Figure 16-13	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 16-14	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 16-15	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 16-16	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 16-17	UVLO_VB Filtering Time vs. T_C
Figure 16-18	UVLO_VCC Filtering Time vs. T_C
Figure 16-19	Current Limit Reference Voltage, V_{LIM} vs. T_C
Figure 16-20	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 16-21	OCL Blanking Time, $t_{BK(OCL)}$ + Propagation Delay, t_D vs. T_C
Figure 16-22	OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, t_D vs. T_C
Figure 16-23	OCP Hold Time, t_P vs. T_C
Figure 16-24	VREG Pin Voltage, V_{REG} vs. T_C

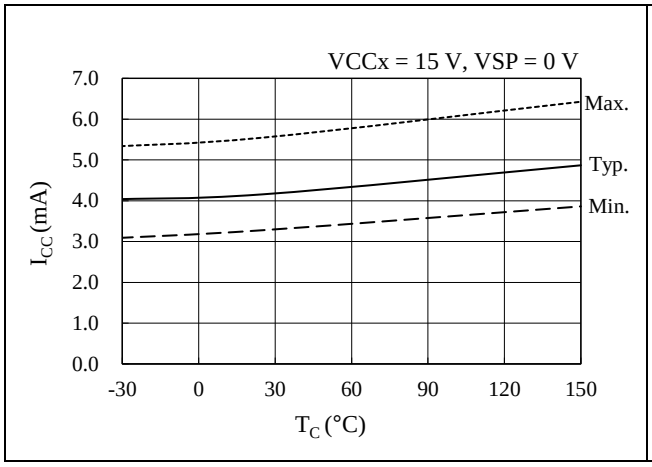


Figure 16-2. Logic Supply Current, I_{CC} vs. T_C (V_{SP} = 0 V)

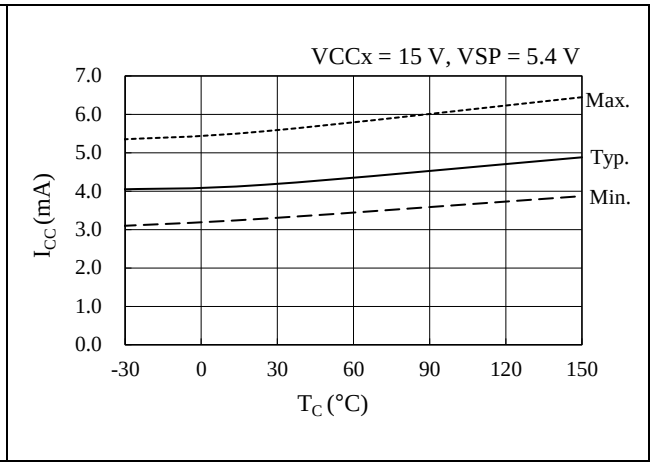


Figure 16-3. Logic Supply Current, I_{CC} vs. T_C (V_{SP} = 5.4 V)

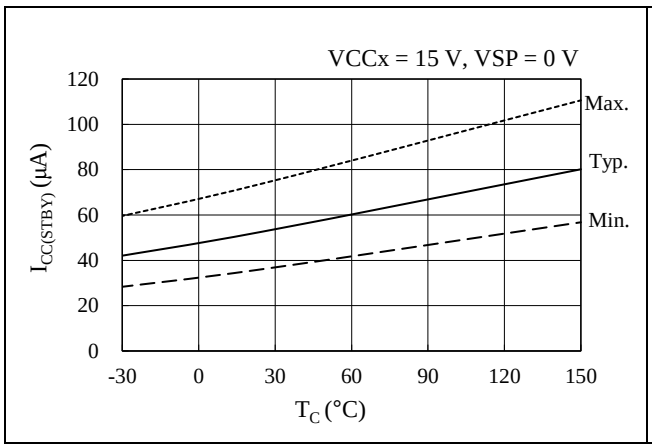


Figure 16-4. Logic Supply Current, $I_{CC(STBY)}$ vs. T_C (V_{SP} = 0 V)

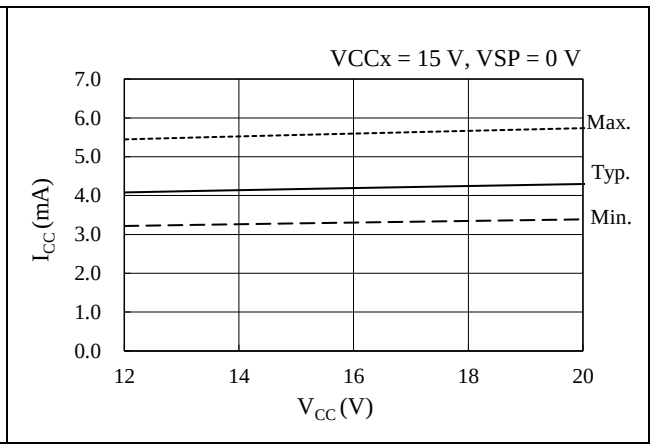


Figure 16-5. Logic Supply Current, I_{CC} vs. Logic Supply Voltage, V_{CC}

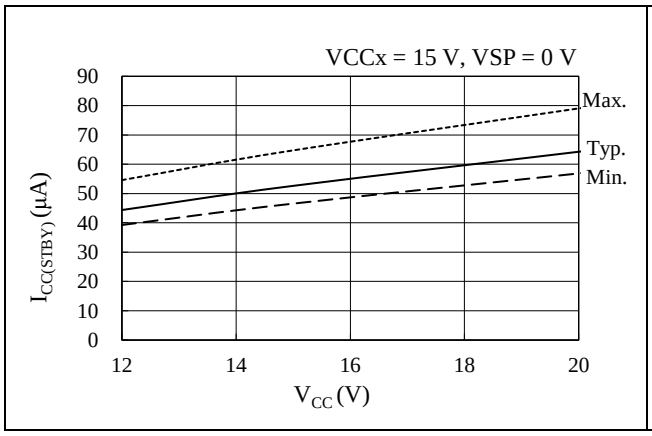


Figure 16-6. Logic Supply Current, $I_{CC(STBY)}$ vs. Logic Supply Voltage, V_{CC}

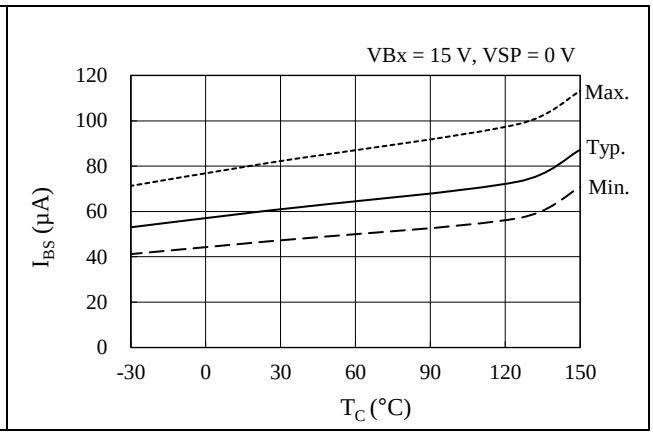


Figure 16-7. Logic Supply Current in 1-phase Operation (V_{SP} = 0 V), I_{BS} vs. T_C

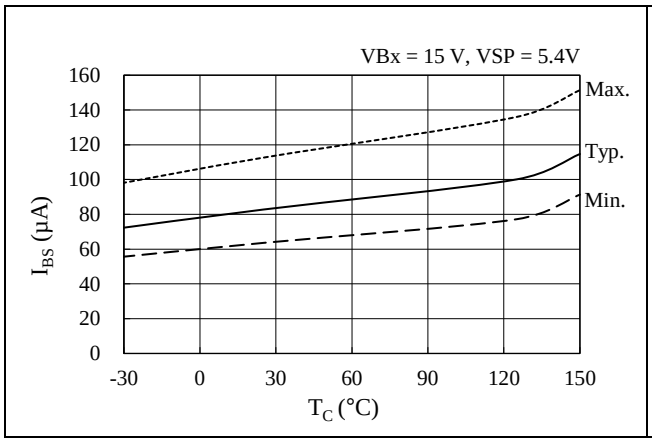


Figure 16-8. Logic Supply Current in 1-phase Operation (V_{SP} = 5.4 V), I_{BS} vs. T_C

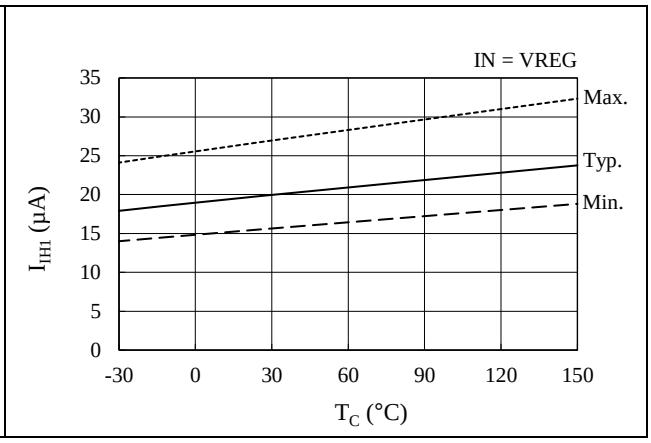


Figure 16-9. IS1/IS2/IS3/LA Pin High Level Input Current, I_{IH1} vs. T_C

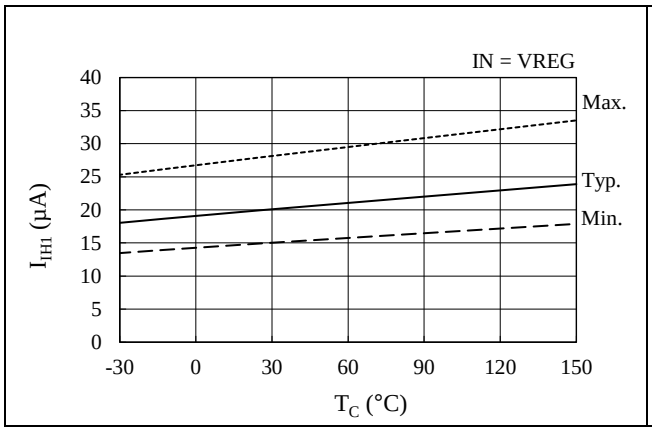


Figure 16-10. VSP Pin High Level Input Current, I_{IH1} vs. T_C

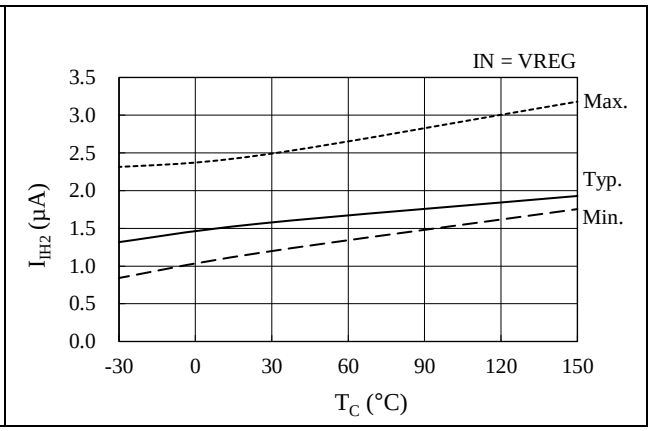


Figure 16-11. OCP Pin High Level Input Current, I_{IH2} vs. T_C

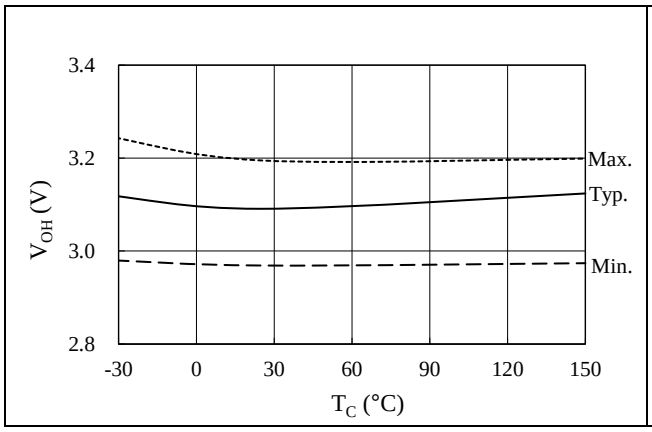


Figure 16-12. Pin High Level Output Voltage, V_{OH} vs. T_C

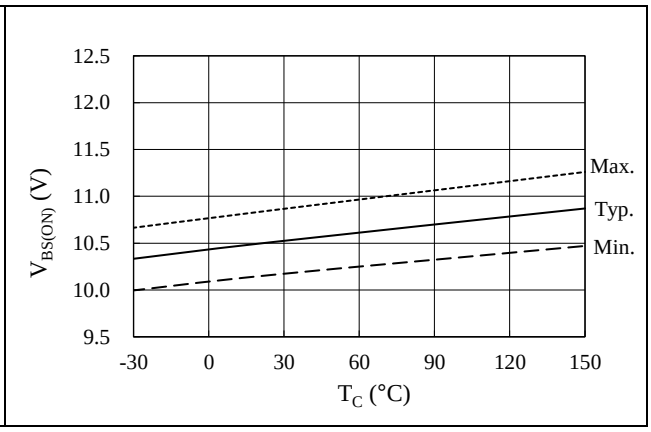


Figure 16-13. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

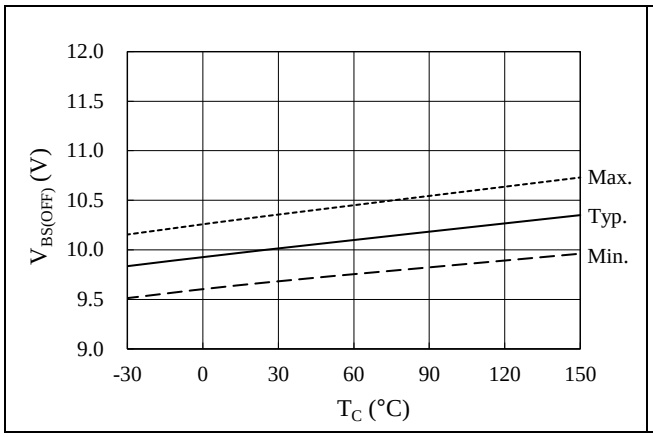


Figure 16-14. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

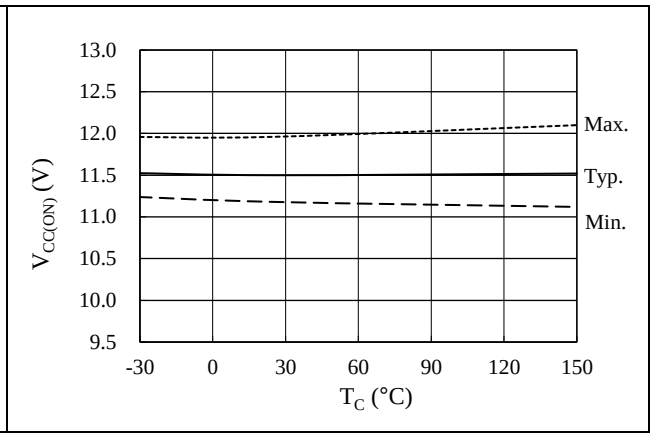


Figure 16-15. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

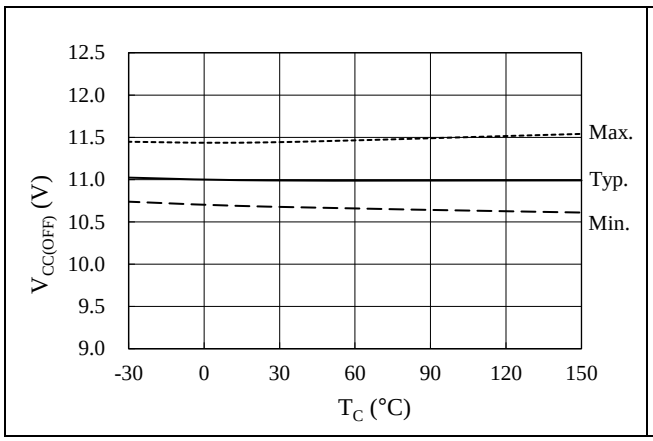


Figure 16-16. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

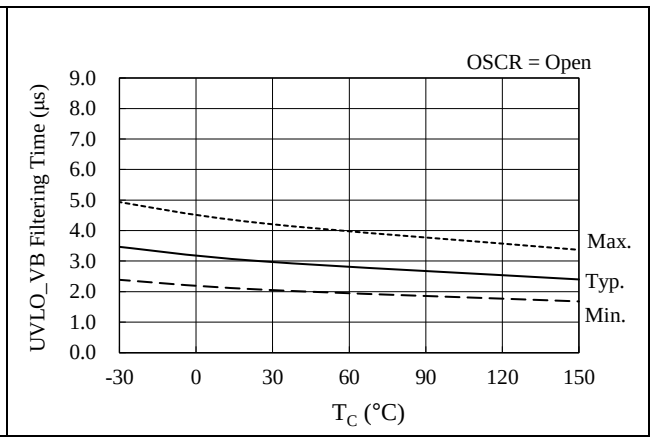


Figure 16-17. UVLO_VB Filtering Time vs. T_C

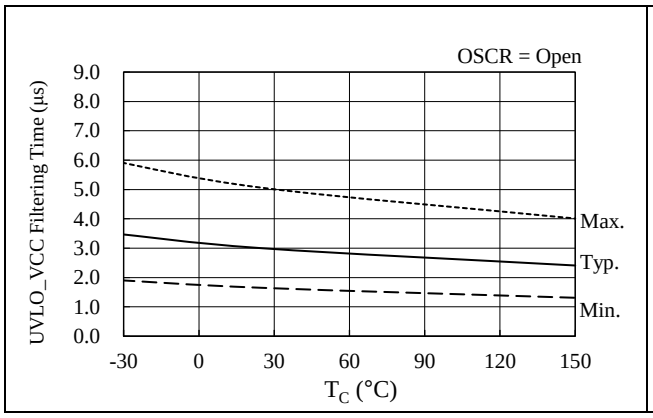


Figure 16-18. UVLO_VCC Filtering Time vs. T_C

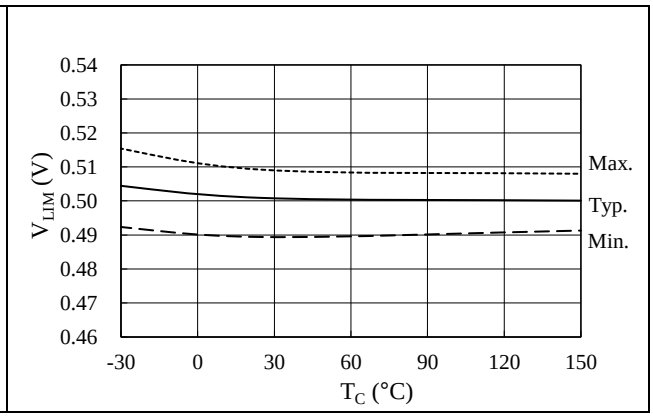


Figure 16-19. Current Limit Reference Voltage, V_{LIM} vs. T_C

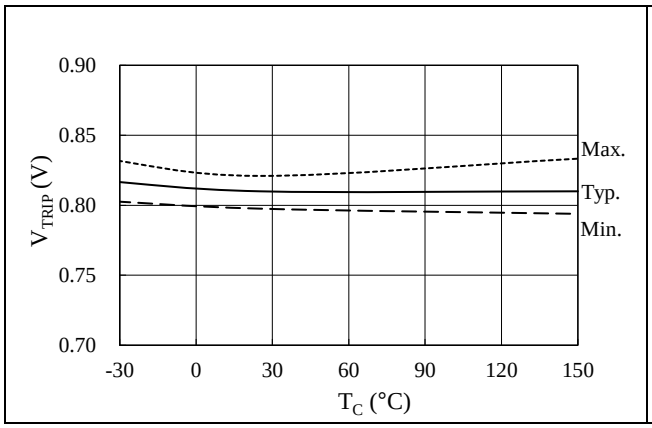


Figure 16-20. OCP Threshold Voltage, V_{TRIP} vs. T_C

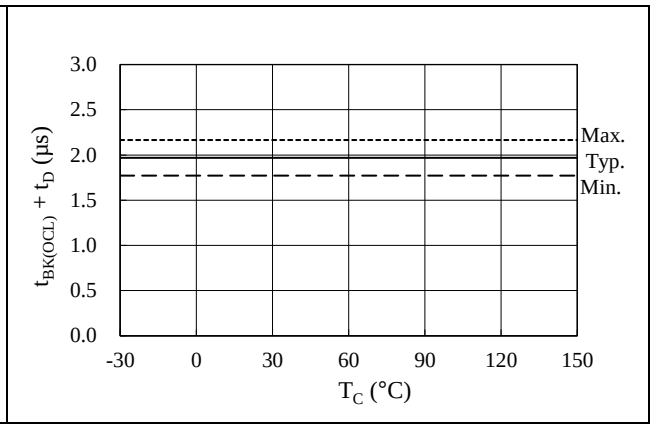


Figure 16-21. OCL Blanking Time, $t_{BK(OCL)}$ + Propagation Delay, t_D vs. T_C

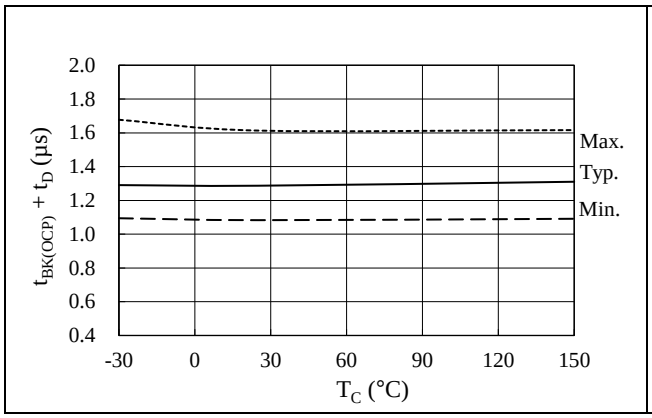


Figure 16-22. OCP Blanking Time, $t_{BK(OCP)}$ + Propagation Delay, t_D vs. T_C

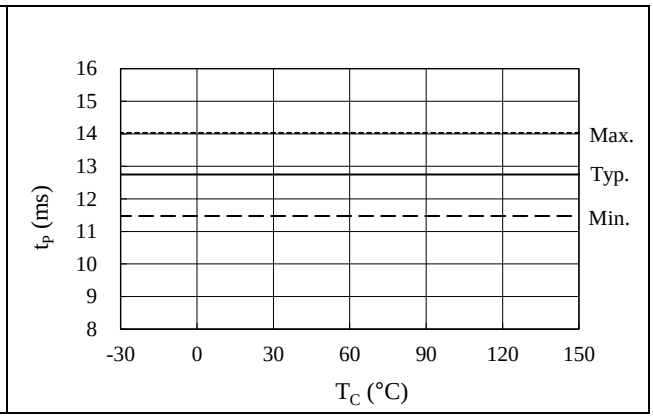


Figure 16-23. OCP Hold Time, t_P vs. T_C

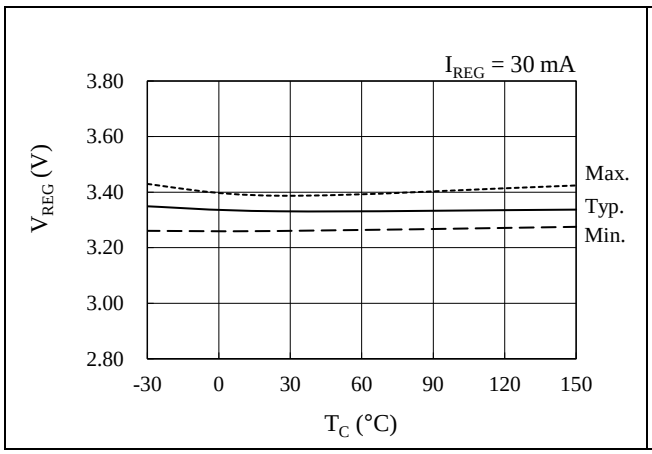


Figure 16-24. VREG Pin Voltage, V_{REG} vs. T_C

16.3 Performance Curves of Output Parts

16.3.1 Output Transistor Performance Curves

16.3.1.1. SX68140M

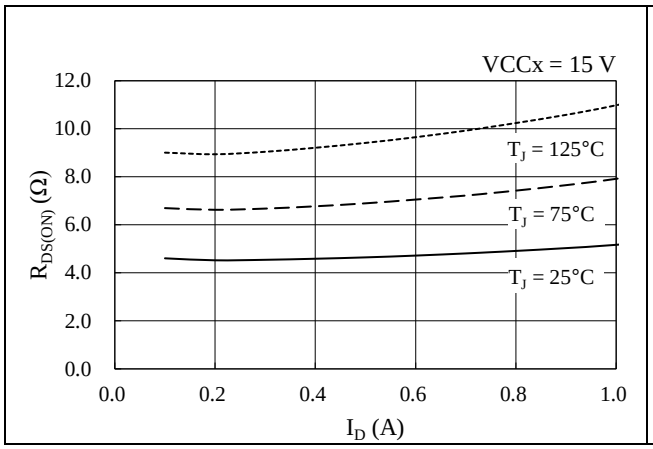


Figure 16-25. Power MOSFET $R_{DS(ON)}$ vs. I_D

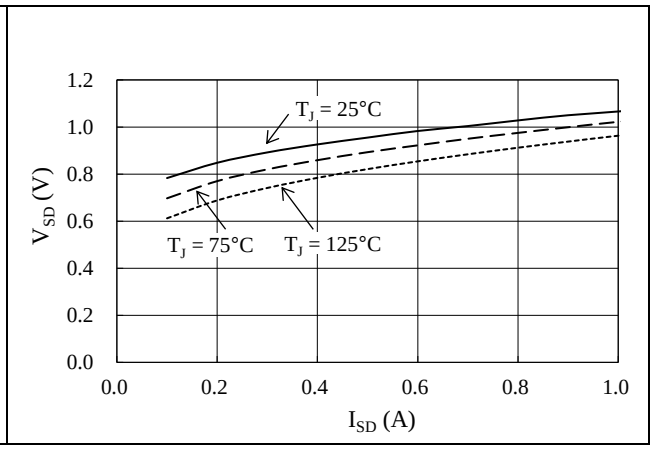


Figure 16-26. Power MOSFET V_{SD} vs. I_{SD}

16.3.1.2. SX68141M

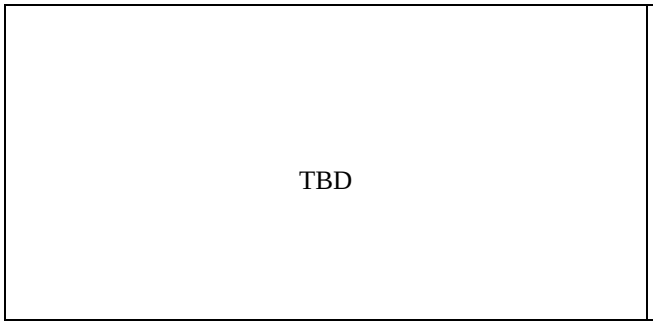


Figure 16-27. Power MOSFET $R_{DS(ON)}$ vs. I_D

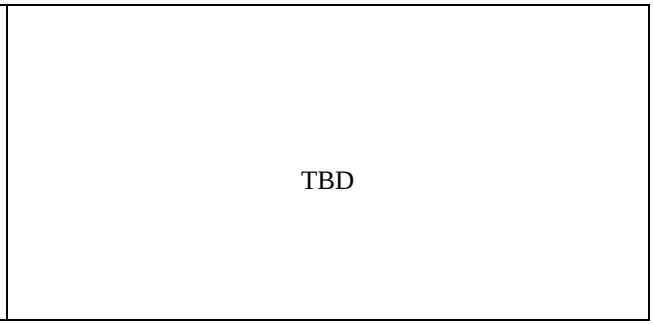


Figure 16-28. Power MOSFET V_{SD} vs. I_{SD}

16.3.1.3. SX68144M

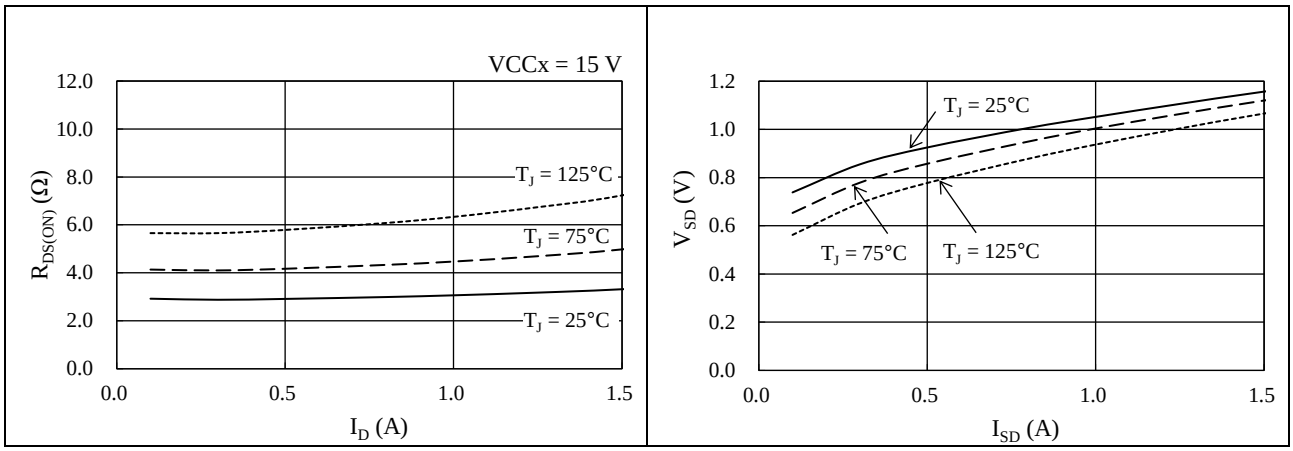


Figure 16-29. Power MOSFET $R_{DS(ON)}$ vs. I_D

Figure 16-30. Power MOSFET V_{SD} vs. I_{SD}

16.3.1.4. SX68145M

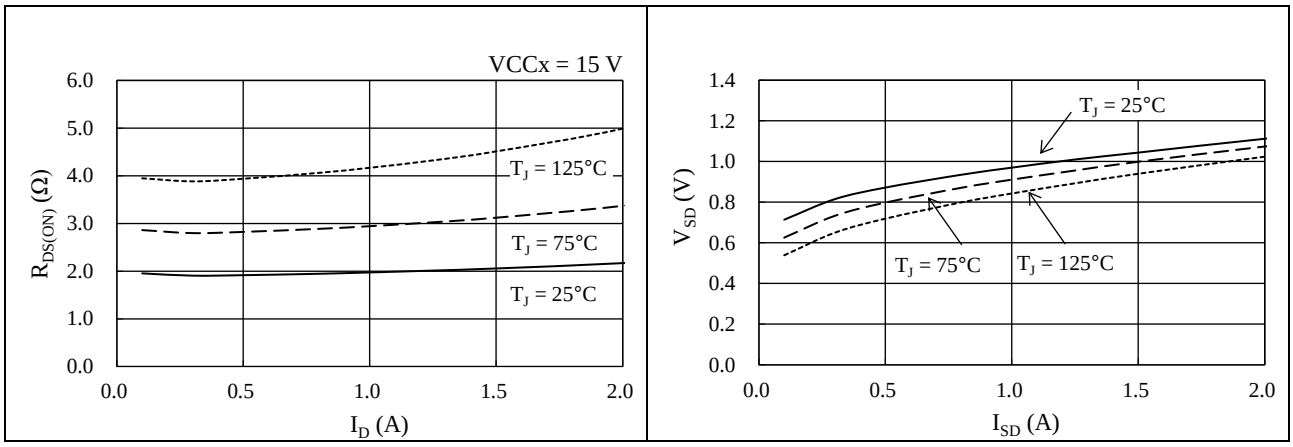


Figure 16-31. Power MOSFET $R_{DS(ON)}$ vs. I_D

Figure 16-32. Power MOSFET V_{SD} vs. I_{SD}

16.3.2 Switching Loss Curves

16.3.2.1. SX68140M

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

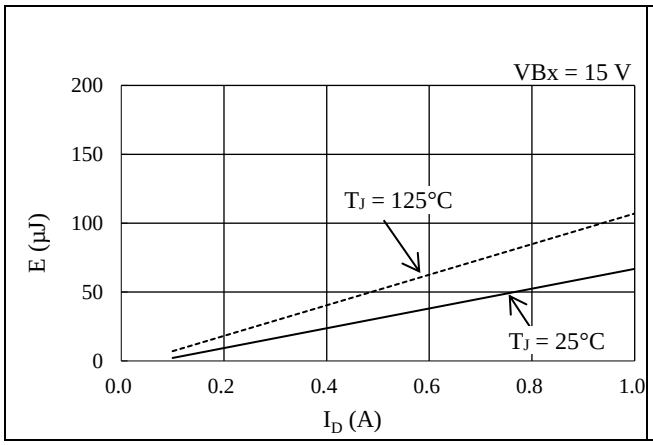


Figure 16-33. High-side Switching Loss

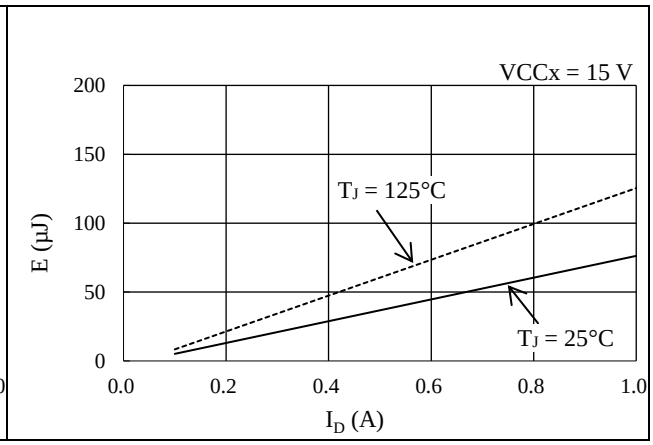


Figure 16-34. Low-side Switching Loss

16.3.2.2. SX68141M

Conditions: VBB pin voltage = 150 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

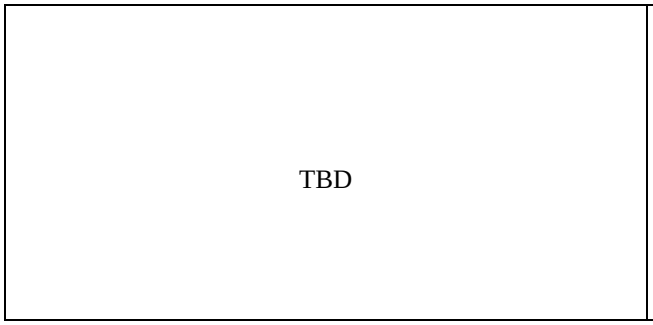


Figure 16-35. High-side Switching Loss

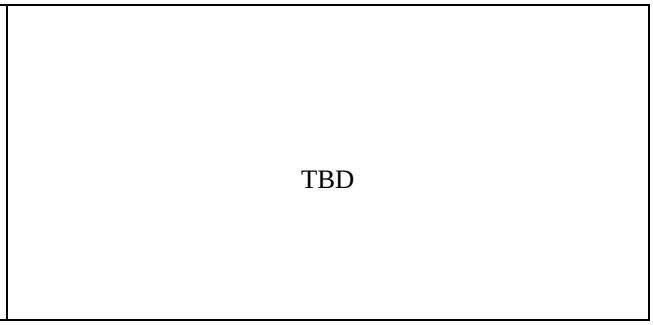


Figure 16-36. Low-side Switching Loss

16.3.2.3. SX68144M

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

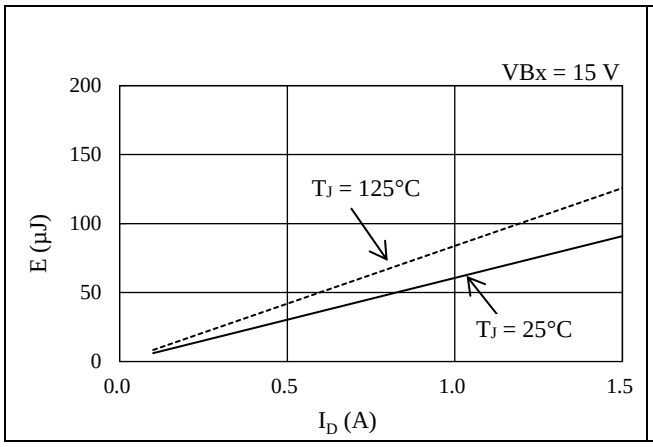


Figure 16-37. High-side Switching Loss

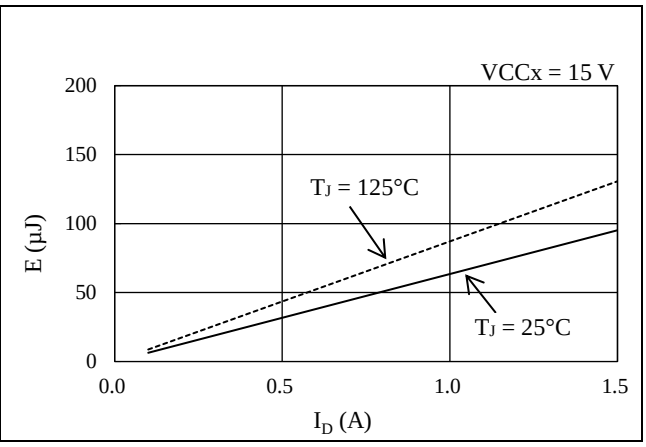


Figure 16-38. Low-side Switching Loss

16.3.2.4. SX68145M

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

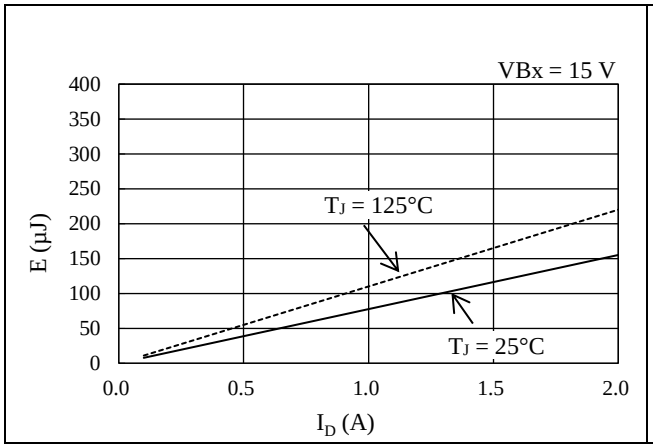


Figure 16-39. High-side Switching Loss

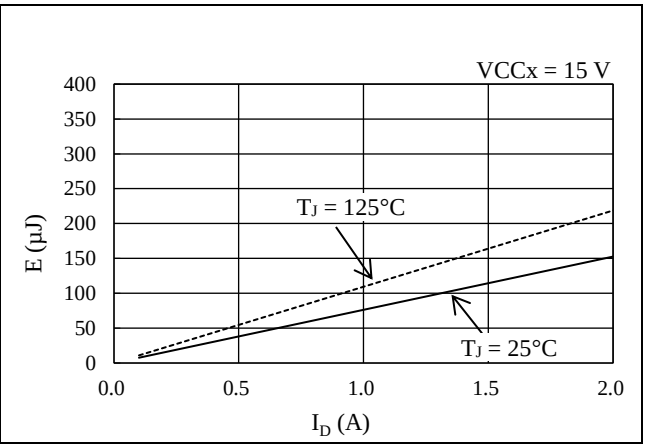


Figure 16-40. Low-side Switching Loss

16.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $R_{DS(ON)}$ or $V_{CE(SAT)}$, and typical switching losses.

16.5 SX68140M

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

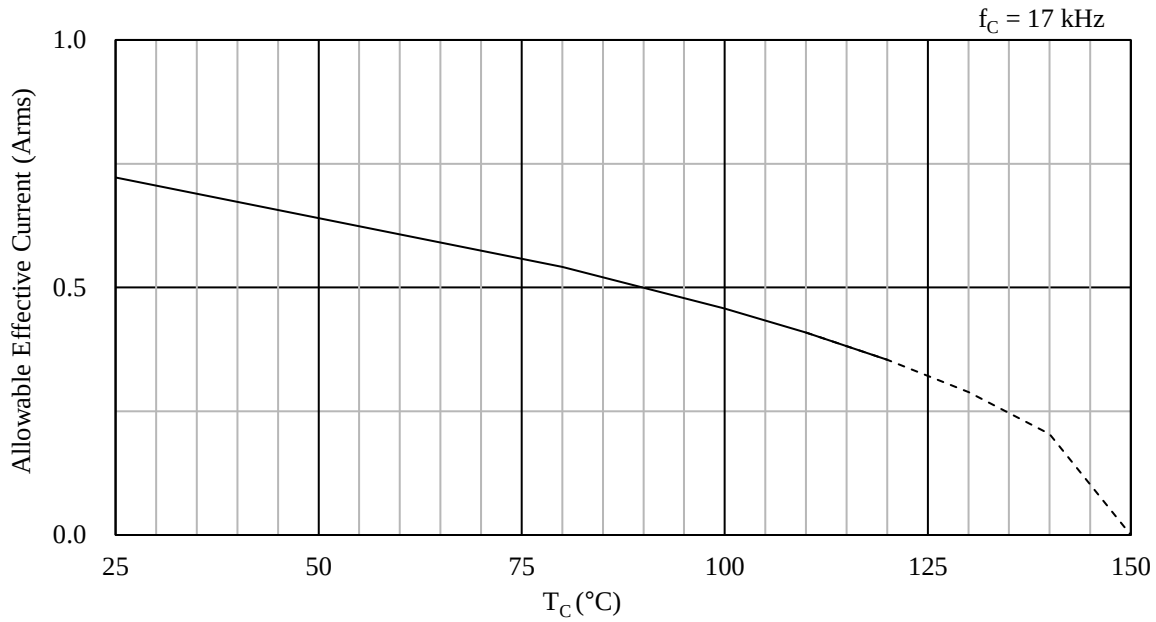


Figure 16-41. Allowable Effective Current (f_C = 17 kHz)

16.6 SX68141M

Operating conditions: VBB pin input voltage, V_{DC} = 150 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

TBD

Figure 16-42. Allowable Effective Current (f_C = 17 kHz)

16.7 SX68144M

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

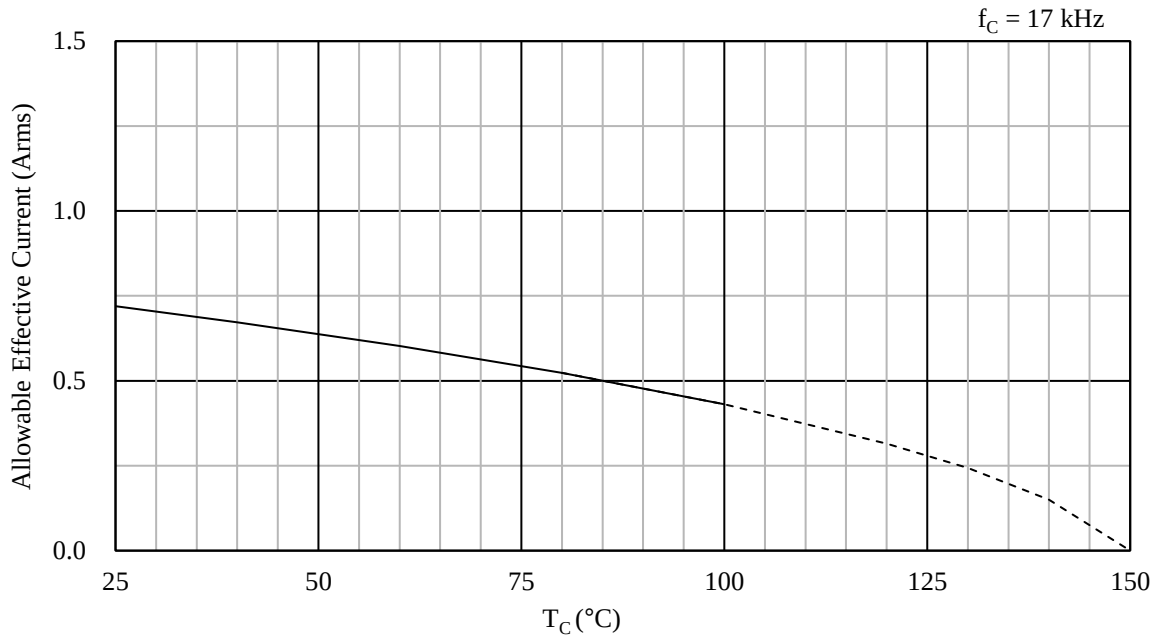


Figure 16-43. Allowable Effective Current (f_C = 17 kHz)

16.8 SX68145M

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

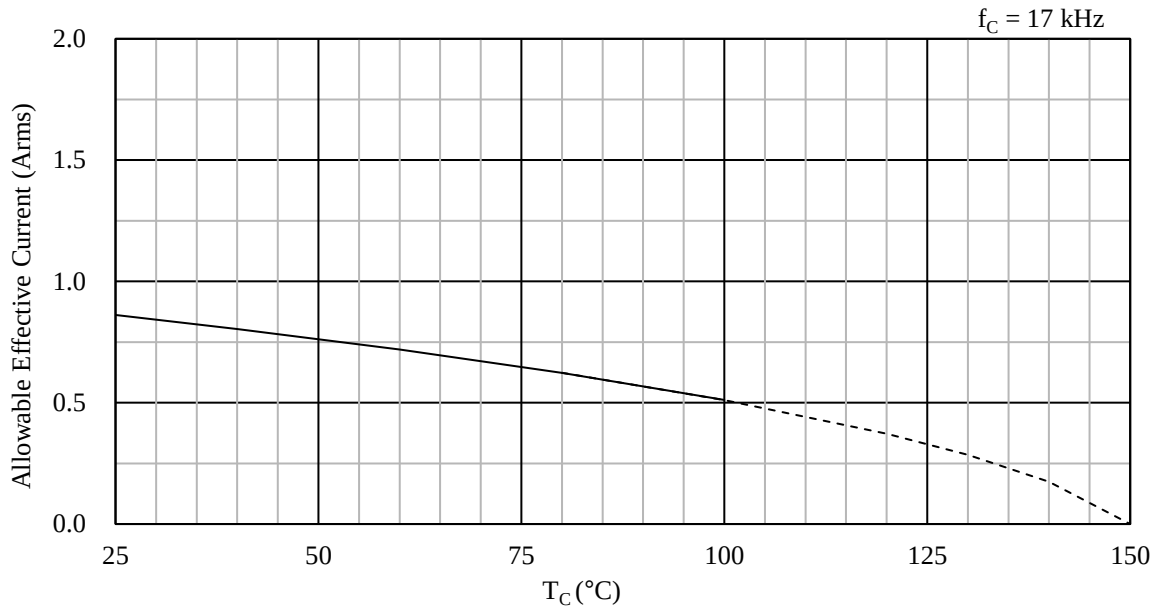
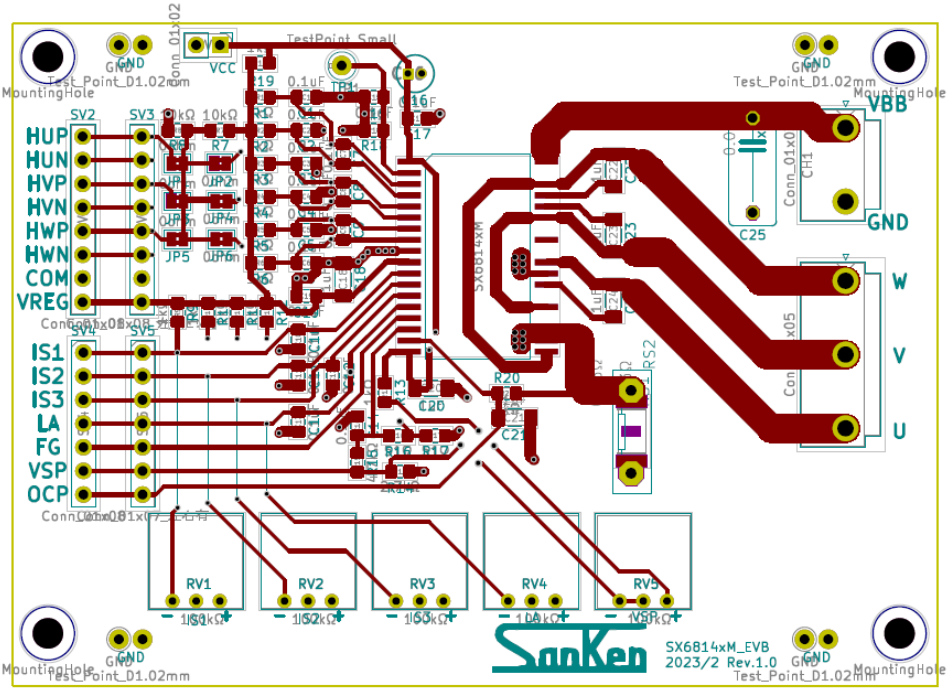


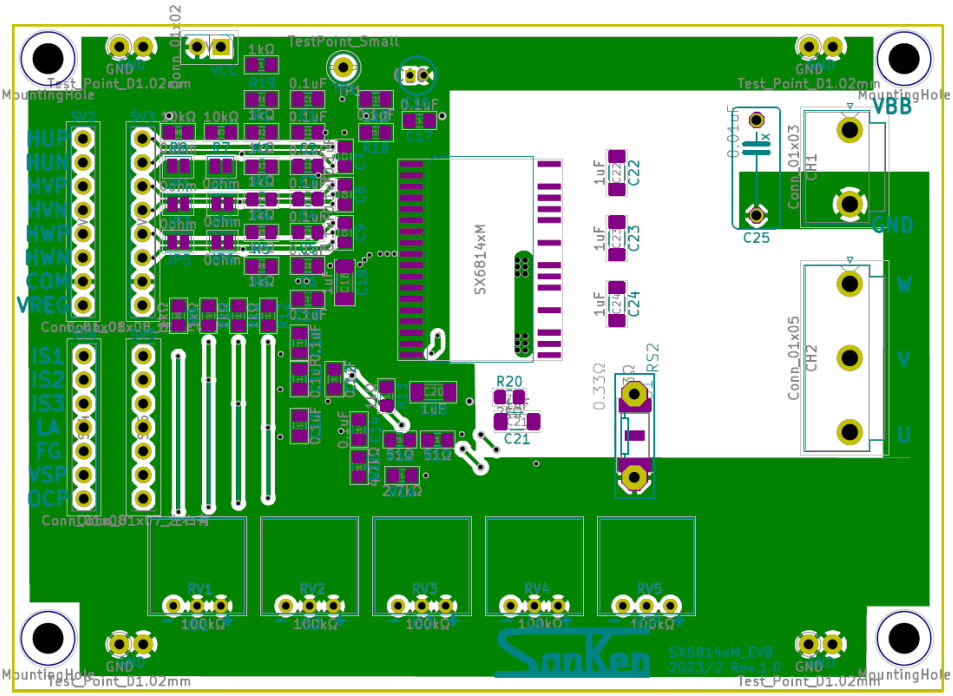
Figure 16-44. Allowable Effective Current (f_C = 17 kHz)

17. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SX6814xM series device. For details on the land pattern example of the IC, see Section 8.



(Top View)



(Bottom View)

Figure 17-1. Pattern Layout Example

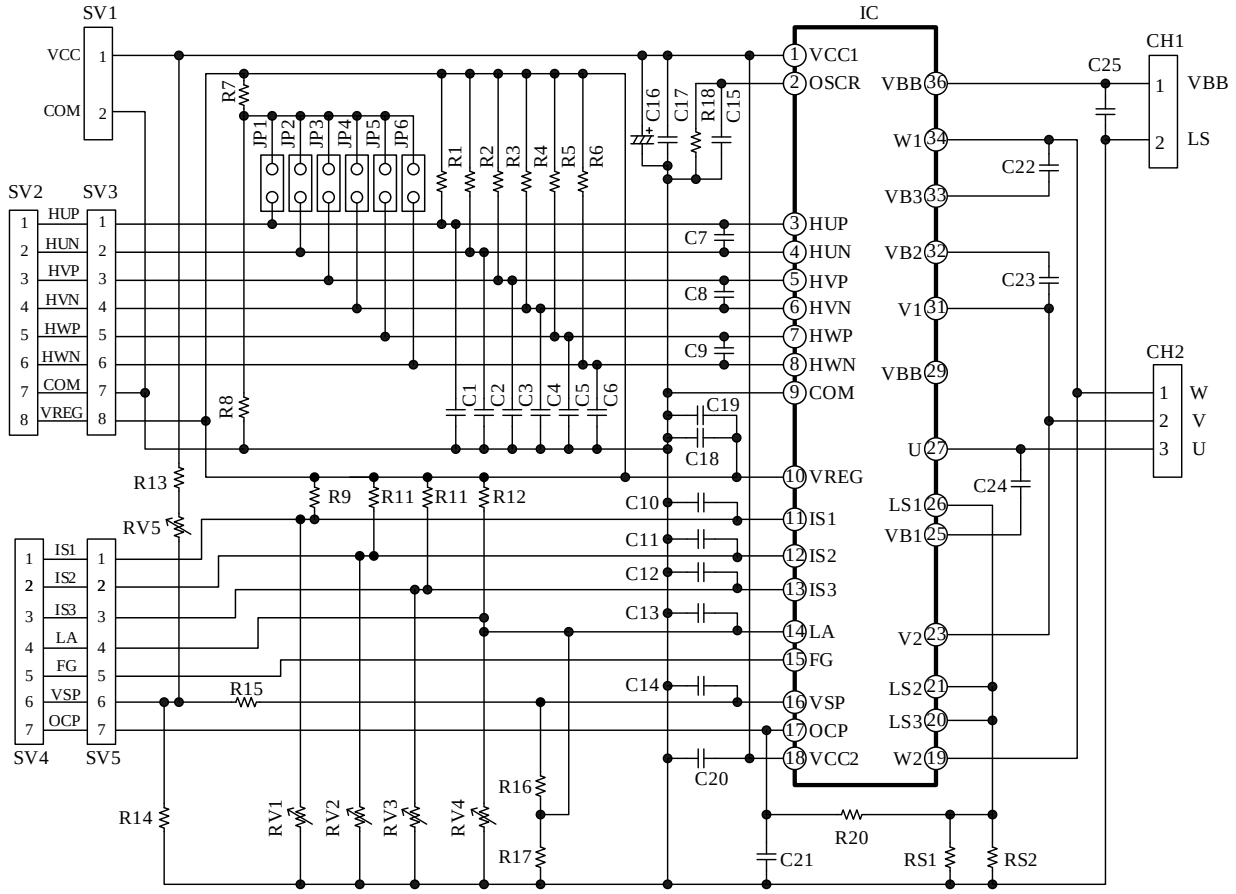


Figure 17-2. Circuit Diagram of PCB Pattern Layout Example

18. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SX68140M
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	50 W

- **Circuit Diagram**
  See Figure 17-2.

● **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Ceramic	0.1 µF, 35 V	R9	General	1 kΩ, 1/8 W
C2	Ceramic	0.1 µF, 35 V	R10	General	1 kΩ, 1/8 W
C3	Ceramic	0.1 µF, 35 V	R11	General	1 kΩ, 1/8 W
C4	Ceramic	0.1 µF, 35 V	R12	General	1 kΩ, 1/8 W
C5	Ceramic	0.1 µF, 35 V	R13	General	1 kΩ, 1/8 W
C6	Ceramic	0.1 µF, 35 V	R14	General	2.7 kΩ, 1/8 W
C7	Ceramic	0.1 µF, 35 V	R15	General	4.7 kΩ, 1/8 W
C8	Ceramic	0.1 µF, 35 V	R16	General	18 kΩ, 1/8 W
C9	Ceramic	0.1 µF, 35 V	R17	General	18 kΩ, 1/8 W
C10	Ceramic	0.1 µF, 35 V	R18(1)	General	Open
C11	Ceramic	0.1 µF, 35 V	R19	General	1 kΩ, 1/8 W
C12	Ceramic	0.1 µF, 35 V	R20	General	2 kΩ, 1/8 W
C13	Ceramic	0.1 µF, 35 V	RS1	Metal plate	See Section 2.
C14	Ceramic	0.1 µF, 35 V	RS2	Metal plate	See Section 2.
C15	Ceramic	0.1 µF, 35 V	RV1	Trimmer	100 kΩ, 0.5 W
C16	Electrolytic	1 µF, 50 V	RV2	Trimmer	100 kΩ, 0.5 W
C17	Ceramic	0.1 µF, 35 V	RV3	Trimmer	100 kΩ, 0.5 W
C18	Ceramic	1 µF, 35 V	RV4	Trimmer	100 kΩ, 0.5 W
C19	Ceramic	0.1 µF, 35 V	RV5	Trimmer	100 kΩ, 0.5 W
C20	Ceramic	0.1 µF, 35 V	JP1	Jumper	Open
C21	Ceramic	1 µF, 35 V	JP2	Jumper	Short
C22	Ceramic	1 µF, 35 V	JP3	Jumper	Open
C23	Ceramic	1 µF, 35 V	JP4	Jumper	Short
C24	Ceramic	1 µF, 35 V	JP5	Jumper	Open
C25	Ceramic	0.1 µF, 35 V	JP6	Jumper	Short
R1(2)	General	1 kΩ, 1/8 W	CH1	Pin header	Equiv. to B2P3-VH
R2(2)	General	1 kΩ, 1/8 W	CH2	Pin header	Equiv. to B3P5-VH
R3(2)	General	1 kΩ, 1/8 W	SV1	Connector	2.54 mm pitch pin header
R4(2)	General	1 kΩ, 1/8 W	SV2	Connector	2.54 mm pitch pin header
R5(2)	General	1 kΩ, 1/8 W	SV3	Connector	2.54 mm pitch pin header
R6(2)	General	1 kΩ, 1/8 W	SV4	Connector	2.54 mm pitch pin header
R7 (3)	General	1 kΩ, 1/8 W	SV5	Connector	2.54 mm pitch pin header
R8(3)	General	1 kΩ, 1/8 W	IC	IC	SX68140M

(1) Refers to the setting value when f_{PWM} = 17 kHz (typ.).
(2) Should be connected for noise filtering.
(3) Should be connected when your application employs Hall IC inputs.

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